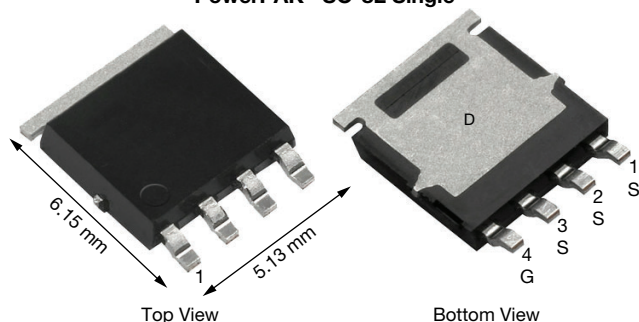


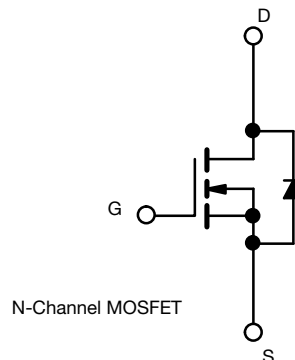
# Automotive N-Channel 200 V (D-S) 175 °C MOSFET

**PowerPAK® SO-8L Single**


## FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**


## PRODUCT SUMMARY

$V_{DS}$ (V)	200
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.145
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.150
$I_D$ (A)	13
Configuration	Single

## ORDERING INFORMATION

Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ454EP (for detailed order number please see <a href="http://www.vishay.com/doc?79771">www.vishay.com/doc?79771</a> )

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	200	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$I_D$	$T_C = 25$ °C	13
		$T_C = 125$ °C	7.5
Continuous source current (diode conduction) <sup>a</sup>	$I_S$	60	A
Pulsed drain current <sup>b</sup>	$I_{DM}$	30	
Single pulse avalanche current	$I_{AS}$	15	
Single pulse avalanche energy	$E_{AS}$	11.2	mJ
Maximum power dissipation <sup>b</sup>	$P_D$	$T_C = 25$ °C	68
		$T_C = 125$ °C	22
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	$R_{thJA}$	68	°C/W
Junction-to-case (drain)	$R_{thJC}$	2.2	

### Notes

- Package limited
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

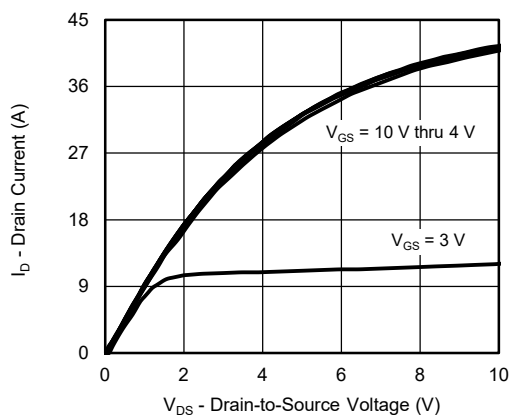
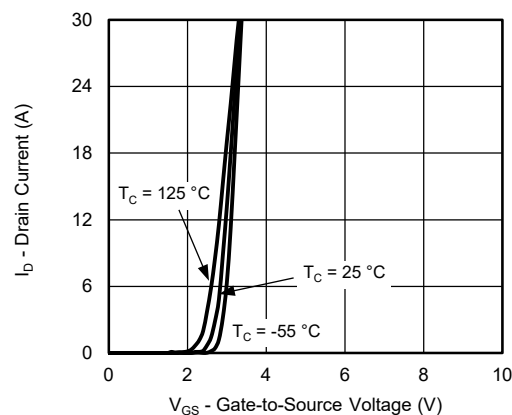
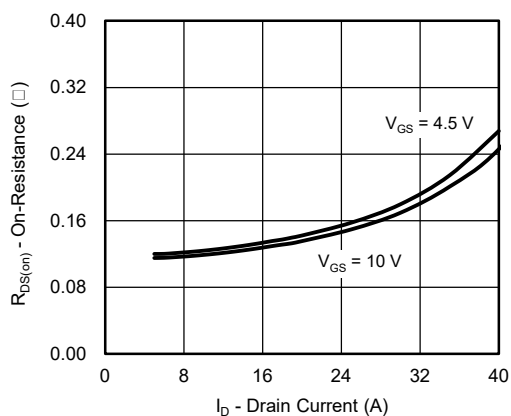
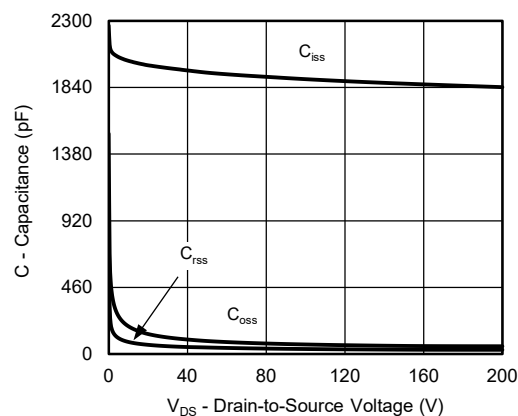
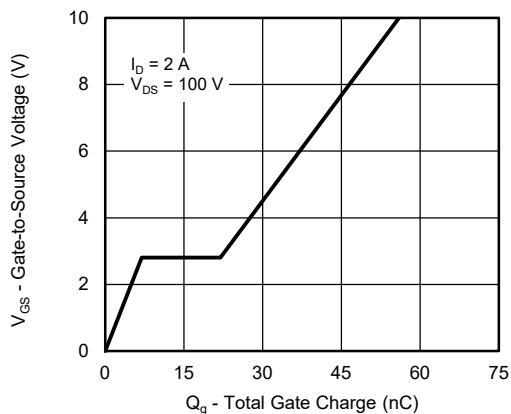
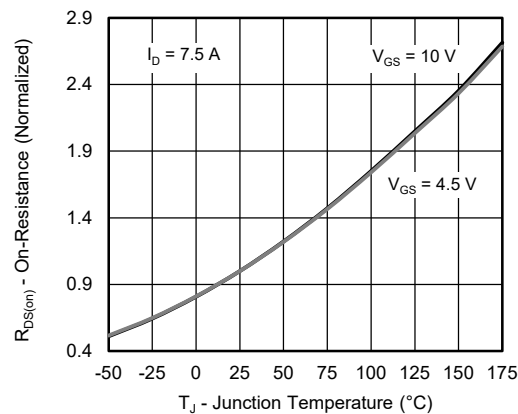


SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		200	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.5	2.0	2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 200 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 200 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 200 V, T <sub>J</sub> = 175 °C	-	-	250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	10	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 7.5 A	-	0.118	0.145	Ω
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 5 A	-	0.123	0.150	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 7.5 A, T <sub>J</sub> = 125 °C	-	-	0.298	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 7.5 A, T <sub>J</sub> = 175 °C	-	-	0.394	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 7.5 A		-	33	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	1990	2600	pF
Output capacitance	C <sub>oss</sub>			-	133	180	
Reverse transfer capacitance	C <sub>rss</sub>			-	62	85	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 100 V, I <sub>D</sub> = 2 A	-	56	85	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	7	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	15	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		0.20	0.45	0.80	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, R <sub>L</sub> = 50 Ω I <sub>D</sub> ≅ 2 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	14	25	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	5	10	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	33	55	
Fall time <sup>c</sup>	t <sub>f</sub>			-	8	15	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	30	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 7.5 A, V <sub>GS</sub> = 0		-	0.83	1.2	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 5 A, di/dt = 100 A/μs		-	86	175	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	335	700	nC
Reverse recovery fall time	t <sub>a</sub>			-	64	-	ns
Reverse recovery rise time	t <sub>b</sub>			-	22	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-7.6	-	A

**Notes**

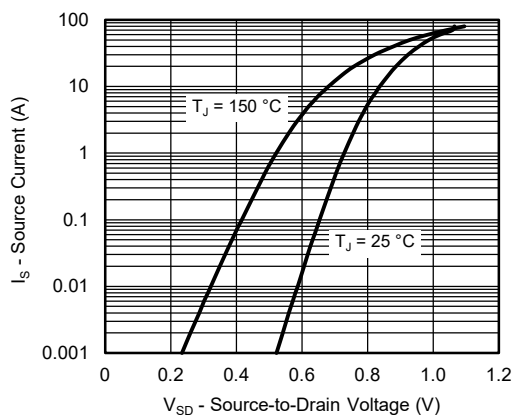
- f. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
g. Guaranteed by design, not subject to production testing.  
h. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

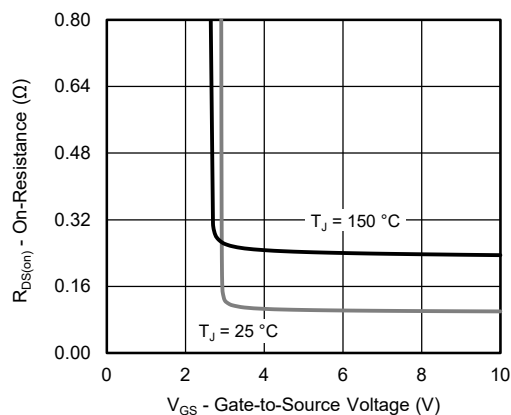
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**



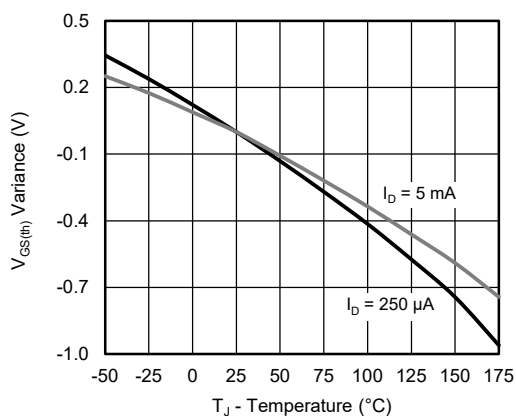
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)



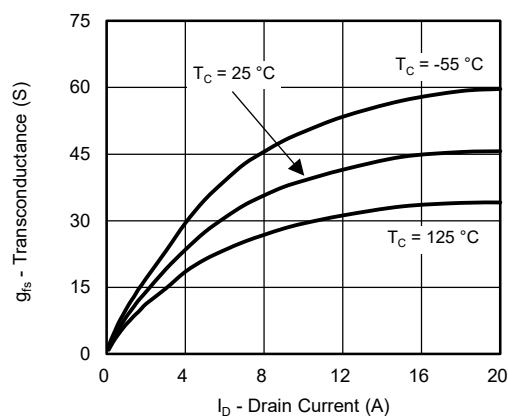
**Source Drain Diode Forward Voltage**



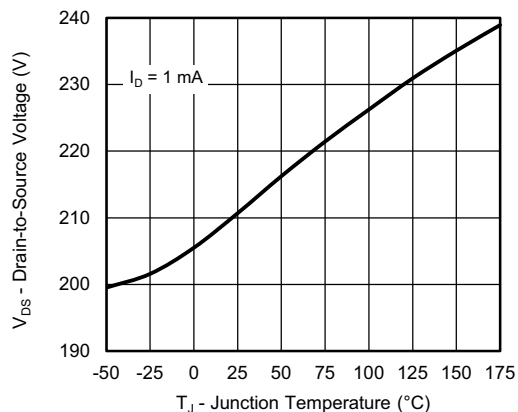
**On-Resistance vs. Gate-to Source Voltage**



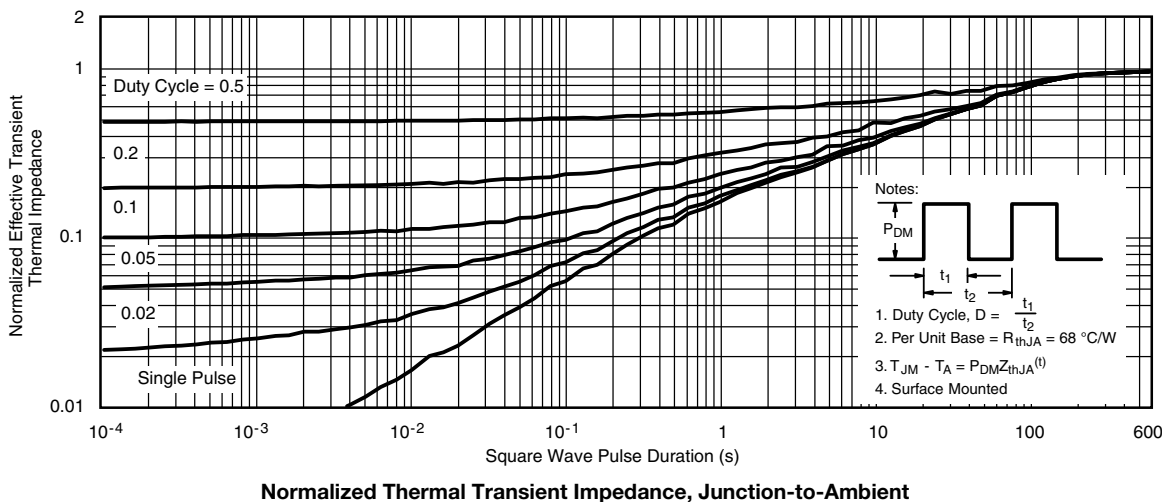
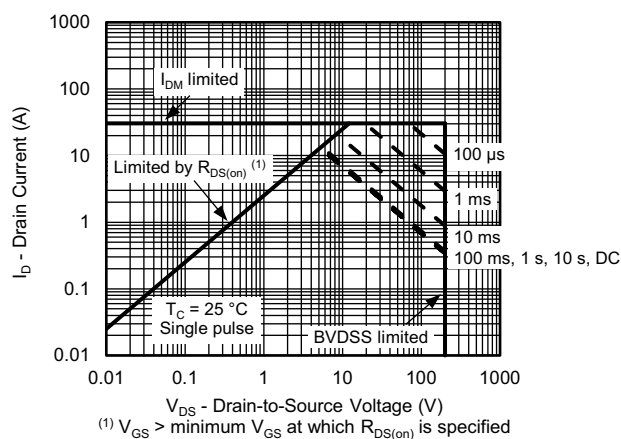
**Threshold Voltage**

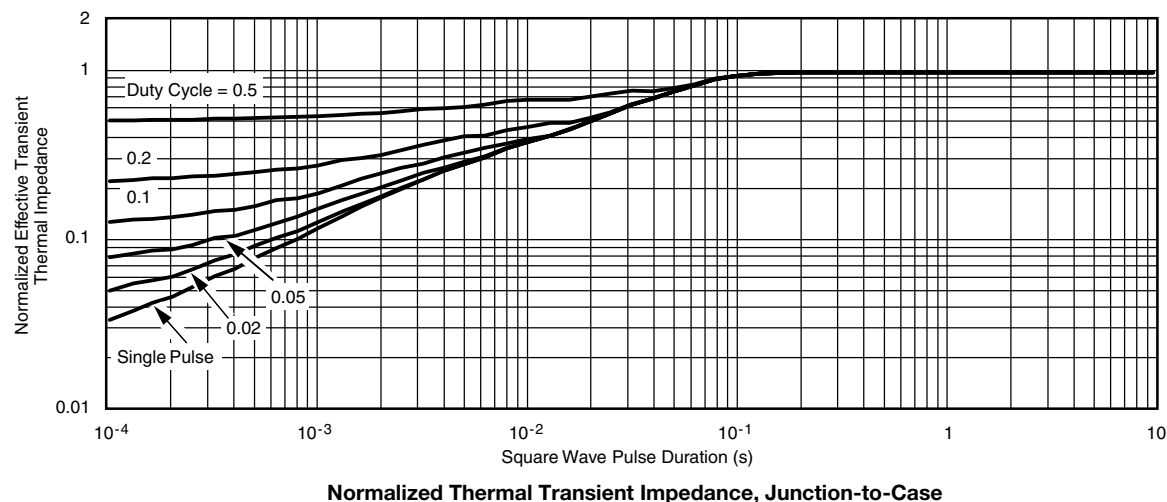


**Transconductance**



**Drain Source Breakdown vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)


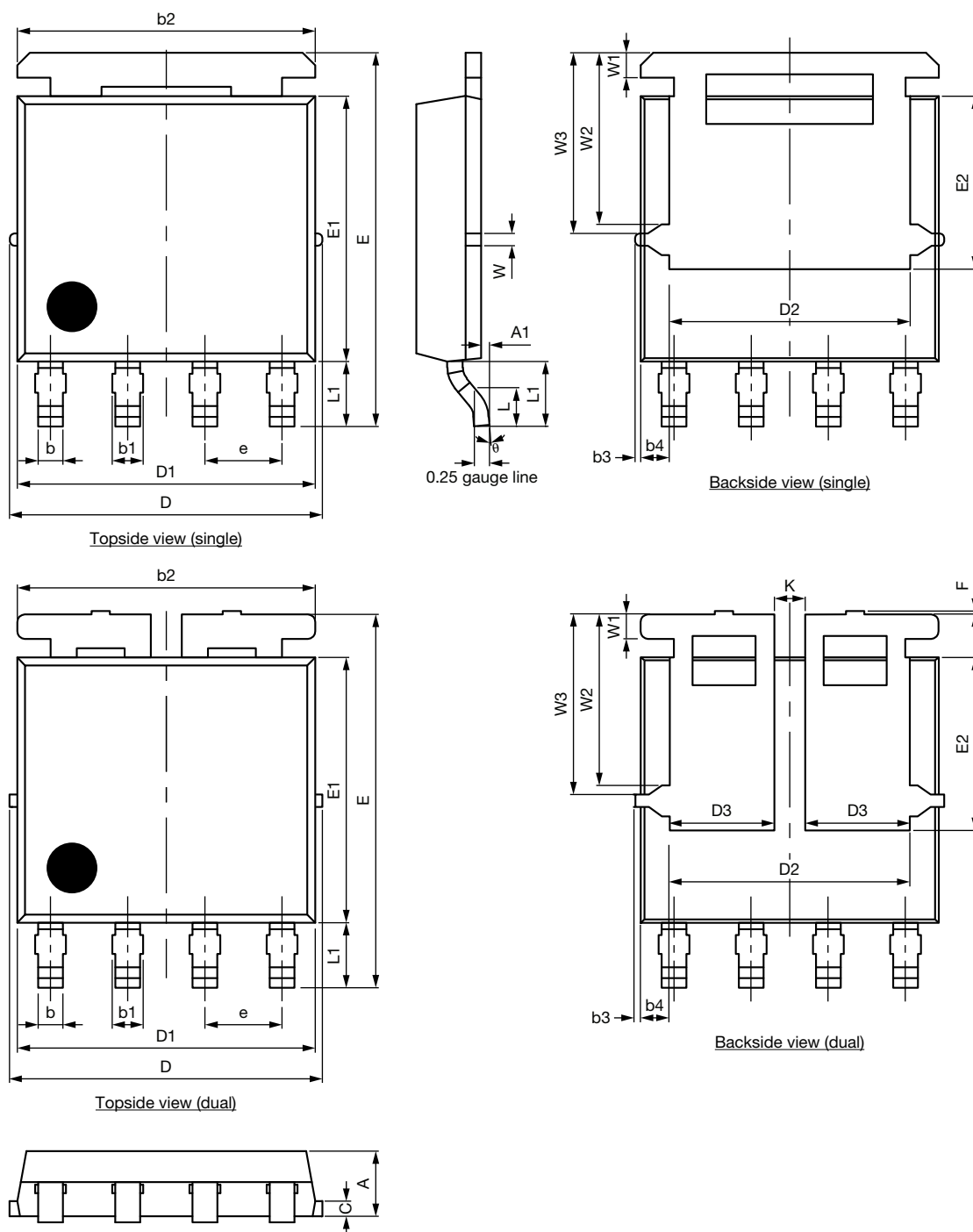
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?75925](http://www.vishay.com/ppg?75925).



## PowerPAK® SO-8L Case Outline 2





DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: C21-1498-Rev. C, 01-Nov-2021						
DWG: 6044						

### Note

- Millimeters will govern





## RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads  
Dimensions in mm (inches)



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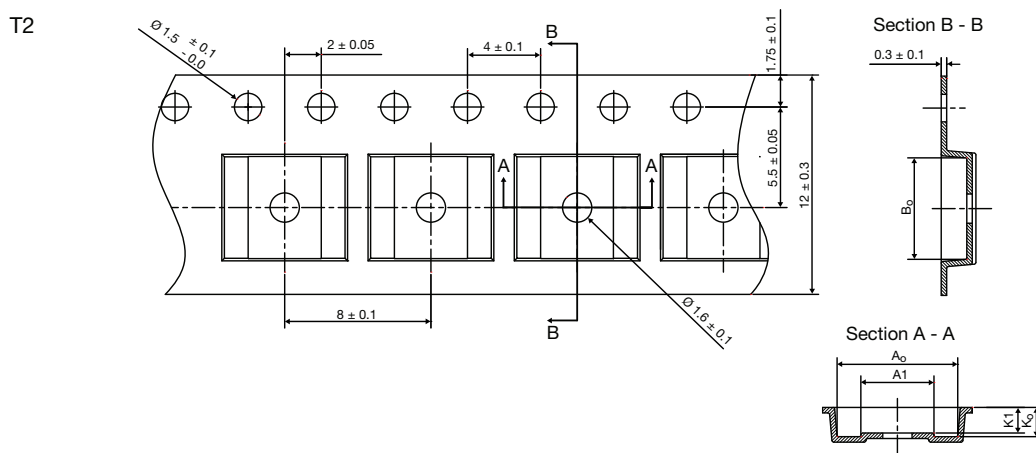
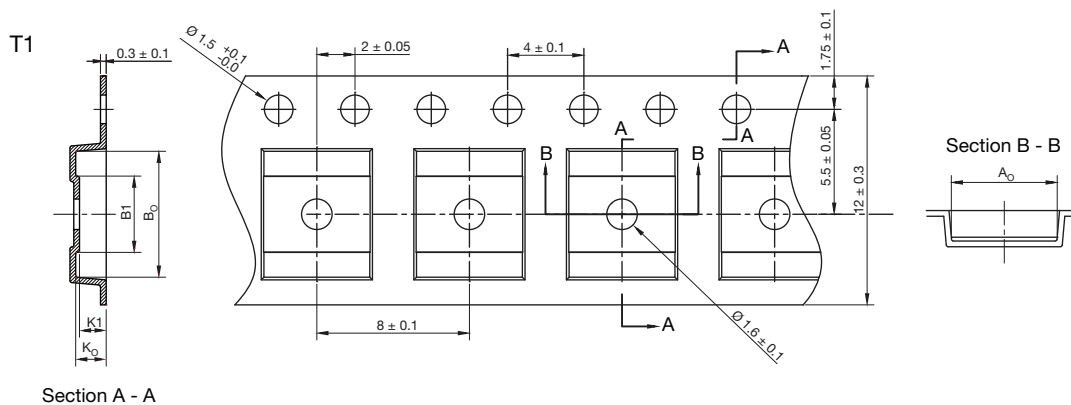
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## PowerPAK® SO-8L Carrier Tape



Version	A <sub>0</sub>	A1	B <sub>0</sub>	B1	K <sub>0</sub>	K1	Quantity per reel
T1 / - 1	5.55 ± 0.1	-	6.60 ± 0.1	4 ± 0.15	1.6 ± 0.1	1.4 ± 0.1	3000
T2 / - 2 <sup>a</sup>	6.60 ± 0.1	4 ± 0.15	5.55 ± 0.1	-	1.6 ± 0.1	1.4 ± 0.1	

## Notes

a. Not standard offering. Please contact local sales office for availability.

- (1) 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$  mm.
- (2) Camber not to exceed 1 mm in 100 mm, also not to exceed 1.5 cm in 1 m actually.
- (3) Material: black conductive or black static dissipative.
- (4)  $A_o$  and  $B_o$  measured on a plane 0.3 mm above the bottom of the pocket.
- (5)  $K_o$  measured from a plane on the inside bottom of the pocket to the top surface of carrier.
- (6) It should be measured from:
  - a. sprocket hole to pocket center.
  - b. sprocket hole to pocket hole.
- (7) All size in mm unless specified.
- (8) Tolerance will be  $\pm 0.1$  mm unless specified.
- (9) Vishay part number must be labeled at all reels of carrier tape.
- (10) Surface resistivity:  $10^4$  to  $10^{11} \Omega$ .
- (11) Version suffix as above table shown.

ECN: C15-1433-Rev. F, 02-Nov-15  
DWG: 93-5259-X



## **SQ Series Automotive MOSFET Ordering Code for Parts with Alternate Manufacturing Locations**

Standard ordering code for SQ series of automotive MOSFETs can be derived per the following table:

<b>PACKAGE TYPE</b>	<b>DATASHEET PART NUMBER</b>	<b>ORDERING SUFFIX</b>	<b>ORDERING PART NUMBER</b>
PowerPAK® 1212	Datasheet part number (example: SQS401EN)	-T1_GE3, -T1_BE3 <sup>a</sup>	Datasheet part number + "-T1_GE3" or "-T1_BE3" (example: SQS401EN-T1_GE3, SQS401EN-T1_BE3)
PowerPAK® SO-8L	Datasheet part number (example: SQJ488EP)	-T1_GE3, -T1_BE3 <sup>a</sup>	Datasheet part number + "-T1_GE3" or "-T1_BE3" (example: SQJ488EP-T1_GE3, SQS488EP-T1_BE3)
SOT-23	Datasheet part number (example: SQ2309ES)	-T1_GE3, -T1_BE3 <sup>a</sup>	Datasheet part number + "-T1_GE3" or "-T1_BE3" (example: SQ2309ES-T1_GE3, SQ2309ES-T1_BE3)
TSOP-6	Datasheet part number (example: SQ3427EV)	-T1_GE3, -T1_BE3 <sup>a</sup>	Datasheet part number + "-T1_GE3" or "-T1_BE3" (example: SQ3427EV-T1_GE3, SQ3427EV-T1_BE3)
SO-8	Datasheet part number (example: SQ4182EY)	-T1_GE3, -T1_BE3 <sup>a</sup>	Datasheet part number + "-T1_GE3" or "-T1_BE3" (example: SQ4182EY-T1_GE3, SQ4182EY-T1_BE3)

**Notes**

- For bare die parts and for non-standard orientations in tape (such as T2, T4) please contact your local sales or marketing for ordering code information
- a. "\_BE3" denotes alternate manufacturing location