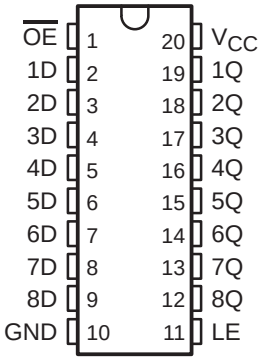
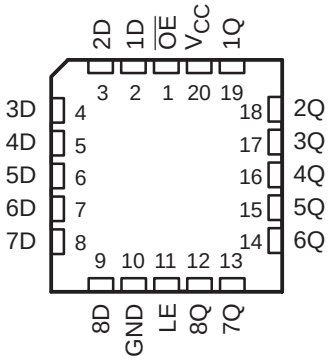
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V $V_{CC}$)**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and DIPs (J)**

**SN54LVC573A . . . J OR W PACKAGE**
**SN74LVC573A . . . DB, DW, OR PW PACKAGE**
**(TOP VIEW)**




**SN54LVC573A . . . FK PACKAGE**
**(TOP VIEW)**




## description

The SN54LVC573A octal transparent D-type latch is designed for 2.7-V to 3.6-V $V_{CC}$ operation and the SN74LVC573A octal transparent D-type latch is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

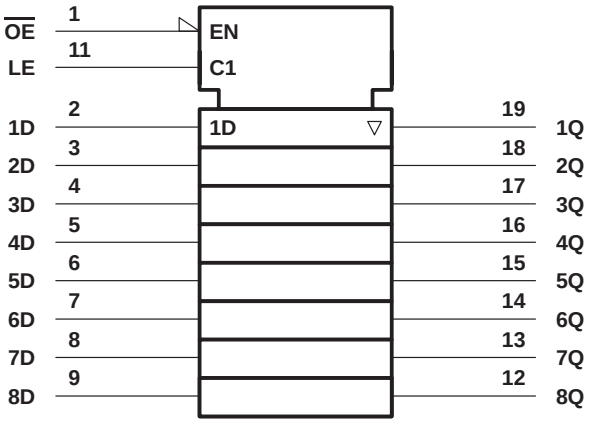
## description (continued)

The SN54LVC573A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVC573A is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(each latch)**

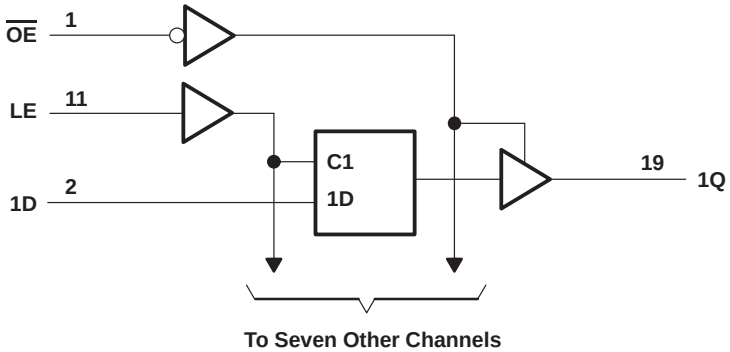
| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package . . . . . 115°C/W
DW package . . . . . 97°C/W
PW package . . . . . 128°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of $V_{CC}$ is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 4)

| | | | SN54LVC573A | | SN74LVC573A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | Operating | 2 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| | | 3 state | 0 | 5.5 | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | | | –8 | |
| | | $V_{CC}$ = 2.7 V | | –12 | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 0 | 6 | 0 | 6 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | SN54LVC573A | | | SN74LVC573A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100 µA | | 1.65 V to 3.6 V | | | | $V_{CC}$–0.2 | | | V |
| | | | 2.7 V to 3.6 V | $V_{CC}$–0.2 | | | | | | |
| | $I_{OH}$ = –4 mA | | 1.65 V | | | | 1.2 | | | |
| | $I_{OH}$ = –8 mA | | 2.3 V | | | | 1.7 | | | |
| | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | | 2.2 | | | |
| | | | 3 V | 2.4 | | | 2.4 | | | |
| | $I_{OH}$ = –24 mA | | 3 V | 2.2 | | | 2.2 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | | 1.65 V to 3.6 V | | | | | | 0.2 | V |
| | | | 2.7 V to 3.6 V | | | 0.2 | | | | |
| | $I_{OL}$ = 4 mA | | 1.65 V | | | | | | 0.45 | |
| | $I_{OL}$ = 8 mA | | 2.3 V | | | | | | 0.7 | |
| | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | | | 0.55 | |
| $I_I$ | $V_I$ = 0 to 5.5 V | | 3.6 V | | | ±5 | | | ±5 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | | 0 | | | | | | ±10 | µA |
| $I_{OZ}$ | $V_O$ = 0 to 5.5 V | | 3.6 V | | | ±15 | | | ±10 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND | $I_O$ = 0 | 3.6 V | | | 10 | | | 10 | µA |
| | 3.6 V ≤ $V_I$ ≤ 5.5 V‡ | | | | | 10 | | | 10 | |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | 2.7 V to 3.6 V | | | 500 | | | 500 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 4 | | | 4 | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 5.5 | | | 5.5 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ This applies in the disabled state only.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| | | SN54LVC573A | | | | UNIT |
|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 2 | | 2 | | ns |
| $t_h$ | Hold time, data after LE↓ | 2.5 | | 2.5 | | ns |

### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

| | | SN74LVC573A | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | † | | † | | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | † | | † | | 2 | | 2 | | ns |
| $t_h$ | Hold time, data after LE↓ | † | | † | | 1.5 | | 1.5 | | ns |

† This information was not available at the time of publication.

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVC573A | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | Q | | 7.7 | 1 | 6.9 | ns |
| | LE | | | 8.4 | 1 | 7.7 | |
| $t_{en}$ | $\overline{OE}$ | Q | | 8.5 | 1 | 7.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | Q | | 7 | 0.5 | 6.7 | ns |

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC573A | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | Q | † | † | † | † | | 7.7 | 1.5 | 6.9 | ns |
| | LE | | † | † | † | † | | 8.4 | 2 | 7.7 | |
| $t_{en}$ | $\overline{OE}$ | Q | † | † | † | † | | 8.5 | 1.5 | 7.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | Q | † | † | † | † | | 7 | 1.6 | 6.5 | ns |
| $t_{sk(o)}$‡ | | | | | | | | | | 1 | ns |

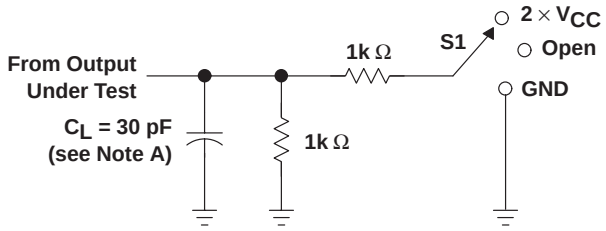
† This information was not available at the time of publication.
‡ Skew between any two outputs of the same package switching in the same direction

### operating characteristics, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V ± 0.15 V | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance per latch | Outputs enabled | f = 10 MHz | † | † | 37 | pF |
| | | Outputs disabled | | † | † | 4 | |

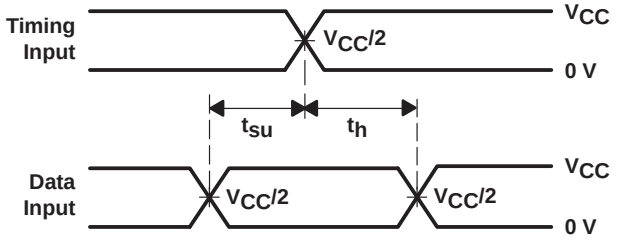
† This information was not available at the time of publication.

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.8 V ± 0.15 V

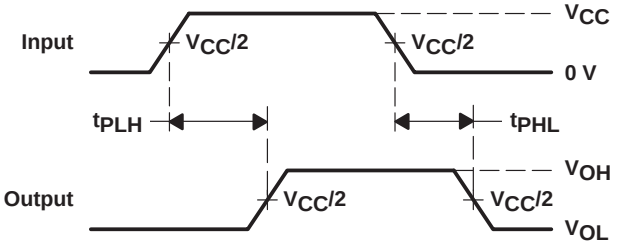



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open |

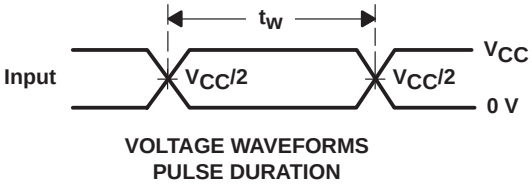
LOAD CIRCUIT



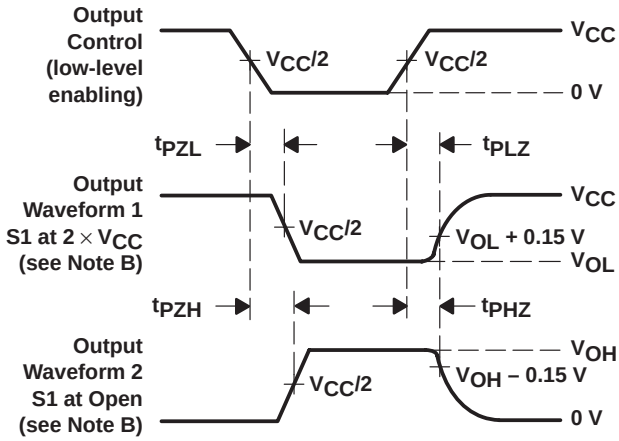

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

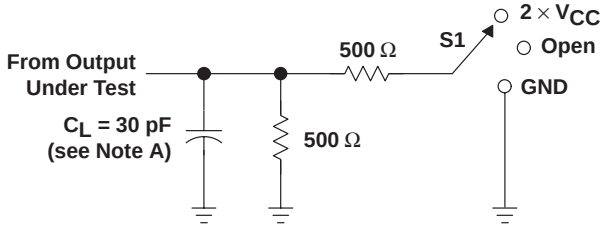



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

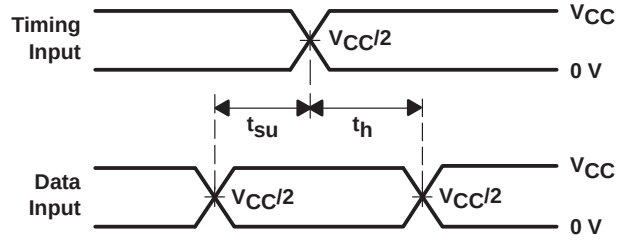
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

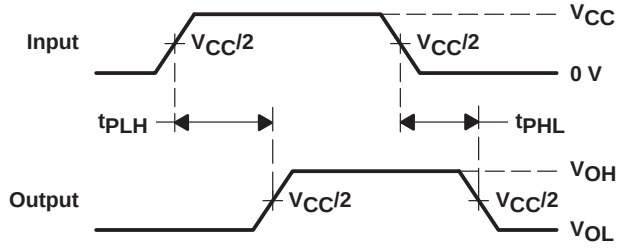



| TEST | S1 |
|---|---|
| $t_{pd}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>2 × $V_{CC}$<br>GND |

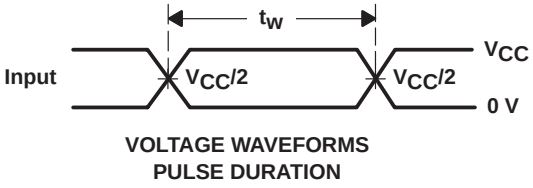
LOAD CIRCUIT



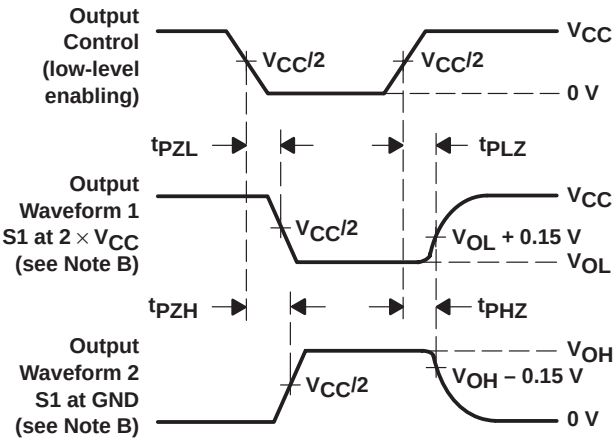

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

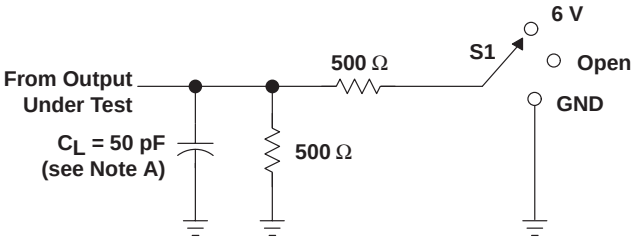



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, $Z_O$ = 50 Ω, $t_r$≤2 ns, $t_f$≤2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

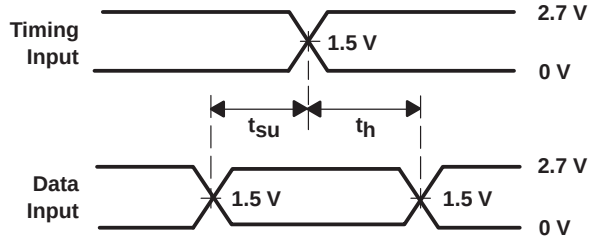
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

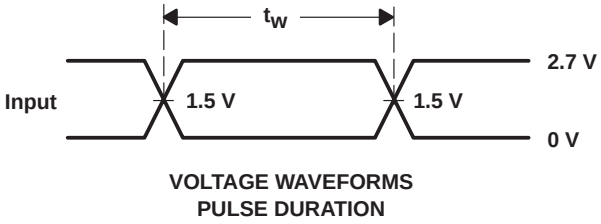



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

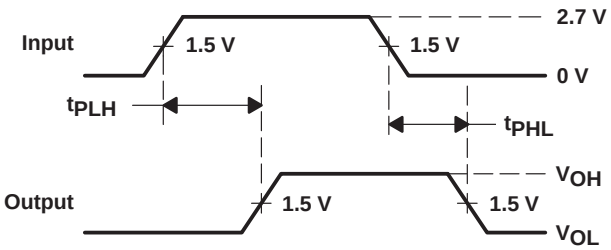
LOAD CIRCUIT



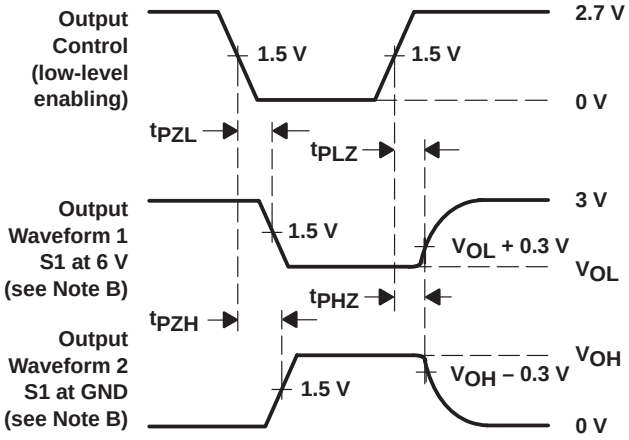

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 3. Load Circuit and Voltage Waveforms**

## IMPORTANT NOTICE

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