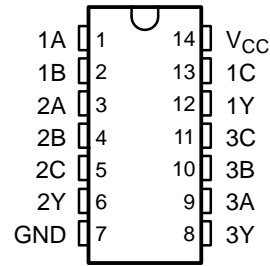


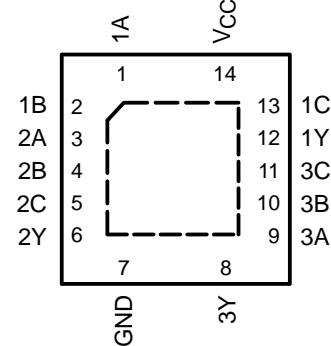
FEATURES

- Operates From 1.65 V to 3.6 V
- Specified From –40°C to 85°C and –40°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.9 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

**D, DB, NS, OR PW PACKAGE
(TOP VIEW)**



**RGY PACKAGE
(TOP VIEW)**



DESCRIPTION/ORDERING INFORMATION

This triple 3-input positive-NAND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC10A performs the Boolean function $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C | QFN - RGY | Reel of 1000 | SN74LVC10ARGYR | LC10A |
| –40°C to 125°C | SOIC - D | Tube of 50 | SN74LVC10AD | LVC10A |
| | | Reel of 2500 | SN74LVC10ADR | |
| | | Reel of 250 | SN74LVC10ADT | |
| | SOP - NS | Reel of 2000 | SN74LVC10ANSR | LVC10A |
| | SSOP - DB | Reel of 2000 | SN74LVC10ADBR | LC10A |
| | TSSOP - PW | Tube of 90 | SN74LVC10APW | LC10A |
| | | Reel of 2000 | SN74LVC10APWR | |
| | | Reel of 250 | SN74LVC10APWT | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN74LVC10A

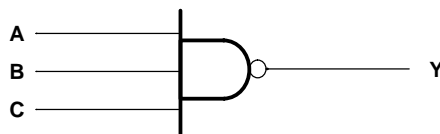
TRIPLE 3-INPUT POSITIVE-NAND GATE

SCAS284N–JANUARY 1993–REVISED FEBRUARY 2005

**FUNCTION TABLE
(EACH GATE)**

| INPUTS | | | OUTPUT Y |
|--------|---|---|-------------|
| A | B | C | |
| H | H | H | L |
| L | X | X | H |
| X | L | X | H |
| X | X | L | H |

LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)



Absolute Maximum Ratings ⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|--|--|----------------|------|
| V_{CC} | Supply voltage range | –0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾ | –0.5 | 6.5 | V |
| V_O | Output voltage range ⁽²⁾⁽³⁾ | –0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | | –50 | mA |
| I_{OK} | Output clamp current | | –50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | ±100 | mA |
| θ_{JA} | Package thermal impedance | D package ⁽⁴⁾ | 86 | °C/W |
| | | DB package ⁽⁴⁾ | 96 | |
| | | NS package ⁽⁴⁾ | 76 | |
| | | PW package ⁽⁴⁾ | 113 | |
| | | RGY package ⁽⁵⁾ | 47 | |
| T_{stg} | Storage temperature range | –65 | 150 | °C |
| P_{tot} | Power dissipation | $T_A = -40^{\circ}\text{C}$ to 125°C ⁽⁶⁾⁽⁷⁾ | 500 | mW |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.
- (6) For the D package: above 70°C , the value of P_{tot} derates linearly with 8 mW/K.
- (7) For the DB, NS, and PW packages: above 60°C , the value of P_{tot} derates linearly with 5.5 mW/K.

Recommended Operating Conditions⁽¹⁾

| | | | T _A = 25°C | | –40 TO 85°C | | –40 TO 125°C | | UNIT |
|-----------------|---------------------------|------------------------------------|------------------------|-----------------|------------------------|-----------------|------------------------|-----------------|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | Operating | 1.65 | 3.6 | 1.65 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | 0.65 × V _{CC} | | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | 1.7 | | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | 2 | | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | | 0.35 × V _{CC} | | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | | 0.7 | | 0.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 0.8 | | 0.8 | | 0.8 | | |
| V _I | Input voltage | | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | –4 | | –4 | | –4 | | mA |
| | | V _{CC} = 2.3 V | –8 | | –8 | | –8 | | |
| | | V _{CC} = 2.7 V | –12 | | –12 | | –12 | | |
| | | V _{CC} = 3 V | –24 | | –24 | | –24 | | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | 4 | | 4 | | 4 | | mA |
| | | V _{CC} = 2.3 V | 8 | | 8 | | 8 | | |
| | | V _{CC} = 2.7 V | 12 | | 12 | | 12 | | |
| | | V _{CC} = 3 V | 24 | | 24 | | 24 | | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PAR-AMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | −40 TO 85°C | | −40 TO 125°C | | UNIT |
|--------------------------|---|-----------------|-----------------------|-----|-----|-----------------------|-----|-----------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = −100 μA | 1.65 V to 3.6 V | V _{CC} − 0.2 | | | V _{CC} − 0.2 | | V _{CC} − 0.3 | | V |
| | I _{OH} = −4 mA | 1.65 V | 1.29 | | | 1.2 | | 1.05 | | |
| | I _{OH} = −8 mA | 2.3 V | 1.9 | | | 1.7 | | 1.55 | | |
| | I _{OH} = −12 mA | 2.7 V | 2.2 | | | 2.2 | | 2.05 | | |
| | | 3 V | 2.4 | | | 2.4 | | 2.25 | | |
| I _{OH} = −24 mA | 3 V | 2.3 | | | 2.2 | | 2 | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 3.6 V | 0.1 | | | 0.2 | | 0.3 | | V |
| | I _{OL} = 4 mA | 1.65 V | 0.24 | | | 0.45 | | 0.6 | | |
| | I _{OL} = 8 mA | 2.3 V | 0.3 | | | 0.7 | | 0.75 | | |
| | I _{OL} = 12 mA | 2.7 V | 0.4 | | | 0.4 | | 0.6 | | |
| | I _{OL} = 24 mA | 3 V | 0.55 | | | 0.55 | | 0.8 | | |
| I _I | V _I = 5.5 V or GND | 3.6 V | ±1 | | | ±5 | | ±20 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 1 | | | 10 | | 40 | | μA |
| ΔI _{CC} | One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND | 2.7 V to 3.6 V | 500 | | | 500 | | 5000 | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | 5 | | | | | | | pF |

SN74LVC10A

TRIPLE 3-INPUT POSITIVE-NAND GATE

SCAS284N–JANUARY 1993–REVISED FEBRUARY 2005

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | –40 TO 85°C | | –40 TO 125°C | | UNIT |
|--------------------|-----------------|----------------|-----------------|-----------------------|-----|------|-------------|------|--------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A, B, or C | Y | 1.8 V ± 0.15 V | 1 | 4.2 | 10.1 | 1 | 10.6 | 1 | 12.1 | ns |
| | | | 2.5 V ± 0.2 V | 1 | 2.9 | 7.3 | 1 | 7.8 | 1 | 9.9 | |
| | | | 2.7 V | 1 | 3.1 | 5.6 | 1 | 5.8 | 1 | 7.4 | |
| | | | 3.3 V ± 0.3 V | 1 | 2.7 | 4.7 | 1 | 4.9 | 1 | 6 | |
| t _{sk(o)} | | | 3.3 V ± 0.3 V | | | | | 1 | | 1.5 | ns |

Operating Characteristics

T_A = 25°C

| PARAMETER | | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|-----------------|--|--------------------|-----------------|-----|------|
| C _{pd} | Power dissipation capacitance per gate | f = 10 MHz | 1.8 V | 9 | pF |
| | | | 2.5 V | 10 | |
| | | | 3.3 V | 11 | |

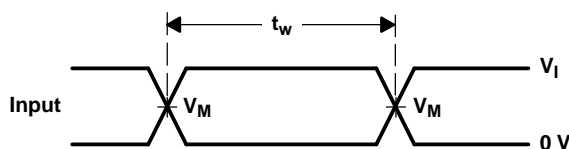
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

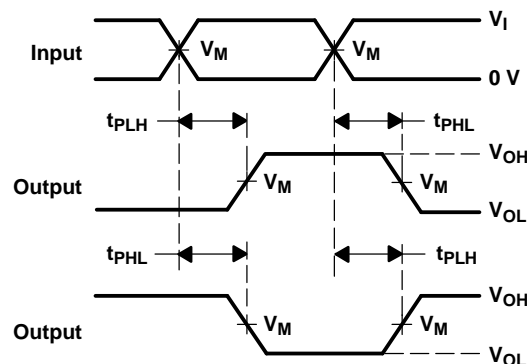
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



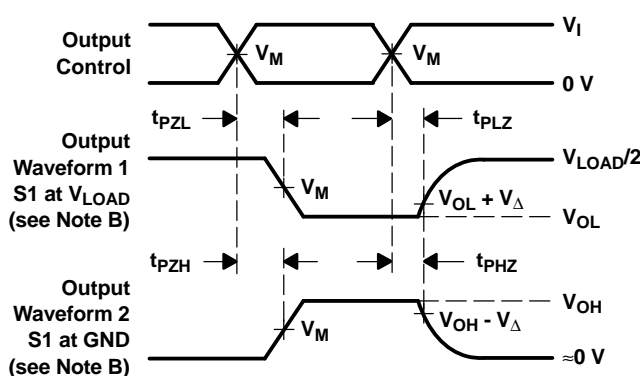
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| SN74LVC10AD | ACTIVE | SOIC | D | 14 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LVC10ADBLE | OBSOLETE | SSOP | DB | 14 | | None | Call TI | Call TI |
| SN74LVC10ADBR | ACTIVE | SSOP | DB | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LVC10ADR | ACTIVE | SOIC | D | 14 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LVC10ADT | ACTIVE | SOIC | D | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LVC10ANSR | ACTIVE | SO | NS | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LVC10APW | ACTIVE | TSSOP | PW | 14 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74LVC10APWLE | OBSOLETE | TSSOP | PW | 14 | | None | Call TI | Call TI |
| SN74LVC10APWR | ACTIVE | TSSOP | PW | 14 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74LVC10APWT | ACTIVE | TSSOP | PW | 14 | 250 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| SN74LVC10ARGYR | ACTIVE | QFN | RGY | 14 | 1000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G14)

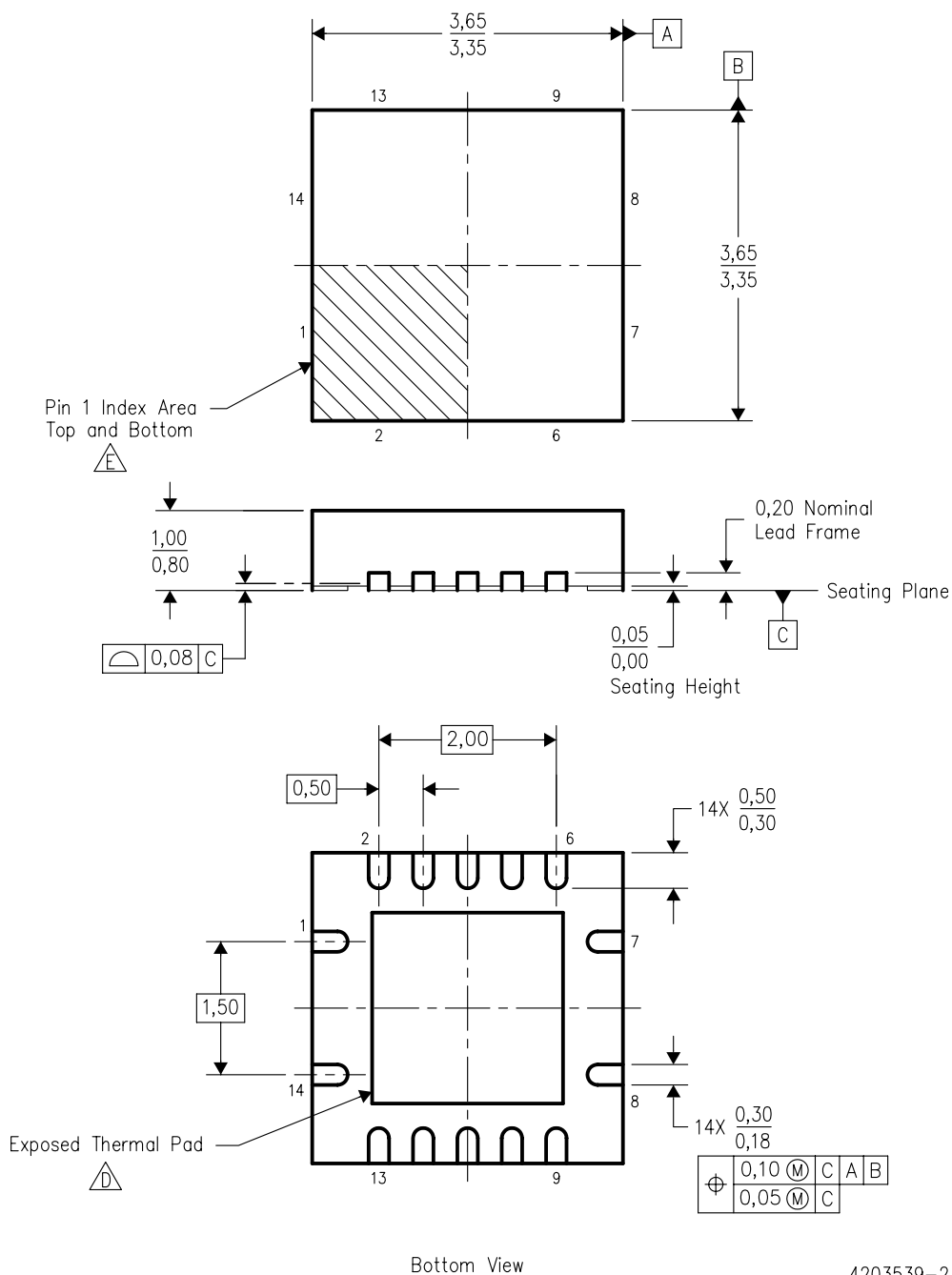
PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/F 07/2004

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



Bottom View

4203539-2/F 02/2005

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---------------|-------|-------|-------|-------|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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