edited: 05/09/2023

Dual-Channel SiC/IGBT Gate Driver

1. Product Features

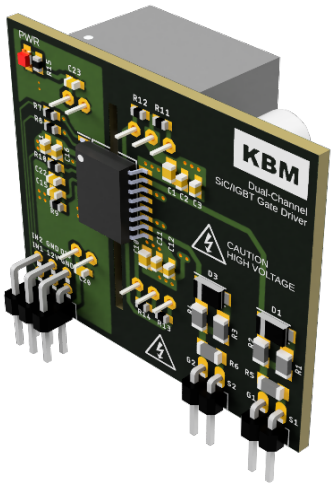


Fig.1 Dual-Channel SiC/IGBT Gate Driver Isometric View

- Dual-channel gate driver in 1 module
- Compact size right angle PCB mount
- Suitable for SiC MOSFET (Default Setting) and IGBT maximum voltage up to 1200 V
- Output of driver +15/-4 V
- High speed switching frequency up to 200 kHz
- Isolated input and output circuit
- Build-in dead time and overlap signals protection
- Universal configuration: dual high side, dual low side or half bridge driver (default setting)
- Power on LED indicator
- Single power supply +12 V
- Supply voltage pins have under voltage lock-out (UVLO) protection
- TTL and CMOS Level compatible inputs (supported for DSP, MCU, hardware-in-the-loop, Typhoon HIL, OPAL-RT and dSPACE)

2. Applications

- 2 Channel SiC MOSFET and IGBT Gate Driver
- Half Bridge Drives
- High power resonant converter
- On broad charger unit
- Inverter drives
- Multi state power factor correction

0 2983 3737
sales@kbmeng.com
http://www.kbmeng.com
27/19 Moo.5, Talingchan-Suphanburi, Lahan, Bangbuathong, Nonthaburi 11110

3. Functional Block Diagram of Dual-Channel SiC/IGBT Gate Driver

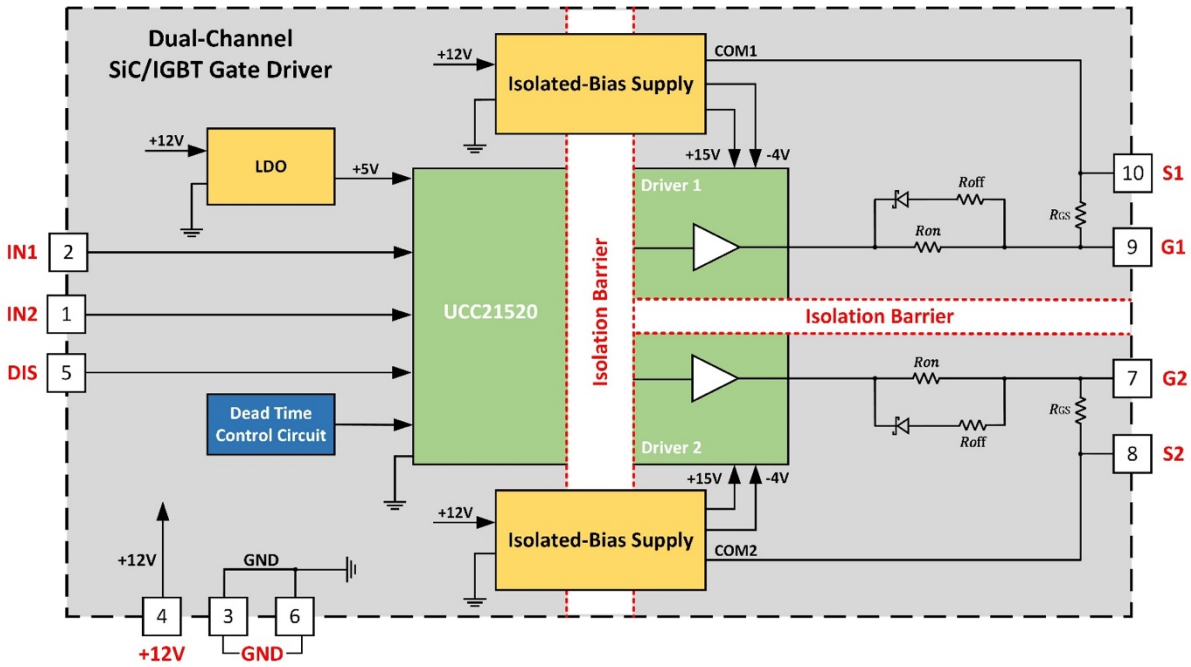


Fig.2 Function Block Diagram

4. Inputs and Outputs Logic Table

Table 1. Inputs/Outputs Logic Table

INPUTS		DISABLE (DIS pin)	OUTPUTS	
IN1	IN2		Driver 1	Driver 2
L	L	L or Left Open	L	L
L	H	L or Left Open	L	H
H	L	L or Left Open	H	L
H	H	L or Left Open	L	L
X	X	H	L	L

"X" means L, H or left open

5. Pin Configuration

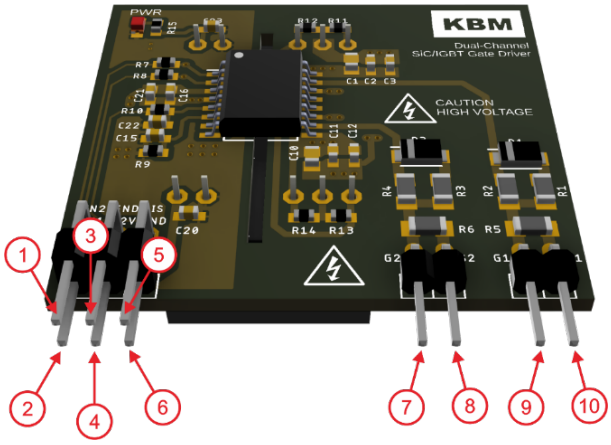


Fig.3 Pin Configuration

Table 2. Pin Functions Table

Pin Number	Pin Name	Description
1	IN2	Input signal for channel 2. IN2 input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
2	IN1	Input signal for channel 1. IN1 input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity.
3	GND	Ground pin reference. All signals in the primary side are referenced to this ground.
4	12V	Input power supply pin +12 V
5	DIS	Input logic (TTL/CMOS Level) to disables both driver outputs if asserted high, enables if set low or left open. This pin is pulled low internally if left open.
6	GND	Ground pin reference. All signals in the primary side are referenced to this ground.
7	G2	Output of driver 2. Connect this pin to the gate junction of MOSFET or IGBT.
8	S2	Output of driver 2. Connect this pin to the source or emitter junction of MOSFET or IGBT.
9	G1	Output of driver 1. Connect this pin to the gate junction of MOSFET or IGBT.
10	S1	Output of driver 1. Connect this pin to the source or emitter junction of MOSFET or IGBT.

NOTE : Output pin of driver (pin 7,8,9 and 10) should be connected to SiC MOSFET or IGBT as close as possible.

6. Technical Data

Table 3. Technical Data Table

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Dimension (PCB)		44 x 40		mm	length x width
Supply voltage	11.8	12	12.2	V	V DC
Current consumption	38	45	50	mA	@ standby state
Power indicator		Red LED		-	-
↑ Input logic high level (IN1, IN2 and DIS pin)	2.1	3.3	5.3	V	3.3 V and 5 V compatible inputs
↓ Input logic low level (IN1, IN2 and DIS pin)	-0.3	0	0.8	V	3.3 V and 5 V compatible inputs
Positive supply voltage output driver	+14.8	+15	+15.8	V	-
Negative supply voltage output driver	-3.8	-4	-4.5	V	-
Operating frequency	-	-	200	kHz	-
Deadtime and overlap designed *(1)	90	100	110	ns	default setting
R_{on} Gate turn-on resistance *(2)	-	10	-	Ω	-
R_{off} Gate turn-off resistance *(2)	-	4.7	-	Ω	-
R_{GS} Gate to source resistance	-	10	-	kΩ	-
Output rise time (20% to 80%)	-	-	50	ns	-
Output fall time (80% to 20%)	-	-	40	ns	-
Propagation delay from INx to OUTx rising edges	-	-	70	ns	-
Propagation delay from INx to OUTx falling edges	-	-	70	ns	-

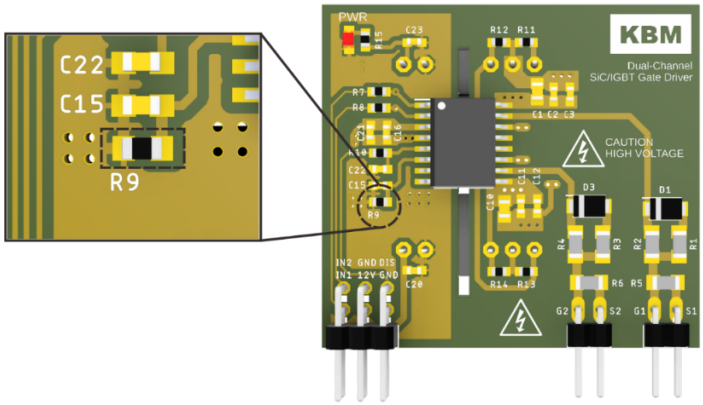


Fig.4 R9 Position

*(1) If user apply deadtime from microcontroller or controller unit greater than build in programming deadtime, driver will obey input signal. In the other hand if user doesn't apply deadtime, driver will use build in deadtime to prevent short circuit event.

According to gate driver IC (UCC 21520 TI) deadtime and overlap designed by resistance $\boldsymbol{R_{DT}}$ default 10 kΩ from manufacturing process. User can change programming time by resolder and replacement resistor R9 position **(recommend: SMD 0603 size ±1%)** in PCB.

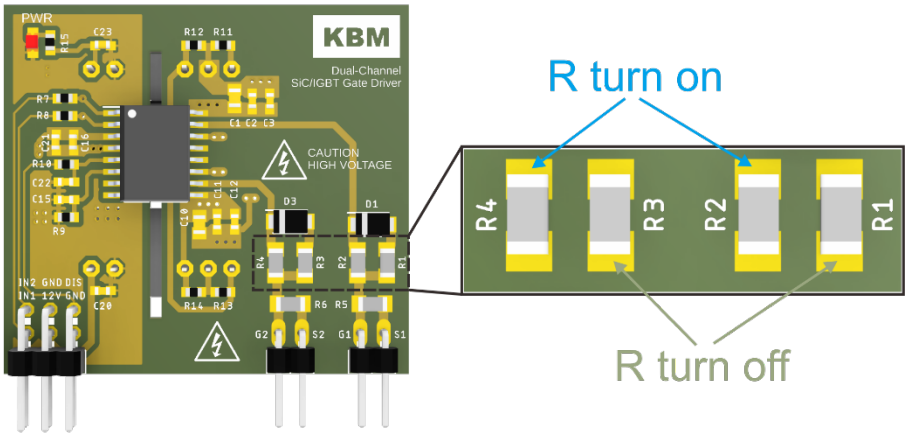


Fig.5 R1, R2, R3 and R4 Position

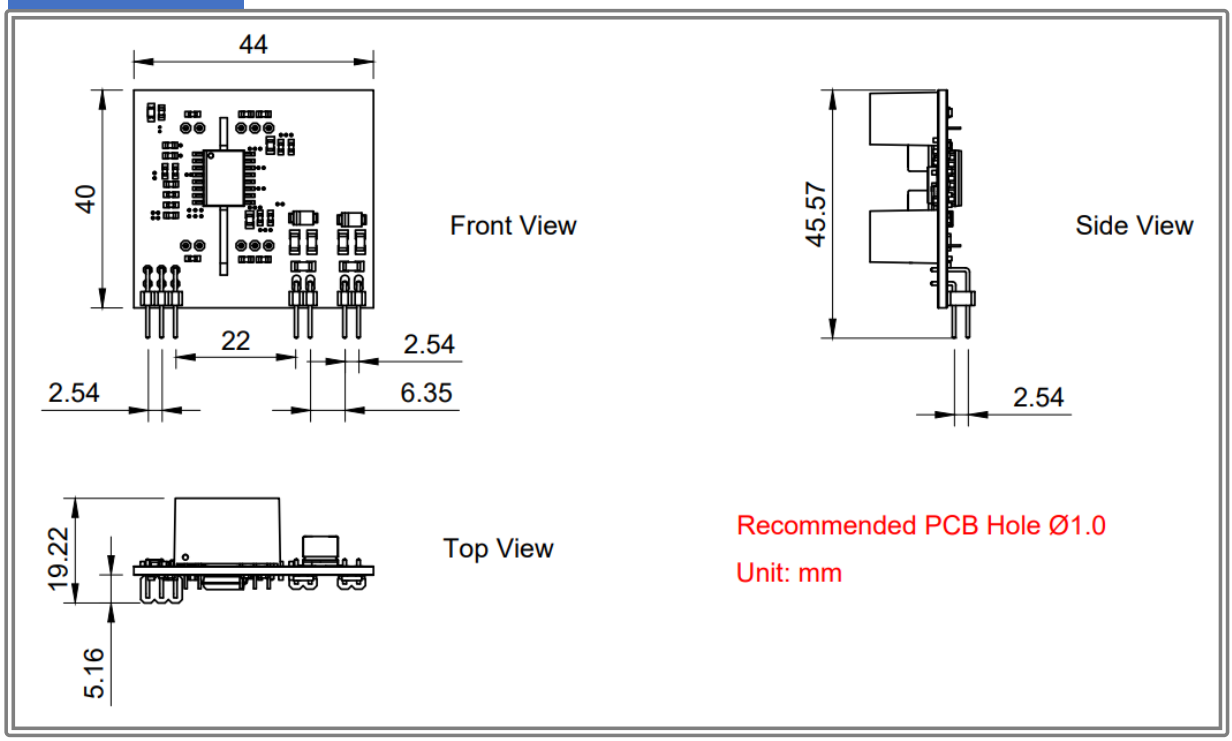
*(2) $\boldsymbol{R_{on}}$ (Gate turn-on resistor) and $\boldsymbol{R_{off}}$ (Gate turn-off resistor) can be change by resolder and replacement R2, R4 and R1, R3 respectively. **(recommend: SMD 1206 size ±1% ¼ W)**

- R1 position = Gate turn-off resistor of driver 1.
- R2 position = Gate turn-on resistor of driver 1.
- R3 position = Gate turn-off resistor of driver 2.
- R4 position = Gate turn-on resistor of driver 2.

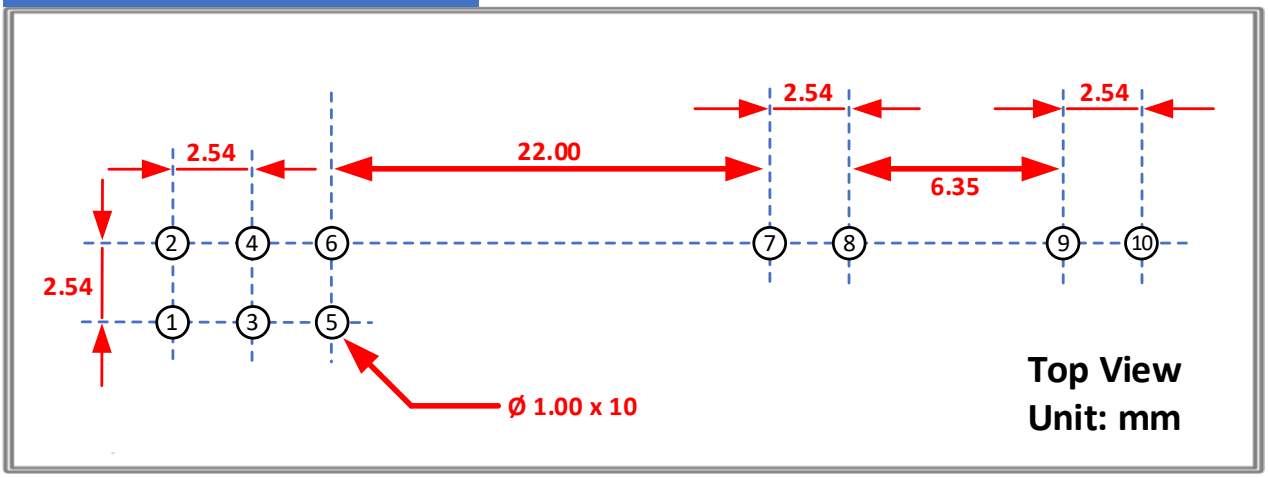
0 2983 3737
sales@kbmeng.com
http://www.kbmeng.com
27/19 Moo.5, Talingchan-Suphanburi, Lahan, Bangbuathong, Nonthaburi 11110

7. Dimensions and Footprint

Dimensions



Recommended PCB Layout



0 2983 3737
sales@kbmeng.com
http://www.kbmeng.com
27/19 Moo.5, Talingchan-Suphanburi, Lahan,
Bangbuathong, Nonthaburi 11110

8. Report Test

8.1 Test Condition 1

- Power Circuit Topology: Half-Bridge Inverter.
- $\mathbf{f_{sw}}$: 100 kHz.
- V DC BUS: 0 V.
- Dead-time generated from input of IN1 and IN2: 300 ns.

Fig.6 Waveform of IN1, IN2 and output of driver1, driver2

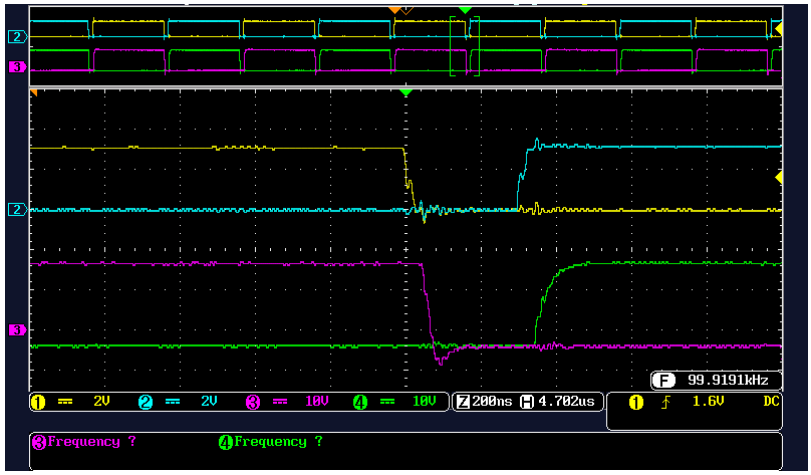


Fig.7 Waveform of IN1, IN2 and output of driver1, driver2 (zoomed in)

- Channel 1 (yellow): input signal of IN1 pin.
- Channel 2 (blue): input signal of IN2 pin.
- Channel 3 (pink): output signal of driver1 (G1 pin ref to S1 pin).
- Channel 4 (green): output signal of driver2 (G2 pin ref to S2 pin).

8.2 Test Condition 2

- Power Circuit Topology: Half-Bridge Inverter.
- $\mathbf{f_{sw}}$: 100 kHz.
- V DC BUS: 0 V.
- Dead-time generated from input of IN1 and IN2: 0 ns.

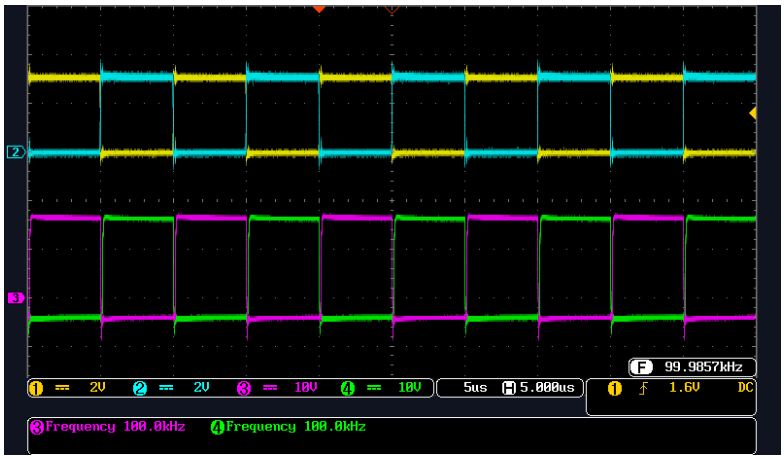


Fig.8 Waveform of IN1, IN2 and output of driver1, driver2

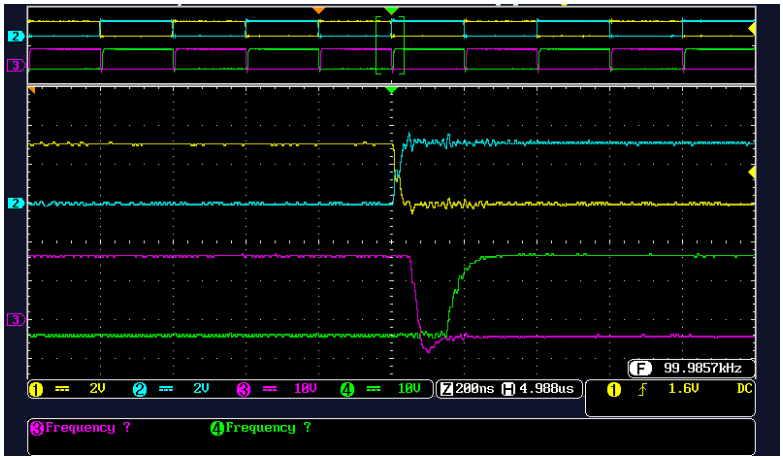


Fig.9 Waveform of IN1, IN2 and output of driver1, driver2 (zoomed in)

- Channel 1 (yellow): input signal of IN1 pin.
- Channel 2 (blue): input signal of IN2 pin.
- Channel 3 (pink): output signal of driver1 (G1 pin ref to S1 pin).
- Channel 4 (green): output signal of driver2 (G2 pin ref to S2 pin).