FM0+ S6E1A1 Series

32-bit ARM® Cortex®-M0+ based Microcontroller S6E1A11B0A/S6E1A11C0A,S6E1A12B0A/S6E1A12C0A

Data Sheet (Full Production)

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur.

Publication Number S6E1A1_DS710-00001 Revision 1.0 Issue Date July 16, 2014

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FM0+ S6E1A1 Series

32-bit ARM® Cortex®-M0+ based Microcontroller
S6E1A11B0A/S6E1A11C0A,S6E1A12B0A/S6E1A12C0A

Data Sheet (Full Production)

1. Description

The S6E1A1 Series is a series of highly integrated 32-bit microcontrollers designed for embedded controllers aiming at low power consumption and low cost.

This series has the ARM Cortex-M0+ Processor with on-chip Flash memory and SRAM, and consists of peripheral functions such as various timers, ADCs and communication interfaces (UART, CSIO, I^{2}C, LIN).

The products which are described in this data sheet are placed into TYPE1-M0+ product categories in "FM0+ Family PERIPHERAL MANUAL".

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Table of Contents

2. Features

32-bit ARM Cortex-M0+ Core

- Processor version: r0p1
- Maximum operating frequency: 40 MHz
- Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 32 peripheral interrupt with 4 selectable interrupt priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

Bit Band operation

Compatible with Cortex-M3 bit band operation.

On-chip Memory

- Flash memory
  - Up to 88 Kbyte
  - Read cycle:0 wait-cycle
  - Security function for code protection
- SRAM

The on-chip SRAM of this series has one independent SRAM .

  - SRAM: 6 Kbyte

Multi-function Serial Interface (Max 3channels)

- 128 bytes with FIFO in all channels (The number of FIFO steps varies depending on the settings of the communication mode or bit length.)
- The operation mode of each channel can be selected from one of the following.
  - UART
  - CSIO
  - LIN
  - I^{2}C
- UART
  - Full duplex double buffer
  - Parity can be enabled or disabled.
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detection functions (parity errors, framing errors, and overrun errors)
- CSIO
  - Full duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detection function
  - Serial chip select function (ch.1 and ch.3 only)
  - Data length: 5 to 16 bits
- LIN
  - LIN protocol Rev.2.1 supported
  - Full duplex double buffer
  - Master/Slave mode supported
  - LIN break field generation function (The length is variable between 13 bits and 16 bits.)
  - LIN break delimiter generation function (The length is variable between 1 bit and 4 bits.)
  - Various error detection functions available (parity errors, framing errors, and overrun errors)
- I^{2}C
  - Standard-mode (Max: 100 kbps) supported / Fast-mode (Max 400kbps) supported.

DMA Controller (2 channels)

The DMA Controller has its own bus independent of the CPU, and CPU and DMA Controller can process simultaneously.

- 2 independently configurable and operable channels
- It can start a transfer with a software request or a request from a built-in peripheral.
- Transfer address area: 32 bits (4 Gbyte)
- Transfer mode: block transfer/burst transfer/demand transfer
- Transfer data type: byte/halfword/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

A/D Converter (Max: 8 channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Conversion time: 0.8 μs @ 5 V (S6E1A1xC0A) / 2.0 μs (S6E1A1xB0A)
  - Priority conversion available (2 levels of priority)
  - Scan conversion mode
  - Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

Base Timer (Max: 4 channels)

The operation mode of each channel can be selected from one of the following.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

General-purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 37 fast general-purpose I/O ports @48pin package
- Certain ports are 5 V tolerant.
  See "5. Pin Assignment" and "7. I/O Circuit Type" for details of such pins.

Dual Timer (32/16-bit Down Counter)

The Dual Timer consists of two programmable 32/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

Quadrature Position/Revolution Counter (QPRC)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. In addition, it can be used as an up/down counter.

- The detection edge for the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Multi-function Timer

The Multi-function Timer consists of the following blocks.

- 16-bit free-run timer × 3 channels
- Input capture × 4 channels
- Output compare × 6 channels
- ADC start compare × 6 channel
- Waveform generator × 3 channels
- 16-bit PPG timer × 3 channels

  IGBT mode is contained.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- ADC start function
- DTIF (motor emergency stop) interrupt function

Real-time Clock (RTC)

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 01 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

Watch Counter

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

External Interrupt Controller Unit

- Up to 8 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

Watchdog Timer (2 channels)

The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, "hardware" watchdog and "software" watchdog.

The "hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the "hardware" watchdog is active in any low-power consumption modes except RTC mode and STOP mode.

Clock and Reset

- Clocks

A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

  - Main clock : 4 MHz to 40MHz
  - Sub clock : 32.768 kHz
  - Built-in high-speed CR clock : 4 MHz
  - Built-in low-speed CR clock : 100 kHz
  - Main PLL clock

- Resets
  - Reset request from the INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detection reset
  - Clock supervisor reset

Clock Supervisor (CSV)

The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

- If an external clock failure (clock stop) is detected, a reset is asserted.
- If an external frequency anomaly is detected, an interrupt or a reset is asserted.

Low-voltage Detector (LVD)

This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

- LVD1: error reporting via an interrupt
- LVD2: auto-reset operation

Low Power Consumption Mode

This series has four low power consumption modes.

- SLEEP
- TIMER
- RTC
- STOP

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

Debug

- Serial Wire Debug Port (SW-DP)
- Micro Trace Buffer (MTB)

Unique ID

A 41-bit unique value of the device has been set.

Power Supply

Wide voltage range: VCC = 2.7 V to 5.5 V

3. Product Lineup

Memory size

Product name	**S6E1A11B0A** **S6E1A11C0A**	**S6E1A12B0A** **S6E1A12C0A**
On-chip Flash memory	56 Kbyte	88 Kbyte
On-chip SRAM	6 Kbyte	6 Kbyte

Function

<table>
<tr><th colspan="3">Product name</th><th>S6E1A11B0A
S6E1A12B0A</th><th>S6E1A11C0A
S6E1A12C0A</th></tr>
<tr><td colspan="3">Pin count</td><td>32</td><td>48/52</td></tr>
<tr><td rowspan="2">CPU</td><td colspan="2"></td><td colspan="2">Cortex-M0+</td></tr>
<tr><td colspan="2">Frequency</td><td colspan="2">40 MHz</td></tr>
<tr><td colspan="3">Power supply voltage range</td><td colspan="2">2.7 V to 5.5 V</td></tr>
<tr><td colspan="3">DMAC</td><td colspan="2">2 ch.</td></tr>
<tr><td colspan="3">Multi-function Serial Interface
(UART/CSIO/I^{2}C)</td><td colspan="2">3 ch. (Max)
ch.0/ch.1/ch.3: FIFO</td></tr>
<tr><td colspan="3">Base Timer
(PWC/Reload timer/PWM/PPG)</td><td colspan="2">4 ch. (Max)</td></tr>
<tr><td rowspan="6">Multi-function Timer</td><td>A/D start compare</td><td>6 ch.</td><td colspan="2" rowspan="6">1 unit</td></tr>
<tr><td>Input capture</td><td>4 ch.</td></tr>
<tr><td>Free-run timer</td><td>3 ch.</td></tr>
<tr><td>Output compare</td><td>6 ch.</td></tr>
<tr><td>Waveform generator</td><td>3 ch.</td></tr>
<tr><td>PPG</td><td>3 ch.</td></tr>
<tr><td colspan="3">QPRC</td><td colspan="2">1 ch.</td></tr>
<tr><td colspan="3">Dual Timer</td><td colspan="2">1 unit</td></tr>
<tr><td colspan="3">Real-time Clock</td><td colspan="2">1 unit</td></tr>
<tr><td colspan="3">Watch Counter</td><td colspan="2">1 unit</td></tr>
<tr><td colspan="3">Watchdog timer</td><td colspan="2">1 ch. (SW) + 1 ch. (HW)</td></tr>
<tr><td colspan="3">External Interrupt</td><td colspan="2">8 pins (Max) + NMI × 1</td></tr>
<tr><td colspan="3">I/O port</td><td>23 pins (Max)</td><td>37 pins (Max)</td></tr>
<tr><td colspan="3">12-bit A/D converter</td><td>5 ch. (1 unit)</td><td>8 ch. (1 unit)</td></tr>
<tr><td colspan="3">CSV (Clock Supervisor)</td><td colspan="2">Yes</td></tr>
<tr><td colspan="3">LVD (Low-voltage Detection)</td><td colspan="2">2 ch.</td></tr>
<tr><td rowspan="2">Built-in CR</td><td colspan="2">High-speed</td><td colspan="2">4 MHz</td></tr>
<tr><td colspan="2">Low-speed</td><td colspan="2">100 kHz</td></tr>
<tr><td colspan="3">Debug Function</td><td colspan="2">SW-DP</td></tr>
<tr><td colspan="3">Unique ID</td><td colspan="2">Yes</td></tr>
</table>

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
  See "14. ELECTRICAL CHARACTERISTICS 14.4 AC Characteristics 14.4.3 Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

4. Packages

Product name / Package	S6E1A11B0A S6E1A12B0A	S6E1A11C0A S6E1A12C0A
LQFP: FPT-32P-M30 (0.80 mm pitch)	❍	-
QFN: LCC-32P-M73 (0.50 mm pitch)	❍	-
LQFP: FPT-48P-M49 (0.50 mm pitch)	-	❍
QFN: LCC-48P-M74 (0.50 mm pitch)	-	❍
LQFP: FPT-52P-M02 (0.65 mm pitch)	-	❍

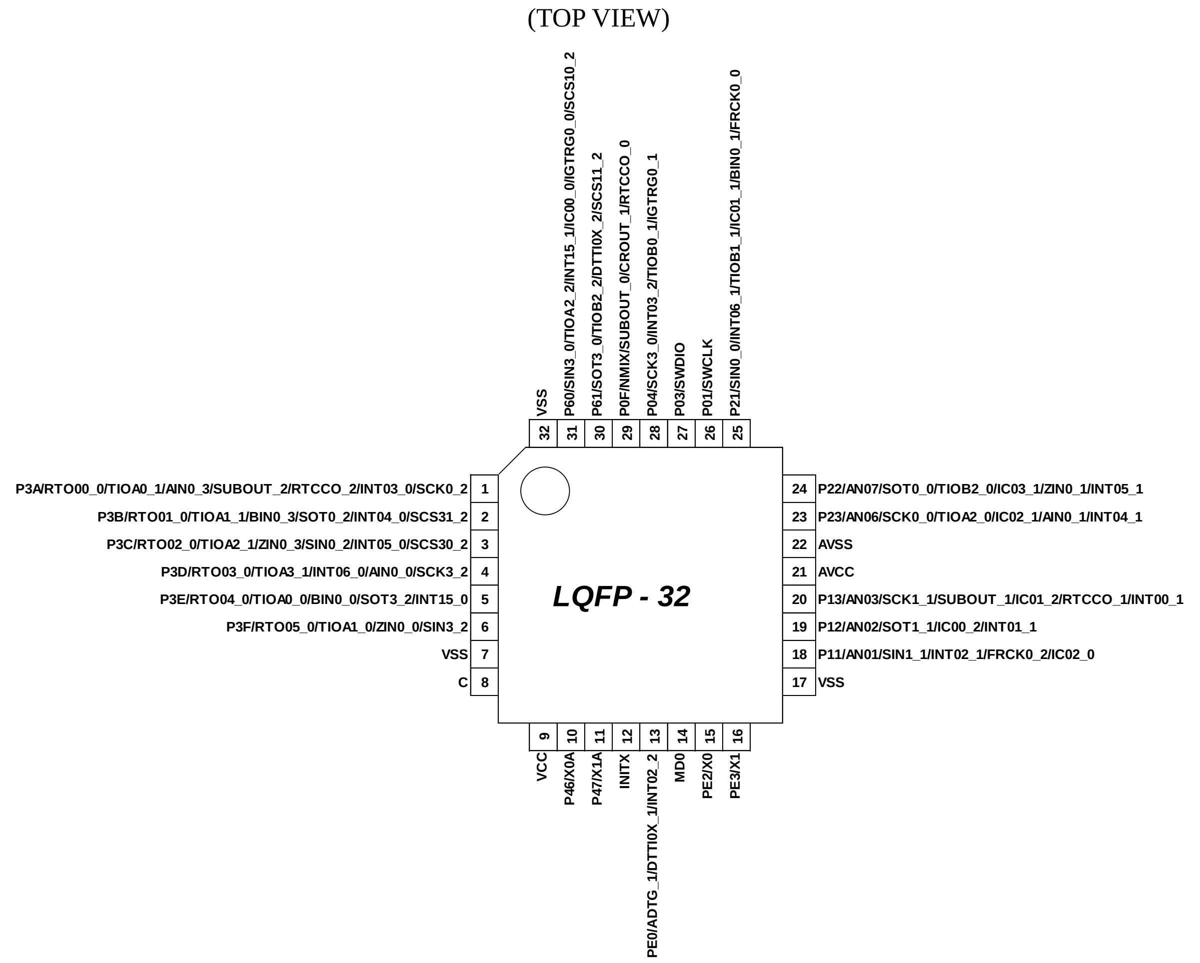
❍: Available

Note:

- *See "16. Package Dimensions" for detailed information on each package.*

5. Pin Assignment

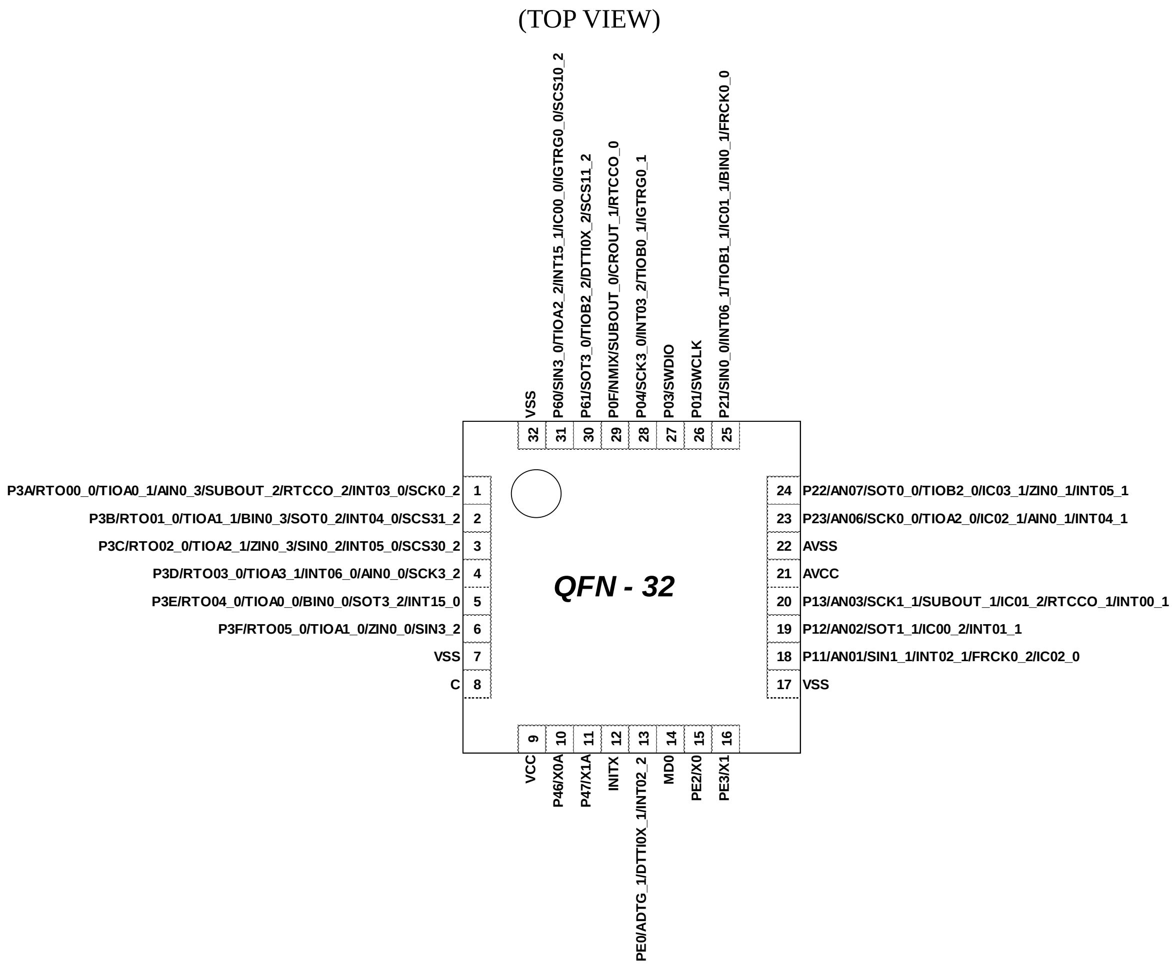
FPT-32P-M30



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

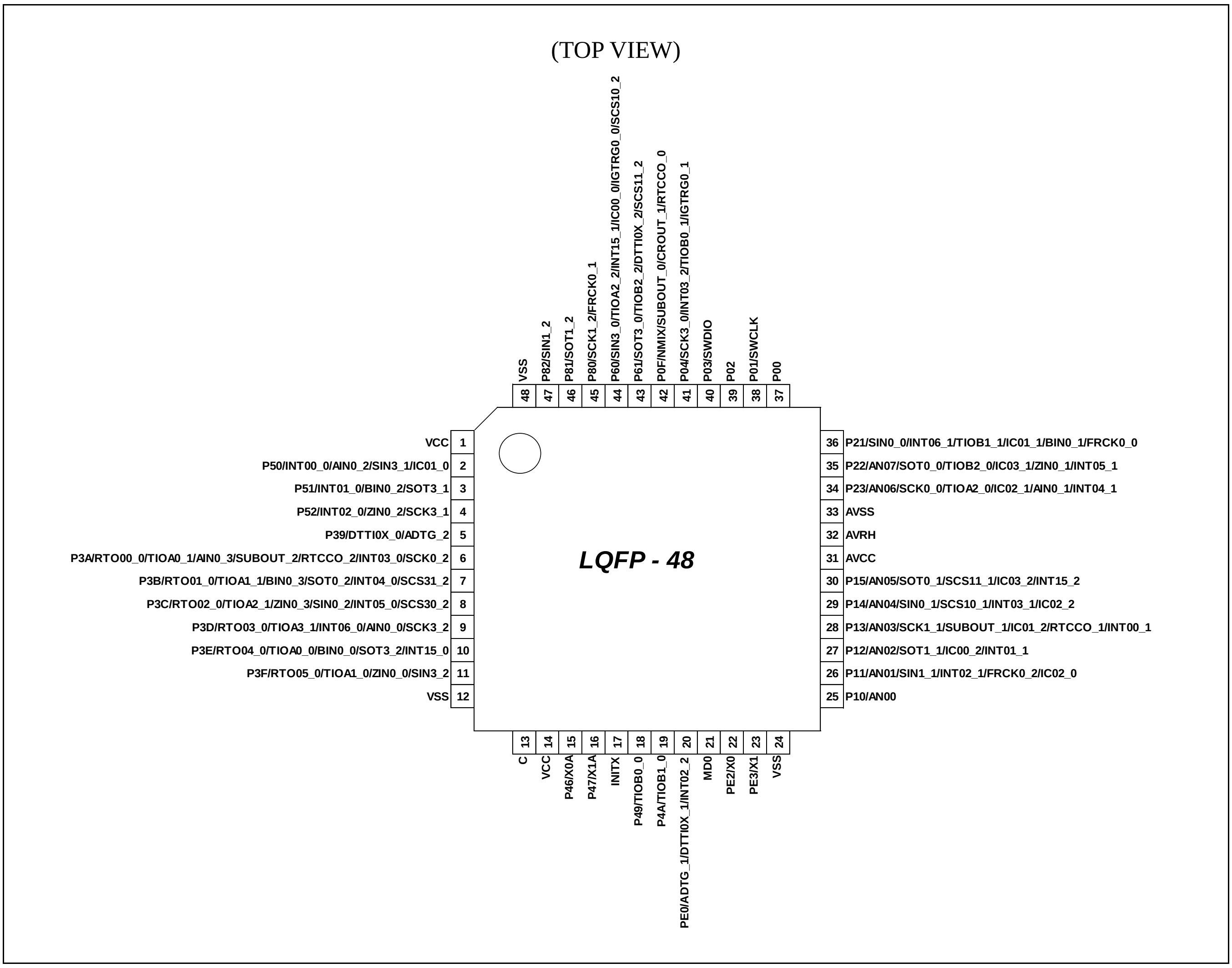
LCC-32P-M73



Note:

- The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

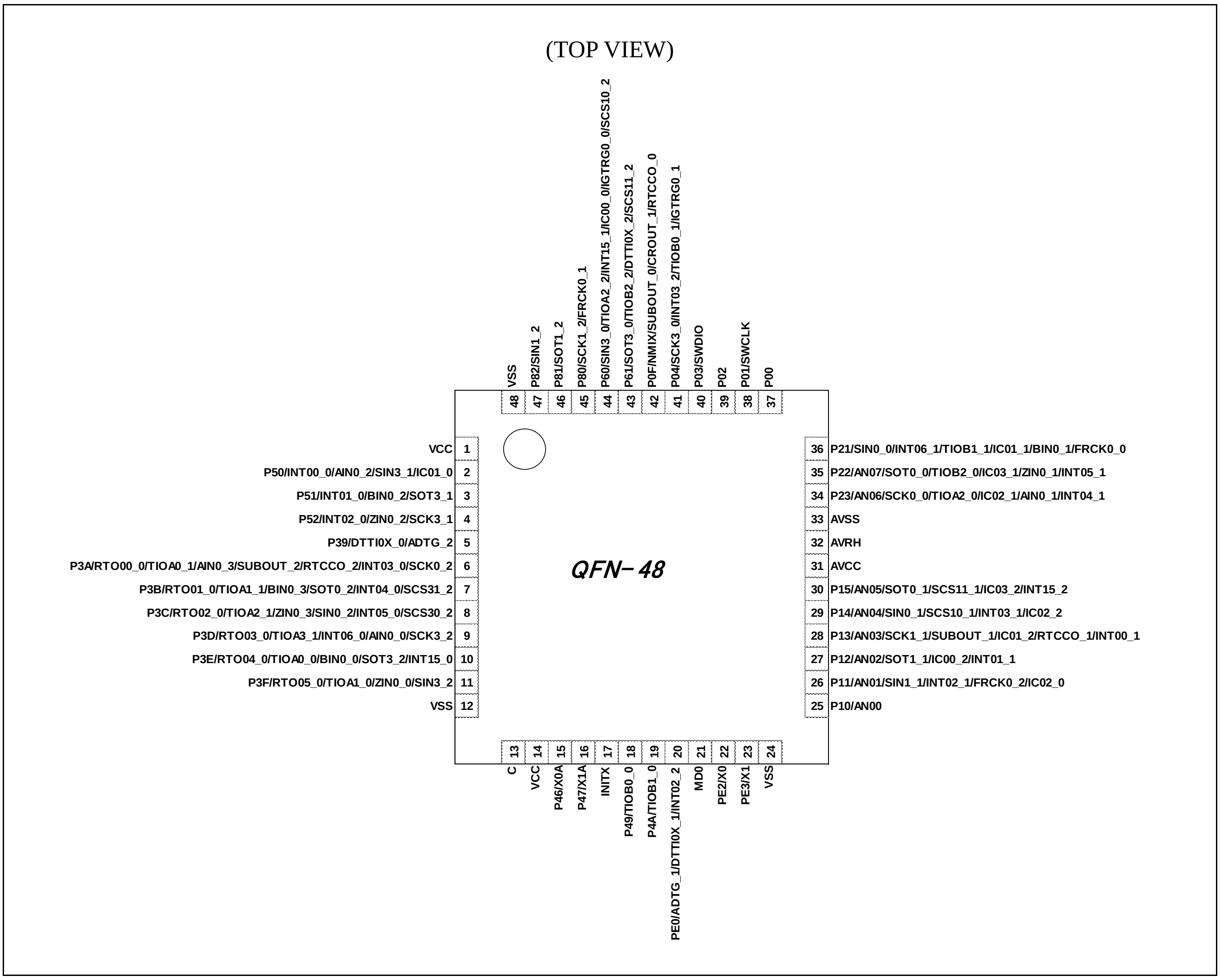
FPT-48P-M49



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

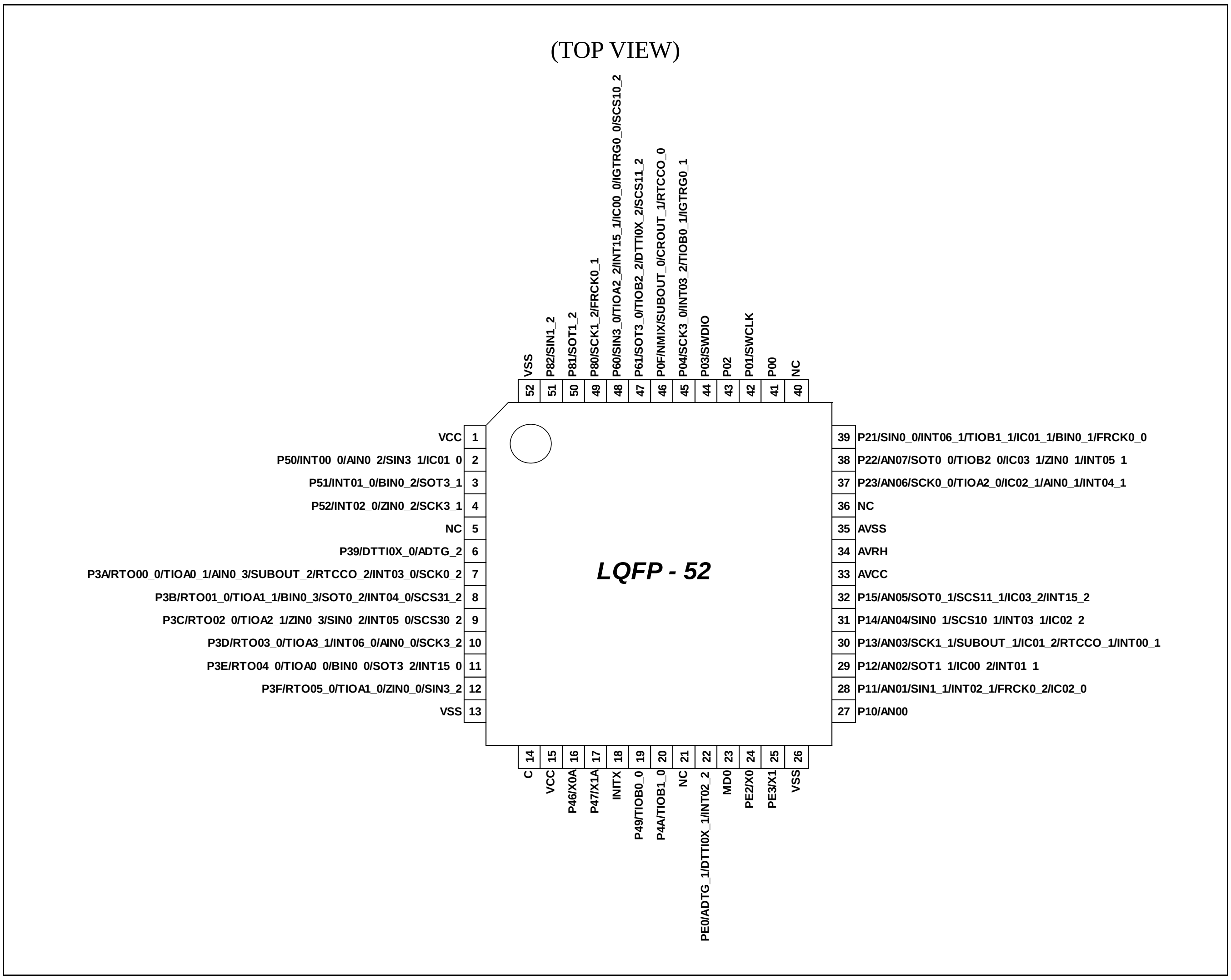
LCC-48P-M74



Note:

- The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

FPT-52P-M02



Note:

- *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

6. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
1	1	-	VCC	-	
2	2	-	P50	I*	J
			INT00_0		
			AIN0_2		
			SIN3_1		
			IC01_0		
3	3	-	P51	I*	J
			INT01_0		
			BIN0_2		
			SOT3_1		
4	4	-	P52	I*	J
			INT02_0		
			ZIN0_2		
			SCK3_1		
6	5	-	P39	E	I
			DTTI0X_0		
			ADTG_2		
7	6	1	P3A	F	J
			RTO00_0		
			TIOA0_1		
			AIN0_3		
			SUBOUT_2		
			RTCCO_2		
			INT03_0		
			SCK0_2		
8	7	2	P3B	F	J
			RTO01_0		
			TIOA1_1		
			BIN0_3		
			SOT0_2		
			INT04_0		
			SCS31_2		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
9	8	3	P3C RTO02_0 TIOA2_1 ZIN0_3 SIN0_2 INT05_0 SCS30_2	F	J
10	9	4	P3D RTO03_0 TIOA3_1 INT06_0 AIN0_0 SCK3_2	F	J
11	10	5	P3E RTO04_0 TIOA0_0 BIN0_0 SOT3_2 INT15_0	F	J
12	11	6	P3F RTO05_0 TIOA1_0 ZIN0_0 SIN3_2	F	I
13	12	7	VSS	-	
14	13	8	C	-	
15	14	9	VCC	-	
16	15	10	P46 X0A	D	E
17	16	11	P47 X1A	D	F
18	17	12	INITX	B	C
19	18	-	P49 TIOB0_0	E	I
20	19	-	P4A TIOB1_0	E	I
22	20	13	PE0 ADTG_1 DTTI0X_1 INT02_2	C	J

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
23	21	14	MD0	J	D
24	22	15	PE2	A	A
			X0		
25	23	16	PE3	A	B
			X1		
26	24	17	VSS	-	
27	25	-	P10	G	K
			AN00		
28	26	18	P11	H*	L
			AN01		
			SIN1_1		
			INT02_1		
			FRCK0_2		
			IC02_0		
29	27	19	P12	H*	L
			AN02		
			SOT1_1		
			IC00_2		
			INT01_1		
30	28	20	P13	H*	L
			AN03		
			SCK1_1		
			SUBOUT_1		
			IC01_2		
			RTCCO_1		
			INT00_1		
31	29	-	P14	H*	L
			AN04		
			SIN0_1		
			SCS10_1		
			INT03_1		
			IC02_2		
32	30	-	P15	H*	L
			AN05		
			SOT0_1		
			SCS11_1		
			IC03_2		
			INT15_2		
33	31	21	AVCC	-	
34	32	-	AVRH	-	

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32			
35	33	22	AVSS	-	
37	34	23	P23	G	L
			AN06		
			SCK0_0		
			TIOA2_0		
			IC02_1		
			AIN0_1		
			INT04_1		
38	35	24	P22	G	L
			AN07		
			SOT0_0		
			TIOB2_0		
			IC03_1		
			ZIN0_1		
			INT05_1		
39	36	25	P21	E	J
			SIN0_0		
			INT06_1		
			TIOB1_1		
			IC01_1		
			BIN0_1		
			FRCK0_0		
41	37	-	P00	E	I
42	38	26	P01	E	H
			SWCLK		
43	39	-	P02	E	I
44	40	27	P03	E	H
			SWDIO		
45	41	28	P04	I*	J
			SCK3_0		
			INT03_2		
			TIOB0_1		
			IGTRG0_1		
46	42	29	P0F	E	G
			NMIX		
			SUBOUT_0		
			CROUT_1		
			RTCCO_0		

Pin no.			Pin name	I/O circuit type	Pin state type
LQFP-52	**LQFP-48** **QFN-48**	**LQFP-32** **QFN-32**			
47	43	30	P61	I*	I
			SOT3_0		
			TIOB2_2		
			DTTI0X_2		
			SCS11_2		
48	44	31	P60	I*	J
			SIN3_0		
			TIOA2_2		
			INT15_1		
			IC00_0		
			IGTRG0_0		
			SCS10_2		
49	45	-	P80	K	I
			SCK1_2		
			FRCK0_1		
50	46	-	P81	K	I
			SOT1_2		
51	47	-	P82	K	I
			SIN1_2		
52	48	32	VSS	-	
5,21,36,40	-	-	NC	-	

*: 5V tolerant I/O

List of pin functions

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin function	**Pin name**	**Function description**	**Pin no.**		
			LQFP-52	**LQFP-48 QFN-48**	**LQFP-32 QFN-32**
ADC	ADTG_1	A/D converter external trigger input pin	22	20	13
	ADTG_2		6	5	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	27	25	-
	AN01		28	26	18
	AN02		29	27	19
	AN03		30	28	20
	AN04		31	29	-
	AN05		32	30	-
	AN06		37	34	23
	AN07		38	35	24
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	11	10	5
	TIOA0_1		7	6	1
	TIOB0_0	Base timer ch.0 TIOB pin	19	18	-
	TIOB0_1		45	41	28
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	12	11	6
	TIOA1_1		8	7	2
	TIOB1_0	Base timer ch.1 TIOB pin	20	19	-
	TIOB1_1		39	36	25
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	37	34	23
	TIOA2_1		9	8	3
	TIOA2_2		48	44	31
	TIOB2_0	Base timer ch.2 TIOB pin	38	35	24
	TIOB2_2		47	43	30
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	10	9	4
Debugger	SWCLK	Serial wire debug interface clock input pin	42	38	26
	SWDIO	Serial wire debug interface data input / output pin	44	40	27

Pin function	Pin name	Function description	Pin no.		
			LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	-
	INT00_1		30	28	20
	INT01_0	External interrupt request 01 input pin	3	3	-
	INT01_1		29	27	19
	INT02_0	External interrupt request 02 input pin	4	4	-
	INT02_1		28	26	18
	INT02_2		22	20	13
	INT03_0	External interrupt request 03 input pin	7	6	1
	INT03_1		31	29	-
	INT03_2		45	41	28
	INT04_0	External interrupt request 04 input pin	8	7	2
	INT04_1		37	34	23
	INT05_0	External interrupt request 05 input pin	9	8	3
	INT05_1		38	35	24
	INT06_0	External interrupt request 06 input pin	10	9	4
	INT06_1		39	36	25
	INT15_0	External interrupt request 15 input pin	11	10	5
	INT15_1		48	44	31
	INT15_2		32	30	-
	NMIX	Non-Maskable Interrupt input pin	46	42	29
GPIO	P00	General-purpose I/O port 0	41	37	-
	P01		42	38	26
	P02		43	39	-
	P03		44	40	27
	P04		45	41	28
	P0F		46	42	29
	P10	General-purpose I/O port 1	27	25	-
	P11		28	26	18
	P12		29	27	19
	P13		30	28	20
	P14		31	29	-
	P15		32	30	-
	P21	General-purpose I/O port 2	39	36	25
	P22		38	35	24
	P23		37	34	23
	P39	General-purpose I/O port 3	6	5	-
	P3A		7	6	1
	P3B		8	7	2
	P3C		9	8	3
	P3D		10	9	4
	P3E		11	10	5
	P3F		12	11	6

Pin function	Pin name	Function description	Pin no.		
			LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32
GPIO	P46	General-purpose I/O port 4	16	15	10
	P47		17	16	11
	P49		19	18	-
	P4A		20	19	-
	P50	General-purpose I/O port 5	2	2	-
	P51		3	3	-
	P52		4	4	-
	P60	General-purpose I/O port 6	48	44	31
	P61		47	43	30
	P80	General-purpose I/O port 8	49	45	-
	P81		50	46	-
	P82		51	47	-
	PE0*	General-purpose I/O port E	22	20	13
	PE2		24	22	15
	PE3		25	23	16
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	39	36	25
	SIN0_1		31	29	-
	SIN0_2		9	8	3
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA0 when used as an I^2C pin (operation mode 4).	38	35	24
	SOT0_1 (SDA0_1)		32	30	-
	SOT0_2 (SDA0_2)		8	7	2
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when used as a CSIO pin (operation mode 2) and as SCL0 when used as an I^2C pin (operation mode 4).	37	34	23
	SCK0_2 (SCL0_2)		7	6	1
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	28	26	18
	SIN1_2		51	47	-
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA1 when used as an I^2C pin (operation mode 4).	29	27	19
	SOT1_2 (SDA1_2)		50	46	-
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when used as a CSIO pin (operation mode 2) and as SCL1 when used as an I^2C pin (operation mode 4).	30	28	20
	SCK1_2 (SCL1_2)		49	45	-
	SCS10_1	Multi-function serial interface ch.1 serial chip select 0 output/input pin.	31	29	-
	SCS10_2		48	44	31
	SCS11_1	Multi-function serial interface ch.1 serial chip select 1 output pin.	32	30	-
	SCS11_2		47	43	30

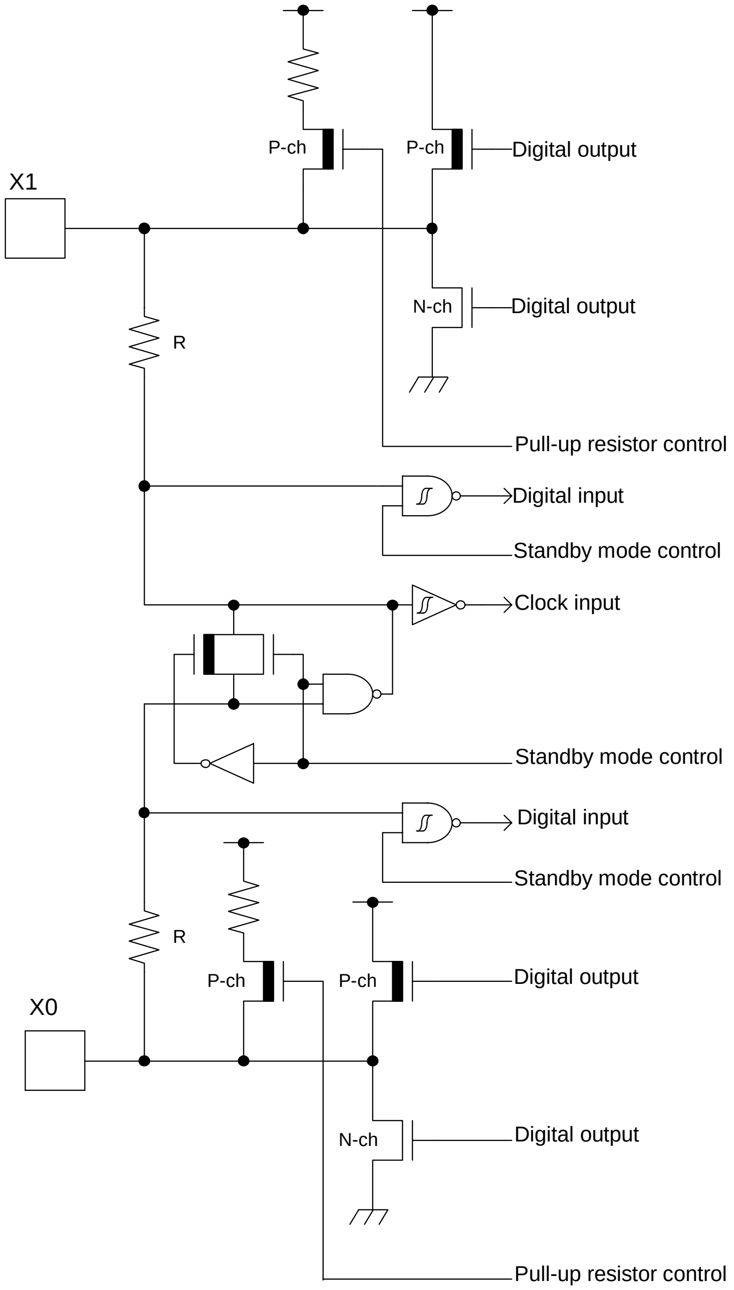
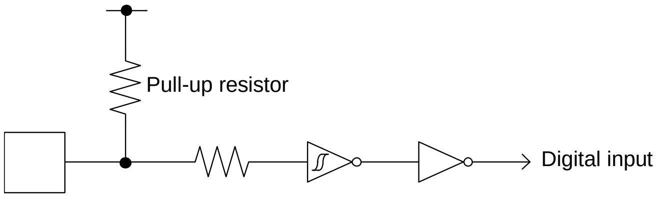
Pin function	Pin name	Function description	Pin no.		
			LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	48	44	31
	SIN3_1		2	2	-
	SIN3_2		12	11	6
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I^{2}C pin (operation mode 4).	47	43	30
	SOT3_1 (SDA3_1)		3	3	-
	SOT3_2 (SDA3_2)		11	10	5
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I^{2}C pin (operation mode 4).	45	41	28
	SCK3_1 (SCL3_1)		4	4	-
	SCK3_2 (SCL3_2)		10	9	4
	SCS30_2	Multi-function serial interface ch.3 serial chip select 0 input/output pin.	9	8	3
	SCS31_2	Multi-function serial interface ch.3 serial chip select 1 output pin.	8	7	2

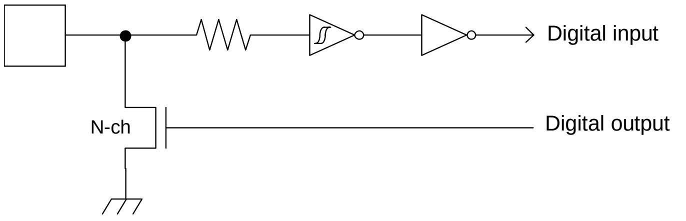
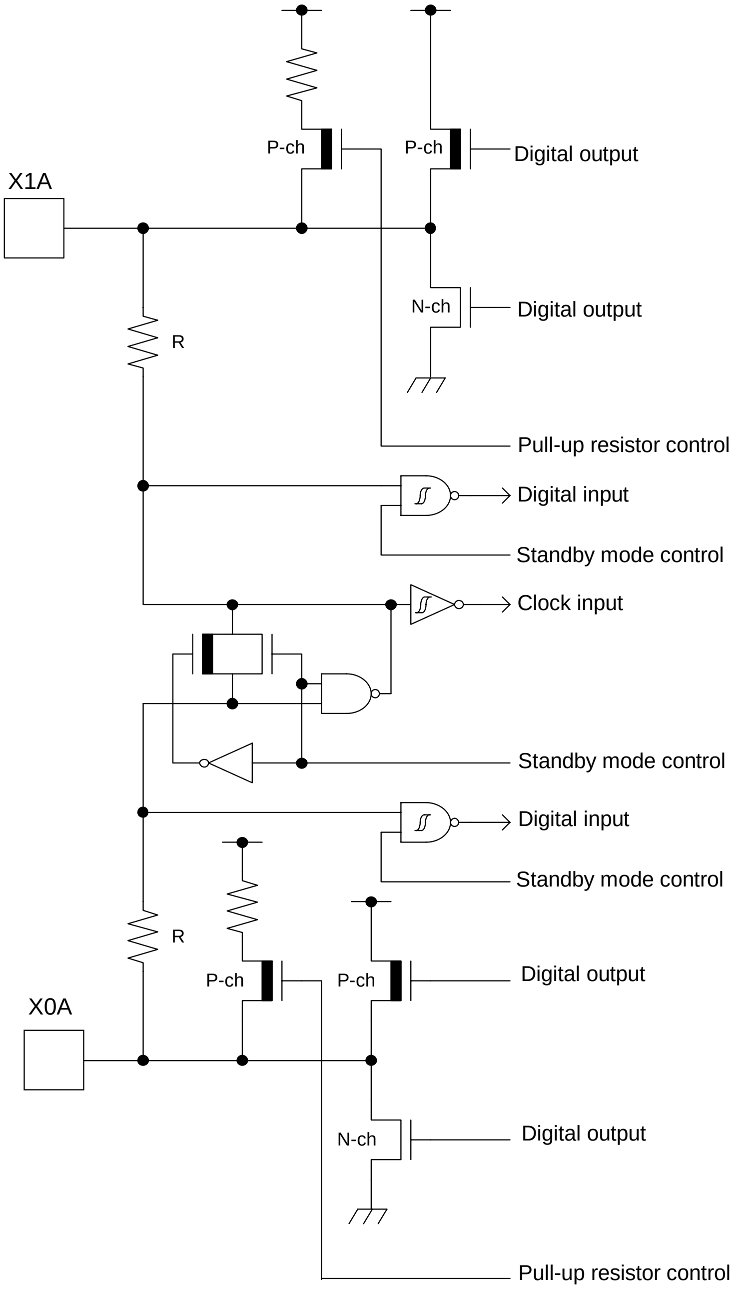
Pin function	Pin name	Function description	Pin no.		
			LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator controlling RTO00 to RTO05 outputs of Multi-function Timer 0.	6	5	-
	DTTI0X_1		22	20	13
	DTTI0X_2		47	43	30
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin.	39	36	25
	FRCK0_1		49	45	-
	FRCK0_2		28	26	18
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	48	44	31
	IC00_2		29	27	19
	IC01_0		2	2	-
	IC01_1		39	36	25
	IC01_2		30	28	20
	IC02_0		28	26	18
	IC02_1		37	34	23
	IC02_2		31	29	-
	IC03_1		38	35	24
	IC03_2		32	30	-
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	7	6	1
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	8	7	2
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	9	8	3
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	10	9	4
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	11	10	5
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	12	11	6
	IGTRG0_0	PPG IGBT mode external trigger input pin	48	44	31
	IGTRG0_1		45	41	28

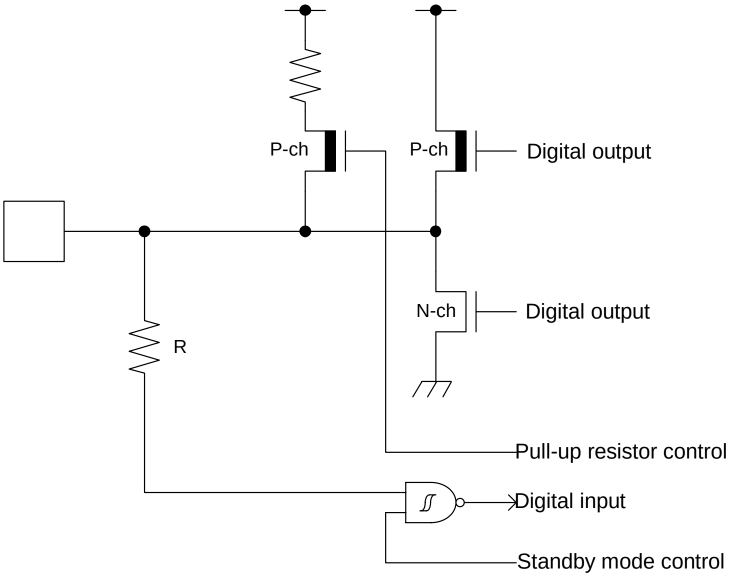
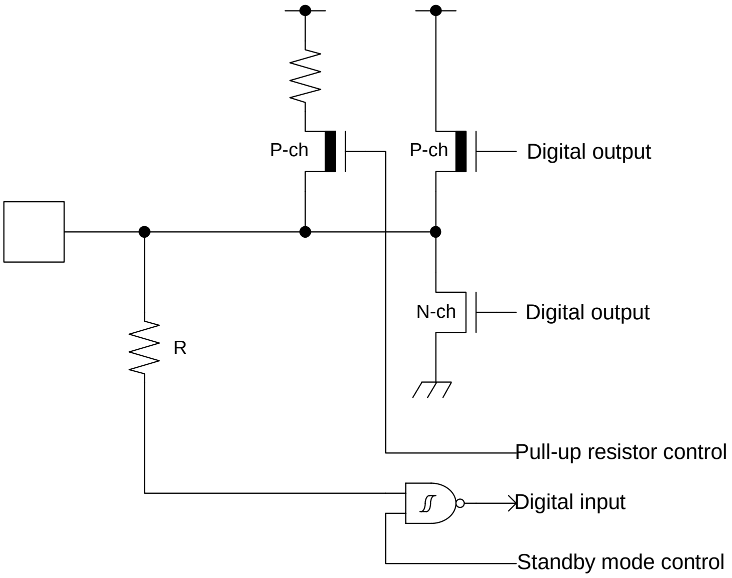
Pin function	Pin name	Function description	Pin no.		
			LQFP-52	LQFP-48 QFN-48	LQFP-32 QFN-32
Quadrature Position/ Revolution Counter	AIN0_0	QPRC ch.0 AIN input pin	10	9	4
	AIN0_1		37	34	23
	AIN0_2		2	2	-
	AIN0_3		7	6	1
	BIN0_0	QPRC ch.0 BIN input pin	11	10	5
	BIN0_1		39	36	25
	BIN0_2		3	3	-
	BIN0_3		8	7	2
	ZIN0_0	QPRC ch.0 ZIN input pin	12	11	6
	ZIN0_1		38	35	24
	ZIN0_2		4	4	-
	ZIN0_3		9	8	3
Real-time clock	RTCCO_0	0.5-seconds pulse output pin of Real-time clock	46	42	29
	RTCCO_1		30	28	20
	RTCCO_2		7	6	1
	SUBOUT_0	Sub clock output pin	46	42	29
	SUBOUT_1		30	28	20
	SUBOUT_2		7	6	1
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	18	17	12
Mode	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	23	21	14
POWER	VCC	Power supply pin	1	1	-
	VCC	Power supply pin	15	14	9
GND	VSS	GND pin	13	12	7
	VSS	GND pin	26	24	17
	VSS	GND pin	52	48	32
CLOCK	X0	Main clock (oscillation) input pin	24	22	15
	X0A	Sub clock (oscillation) input pin	16	15	10
	X1	Main clock (oscillation) I/O pin	25	23	16
	X1A	Sub clock (oscillation) I/O pin	17	16	11
	CROUT_1	Built-in high-speed CR oscillation clock output port	46	42	29
Analog POWER	AVCC	A/D converter analog power supply pin	33	31	21
	AVRH	A/D converter analog reference voltage input pin	34	32	-
Analog GND	AVSS	A/D converter analog reference voltage input pin	35	33	22
C pin	C	Power supply stabilization capacitance pin	14	13	8

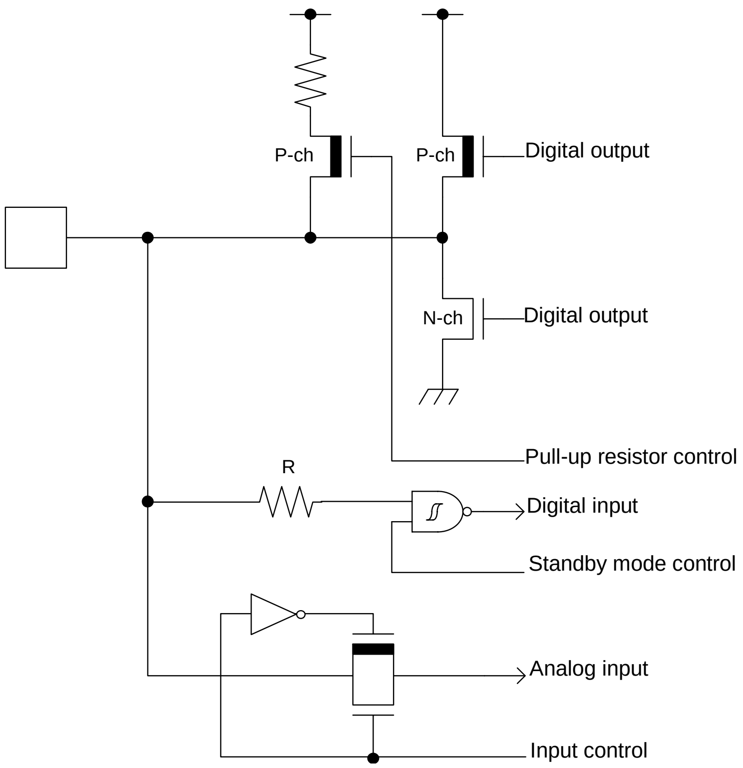
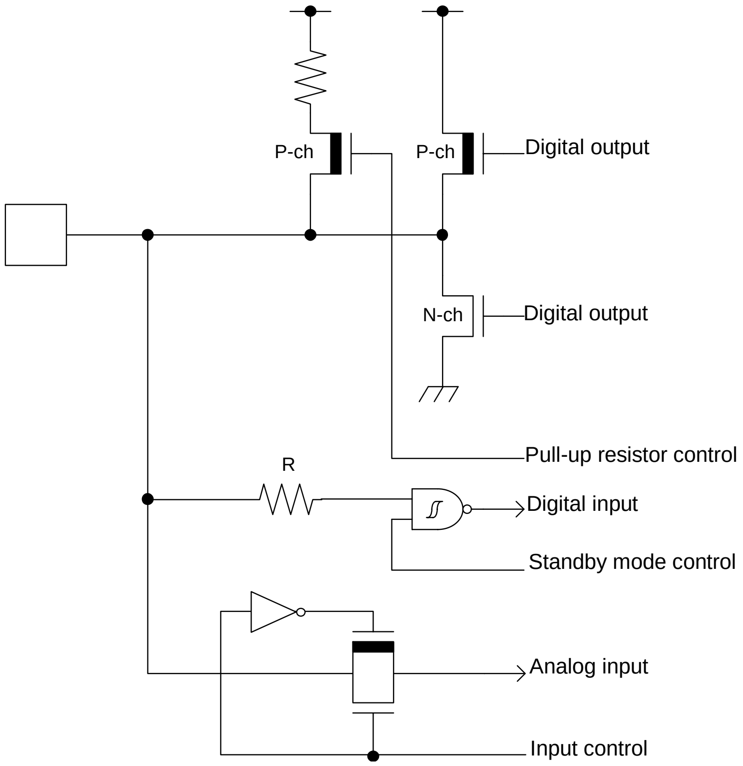
*: PE0 is an open drain pin, cannot output high.

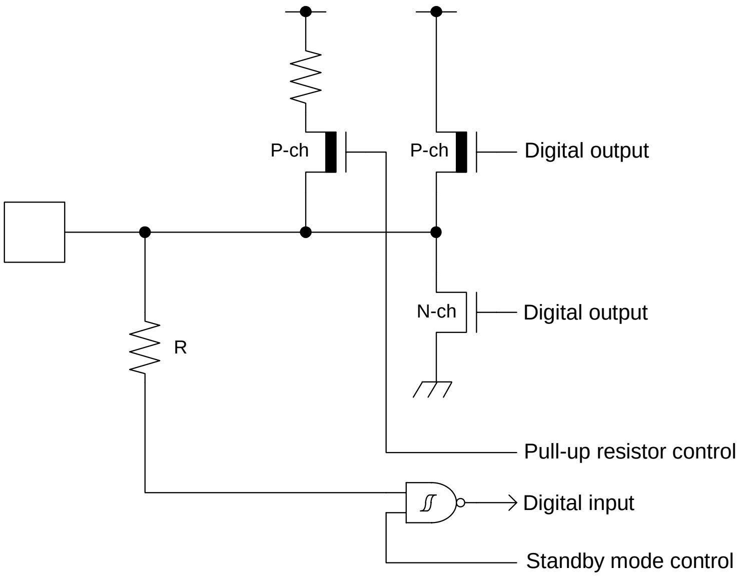
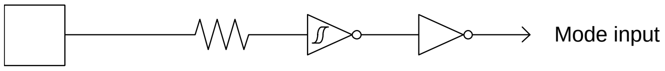
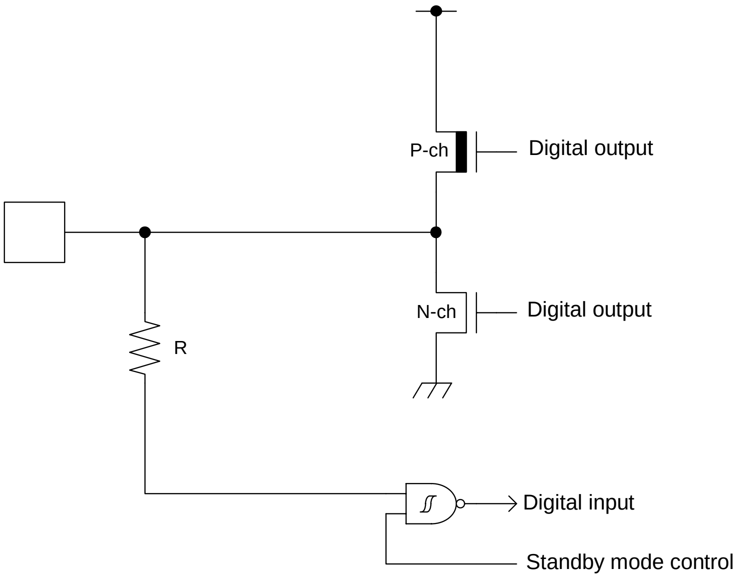
7. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. − Oscillation feedback resistor : Approximately 1MΩ − With standby mode control When the GPIO is selected. − CMOS level output. − CMOS level hysteresis input − With pull-up resistor control − With standby mode control − Pull-up resistor : Approximately 50kΩ − I_{OH}= -4mA, I_{OL}= 4mA
B		− CMOS level hysteresis input − Pull-up resistor : Approximately 50kΩ

Type	Circuit	Remarks
C		– Open drain output – CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. – Oscillation feedback resistor : Approximately 5MΩ – With standby mode control When the GPIO is selected. – CMOS level output. – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50kΩ – I_{OH}= -4mA, I_{OL}= 4mA

Type	Circuit	Remarks
E		− CMOS level output − CMOS level hysteresis input − With pull-up resistor control − With standby mode control − Pull-up resistor : Approximately 50kΩ − I_{OH}= -4mA, I_{OL}= 4mA − When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
F		− CMOS level output − CMOS level hysteresis input − With pull-up resistor control − With standby mode control − Pull-up resistor : Approximately 50kΩ − I_{OH}= -12mA, I_{OL}= 12mA − When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
G		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50kΩ – I_{OH}= -4mA, I_{OL}= 4mA – When this pin is used as an I^{2}C pin, the digital output P-ch transistor is always off
H		– CMOS level output – CMOS level hysteresis input – With input control – Analog input – 5V tolerant – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50kΩ – I_{OH}= -4mA, I_{OL}= 4mA – Available to control of PZR registers. – When this pin is used as an I^{2}C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
I		– CMOS level output – CMOS level hysteresis input – 5V tolerant – With pull-up resistor control – With standby mode control – Pull-up resistor : Approximately 50kΩ – I_{OH}= -4mA, I_{OL}= 4mA – Available to control PZR registers – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input
K		– CMOS level output – CMOS level hysteresis input – With standby mode control – I_{OH}= -4mA, I_{OL}= 4mA – When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

8. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

8.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Code: DS00-00004-2Ea

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

8.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

8.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Spansion products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.
http://www.spansion.com/fjdocuments/fj/datasheet/e-ds/DS00-00004.pdf

9. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin near this device.

Stabilizing supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub crystal oscillator

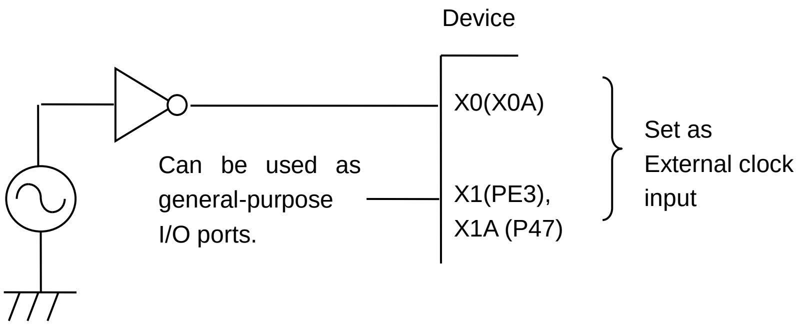
This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  Size: More than 3.2mm × 1.5mm
  Load capacitance: Approximately 6pF to 7pF
- Lead type
  Load capacitance: Approximately 6pF to 7pF

Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

Example of Using an External Clock

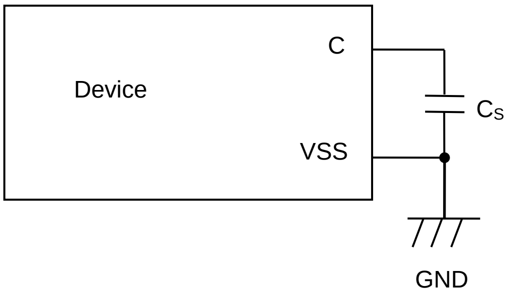


Handling when using Multi-function serial pin as I²C pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7μF would be recommended for this series.



Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on power-on

Turn power on/off in the following order or at the same time.

Turning on :	VCC → AVCC → AVRH
Turning off :	AVRH →AVCC →VCC

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash memory products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

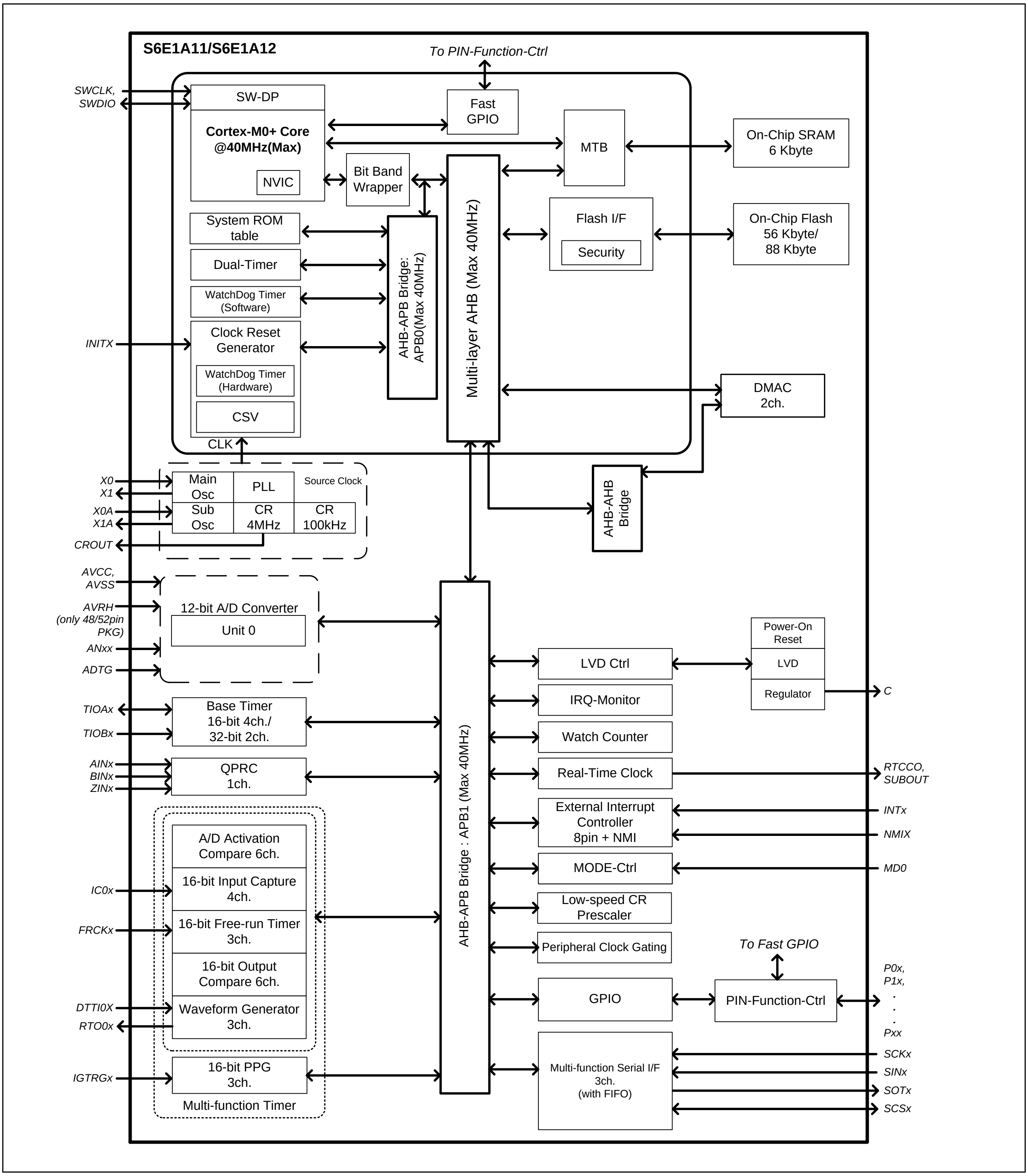
Pull-Up function of 5V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

Handling when using debug pins

When debug pins (SWDIO/SWCLK) are set to GPIO or other peripheral functions, only set them as output, do not set them as input.

10. Block Diagram

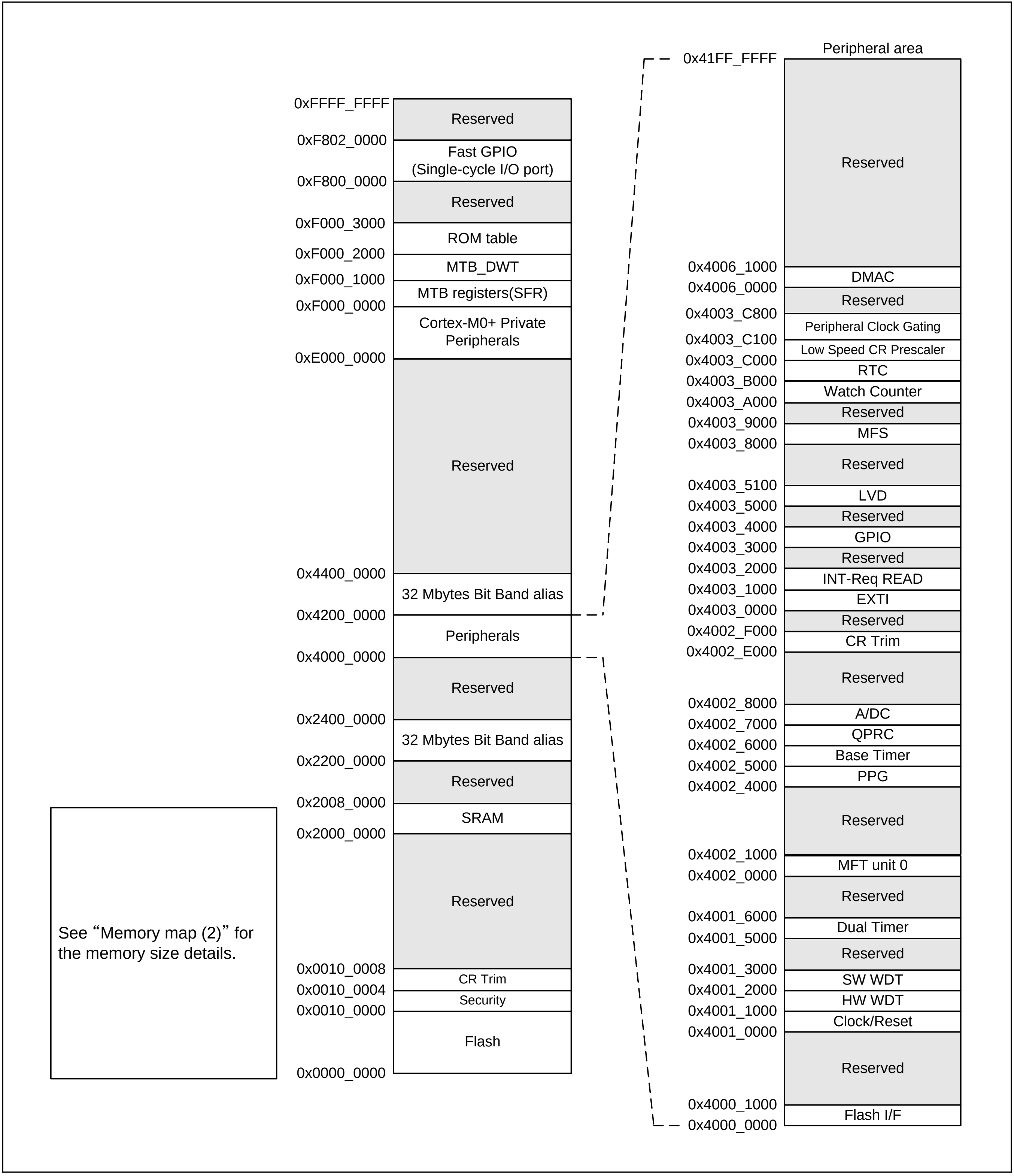


11. Memory Size

See "Memory size" in "3. Product Lineup" to confirm the memory size.

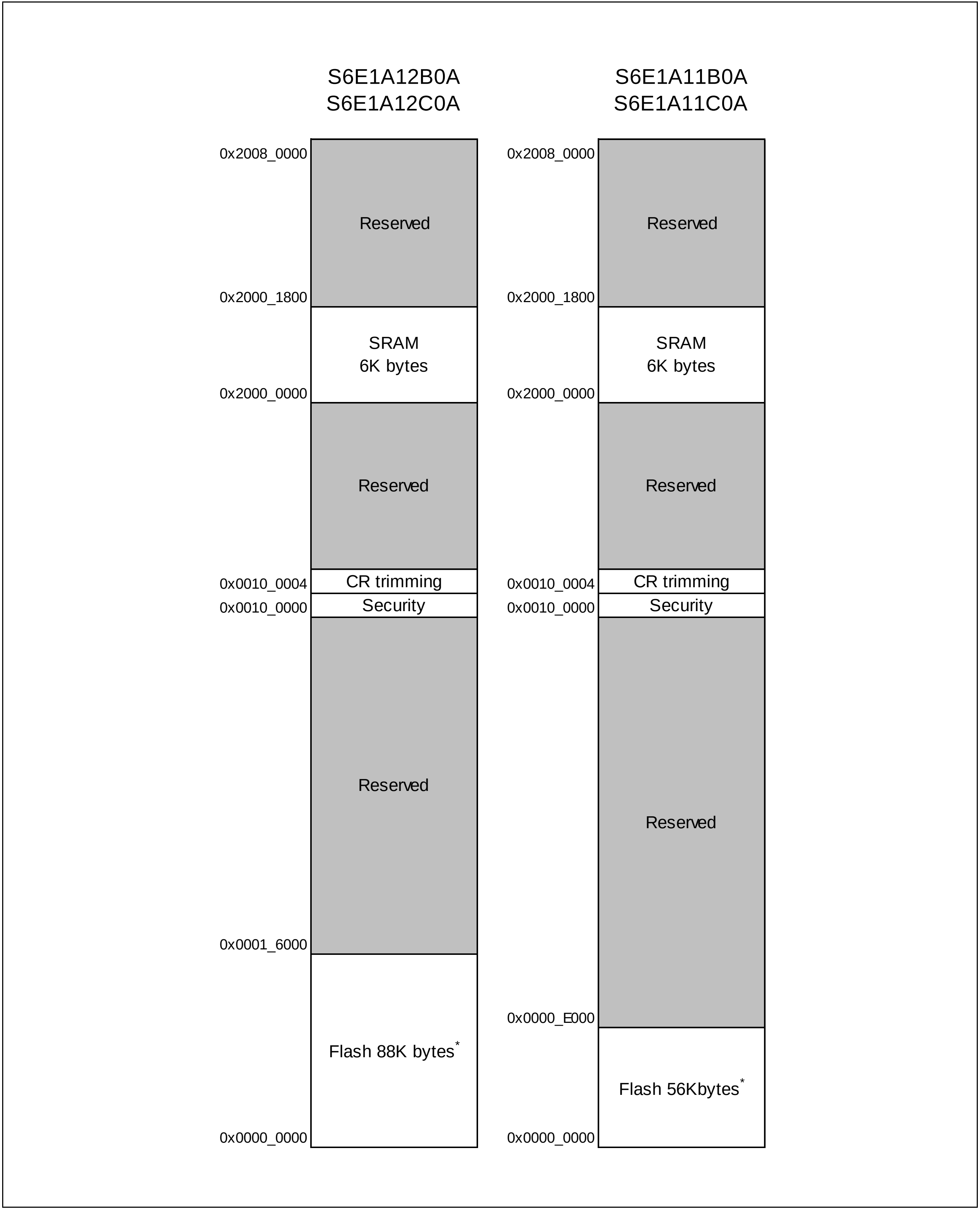
12. Memory Map

Memory map (1)



See “Memory map (2)” for the memory size details.

Memory map (2)



*: See "S6E1A11/S6E1A12 Series Flash Programming Manual" to check details of the Flash memory.

Peripheral Address Map

Start address	End address	Bus	Peripheral
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog Timer
0x4001_2000	0x4001_2FFF		Software Watchdog Timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function Timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF		External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low-Voltage Detection
0x4003_5800	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function Serial Interface
0x4003_9000	0x4003_9FFF		Reserved
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_FFFF		Reserved
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x41FF_FFFF		Reserved

13. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

  This is the period when the INITX pin is the "L" level.

- INITX=1

  This is the period when the INITX pin is the "H" level.

- SPL=0

  This is the status that the standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "0".

- SPL=1

  This is the status that the standby pin level setting bit (SPL) in the Standby Mode Control Register (STB_CTL) is set to "1".

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at "0"

  This is the status that the input function cannot be used. Internal input is fixed at "L".

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state in which a pin was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

List of Pin Status

Pin status type	Function group	State upon power-on reset or low-voltage detection	State at INITX input	State upon device internal reset	State in Run mode or SLEEP mode	State in TIMER mode, RTC mode, or STOP mode	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ Input enabled	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[1], Hi-Z / Internal input fixed at "0"
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ Input enabled	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state/When oscillation stops*[2], Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*[2], Hi-Z / Internal input fixed at "0"

Pin status type	Function group	State upon power-on reset or low-voltage detection	State at INITX input	State upon device internal reset	State in Run mode or SLEEP mode	State in TIMER mode, RTC mode, or STOP mode	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
G	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than the above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"
	GPIO selected						
H	Serial wire debug selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at "0"
I	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	GPIO selected						
J	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than the above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"
	GPIO selected						
K	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Resource other than the above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"
	GPIO selected						
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than the above selected						Hi-Z / Internal input fixed at "0"
	GPIO selected						

*1: Oscillation stops in Sub timer mode, Low-speed CR timer mode, STOP mode, RTC mode.

*2: Oscillation stops in STOP mode.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	Only S6E1A1xC0A
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	Vcc + 0.5 (≤ 6.5 V)	V	
"L" level maximum output current*4	I_{OL}	-	10	mA	4 mA type
			20	mA	12 mA type
"L" level average output current*5	I_{OLAV}	-	4	mA	4 mA type
			12	mA	12 mA type
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current*4	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	12 mA type
"H" level average output current*5	I_{OHAV}	-	- 4	mA	4 mA type
			- 12	mA	12 mA type
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	200	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that V_{SS} = AVss = 0 V.

*2: Vcc must not drop below V_{SS} - 0.5 V.

*3: Ensure that the voltage does not to exceed V_{CC} + 0.5 V at power-on.

*4: The maximum output current is the peak value for a single pin.

*5: The average output is the average current for a single pin over a period of 100 ms.

*6: The total average output current is the average current for all pins over a period of 100 ms.

<WARNING>

– *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

14.2 Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	2.7*[2]	5.5	V	
Analog power supply voltage	AV_{CC}	-	2.7	5.5	V	$AV_{CC} = V_{CC}$
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	Only S6E1A1xC0A
Smoothing capacitor	C_S	-	1	10	μF	For regulator*[1]
Operating temperature	Ta	-	- 40	+ 105	°C	

*1: See "C Pin" in "9. Handling Devices" for the connection of the smoothing capacitor.

*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

<WARNING>

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

14.3 DC Characteristics

14.3.1 Current Rating

Symbol (Pin name)	Conditions		HCLK Frequency*4	Value		Unit	Remarks
				Typ*1	Max*2		
Icc (VCC)	Run mode, code executed from Flash	4MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	0.7	1.5	mA	*3
			8MHz	1.3	2.3		
			20MHz	2.8	4.0		
			40MHz	5.7	7.3		
		4MHz external clock input, PLL ON*8 Benchmark code executed Built-in high speed CR stopped PCLK1 stopped	4MHz	0.6	1.4	mA	*3
			8MHz	1.2	2.1		
			20MHz	2.6	3.7		
			40MHz	4.8	6.3		
		4MHz crystal oscillation, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	1.0	2.9	mA	*3
			8MHz	1.7	3.6		
			20MHz	3.4	5.6		
			40MHz	5.7	8.2		
	Run mode, code executed from RAM	4MHz external clock input, PLL ON*8 NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4MHz	0.5	1.2	mA	*3
			8MHz	0.9	1.8		
			20MHz	2.0	2.9		
			40MHz	3.7	4.8		
	Run mode, code executed from Flash	4MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40MHz	2.8	3.7	mA	*3,*6,*7
	Run mode, code executed from Flash	Built-in high speed CR*5 NOP code executed All peripheral clock stopped by CKENx	4MHz	0.8	1.5	mA	*3
		32kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32kHz	65	900	μA	*3
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100kHz	73	920	μA	*3
Iccs (VCC)	SLEEP operation	4MHz external clock input, PLL ON*8 All peripheral clock stopped by CKENx	4MHz	0.4	1.2	mA	*3
			8MHz	0.7	1.6		
			20MHz	1.5	2.4		
			40MHz	2.7	3.7		
		Built-in high speed CR*5 All peripheral clock stopped by CKENx	4MHz	0.5	1.2	mA	*3
		32kHz crystal oscillation All peripheral clock stopped by CKENx	32kHz	63	880	μA	*3
		Built-in low speed CR All peripheral clock stopped by CKENx	100kHz	66	890	μA	*3

*1 : Ta=+25℃,V_{CC}=3.0V

*2 : Ta=+105℃,V_{CC}=5.5V

*3 : All ports are fixed

*4 : PCLK0=HCLK/8

*5 : The frequency is set to 4MHz by trimming

*6 : Flash sync down is set to FRWTR.RWT = 11 and FSYNDN.SD = 1111

*7 : V_{CC}=2.7V

*8 : When HCLK=4MHz, PLL OFF

Symbol (Pin name)	Conditions		Value		Unit	Remarks
			Typ	Max		
I_{CCH} (VCC)	STOP mode	Ta=25℃ Vcc=3.0V LVD off	5.6	28	µA	*1
		Ta=25℃ Vcc=5.0V LVD off	6.7	30	µA	*1
		Ta=105℃ Vcc=5.5V LVD off	-	540	µA	*1
I_{CCT} (VCC)	Sub timer mode	Ta=25℃ Vcc=3.0V 32kHz crystal oscillation LVD off	12	42	µA	*1
		Ta=25℃ Vcc=5.0V 32kHz crystal oscillation LVD off	13	44	µA	*1
		Ta=105℃ Vcc=5.5V 32kHz crystal oscillation LVD off	-	730	µA	*1
I_{CCR} (VCC)	RTC mode	Ta=25℃ Vcc=3.0V 32kHz crystal oscillation LVD off	9	36	µA	*1
		Ta=25℃ Vcc=5.0V 32kHz crystal oscillation LVD off	10	38	µA	*1
		Ta=105℃ Vcc=5.5V 32kHz crystal oscillation LVD off	-	570	µA	*1

*1: All ports are fixed.

LVD current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	0.13	0.3	μA	For occurrence of reset
				0.13	0.3	μA	For occurrence of interrupt

Flash memory current

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	11.2	mA	

A/D convertor current (S6E1A1xC0A)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	0.7	0.9	mA	
			At stop	0.13	13	μA	
Reference power supply current (AVRH)	I_{CCAVRH}	AVRH	At operation	1.1	1.97	mA	AVRH=5.5V
			At stop	0.1	1.7	μA	

A/D convertor current (S6E1A1xB0A)

(V_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At operation	1.8	2.87	mA	
			At stop	0.23	14.7	μA	

Peripheral current dissipation

Clock system	Peripheral	Conditions	Frequency (MHz)				Unit	Remarks
			4	8	20	40		
HCLK	GPIO	At all ports operation	0.11	0.22	0.55	1.10	mA	
	DMAC	At 2ch operation	0.05	0.11	0.25	0.51		
PCLK1	Base timer	At 4ch operation	0.03	0.05	0.15	0.30	mA	
	Multi-functional timer/PPG	At 1unit/4ch operation	0.14	0.28	0.68	1.38		
	Quadrature position/Revolution counter	At 1unit operation	0.02	0.04	0.11	0.22		
	ADC	At 1unit operation	0.07	0.14	0.37	0.73		
	Multi-function serial	At 1ch operation	0.15	0.31	0.77	1.54		

14.3.2 Pin Characteristics

(V_{CC} =AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, PE0	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
		5V tolerant input pin	-	V_{CC} × 0.8	-	V_{SS} + 5.5	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, PE0	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
"H" level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2 mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
"L" level output voltage	V_{OL}	4 mA type	V_{CC} ≥ 4.5 V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 2 mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			V_{CC} < 4.5 V, I_{OL} = 8 mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	μA	
Pull-up resistance value	R_{PU}	Pull-up pin	V_{CC} ≥ 4.5 V	33	50	90	kΩ	
			V_{CC} < 4.5 V	-	-	180		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

14.4 AC Characteristics

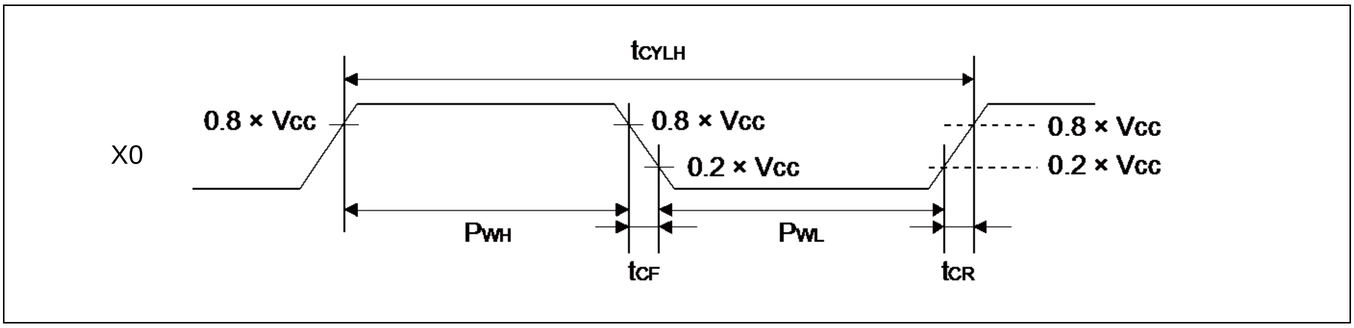
14.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	V_{CC} ≥ 4.5V	4	40	MHz	When the crystal oscillator is connected
			V_{CC} < 4.5V	4	20		
			-	4	40	MHz	When the external clock is used
Input clock cycle	t_{CYLH}		-	25	250	ns	When the external clock is used
Input clock pulse width	-		PWH/tCYLH, PWL/tCYLH	45	55	%	When the external clock is used
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When the external clock is used
Internal operating clock[*1] frequency	F_{CM}	-	-	-	41.2	MHz	Master clock
	F_{CC}	-	-	-	41.2	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	41.2	MHz	APB0 bus clock[*2]
	F_{CP1}	-	-	-	41.2	MHz	APB1 bus clock[*2]
Internal operating clock[*1] cycle time	t_{CYCC}	-	-	24.27	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	24.27	-	ns	APB0 bus clock[*2]
	t_{CYCP1}	-	-	24.27	-	ns	APB1 bus clock[*2]

*1: For details of each internal operating clock, refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

*2: For details of the APB bus to which a peripheral is connected, see "10. Block Diagram".

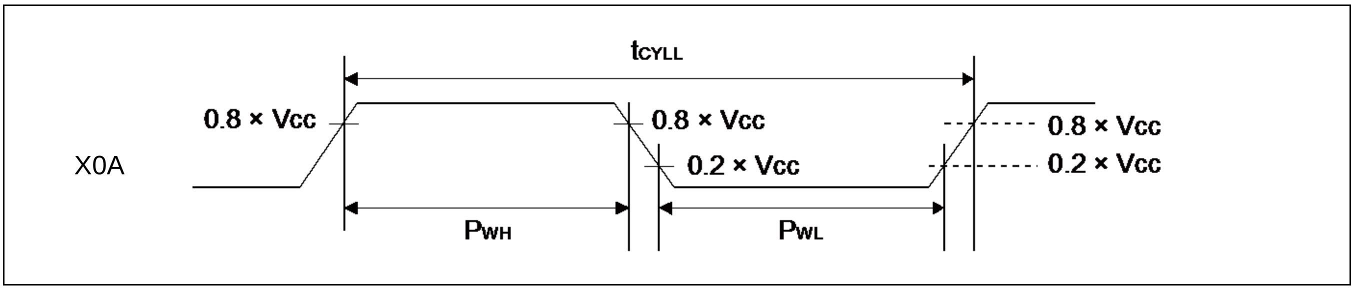


14.4.2 Sub Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	t_{CYLL}		-	10	-	31.25	μs	When the external clock is used
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When the external clock is used

*: See "Sub crystal oscillator" in "9. Handling Devices" for the crystal oscillator used.



14.4.3 Built-in CR Oscillation Characteristics

Built-in high-speed CR

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} =AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRH}	Ta = + 25°C, 3.6V < V_{CC} ≤ 5.5V	3.92	4	4.08	MHz	During trimming*1
		Ta =0°C to + 85°C, 3.6V < V_{CC} ≤ 5.5V	3.9	4	4.1		
		Ta = - 40°C to + 105°C, 3.6V < V_{CC} ≤ 5.5V	3.88	4	4.12		
		Ta = + 25°C, 2.7V ≤ V_{CC} ≤ 3.6V	3.94	4	4.06		
		Ta = - 20°C to + 85°C, 2.7V ≤ V_{CC} ≤ 3.6V	3.92	4	4.08		
		Ta = - 20°C to + 105°C, 2.7V ≤ V_{CC} ≤ 3.6V	3.9	4	4.1		
		Ta = - 40°C to + 105°C, 2.7V ≤ V_{CC} ≤ 3.6V	3.88	4	4.12		
		Ta = - 40°C to + 105°C	2.8	4	5.2		Not during trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	μs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock.
After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

Built-in low-speed CR

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} =AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRL}	-	50	100	150	kHz	

14.4.4 Operating Conditions of Main PLL (In the case of using the main clock as the input clock of the PLL)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*[1] (LOCK UP time)	t_{LOCK}	100	-	-	μs	
PLL input clock frequency	F_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	5	-	37	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*[2]	F_{CLKPLL}	-	-	40	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

14.4.5 Operating Conditions of Main PLL (In the case of using the built-in high-speed CR clock as the input clock of the main PLL)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*[1] (LOCK UP time)	t_{LOCK}	100	-	-	μs	
PLL input clock frequency	F_{PLLI}	3.88	4	4.12	MHz	
PLL multiple rate	-	19	-	35	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*[2]	F_{CLKPLL}	-	-	41.2	MHz	

*1: The wait time is the time it takes for PLL oscillation to stabilize.

*2: For details of the main PLL clock (CLKPLL), refer to "CHAPTER: Clock" in "FM0+ Family PERIPHERAL MANUAL".

Note:

- *For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency has been trimmed.*

14.4.6 Reset Input Characteristics

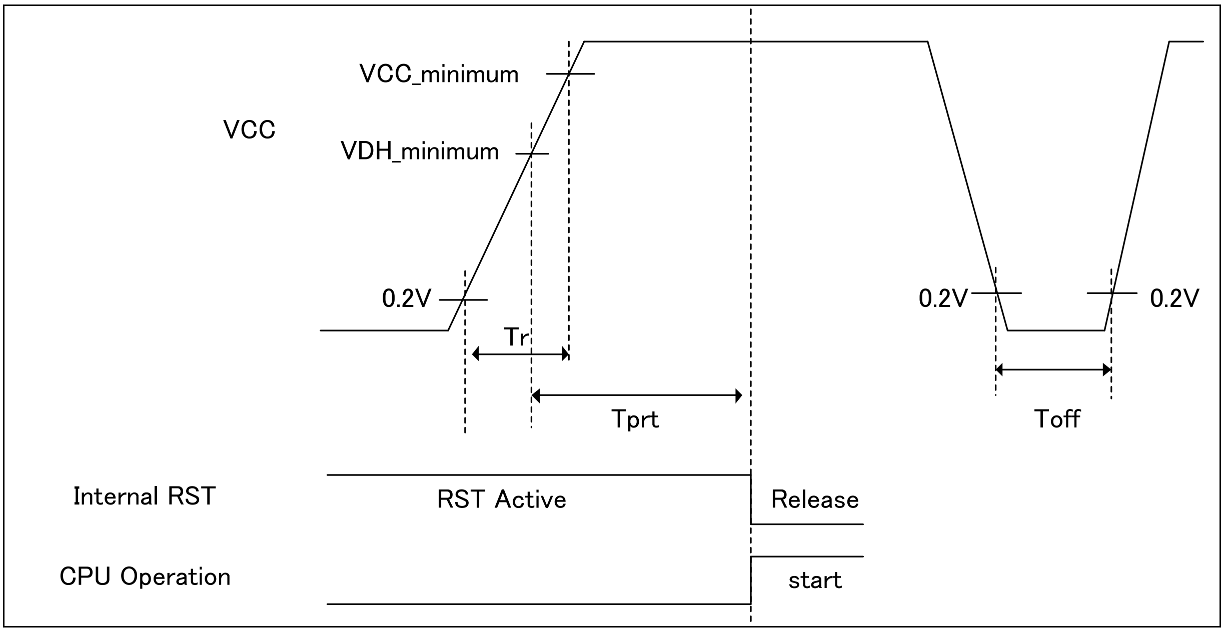
(V_{CC} =AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

14.4.7 Power-on Reset Timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	Tr	VCC	0	-	ms	
Power supply shut down time	Toff		1	-	ms	
Time until releasing Power-on reset	Tprt		0.43	3.4	ms	



Glossary

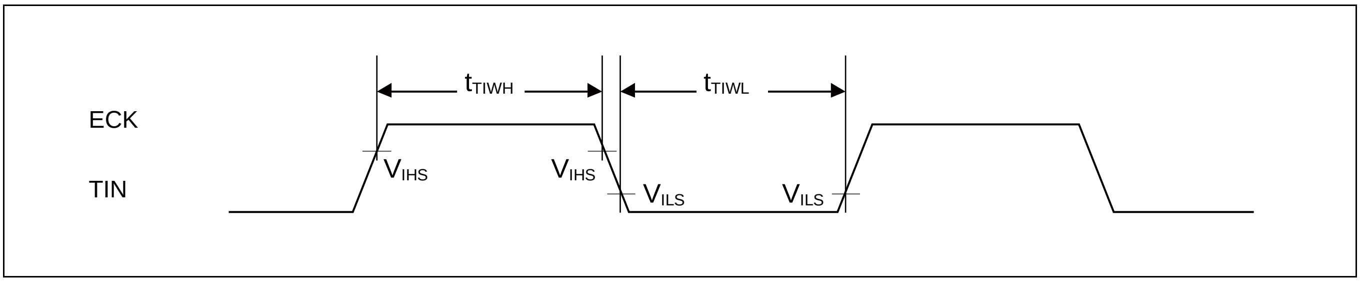
- VCC_minimum : Minimum V_{CC} of recommended operating conditions.
- VDH_minimum : Minimum release voltage (when SVHR=0000) of Low-Voltage detection reset. See "6. Low-Voltage Detection Characteristics".

14.4.8 Base Timer Input Timing

Timer input timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

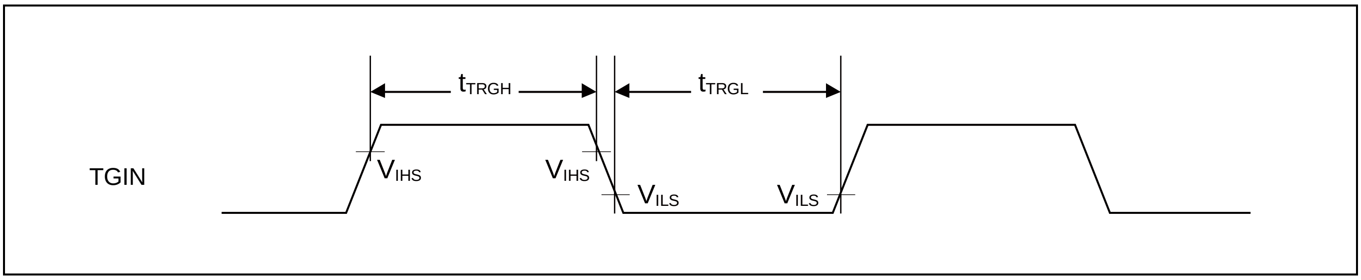
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	2 t_{CYCP}	-	ns	



Trigger input timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	2 t_{CYCP}	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  For the number of the APB bus to which the Base Timer has been connected, see "10. Block Diagram".

14.4.9 CSIO Timing

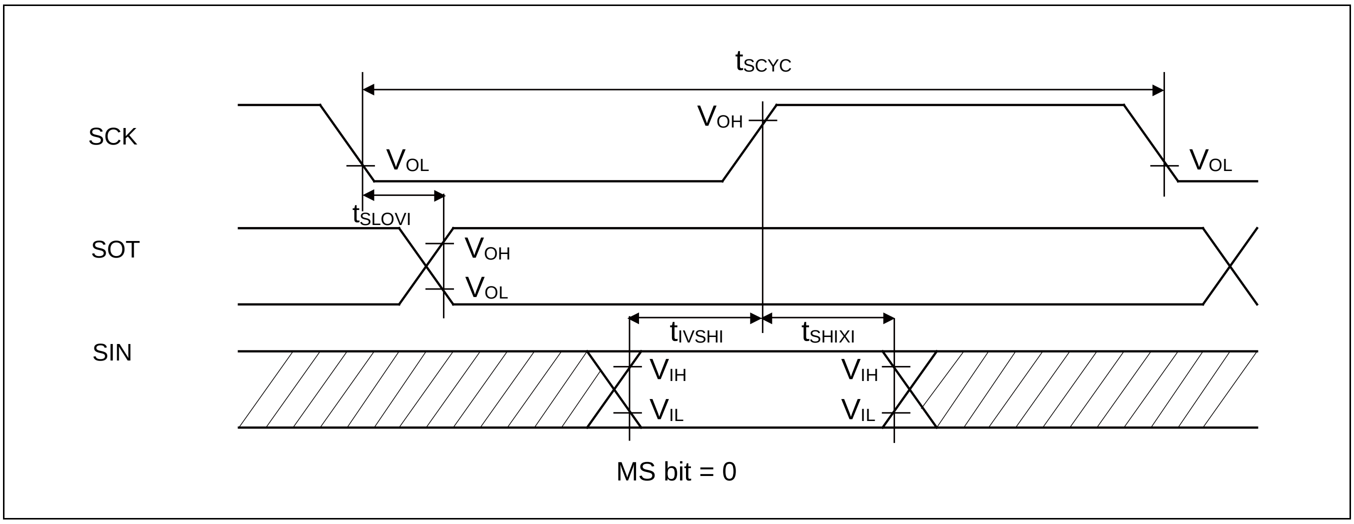
Synchronous serial (SPI = 0, SCINV = 0)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

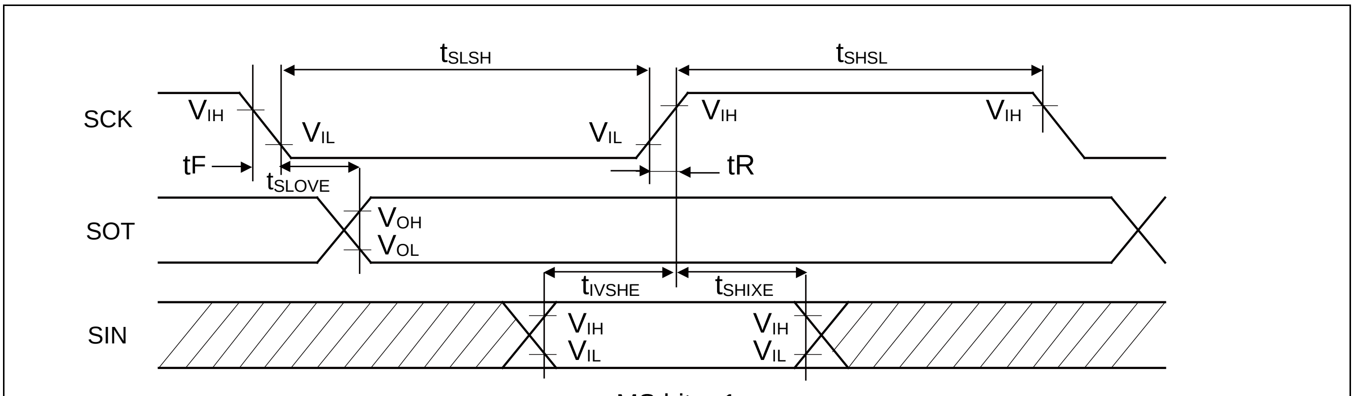
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	**Max**	**Min**	**Max**	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for CLK synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "10. Block Diagram ".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- *External load capacitance C_L = 30 pF*



MS bit = 0



MS bit = 1

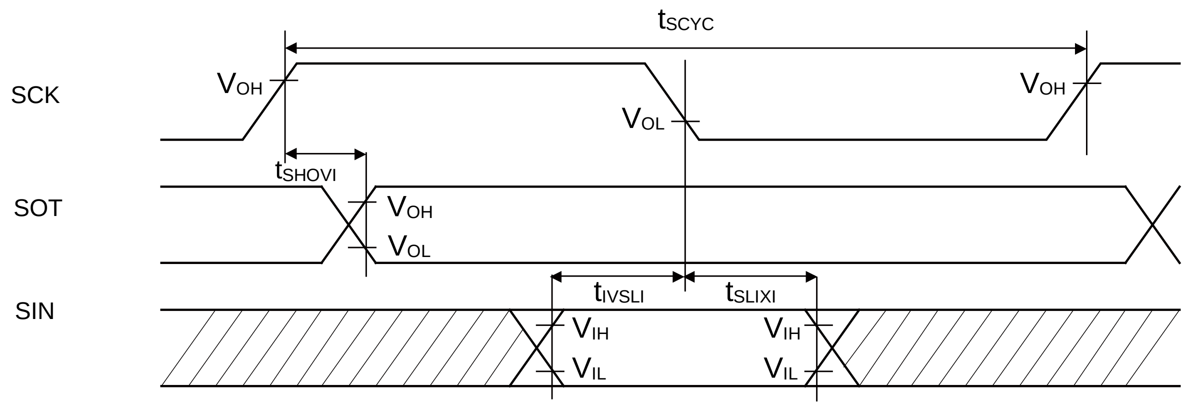
Synchronous serial (SPI = 0, SCINV = 1)

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

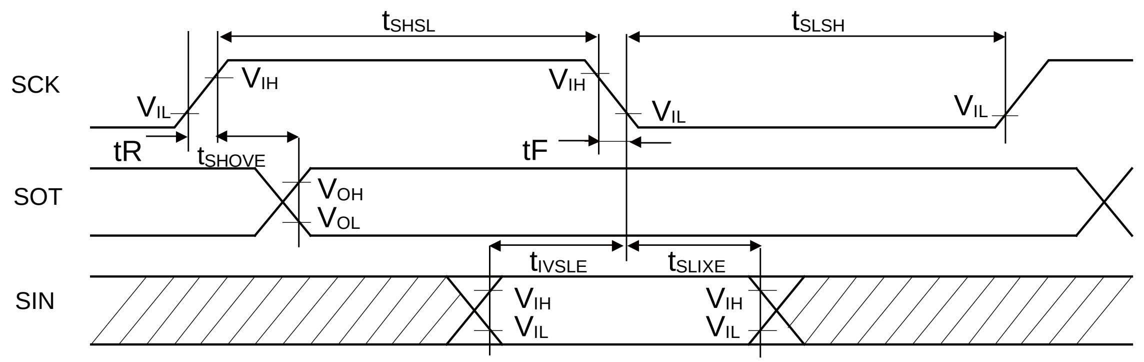
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5V		$V_{CC} \geq$ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for CLK synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "10. Block Diagram ".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- *External load capacitance C_L = 30 pF*



MS bit = 0



MS bit = 1

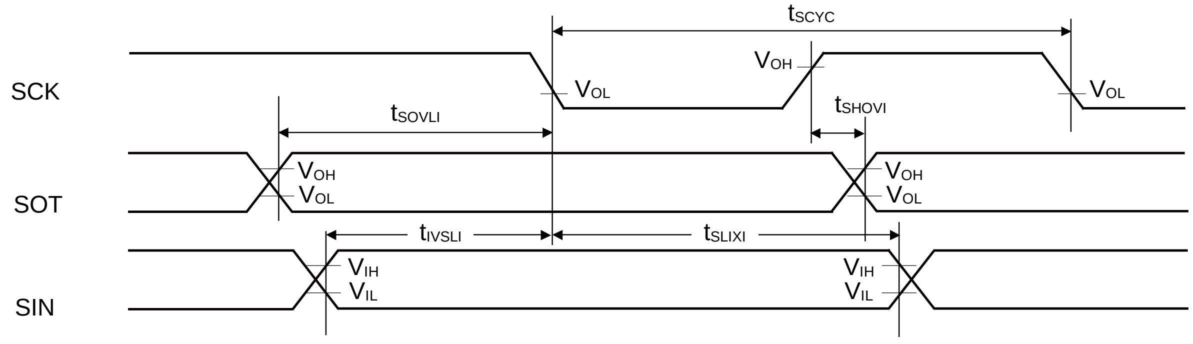
Synchronous serial (SPI = 1, SCINV = 0)

($V_{CC} = AV_{CC} = 2.7$ V to 5.5 V, $V_{SS} = AV_{SS} = 0$ V, Ta = - 40°C to + 105°C)

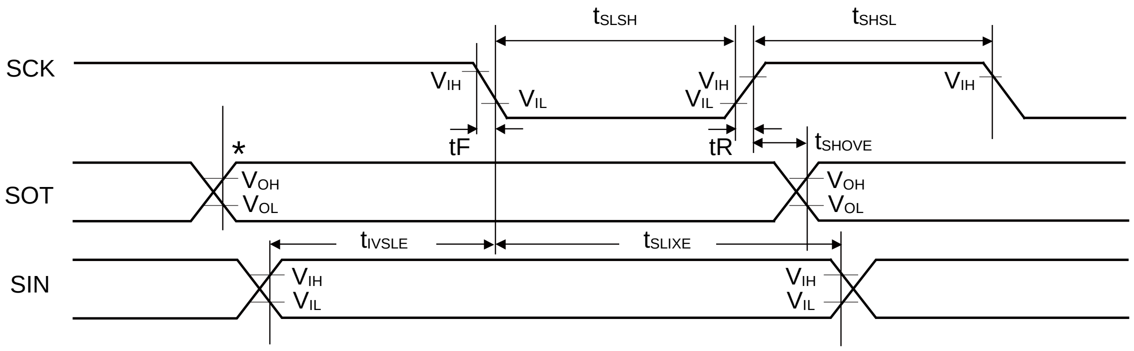
Parameter	Symbol	Pin name	Conditions	$V_{CC} < 4.5$ V		$V_{CC} \geq 4.5$ V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for CLK synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "10. Block Diagram ".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- *External load capacitance C_L = 30 pF*



MS bit = 0



MS bit = 1

*: This changes as data is written to the TDR register.

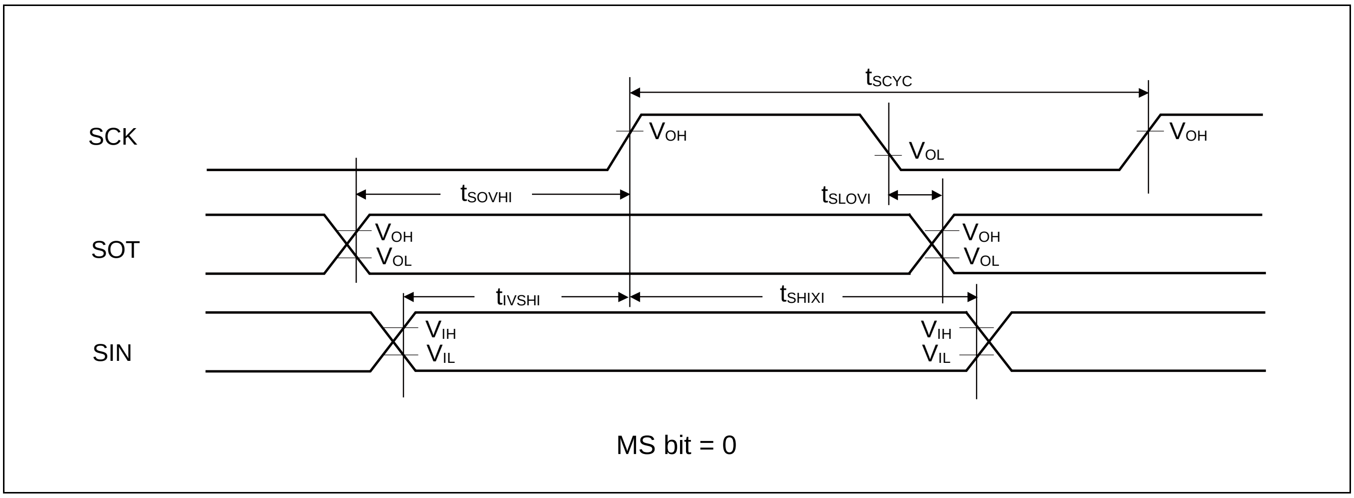
Synchronous serial (SPI = 1, SCINV = 1)

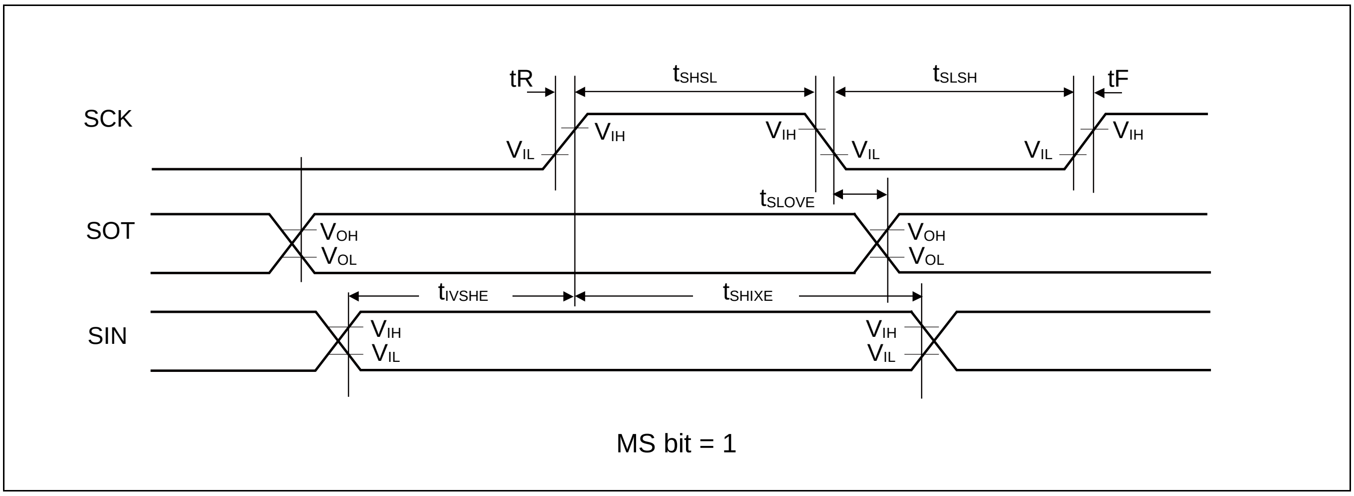
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	**Max**	**Min**	**Max**	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	4 t_{CYCP}	-	4 t_{CYCP}	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		2 t_{CYCP} - 30	-	2 t_{CYCP} - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	2 t_{CYCP} - 10	-	2 t_{CYCP} - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above AC characteristics are for CLK synchronous mode.*
- *t_{CYCP} represents the APB bus clock cycle time.*
  For the number of the APB bus to which Multi-function Serial has been connected, see "10. Block Diagram ".
- *The characteristics are only applicable when the relocate port numbers are the same.*
  For instance, they are not applicable for the combination of SCLKx_0 and SOTx_1.
- *External load capacitance C_L = 30 pF*


t_SCYC
SCK
V_OH
V_OL
V_OH
t_SOVHI
t_SLOVI
SOT
V_OH
V_OL
V_OH
V_OL
t_IVSHI
t_SHIXI
SIN
V_IH
V_IL
V_IH
V_IL
MS bit = 0


tR
t_SHSL
t_SLSH
tF
SCK
V_IL
V_IH
V_IH
V_IL
V_IL
V_IH
t_SLOVE
SOT
V_OH
V_OL
V_OH
V_OL
t_IVSHE
t_SHIXE
SIN
V_IH
V_IL
V_IH
V_IL
MS bit = 1

When using synchronous serial chip select (SPI = 1, SCINV = 0, MS=0, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↓→SUT delay time	t_{DSE}		-	40	-	40	ns
SCS↑→SUT delay time	t_{DEE}		0	-	0	-	ns

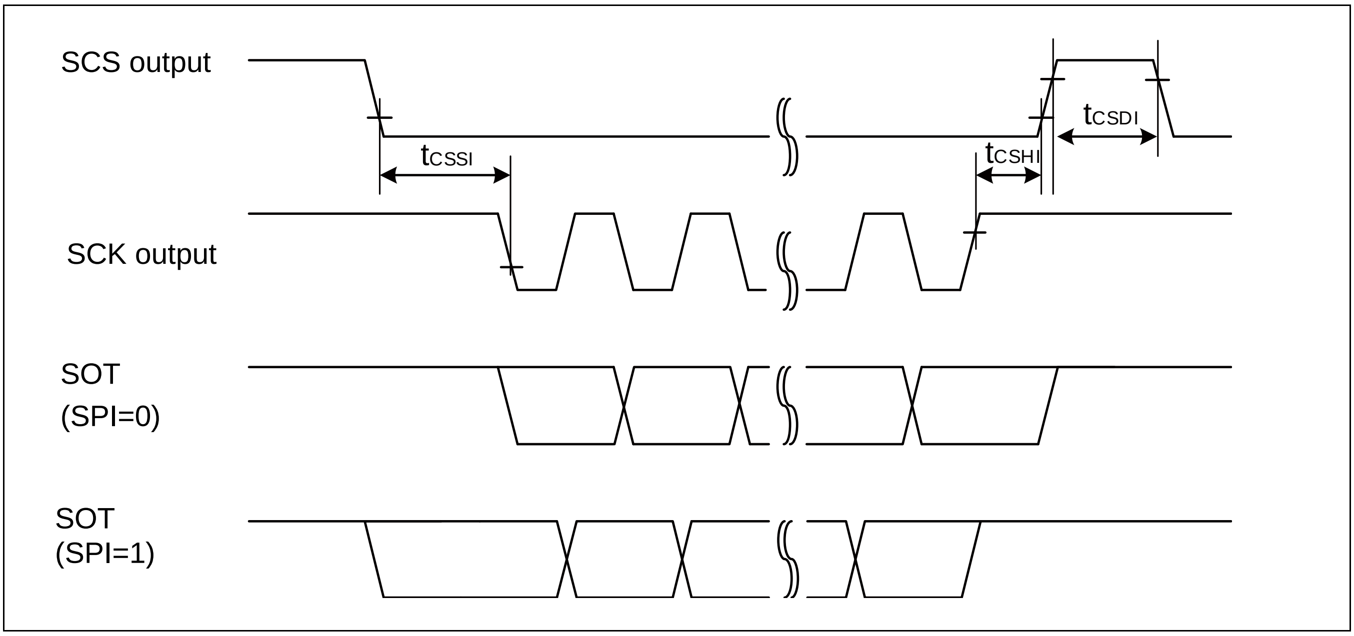
(*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

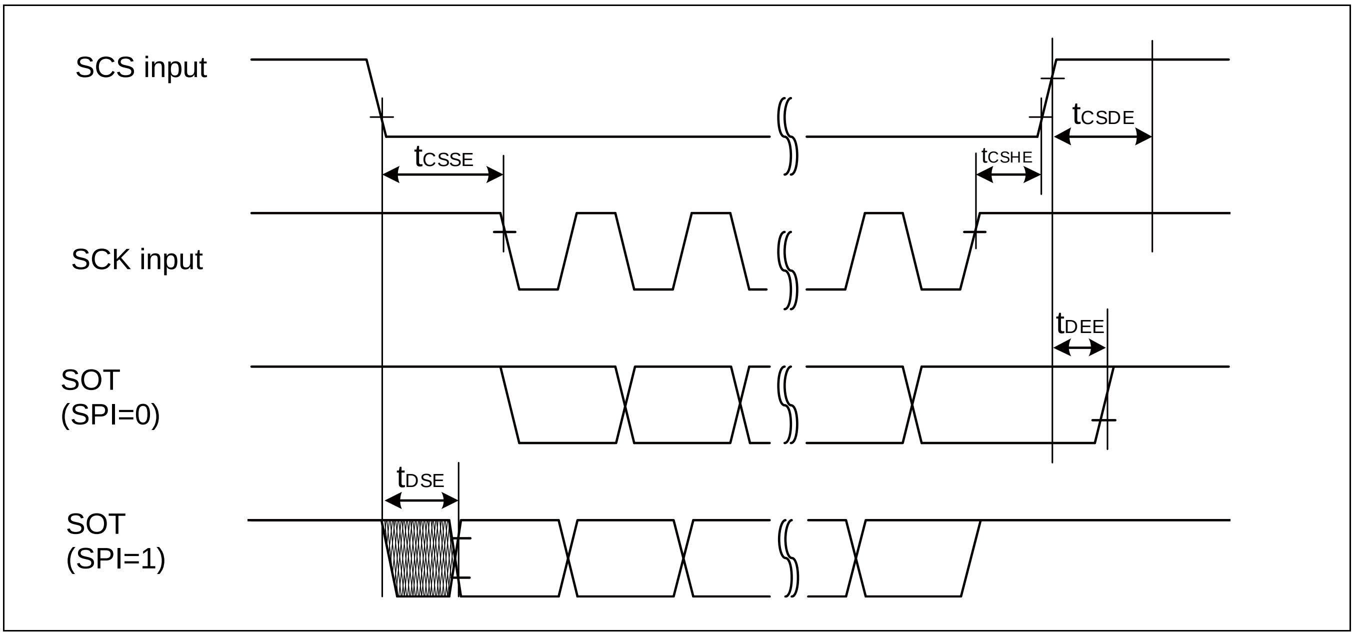
(*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "10. Block Diagram ".
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family PERIPHERAL MANUAL".*
- *When the external load capacitance C_L = 30pF.*


SCS output
tCSSI
tCSHI
tCSDI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSSE
tCSHE
tCSDE
SCK input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

When using synchronous serial chip select (SPI = 1, SCINV = 1, MS=0, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

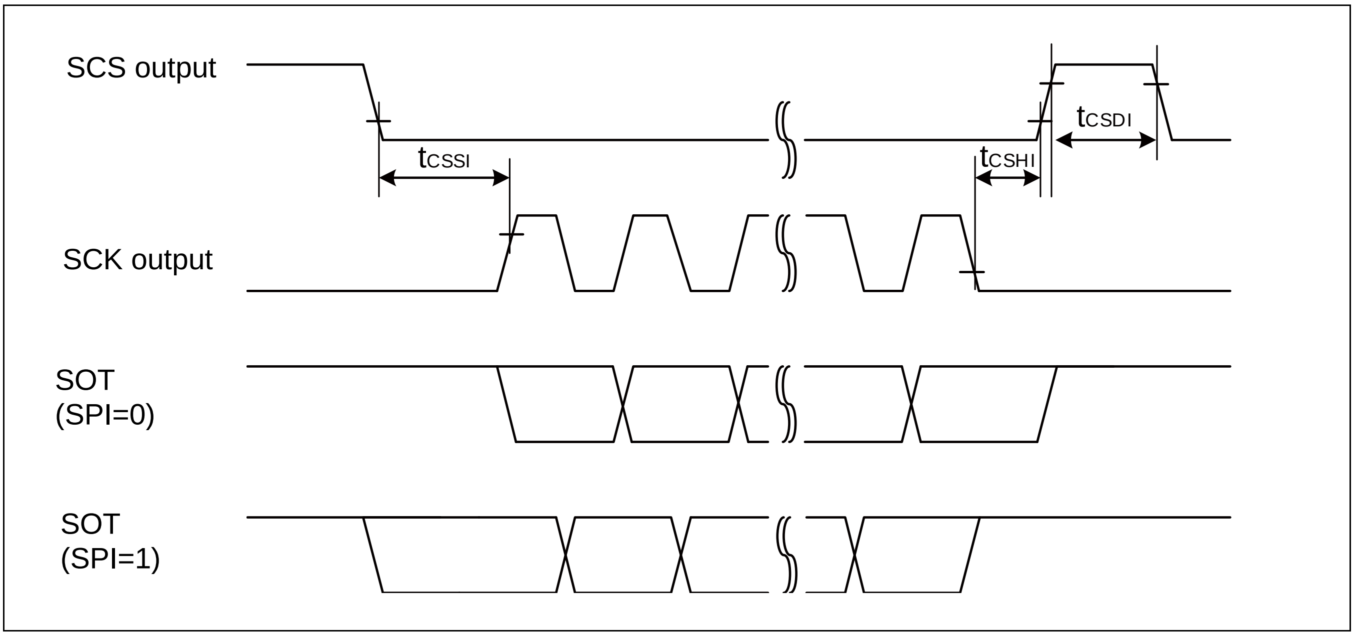
(*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

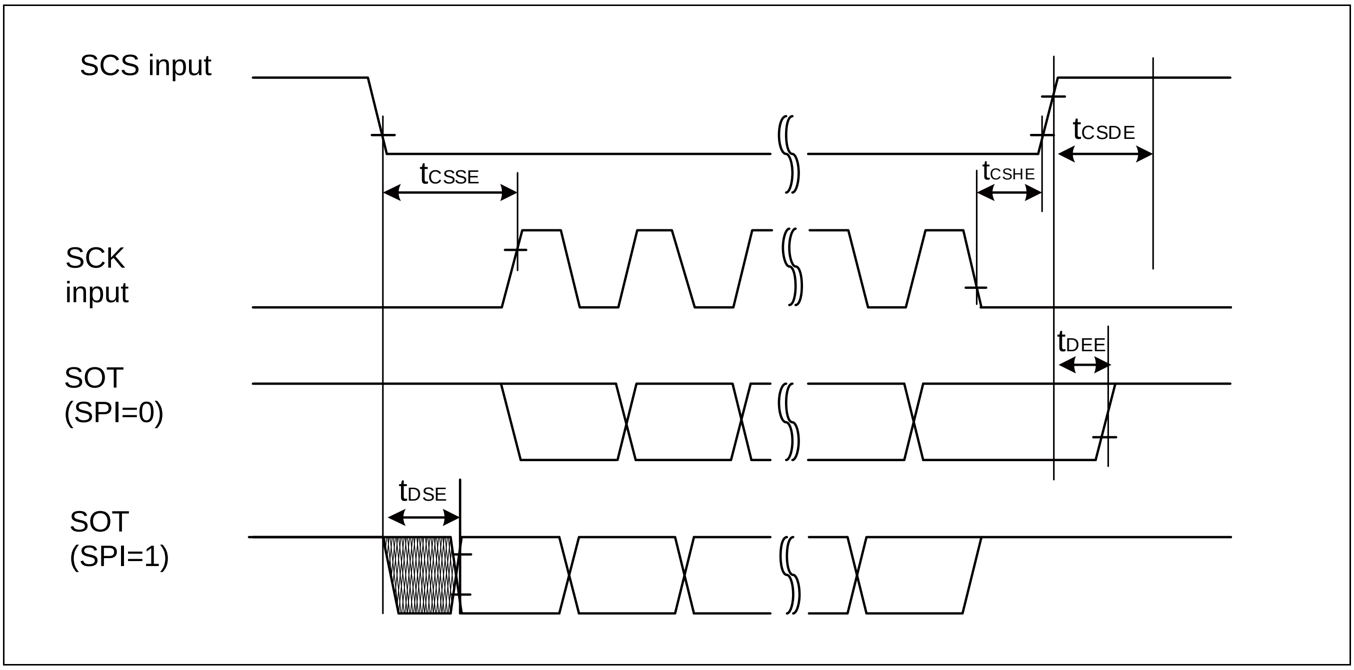
(*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "10. Block Diagram ".
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family PERIPHERAL MANUAL".*
- *When the external load capacitance C_L = 30pF.*


SCS output
tCSSI
tCSHI
tCSDI
SCK output
SOT (SPI=0)
SOT (SPI=1)


SCS input
tCSSE
tCSHE
tCSDE
SCK input
tDEE
SOT (SPI=0)
tDSE
SOT (SPI=1)

When using synchronous serial chip select (SPI = 1, SCINV = 0, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

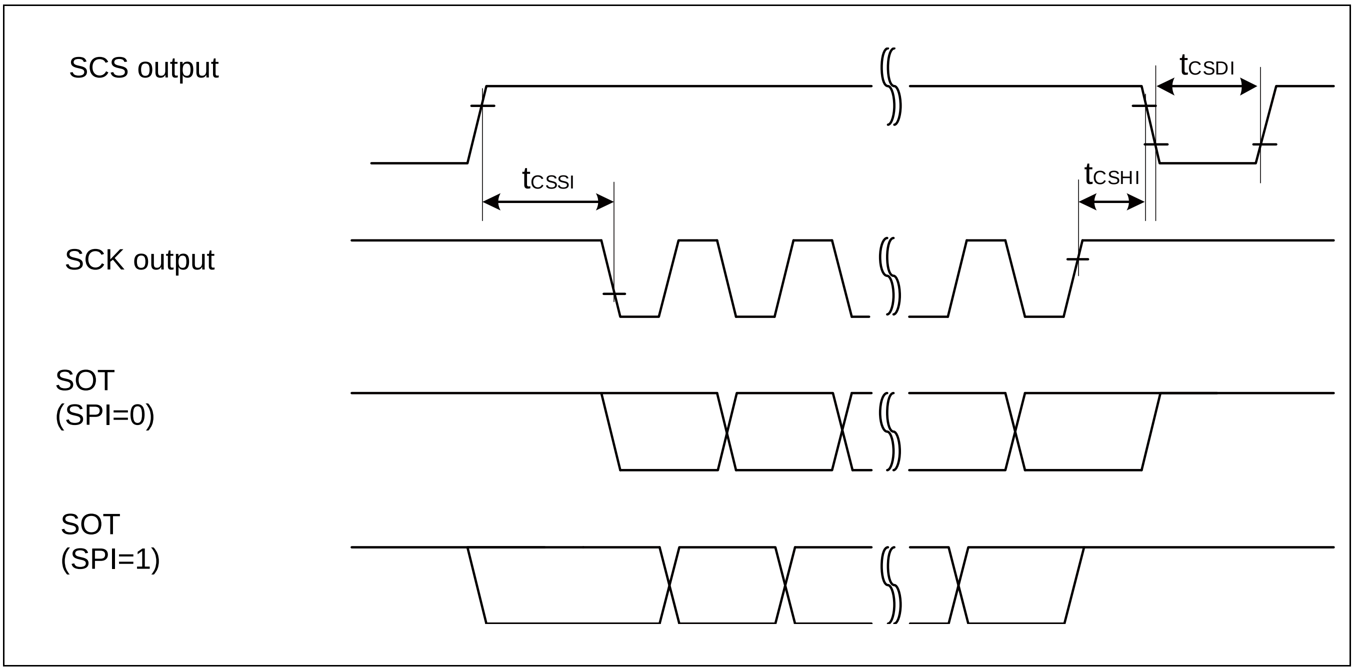
(*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

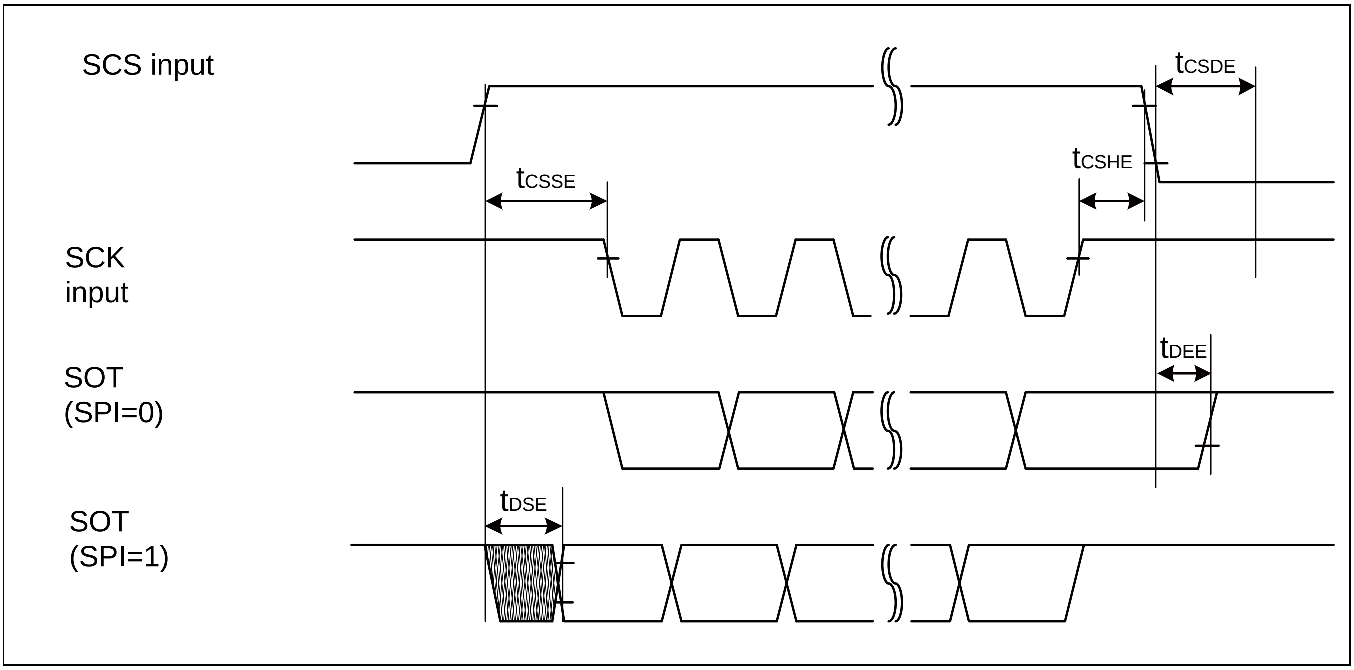
(*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "10. Block Diagram ".
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family PERIPHERAL MANUAL".*
- *When the external load capacitance C_L = 30pF.*


SCS output
tCSDI
tCSSI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSDE
tCSSE
tCSHE
SCK
input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

When using synchronous serial chip select (SPI = 1, SCINV = 1, MS=0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

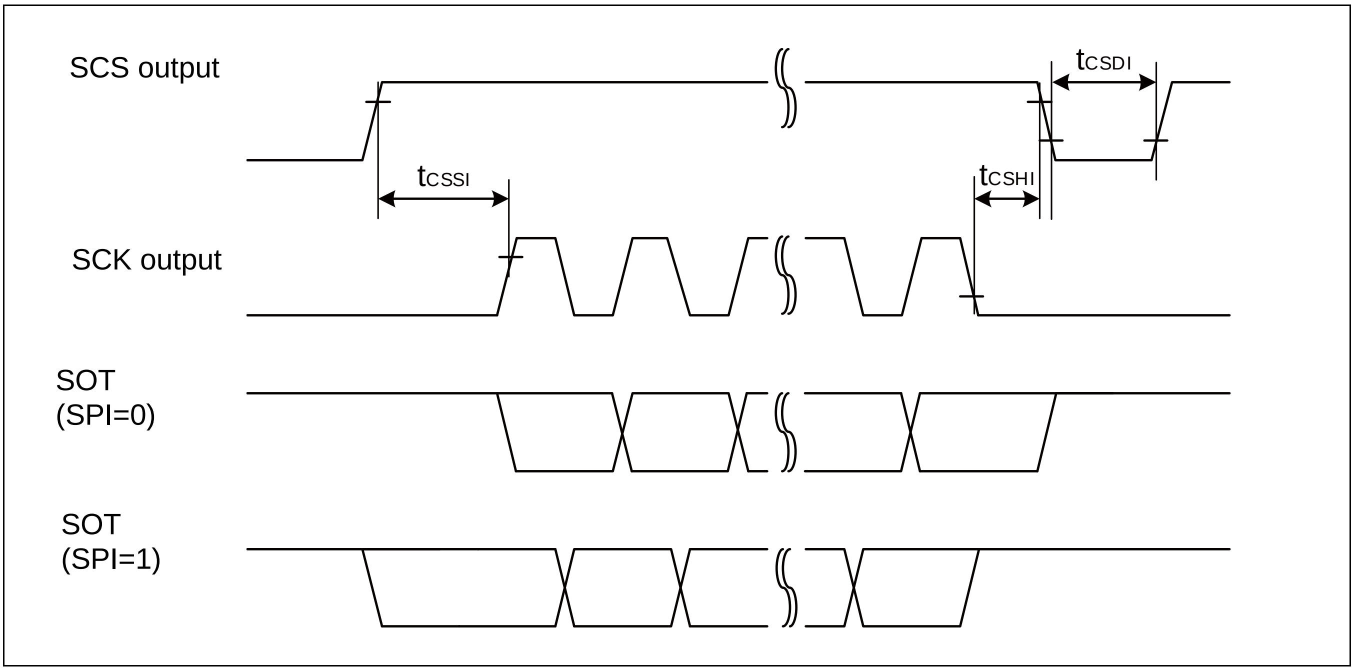
(*1): CSSU bit value × serial chip select timing operating clock cycle [ns]

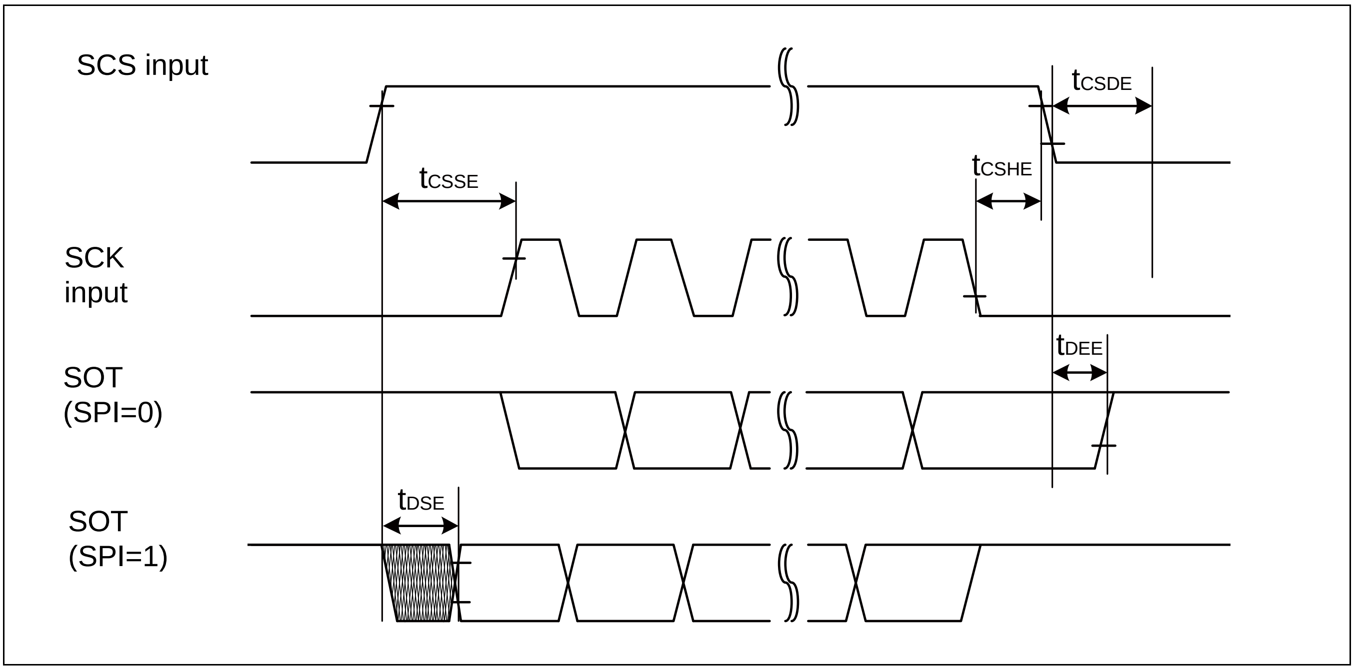
(*2): CSHD bit value × serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value × serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which Multi-function Serial is connected to, see "10. Block Diagram ".
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family PERIPHERAL MANUAL".*
- *When the external load capacitance C_L = 30pF.*

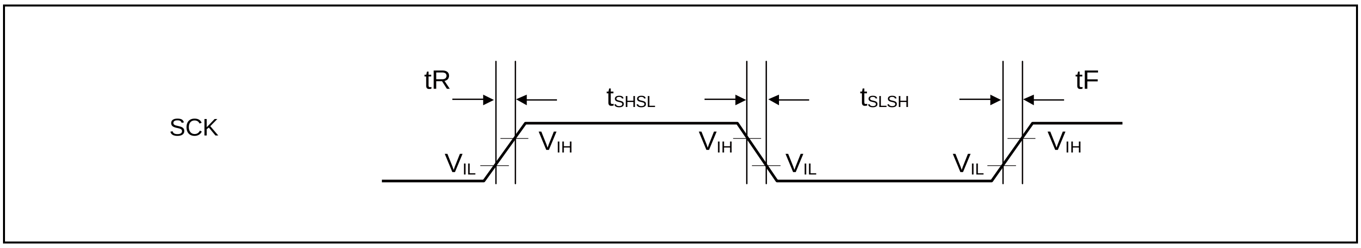

SCS output
tCSDI
tCSSI
tCSHI
SCK output
SOT
(SPI=0)
SOT
(SPI=1)


SCS input
tCSDE
tCSSE
tCSHE
SCK
input
tDEE
SOT
(SPI=0)
tDSE
SOT
(SPI=1)

External clock (EXT = 1): asynchronous only

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock "L" pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	tF		-	5	ns	
SCK rising time	tR		-	5	ns	



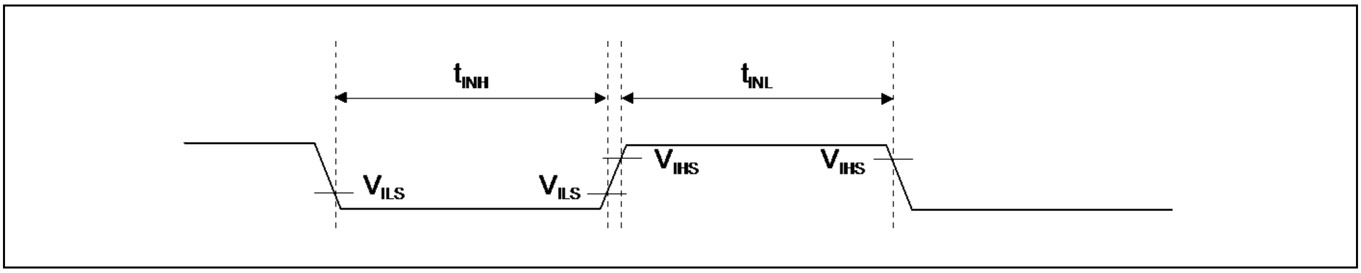
14.4.10 External Input Timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	2 t_{CYCP}*[1]	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	2 t_{CYCP}*[1]	-	ns	Wave form generator
		INTxx, NMIX	-	2 t_{CYCP} + 100*[1]	-	ns	External interrupt, NMI
				500*[2]	-	ns	

*1: t_{CYCP} represents the APB bus clock cycle time except when the APB bus clock stops in STOP mode or in TIMER mode. For the number of the APB bus to which the Multi-function Timer is connected and that of the APB bus to which the External Interrupt Controller is connected, see "10. Block Diagram".

*2: In STOP mode and TIMER mode

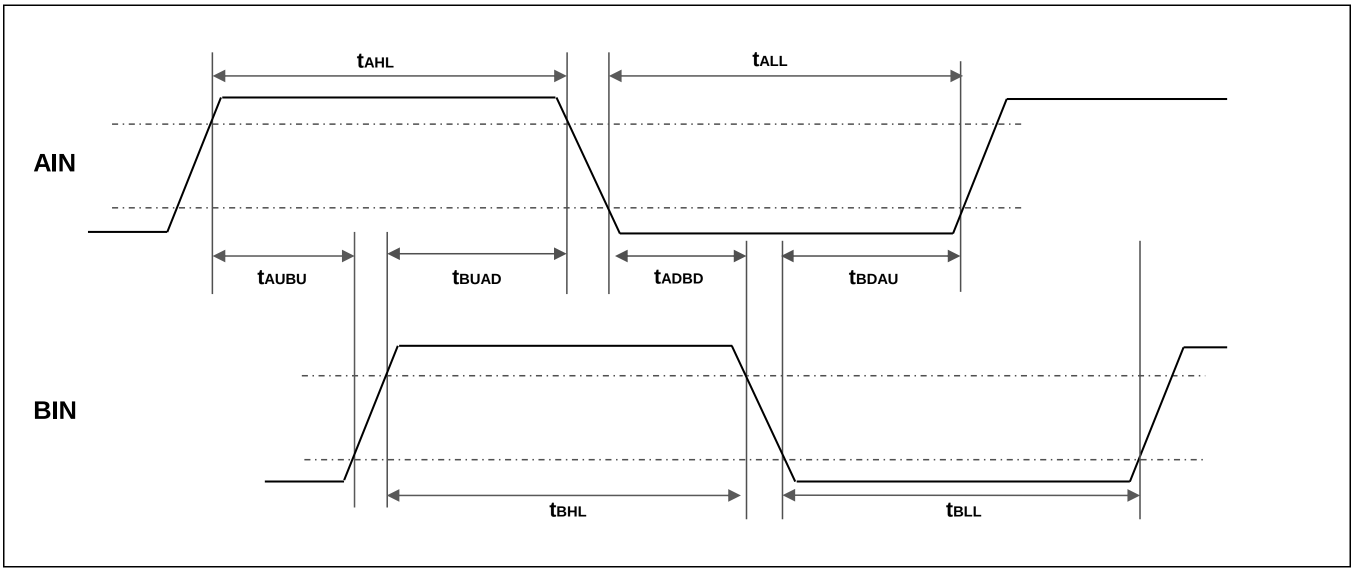


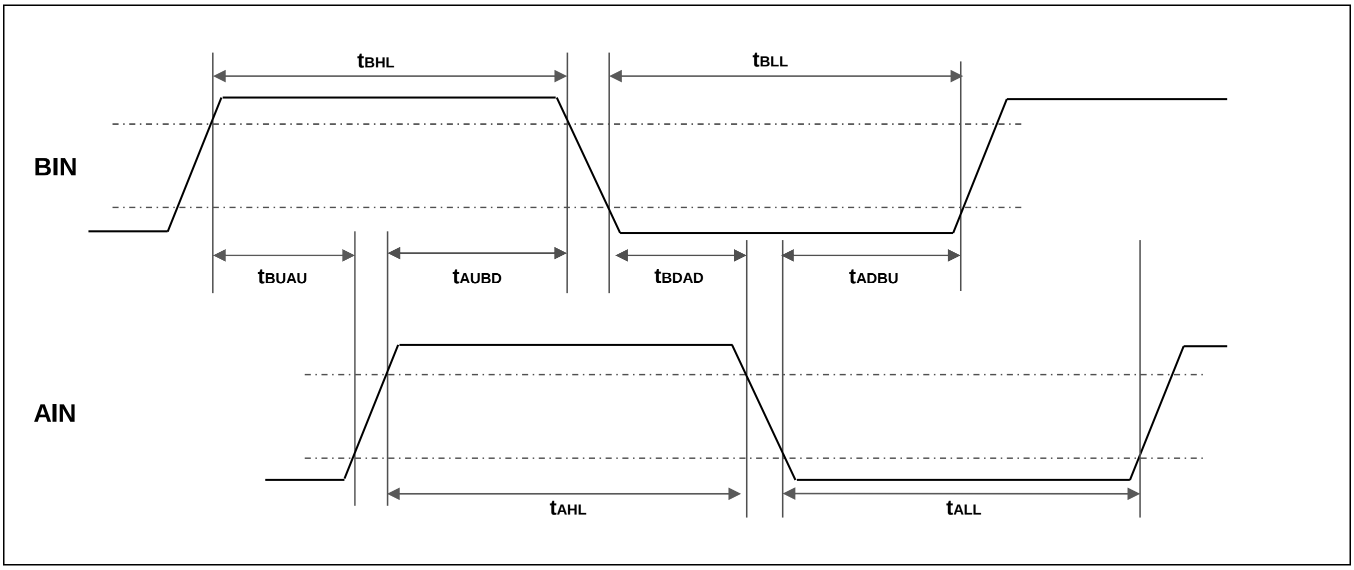
14.4.11 QPRC Timing

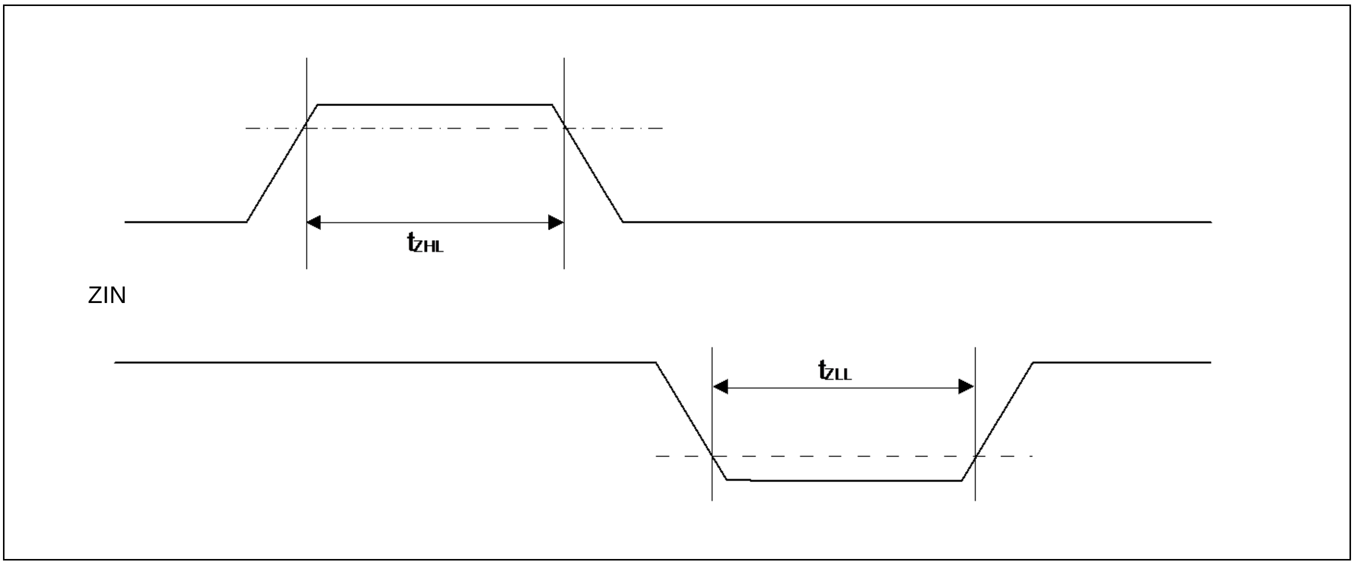
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

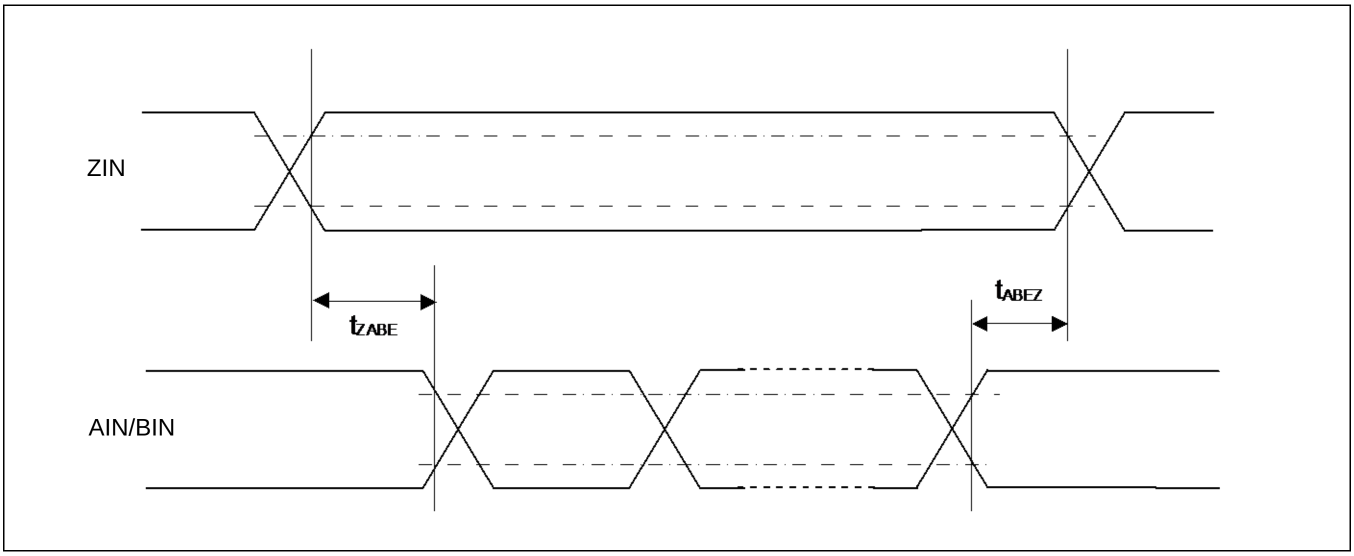
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t_{AHL}	-	2 t_{CYCP}*	-	ns
AIN pin "L" width	t_{ALL}	-			
BIN pin "H" width	t_{BHL}	-			
BIN pin "L" width	t_{BLL}	-			
Time from AIN pin "H" level to BIN rise	t_{AUBU}	PC_Mode2 or PC_Mode3			
Time from BIN pin "H" level to AIN fall	t_{BUAD}	PC_Mode2 or PC_Mode3			
Time from AIN pin "L" level to BIN fall	t_{ADBD}	PC_Mode2 or PC_Mode3			
Time from BIN pin "L" level to AIN rise	t_{BDAU}	PC_Mode2 or PC_Mode3			
Time from BIN pin "H" level to AIN rise	t_{BUAU}	PC_Mode2 or PC_Mode3			
Time from AIN pin "H" level to BIN fall	t_{AUBD}	PC_Mode2 or PC_Mode3			
Time from BIN pin "L" level to AIN fall	t_{BDAD}	PC_Mode2 or PC_Mode3			
Time from AIN pin "L" level to BIN rise	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t_{ZHL}	QCR:CGSC="0"			
ZIN pin "L" width	t_{ZLL}	QCR:CGSC="0"			
Time from determined ZIN level to AIN/BIN rise and fall	t_{ZABE}	QCR:CGSC="1"			
Time from AIN/BIN rise and fall time to determined ZIN level	t_{ABEZ}	QCR:CGSC="1"			

*: t_{CYCP} represents the APB bus clock cycle time except when the APB bus clock stops in STOP mode or in TIMER mode. For the number of the APB bus to which the QPRC is connected, see "10. Block Diagram".




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

14.4.12 I²C Timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

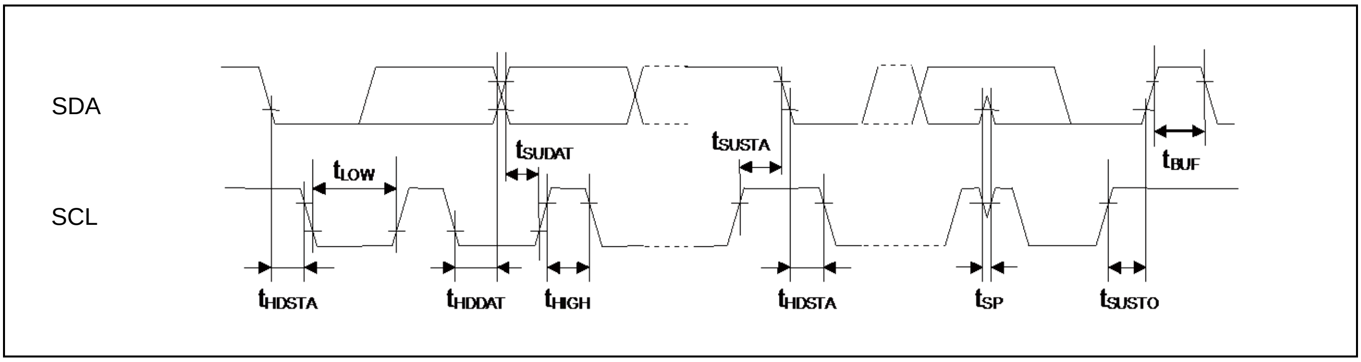
Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	μs	
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	μs	
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	μs	
(Repeated) START setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	μs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	μs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R represents the pull-up resistance of the SCL and SDA lines, and C_L the load capacitance of the SCL and SDA lines. Vp represents the power supply voltage of the pull-up resistance, and I_{OL} the V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy at least the condition that the period during which the device is holding the SCL signal at "L" (t_{LOW}) does not extend.

*3: A Fast-mode I²C bus device can be used in a Standard-mode I²C bus system, provided that the condition of "$t_{SUDAT} \geq 250$ ns" is fulfilled.

*4: t_{CYCP} represents the APB bus clock cycle time.
For the number of the APB bus to which the I²C is connected, see "10. Block Diagram".
To use Standard-mode, set the APB bus clock at 2MHz or more.
To use Fast-mode, set the APB bus clock at 8 MHz or more.



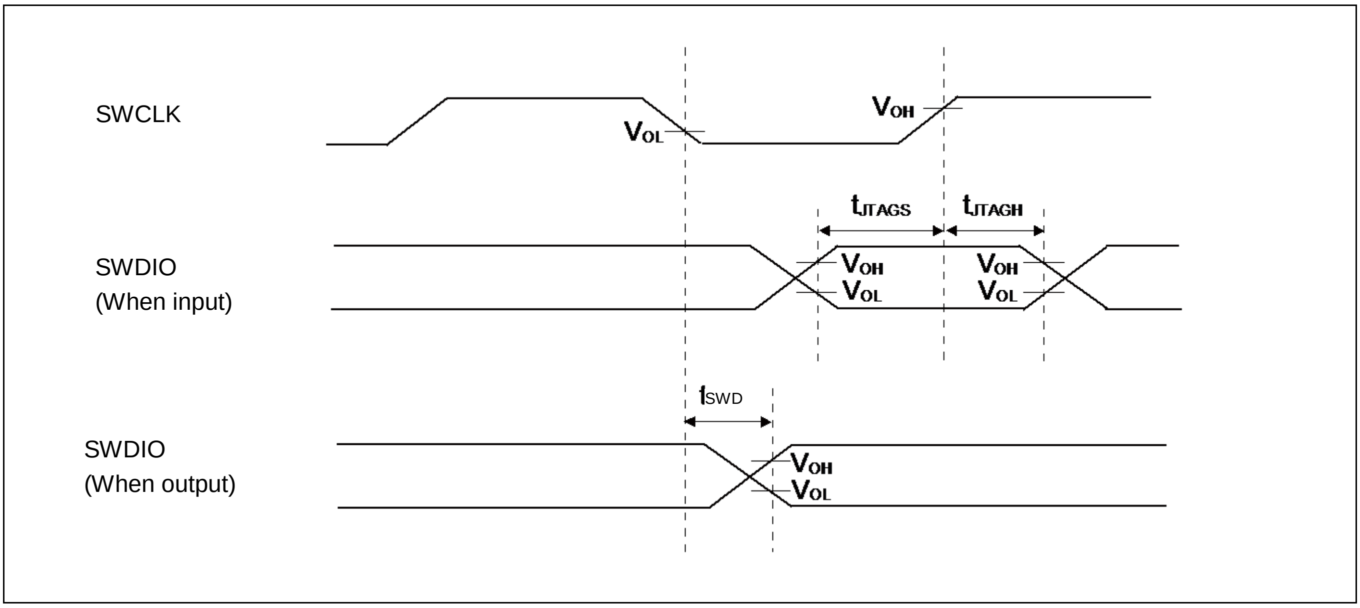
14.4.13 SW-DP Timing

(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	t_{SWS}	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	t_{SWH}	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	t_{SWD}	SWCLK, SWDIO	-	-	45	ns	

Note:

- *External load capacitance C_L = 30 pF*



14.5 12-bit A/D Converter

Electrical characteristics of A/D Converter

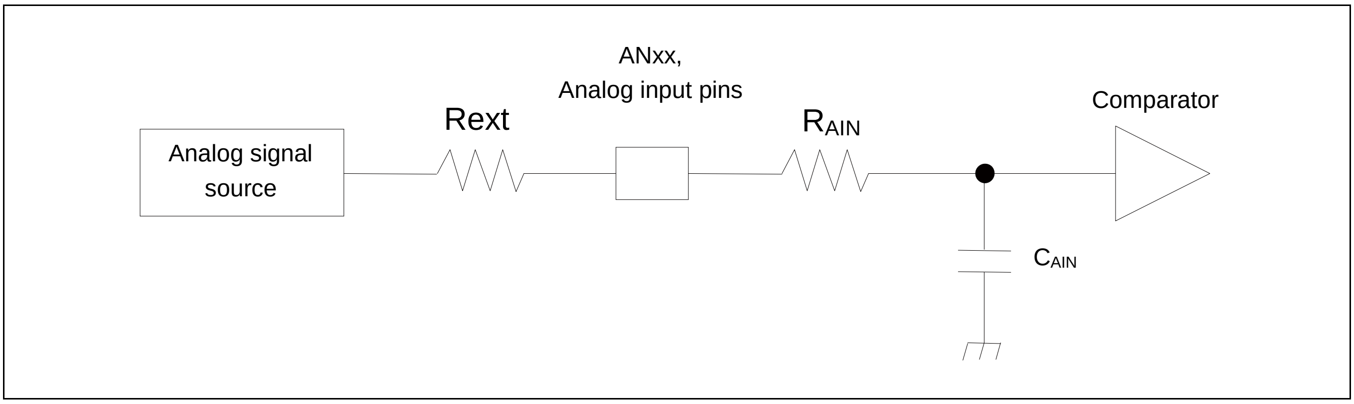
(V_{CC} = AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	- 4.5	-	4.5	LSB	
Differential Nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 20	-	+ 20	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH - 20	-	AVRH+ 20	mV	S6E1A1xC0A
			AV_{CC}-20	-	AV_{CC}+20		S6E1A1xB0A
Conversion time	-	-	0.8*[1]	-	-	μs	S6E1A1xC0A $AV_{CC} \geq 4.5V$
			2.0*[1]	-	-		S6E1A1xB0A
Sampling time*[2]	Ts	-	0.24	-	10	μs	S6E1A1xC0A $AV_{CC} \geq 4.5V$
			0.5				S6E1A1xC0A $AV_{CC} < 4.5V$
			0.6				S6E1A1xB0A
Compare clock cycle*[3]	Tcck	-	40	-	1000	ns	S6E1A1xC0A $AV_{CC} \geq 4.5V$
			50				S6E1A1xC0A $AV_{CC} < 4.5V$
			100				S6E1A1xB0A
State transition time to operation permission	Tstt	-	-	-	1.0	μs	
Analog input capacity	C_{AIN}	-	-	-	9.7	pF	
Analog input resistance	R_{AIN}	-	-	-	1.6	kΩ	$AV_{CC} \geq 4.5V$
					2.3		$AV_{CC} < 4.5V$
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	ANxx	-	-	5	μA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	S6E1A1xC0A
			AV_{SS}	-	AV_{CC}		S6E1A1xB0A
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	Only S6E1A1xB0A

*1: The conversion time is the value of "sampling time (Ts) + compare time (Tc)".
The minimum conversion time is computed according to the following conditions: sampling time = 240 ns, compare time = 560 ns (AVcc ≥ 4.5 V). Must be set 25MHz to the Base clock (HCLK).
Ensure that the conversion time satisfies the specifications of the sampling time (Ts) and compare clock cycle (Tcck).
For details of the settings of the sampling time and compare clock cycle, refer to "CHAPTER: A/D Converter" in "FM0+ Family PERIPHERAL MANUAL Analog Macro Part".
The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.
For the number of the APB bus to which the A/D Converter is connected, see "10. Block Diagram".
The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

*2: The required sampling time varies according to the external impedance.
Set a sampling time that satisfies (Equation 1).

*3: The compare time (Tc) is the result of (Equation 2).



(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

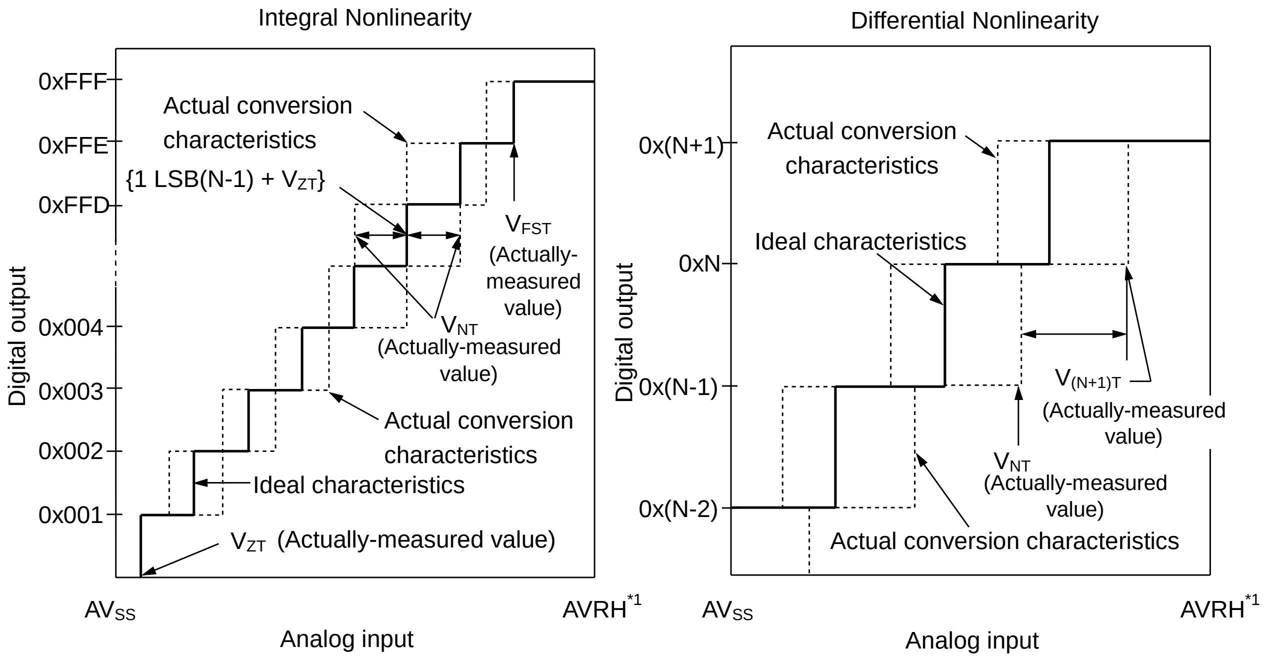
Ts: Sampling time
R_{AIN}: Input resistance of A/D Converter = 1.6 kΩ with $4.5 \leq AVCC \leq 5.5$ ch.1 to ch.5
Input resistance of A/D Converter = 1.4 kΩ with $4.5 \leq AVCC \leq 5.5$ ch.0, ch.6, ch.7
Input resistance of A/D Converter = 2.3 kΩ with $2.7 \leq AVCC < 4.5$ ch.1 to ch.5
Input resistance of A/D Converter = 2.0 kΩ with $2.7 \leq AVCC < 4.5$ ch.0, ch.6, ch.7
C_{AIN}: Input capacitance of A/D Converter = 9.7 pF with $2.7 \leq AVCC \leq 5.5$
Rext: Output impedance of external circuit

(Equation 2) $Tc = Tcck \times 14$

Tc: Compare time
Tcck: Compare clock cycle

Definitions of 12-bit A/D Converter terms

■	Resolution	: Analog variation that is recognized by an A/D converter.
■	Integral Nonlinearity	: Deviation of the line between the zero-transition point (0b000000000000 ←→ 0b000000000001) and the full-scale transition point (0b111111111110 ←→ 0b111111111111) from the actual conversion characteristics.
■	Differential Nonlinearity	: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



*1: At the 32pin product, it is AV_{CC}

$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{ZT}\}}{1\text{LSB}} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 \text{ [LSB]}$$

$$1\text{LSB} = \frac{V_{FST} - V_{ZT}}{4094}$$

N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

14.6 Low-voltage Detection Characteristics

14.6.1 Low-voltage Detection Reset

(Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR[*1] = 00000	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH		2.30	2.50	2.70	V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00001	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00010	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR[*1] = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160× t_{CYCP}[*2]	μs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	μs	

*1: SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is reset to SVHR = 00000 by low voltage detection reset.

*2: t_{CYCP} indicates the APB1 bus clock cycle time.

14.6.2 Low-voltage Detection Interrupt

(Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	8160 × t_{CYCP}*	μs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	μs	

*: t_{CYCP} represents the APB1 bus clock cycle time.

14.7 Flash Memory Write/Erase Characteristics

(V_{CC} = 2.7 V to 5.5 V, Ta = - 40°C to + 105°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large sector	-	0.7	2.2	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector		0.3	0.9		
Halfword (16-bit) write time		-	30	528	μs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	2.6	8	s	The chip erase time includes the time of writing prior to internal erase.

Write/erase cycle and data hold time

Write/erase cycle	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: This value was converted from the result of a technology reliability assessment. (This value was converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature value being + 85°C).

14.8 Return Time from Low-Power Consumption Mode

14.8.1 Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

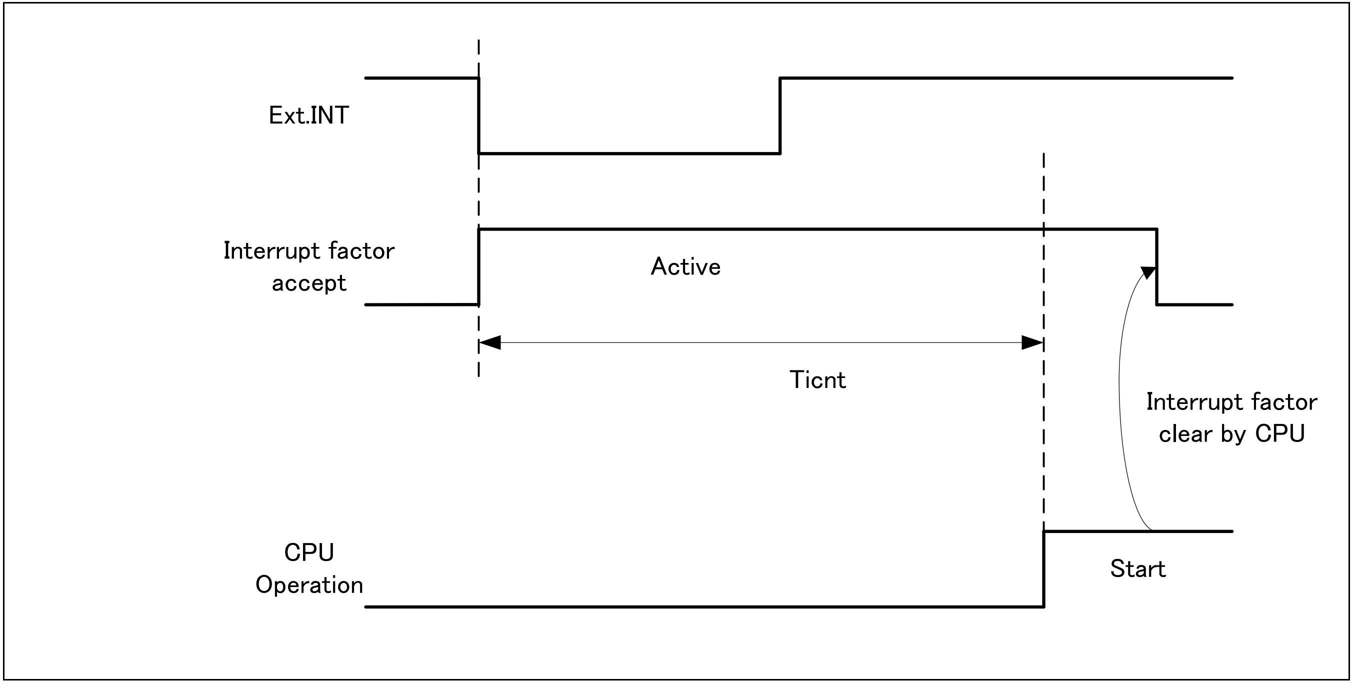
Return Count Time

(V_{CC} = 2.7V to 5.5V, Ta = - 40°C to + 105°C)

Parameter	Symbol	− Value*		Unit	Remarks
		Typ	Max		
SLEEP mode	Ticnt	t_{CYCC}		μs	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		$40 + 17 \times t_{CYCC}$	$80 + 17 \times t_{CYCC}$	μs	
Low-speed CR TIMER mode		360	720	μs	
Sub TIMER mode		191	381	μs	
RTC mode, STOP mode		819	1090	μs	

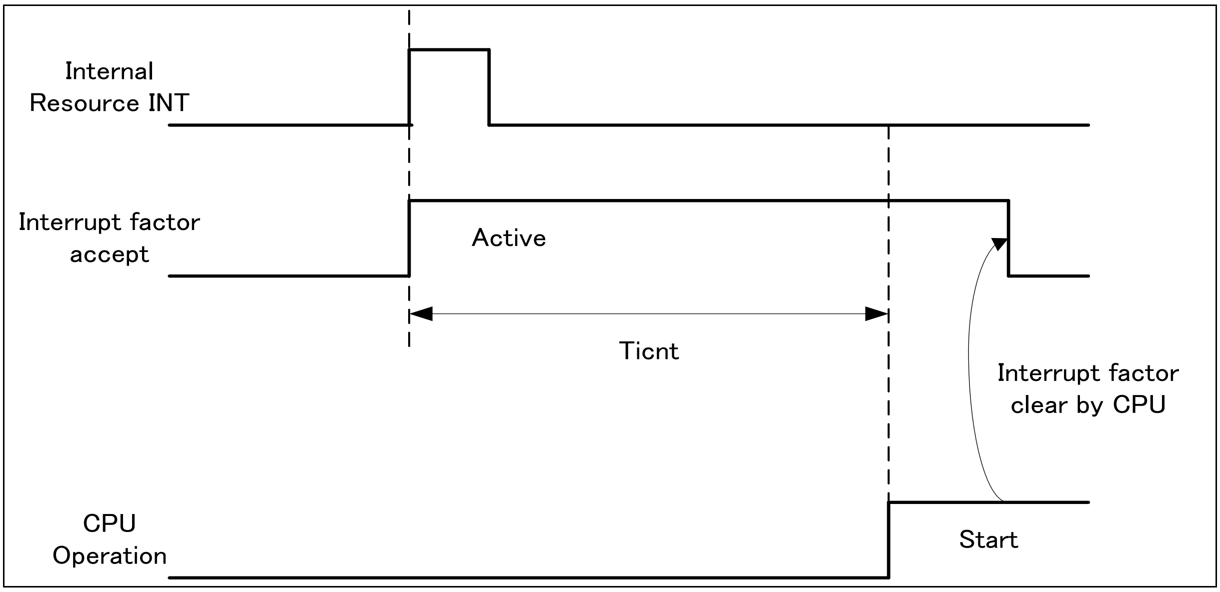
*: The value depends on the accuracy of built-in CR.
The stabilization time of Main clock/Sub clock/Main PLL clock is not included.

Operation example of return from Low-Power consumption mode (by external interrupt*)



*: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt*)



*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family PERIPHERAL MANUAL.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "CHAPTER: Low Power Consumption Mode" in "FM0+ Family PERIPHERAL MANUAL".*

14.8.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

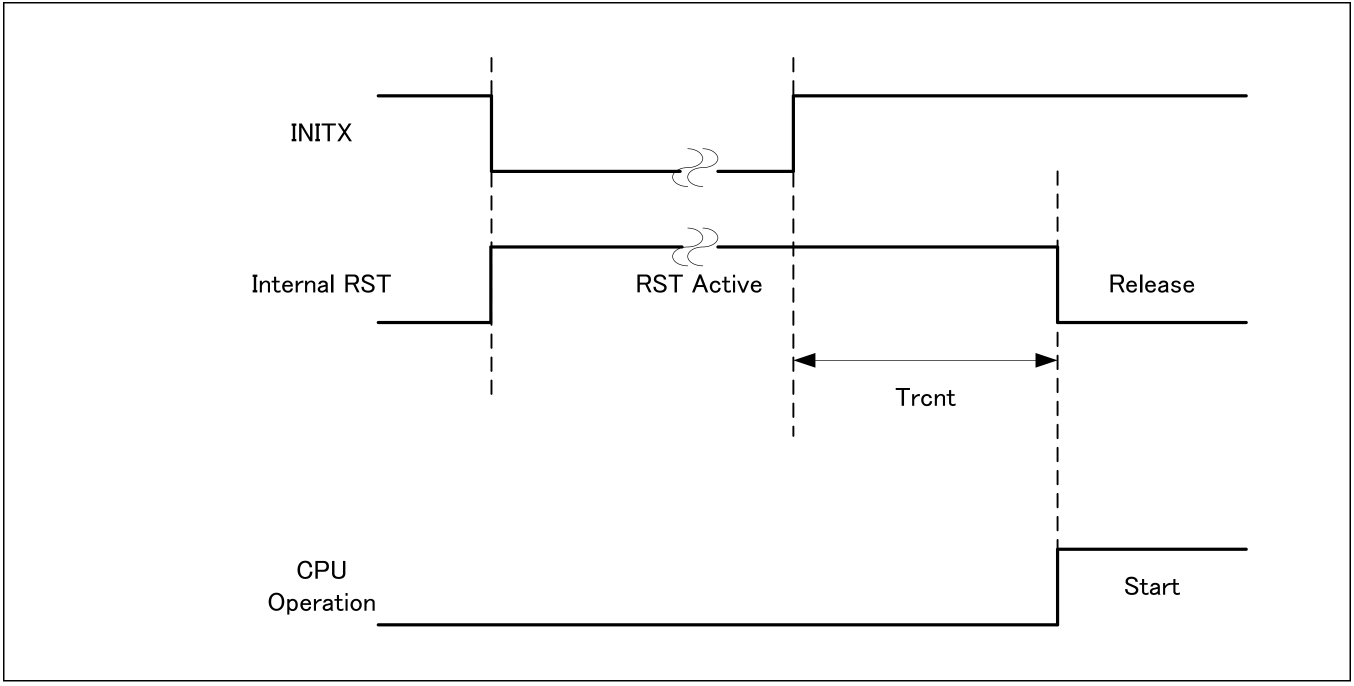
Return Count Time

(V_{CC} = 2.7V to 5.5V, Ta = - 40°C to + 105°C)

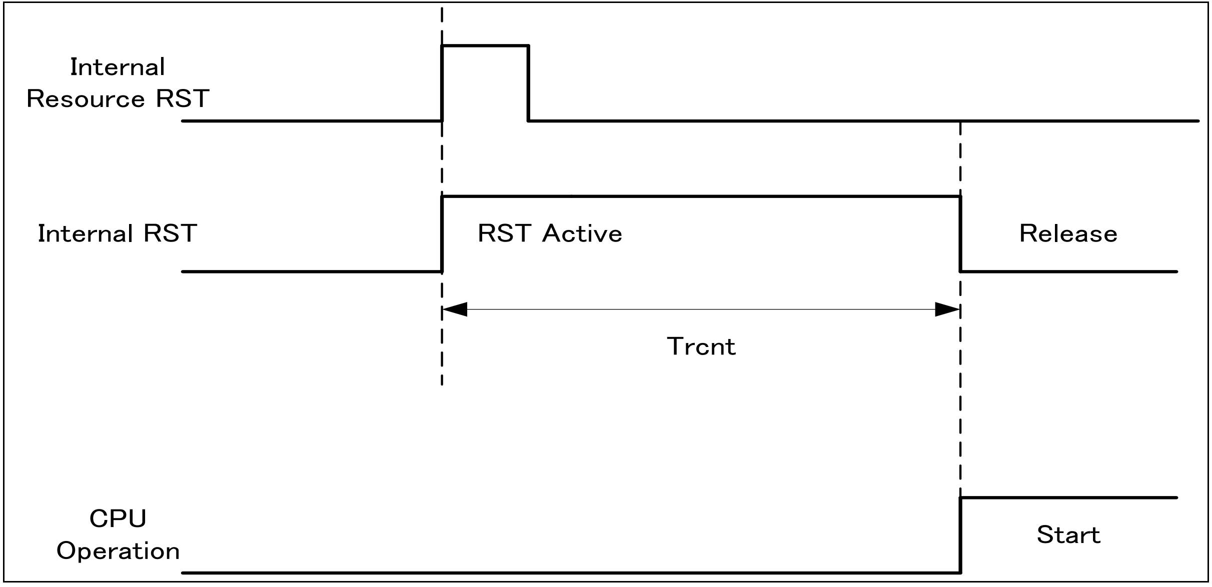
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
SLEEP mode	Trcnt	208	378	μs	
High-speed CR TIMER mode, Main TIMER mode, PLL TIMER mode		208	378	μs	
Low-speed CR TIMER mode		398	758	μs	
Sub TIMER mode		490	849	μs	
RTC/STOP mode		288	538	μs	

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Operation example of return from low power consumption mode (by internal resource reset*)



*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

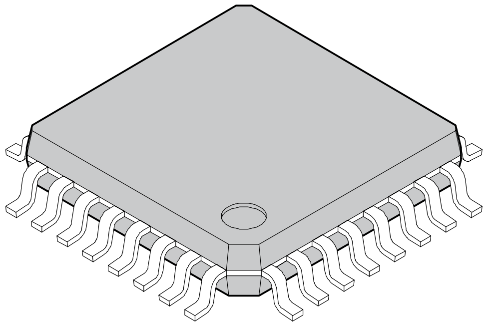
Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family PERIPHERAL MANUAL.
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See "CHAPTER: Low Power Consumption Mode" in "FM0+ Family PERIPHERAL MANUAL".*
- *The time during the power-on reset/low-voltage detection reset is excluded. See "14.4.7 Power-on Reset Timing " for the detail on the time during the power-on reset/low -voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

15. Ordering Information

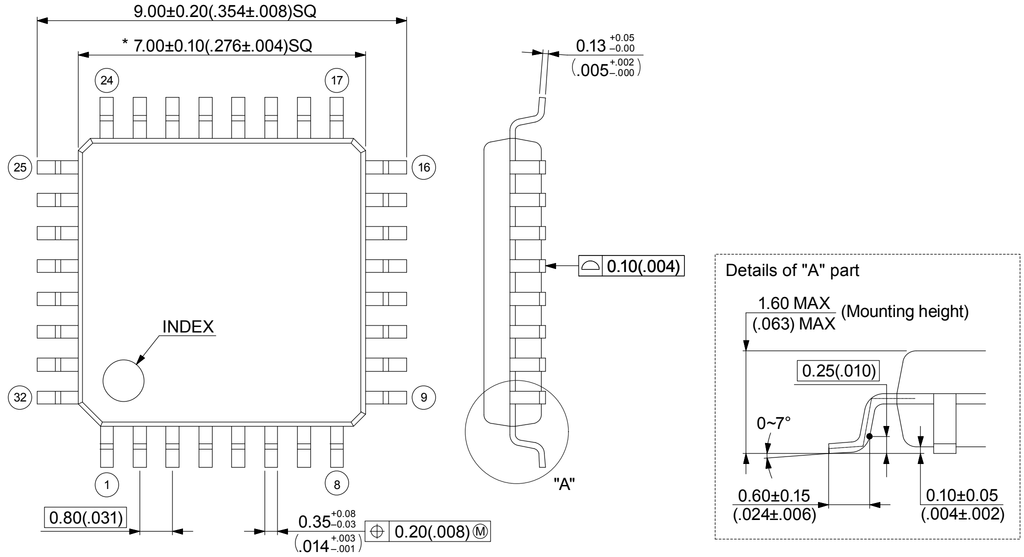
Part number	Package
S6E1A11B0AGP2	Plastic • LQFP (0.80 mm pitch), 32 pins (FPT-32P-M30)
S6E1A12B0AGP2	
S6E1A11B0AGN2	Plastic • QFN (0.50 mm pitch), 32 pins (LCC-32P-M73)
S6E1A12B0AGN2	
S6E1A11C0AGV2	Plastic • LQFP (0.50 mm pitch), 48 pins (FPT-48P-M49)
S6E1A12C0AGV2	
S6E1A11C0AGN2	Plastic • QFN (0.50 mm pitch), 48 pins (LCC-48P-M74)
S6E1A12C0AGN2	
S6E1A11C0AGF2	Plastic • LQFP (0.65 mm pitch), 52 pins (FPT-52P-M02)
S6E1A12C0AGF2	

16. Package Dimensions

<table>
<tr><td rowspan="7">32-pin plastic LQFP

(FPT-32P-M30)</td><td>Lead pitch</td><td>0.80 mm</td></tr>
<tr><td>Package width × package length</td><td>7.00 mm × 7.00 mm</td></tr>
<tr><td>Lead shape</td><td>Gullwing</td></tr>
<tr><td>Sealing method</td><td>Plastic mold</td></tr>
<tr><td>Mounting height</td><td>1.60 mm MAX</td></tr>
<tr><td></td><td></td></tr>
<tr><td></td><td></td></tr>
</table>

32-pin plastic LQFP
(FPT-32P-M30)

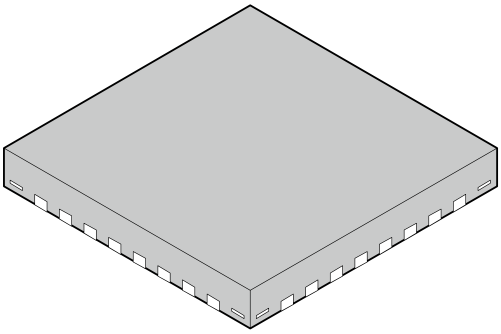
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



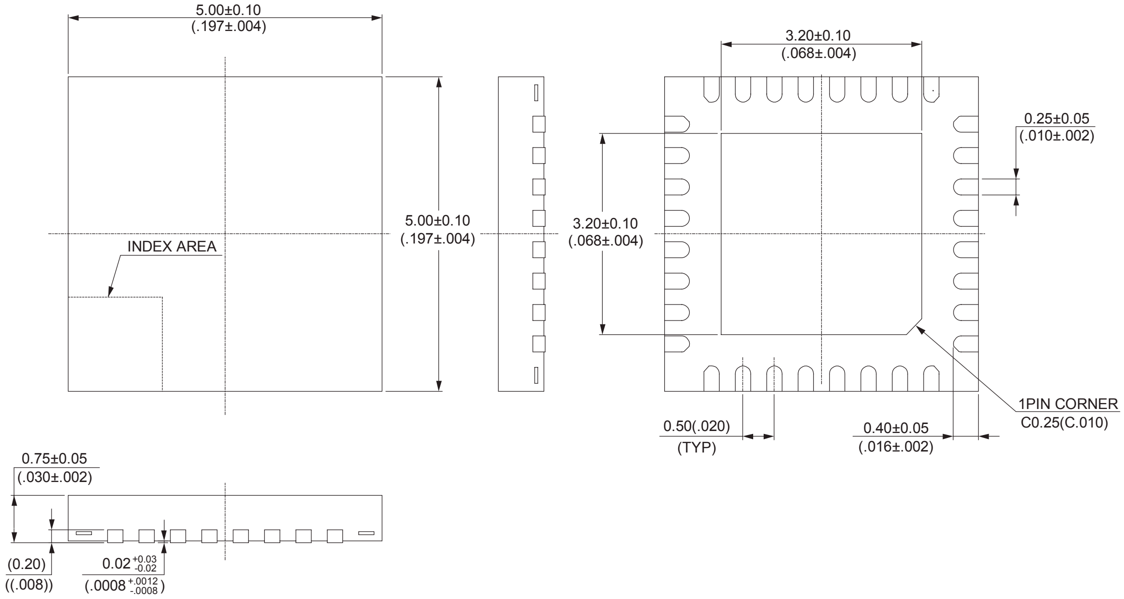
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.

http://edevice.fujitsu.com/package/en-search/

32-pin plastic QFN  (LCC-32P-M73)	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g

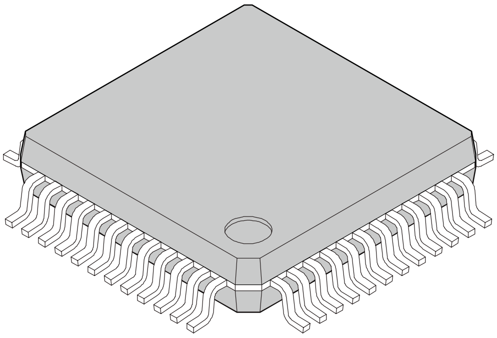
32-pin plastic QFN
(LCC-32P-M73)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

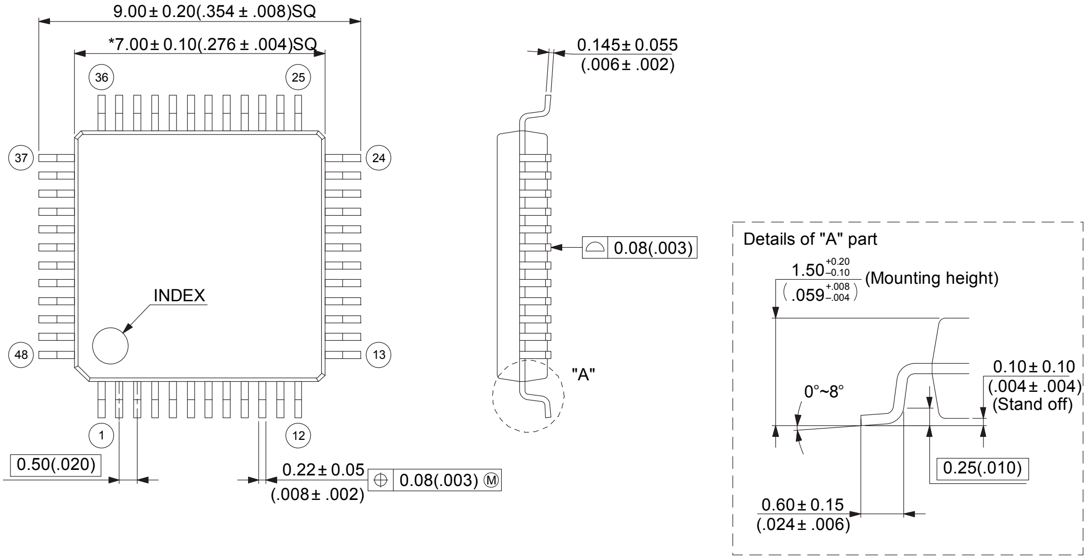
Please check the latest package dimension at the following URL.

http://edevice.fujitsu.com/package/en-search/

48-pin plastic LQFP	Lead pitch	0.50 mm
 (FPT-48P-M49)	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g

48-pin plastic LQFP
(FPT-48P-M49)

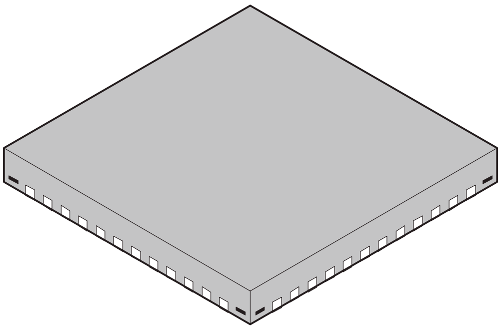
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



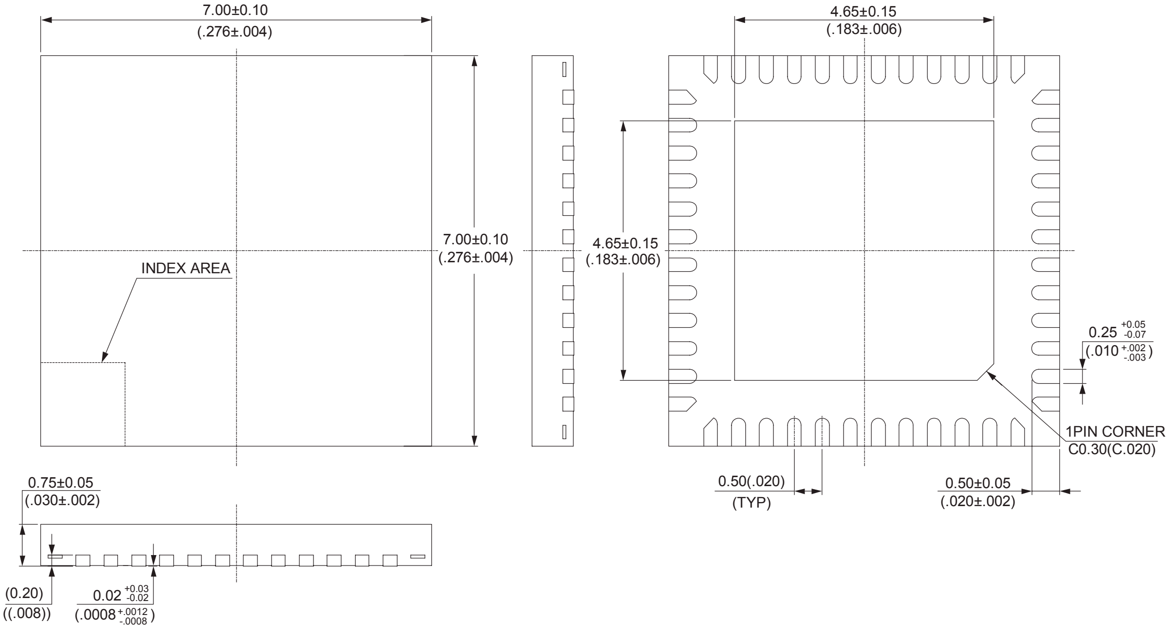
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.

http://edevice.fujitsu.com/package/en-search/

48-pin plastic QFN  (LCC-48P-M74)	Lead pitch	0.50 mm
	Package width× package length	7.00 mm × 7.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.12 g

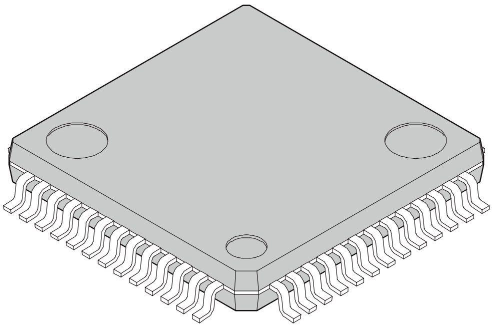
48-pin plastic QFN
(LCC-48P-M74)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

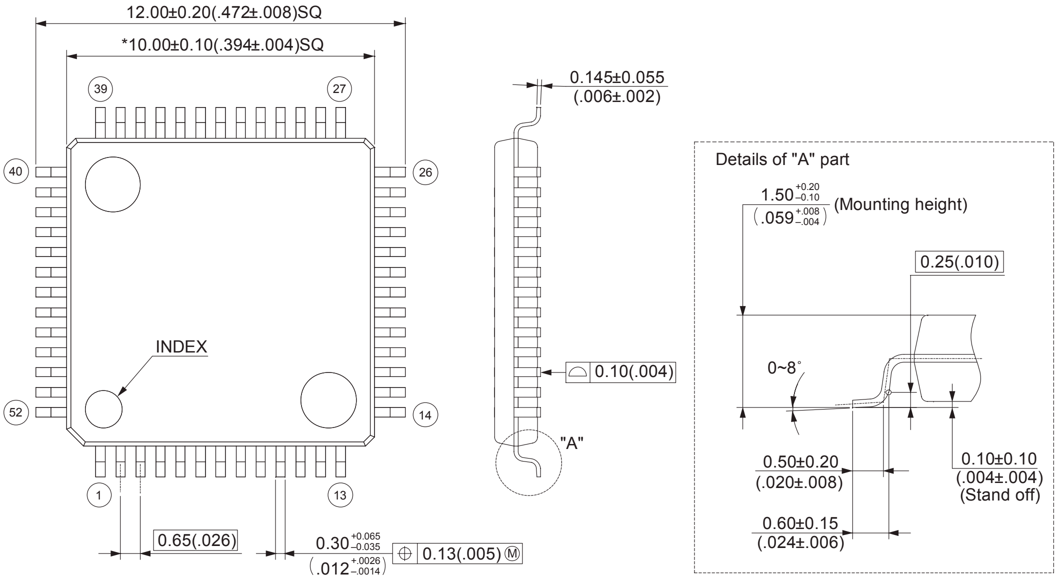
Please check the latest package dimension at the following URL.

http://edevice.fujitsu.com/package/en-search/

52-pin plastic LQFP  (FPT-52P-M02)	Lead pitch	0.65 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
	Code (Reference)	P-LFQFP52-10 × 10-0.65

52-pin plastic LQFP
(FPT-52P-M02)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.

http://edevice.fujitsu.com/package/en-search/

17. Major Changes

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0 [July 16,2014]		
-	-	Revised from "Preliminary" to "Full Production"
3	1. Description	Revised from "TYPE1" product to "TYPE1-M0+" product
5	2. Features	Revised "Processor version"
6	2. Features	Revised "Conversion time" of 12-bit A/D converter
9	3. Product Lineup	Added "Note" for accuracy of built-in CR
21,22,23, 24,25	6. List of Pin Functions List of pin functions	Revised Pin number 30 and 31 of LQFP-32 and QFN-32
23	6. List of Pin Functions List of pin functions	Revised Function description of SOT1_x(SDA1_x)
40	12. Memory Map Memory map (1)	Revised from "MTB resister" to "MTB resister(SFR)"
41	12. Memory Map Memory map (2)	Revised product name and RAM address
46	14. Electrical Characteristics 14.1 Absolute Maximum Ratings	Revised Analog pin input voltage
47	14. Electrical Characteristics 14.2 Recommended Operating Conditions	Added note "*2"
48,49,50	14. Electrical Characteristics 14.3 DC Characteristics 14.3.1 Current Rating	• Revised and added "Conditions" • Revised the value of "TBD"
52	14. Electrical Characteristics 14.4 AC Characteristics 14.4.1 Main Clock Input Characteristics	Revised the value of "Internal operating clock frequency" and "Internal operating clock cycle time"
54	14. Electrical Characteristics 14.4 AC Characteristics 14.4.3 Built-in CR Oscillation Characteristics	Revised the value of "TBD"
55	14. Electrical Characteristics 14.4 AC Characteristics 14.4.5 Operating Conditions of Main PLL(In the case of using the built-in high-speed CR clock as the input clock of the main PLL)	• Revised the value of "TBD" • Revised the maximum value of "Main PLL clock frequency"
56	14. Electrical Characteristics 14.4 AC Characteristics 14.4.7 Power-on Reset Timing	• Revised the value of "TBD" • Revised from "LVDL_minimum" to "VDH_minimum"
78	14. Electrical Characteristics 14.4 AC Characteristics 14.4.12 I2C Timing	• Revised the condition of "Noise filter" • Revised the note for noise filter
80	14. Electrical Characteristics 14.5 12-bit A/D Converter	• Revised the value of "Conversion time", "Sampling time" and "Compare clock cycle" • Revised the value of "State transition time to operation permission" • Revised the note
83,84	14. Electrical Characteristics 14.6 Low-voltage Detection Characteristics	Revised the value of SVHR and SVHI
85	14. Electrical Characteristics 14.7 Flash Memory Write/Erase Characteristics	• Revised the value of "TBD" • Revised the value of typical

Page	Section	Change Results
86,88	14. Electrical Characteristics 14.8 Return Time from Low-Power Consumption Mode	Revised the value of "TBD"
90	15. Ordering Information	Revised from "LCC-52P-M02" to "FPT-52P-M02"

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