

1.TYPE RD3G600GN

2.STRUCTURE SILICON N-CHANNEL MOS FET

3.APPLICATIONS SWITCHING

 4.ABSOLUTE MAXIMUM RATINGS [$T_a=25^{\circ}\text{C}$]

DRAIN-SOURCE VOLTAGE		V_{DSS}	...	40V	
GATE-SOURCE VOLTAGE		V_{GSS}	...	$\pm 20\text{V}$	
DRAIN CURRENT	CONTINUOUS	I_D	...	$\pm 60\text{A}$	
	PULSED	I_{DP}	...	$\pm 120\text{A}$	$P_w \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$
SOURCE CURRENT	CONTINUOUS	I_S	...	33A	
(BODY DIODE)	PULSED	I_{SP}	...	120A	$P_w \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$
AVALANCHE CURRENT		I_{AS}	...	30A	$L \approx 10\mu\text{H}$, $V_{DD}=20\text{V}$, $R_G=25 \Omega$ STARTING $T_{ch}=25^{\circ}\text{C}$ See Fig.3-1, 3-2
AVALANCHE ENERGY		E_{AS}	...	13mJ	$L \approx 10\mu\text{H}$, $V_{DD}=20\text{V}$, $R_G=25 \Omega$ STARTING $T_{ch}=25^{\circ}\text{C}$ See Fig.3-1, 3-2
POWER DISSIPATION		P_D	...	40W	$T_c=25^{\circ}\text{C}$
CHANNEL TEMPERATURE		T_{ch}	...	150°C	
RANGE OF STORAGE TEMPERATURE		T_{stg}	...	$-55 \sim 150^{\circ}\text{C}$	
5.THERMAL RESISTANCE					
CHANNEL TO CASE		$R_{th(ch-c)}$	...	3.1°C/W	$T_c=25^{\circ}\text{C}$

*Limited only by maximum channel temperature allowed.

DESIGN	CHECK	APPROVAL	DATE: 10/APR/2015	SPECIFICATION No. TSQ03139-RD3G600GN
<i>K. Suganuma</i>	<i>H. Niimoto</i>	<i>K. Yoshinochi</i>	REV.: 0	ROHM Co.,Ltd.

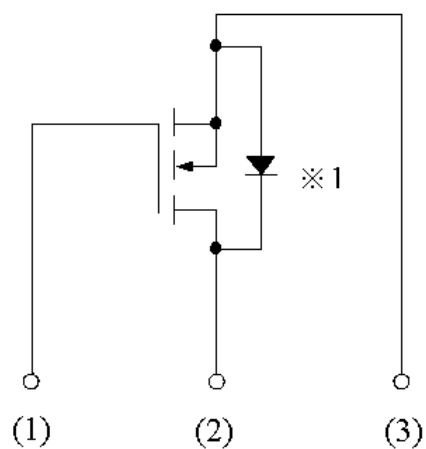
6.ELECTRICAL CHARACTERISTICS [$T_a=25^{\circ}\text{C}$]

PARAMETER	ITEM	CONDITION		MIN.	TYP.	MAX.
GATE-SOURCE-LEAKAGE	I _{GSS}	V _{GS} =±20V / V _{DS} =0V		—	—	±500nA
DRAIN-SOURCE BREAKDOWN VOLTAGE	V _{(BR)DSS}	I _D =1mA / V _{GS} =0V		40V	—	—
ZERO GATE VOLTAGE DRAIN CURRENT	I _{DSS}	V _{DS} =40V / V _{GS} =0V		—	—	1uA
GATE THRESHOLD VOLTAGE	V _{GS(th)}	V _{GS} =V _{DS} / I _D =1mA		1.0V	—	2.5V
STATIC DRAIN-SOURCE ON-STATE RESISTANCE	R _{DS(on)} *PULSED	I _D =60A / V _{GS} =10V		—	2.8mΩ	3.6mΩ
		I _D =60A / V _{GS} =4.5V		—	3.3mΩ	4.3mΩ
FORWARD TRANSFER ADMITTANCE	Y _{fs} *PULSED	V _{DS} =5V / I _D =30A		30S	—	—
INPUT CAPACITANCE	C _{iss}	V _{DS} =20V V _{GS} =0V f=1MHz		—	3400pF	—
OUTPUT CAPACITANCE	C _{oss}			—	550pF	—
REVERSE TRANSFER CAPACITANCE	C _{rss}			—	150pF	—
TURN-ON DELAY TIME	t _{d(on)} *PULSED	V _{DD} ≈20V I _D =30A V _{GS} =10V R _L =0.67Ω R _G =10Ω See Fig.1-1, 1-2		—	11ns	—
RISE TIME	t _r *PULSED			—	11ns	—
TURN-OFF DELAY TIME	t _{d(off)} *PULSED			—	80ns	—
FALL TIME	t _f *PULSED			—	20ns	—
TOTAL GATE CHARGE	Q _g *PULSED	V _{DD} ≈20V I _D =50A See Fig.2-1, 2-2	V _{GS} =10V	—	46.5nC	—
				—	23.5nC	—
GATE-SOURCE CHARGE	Q _{gs} *PULSED		V _{GS} =4.5V	—	8.8nC	—
GATE-DRAIN CHARGE	Q _{gd} *PULSED			—	6.7nC	—

BODY DIODE (SOURCE-DRAIN)

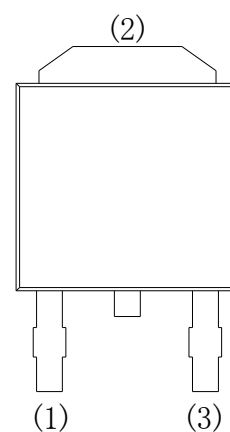
PARAMETER	ITEM	CONDITION	MIN.	TYP.	MAX.
FORWARD VOLTAGE	V_{SD} *PULSED	$I_{\text{S}}=33\text{A} / V_{\text{GS}}=0\text{V}$	–	–	1.2V
REVERSE RECOVERY TIME	t_{rr} *PULSED	$I_{\text{S}}=30\text{A} / V_{\text{GS}}=0\text{V}$ $di/dt=100\text{A}/\mu\text{s}$	–	38ns	–
REVERSE RECOVERY CHARGE	Q_{rr} *PULSED		–	24nC	–

7.INNER CIRCUIT

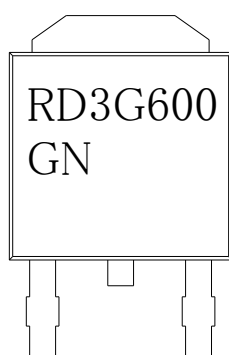


※1 BODY DIODE

- (1) GATE
- (2) DRAIN
- (3) SOURCE



8.MARKING



9. MEASUREMENT CIRCUIT

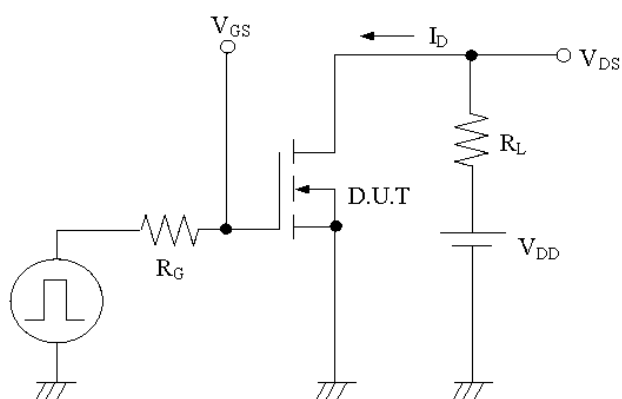


Fig.1-1 SWITCHING TIME MEASUREMENT CIRCUIT

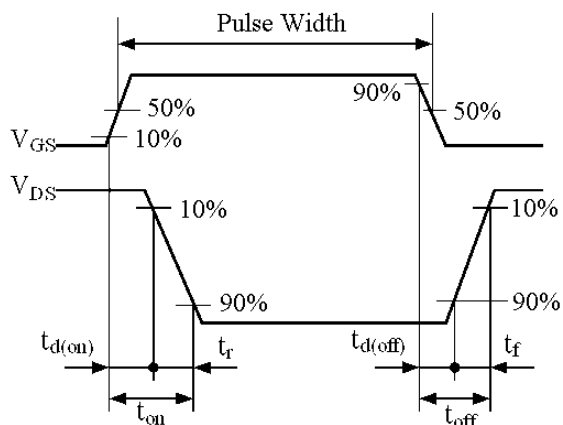


Fig.1-2 SWITCHING WAVEFORMS

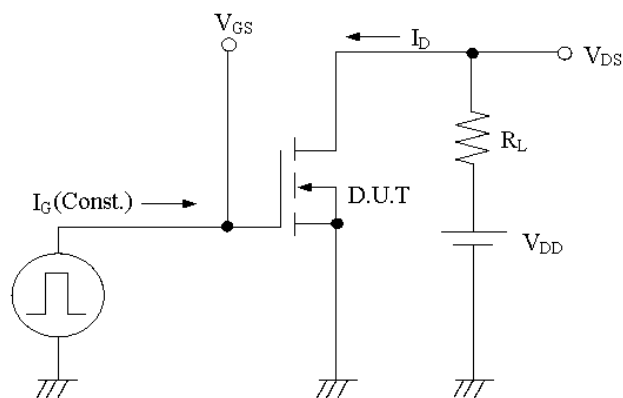


Fig.2-1 GATE CHARGE MEASUREMENT CIRCUIT

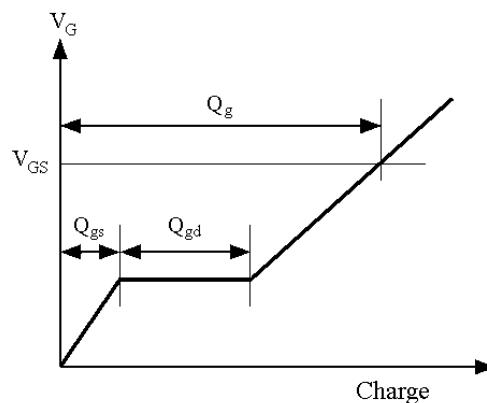


Fig.2-2 GATE CHARGE WAVEFORM

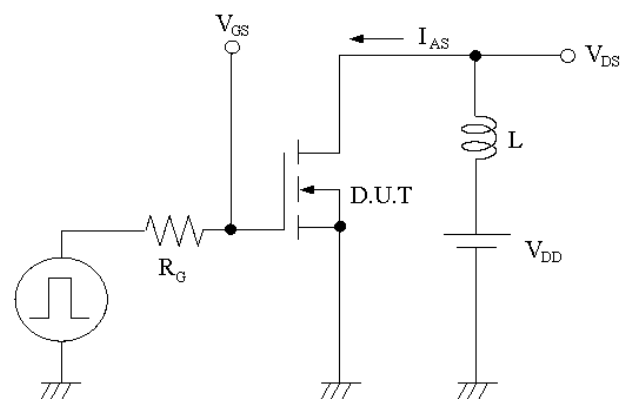


Fig.3-1 AVALANCHE MEASUREMENT CIRCUIT

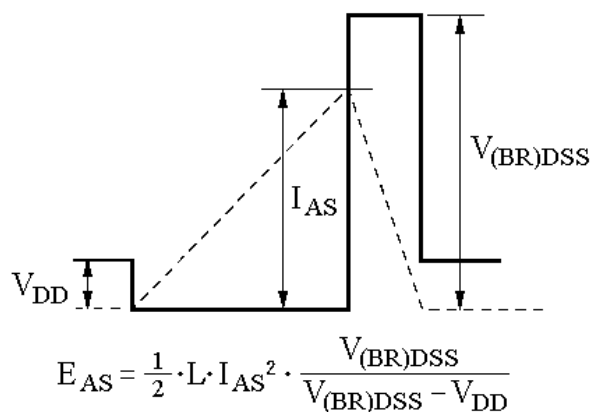


Fig.3-2 AVALANCHE WAVEFORM