# **Dual Type D Flip-Flop**

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and  $\overline{Q}$ ). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

### **Features**

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design
- Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive—going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B
- Pb-Free Packages are Available\*

## MAXIMUM RATINGS (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage Range (DC or Transient)	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient) per Pin	±10	mA
P <sub>D</sub>	Power Dissipation, per Package (Note 1)	500	mW
T <sub>A</sub>	Ambient Temperature Range	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



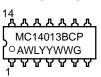
# ON Semiconductor®

http://onsemi.com

# MARKING DIAGRAMS



PDIP-14 P SUFFIX CASE 646





SOIC-14 D SUFFIX CASE 751A



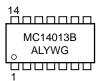


TSSOP-14 DT SUFFIX CASE 948G





SOEIAJ-14 F SUFFIX CASE 965



A = Assembly Location

 $\begin{array}{ll} \text{WL, L} &= \text{Wafer Lot} \\ \text{YY, Y} &= \text{Year} \\ \text{WW, W} &= \text{Work Week} \\ \text{G} &= \text{Pb-Free Indicator} \end{array}$ 

# **ORDERING INFORMATION**

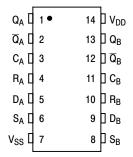
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

TRUTH TABLE

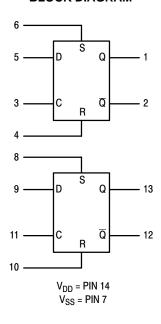
Inputs				Out	outs
Clock†	Data	Reset	Set	Q	Q
	0	0	0	0	1
	1	0	0	1	0
~	Х	0	0	Q	Q
X	Х	1	0	0	1
X	Х	0	1	1	0
Х	Х	1	1	1	1

No Change

# **PIN ASSIGNMENT**



# **BLOCK DIAGRAM**



# **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC14013BCP	PDIP-14	500 Units / Rail
MC14013BCPG	PDIP-14 (Pb-Free)	500 Units / Rail
MC14013BD	SOIC-14	55 Units / Rail
MC14013BDG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14013BDR2	SOIC-14	2500 Units / Tape & Reel
MC14013BDR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel
MC14013BDTR2	TSSOP-14*	2500 Units / Tape & Reel
MC14013BF	SOEIAJ-14	50 Units / Rail
MC14013BFEL	SOEIAJ-14	2000 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
\*This package is inherently Pb–Free.

X = Don't Care

<sup>† =</sup> Level Change

# **ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

		V <sub>DD</sub>	- 5	5°C		25°C		125	5°C	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ <sup>(2)</sup>	Max	Min	Max	Unit
Output Voltage "0" Lev	el V <sub>OL</sub>	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub> "1" Lev	el V <sub>OH</sub>	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Input Voltage "0" Lev $(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$ $(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$ $(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$	el V <sub>IL</sub>	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ "1" Lev $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	el V <sub>IH</sub>	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	Vdc
Output Drive Current $(V_{OH} = 2.5 \text{ Vdc}) \qquad \text{Sour}$ $(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$	I <sub>OH</sub>	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	- - - -	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	- - -	- 1.7 - 0.36 - 0.9 - 2.4	- - - -	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ Sin $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	ık I <sub>OL</sub>	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current	I <sub>in</sub>	15	_	± 0.1	_	±0.00001	± 0.1	-	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	_	_	-	_	5.0	7.5	_	-	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0 10 15	- - -	1.0 2.0 4.0	- - -	0.002 0.004 0.006	1.0 2.0 4.0	- - -	30 60 120	μAdc
Total Supply Current <sup>(3)</sup> <sup>(4)</sup> (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15			$I_T = ($	.75 μΑ/kHz) 1.5 μΑ/kHz) f 2.3 μΑ/kHz) f	+ I <sub>DD</sub>			μAdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF:

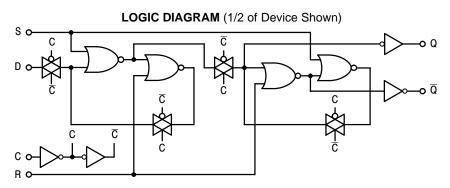
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

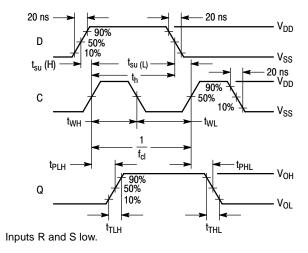
where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts, f in kHz is input frequency, and k = 0.002.

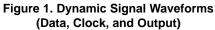
# SWITCHING CHARACTERISTICS <sup>(5)</sup> $(C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C})$

Characteristic	Symbol	$V_{DD}$	Min	Typ <sup>(6)</sup>	Max	Unit
Output Rise and Fall Time	t <sub>TLH</sub> ,					ns
$t_{TLH}$ , $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns	t <sub>THL</sub>	5.0	_	100	200	
$t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		10	_	50	100	
$t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$		15	_	40	80	
Propagation Delay Time	t <sub>PLH</sub>					ns
Clock to Q, Q	t <sub>PHL</sub>					
$t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$		5.0	_	175	350	
$t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$		10	_	75	150	
$t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$		15	_	50	100	
Set to Q, Q						
$t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$		5.0	_	175	350	
$t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 42 \text{ ns}$		10	_	75	150	
$t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 25 \text{ ns}$		15	_	50	100	
Reset to Q, $\overline{Q}$						-
$t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$		5.0	_	225	450	
$t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 67 \text{ ns}$		10	_	100	200	
$t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 50 \text{ ns}$		15	_	75	150	
Setup Times (7)	t <sub>su</sub>	5.0	40	20	_	ns
	Ju	10	20	10	_	
		15	15	7.5	-	
Hold Times (7)	t <sub>h</sub>	5.0	40	20	_	ns
	"	10	20	10	_	
		15	15	7.5	-	
Clock Pulse Width	t <sub>WL</sub> , t <sub>WH</sub>	5.0	250	125	_	ns
		10	100	50	_	
		15	70	35	-	
Clock Pulse Frequency	f <sub>cl</sub>	5.0	_	4.0	2.0	MHz
	o.	10	_	10	5.0	
		15	_	14	7.0	
Clock Pulse Rise and Fall Time	t <sub>TLH</sub>	5.0	_	_	15	μS
	t <sub>THL</sub>	10	_	_	5.0	
	THE	15	_	_	4.0	
Set and Reset Pulse Width	t <sub>WL</sub> , t <sub>WH</sub>	5.0	250	125	_	ns
	- VVL7 - VVII	10	100	50	_	
		15	70	35	-	
Removal Times	t <sub>rem</sub>					ns
Set	10111	5	80	0	_	
		10	45	5	_	
		15	35	5	_	
Reset		5	50	- 35	_	1
		10	30	- 10	-	
		15	25	- 5	-	

- 5. The formulas given are for the typical characteristics only at 25°C.
  6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
  7. Data must be valid for 250 ns with a 5 V supply, 100 ns with 10 V, and 70 ns with 15 V.







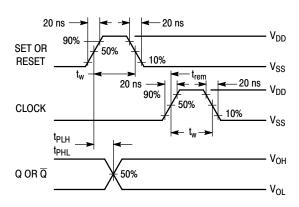
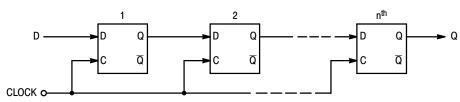


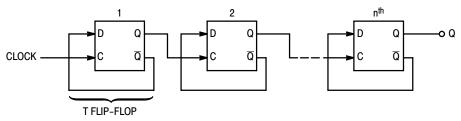
Figure 2. Dynamic Signal Waveforms (Set, Reset, Clock, and Output)

# **TYPICAL APPLICATIONS**

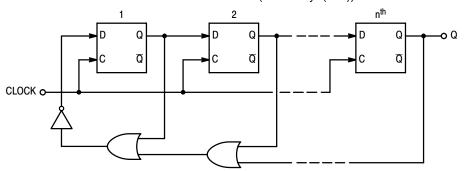
## n-STAGE SHIFT REGISTER



# BINARY RIPPLE UP-COUNTER (Divide-by-2<sup>n</sup>)

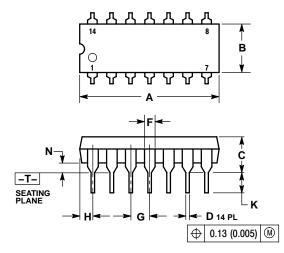


# MODIFIED RING COUNTER (Divide-by-(n+1))



## **PACKAGE DIMENSIONS**

# PDIP-14 **P SUFFIX CASE 646-06 ISSUE N**





#### NOTES:

- NOTES:

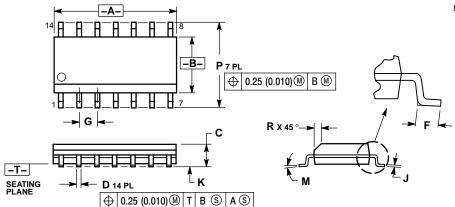
  1. DIMENSIONING AND TOLERANCING
  PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: INCH.

  3. DIMENSION L TO CENTER OF LEADS
  WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.715	0.770	18.16	18.80
В	0.240	0.260	6.10	6.60
O	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
O	0.100	BSC	2.54	BSC
Н	0.052	0.095	1.32	2.41
۲	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M		10 °		10 °
N	0.015	0.039	0.38	1.01

# SOIC-14 **D SUFFIX CASE 751A-03 ISSUE G**



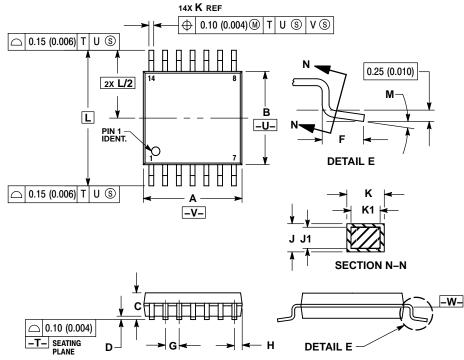
- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) DED SIDE
- 4. MAAIMUM MICLE PROTROSIGN 6.15 (6.6 PER SIDE.

  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
М	0 °	7°	0 °	7°
Р	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

## PACKAGE DIMENSIONS

TSSOP-14 **DT SUFFIX** CASE 948G-01 **ISSUE 0** 



- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.00) PER SIDE

  - MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

    4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

    5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. CONDITION.
    6. TERMINAL NUMBERS ARE SHOWN FOR

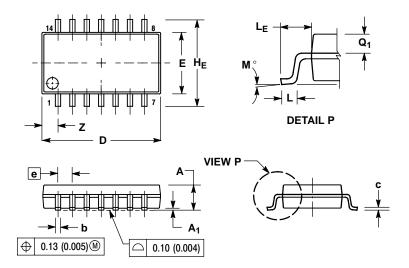
  - REFERENCE ONLY.

    7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
ם	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026 BSC	
Η	0.50	0.60	0.020	0.024
7	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
М	0 °	8°	0 °	8 °

## PACKAGE DIMENSIONS

SOEIAJ-14 **F SUFFIX CASE 965-01 ISSUE 0** 



### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION: MILLIMETER.
  3 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
  THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH
  DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05	-	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
е	1.27	BSC	0.050 BSC	
HE	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z		1.42		0.056

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