MC14013B

Dual Type D Flip-Flop

The MC14013B dual type D flip–flop is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each flip–flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip–flops for counter and toggle applications.

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Features

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge–Clocked Flip–Flop Design
- Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive–going edge of the clock pulse
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin–for–Pin Replacement for CD4013B
- Pb–Free Packages are Available*

MARKING DIAGRAMS

PDIP–14
P SUFFIX
CASE 646

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14
MC14013BCP
 AWLYYWWG
1
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SOIC–14
D SUFFIX
CASE 751A

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14
14013BG
 AWLYWW
1
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TSSOP–14
DT SUFFIX
CASE 948G

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14
14
013B
 ALYW
1
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SOEIAJ–14
F SUFFIX
CASE 965

```
14
MC14013B
 ALYWG
1
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A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb–Free Indicator

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
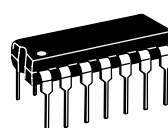
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
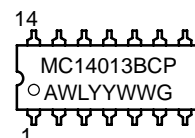
ORDERING INFORMATION
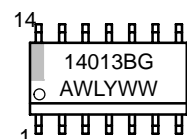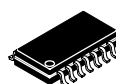
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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TRUTH TABLE

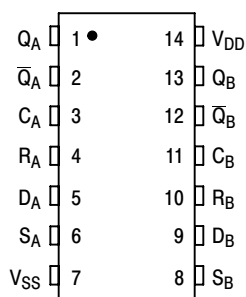| Inputs				Outputs	
Clock†	Data	Reset	Set	Q	$\overline{\text{Q}}$
⌐	0	0	0	0	1
⌐	1	0	0	1	0
⌐	X	0	0	Q	$\overline{\text{Q}}$ No Change
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

X = Don't Care
† = Level Change

PIN ASSIGNMENT

Q_A — 1 ●   14 — V_{DD}
$\overline{Q}_A$ — 2   13 — Q_B
C_A — 3   12 — $\overline{Q}_B$
R_A — 4   11 — C_B
D_A — 5   10 — R_B
S_A — 6   9 — D_B
V_{SS} — 7   8 — S_B

BLOCK DIAGRAM

V_{DD} = PIN 14
V_{SS} = PIN 7
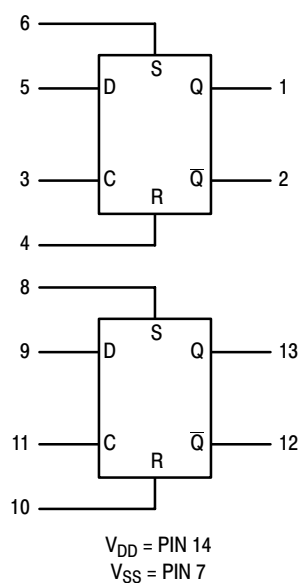
ORDERING INFORMATION

Device	Package	Shipping†
MC14013BCP	PDIP−14	500 Units / Rail
MC14013BCPG	PDIP−14 (Pb−Free)	500 Units / Rail
MC14013BD	SOIC−14	55 Units / Rail
MC14013BDG	SOIC−14 (Pb−Free)	55 Units / Rail
MC14013BDR2	SOIC−14	2500 Units / Tape & Reel
MC14013BDR2G	SOIC−14 (Pb−Free)	2500 Units / Tape & Reel
MC14013BDTR2	TSSOP−14*	2500 Units / Tape & Reel
MC14013BF	SOEIAJ−14	50 Units / Rail
MC14013BFEL	SOEIAJ−14	2000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ [2]	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	 5.0 10 15	 − − −	 1.5 3.0 4.0	 − − −	 2.25 4.50 6.75	 1.5 3.0 4.0	 − − −	 1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	 5.0 5.0 10 15	 − 3.0 − 0.64 − 1.6 − 4.2	 − − − −	 − 2.4 − 0.51 − 1.3 − 3.4	 − 4.2 − 0.88 − 2.25 − 8.8	 − − − −	 − 1.7 − 0.36 − 0.9 − 2.4	 − − − −	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	− − −	0.51 1.3 3.4	0.88 2.25 8.8	− − −	0.36 0.9 2.4	− − −	mAdc
Input Current	I_{in}	15	−	± 0.1	—	±0.00001	± 0.1	−	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	− − −	1.0 2.0 4.0	− − −	0.002 0.004 0.006	1.0 2.0 4.0	− − −	30 60 120	µAdc
Total Supply Current [3] [4] (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15		I_T = (0.75 µA/kHz) f + I_{DD} I_T = (1.5 µA/kHz) f + I_{DD} I_T = (2.3 µA/kHz) f + I_{DD}					µAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.002.

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SWITCHING CHARACTERISTICS [5] (C_L = 50 pF, T_A = 25°C)

| Characteristic	Symbol	V_{DD}	Min	Typ [6]	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	− − −	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q, $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns Set to Q, $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns Reset to Q, $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns	t_{PLH} t_{PHL}	5.0 10 15 5.0 10 15 5.0 10 15	− − − − − − − − −	175 75 50 175 75 50 225 100 75	350 150 100 350 150 100 450 200 150	ns
Setup Times [7]	t_{su}	5.0 10 15	40 20 15	20 10 7.5	− − −	ns
Hold Times [7]	t_h	5.0 10 15	40 20 15	20 10 7.5	− − −	ns
Clock Pulse Width	t_{WL}, t_{WH}	5.0 10 15	250 100 70	125 50 35	− − −	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	− − −	4.0 10 14	2.0 5.0 7.0	MHz
Clock Pulse Rise and Fall Time	t_{TLH} t_{THL}	5.0 10 15	− − −	− − −	15 5.0 4.0	µs
Set and Reset Pulse Width	t_{WL}, t_{WH}	5.0 10 15	250 100 70	125 50 35	− − −	ns
Removal Times Set Reset	t_{rem}	5 10 15 5 10 15	80 45 35 50 30 25	0 5 5 − 35 − 10 − 5	− − − − − −	ns

5. The formulas given are for the typical characteristics only at 25°C.
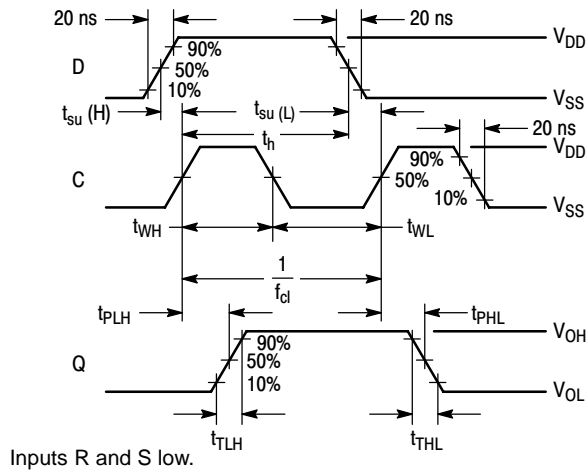6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
7. Data must be valid for 250 ns with a 5 V supply, 100 ns with 10 V, and 70 ns with 15 V.
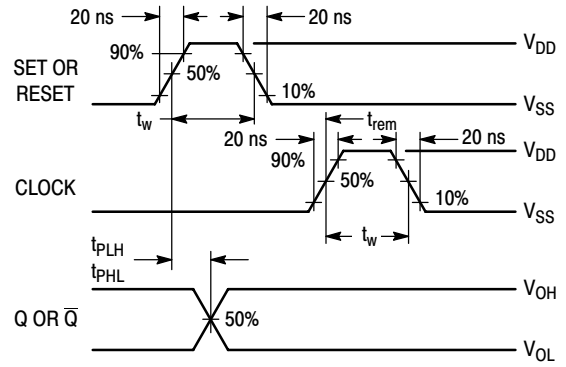
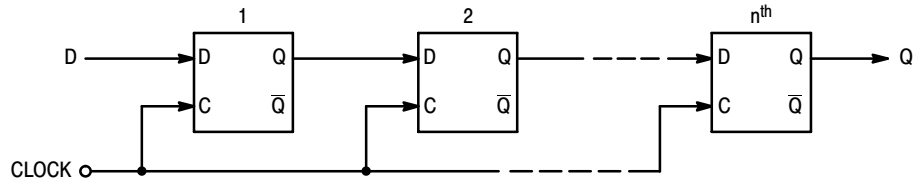## LOGIC DIAGRAM (1/2 of Device Shown)
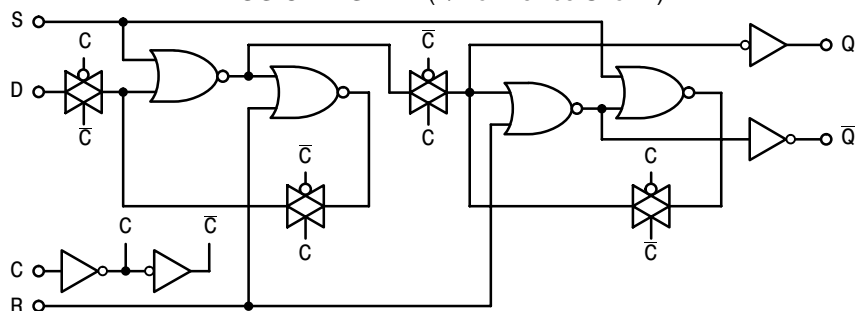
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**Figure 1. Dynamic Signal Waveforms
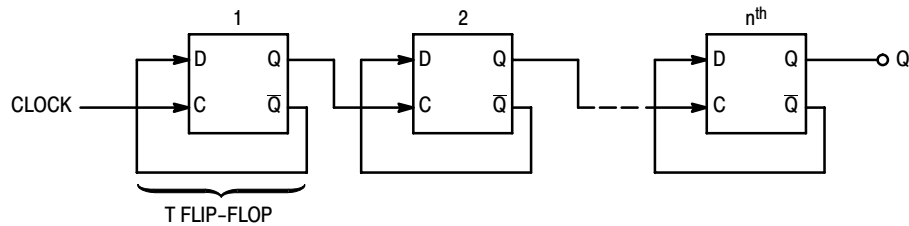(Data, Clock, and Output)**

**Figure 2. Dynamic Signal Waveforms
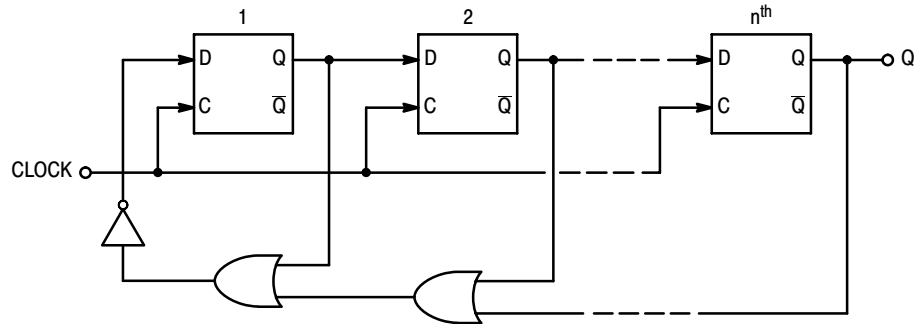(Set, Reset, Clock, and Output)**

TYPICAL APPLICATIONS

n−STAGE SHIFT REGISTER
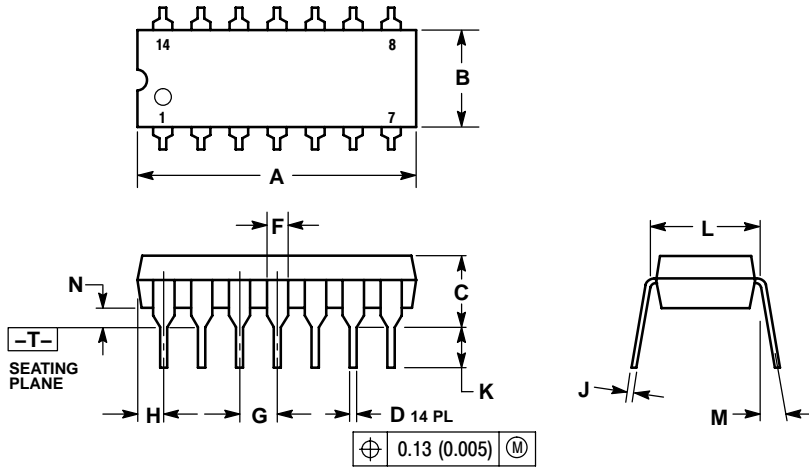

BINARY RIPPLE UP−COUNTER (Divide−by−2^n)

MODIFIED RING COUNTER (Divide−by−(n+1))

MC14013B

## PACKAGE DIMENSIONS

PDIP–14
P SUFFIX
CASE 646–06
ISSUE N

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	–––	10 °	–––	10 °
N	0.015	0.039	0.38	1.01

SOIC–14
D SUFFIX
CASE 751A–03
ISSUE G
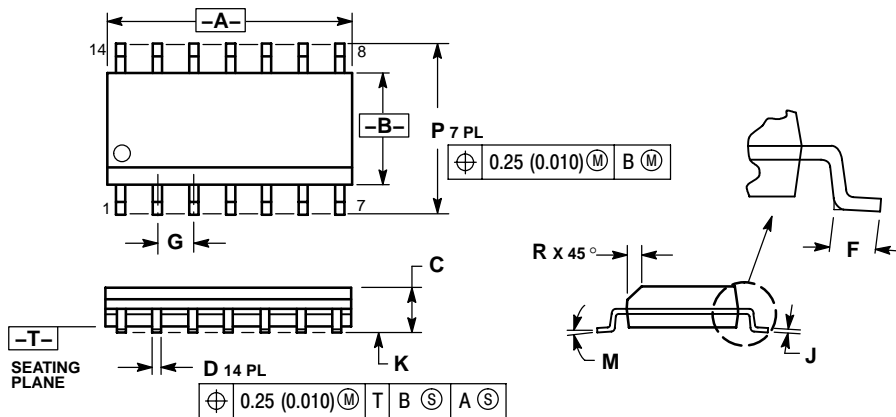
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
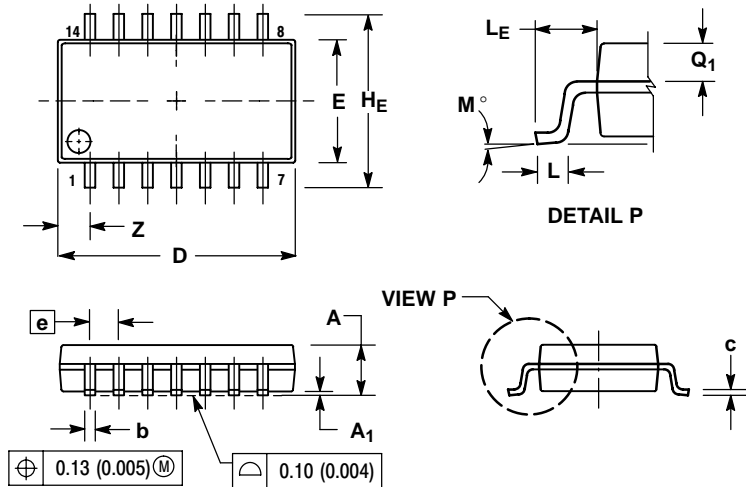
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

MC14013B

PACKAGE DIMENSIONS

TSSOP−14
DT SUFFIX
CASE 948G−01
ISSUE O

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

MC14013B

PACKAGE DIMENSIONS

SOEIAJ–14
F SUFFIX
CASE 965–01
ISSUE O

DETAIL P

VIEW P

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

PUBLICATION ORDERING INFORMATION