MB86S02 CMOS Image Sensor with 1/7 inch 110k Array and Color Processor

Version 0.9

Description

MB86S02 CMOS Image Sensor is a fully integrated digital video-imaging chip. It incorporates a highly sensitive photodiode array, FPN reduction read-out circuitry, analog-to-digital converter, timing generator, and a digital color processor. The excellent analog circuit design enables the very low power operation. All camera functions, such as gain, white balance, black clamp level, color processing, gamma, are programmable through I2C serial interface.

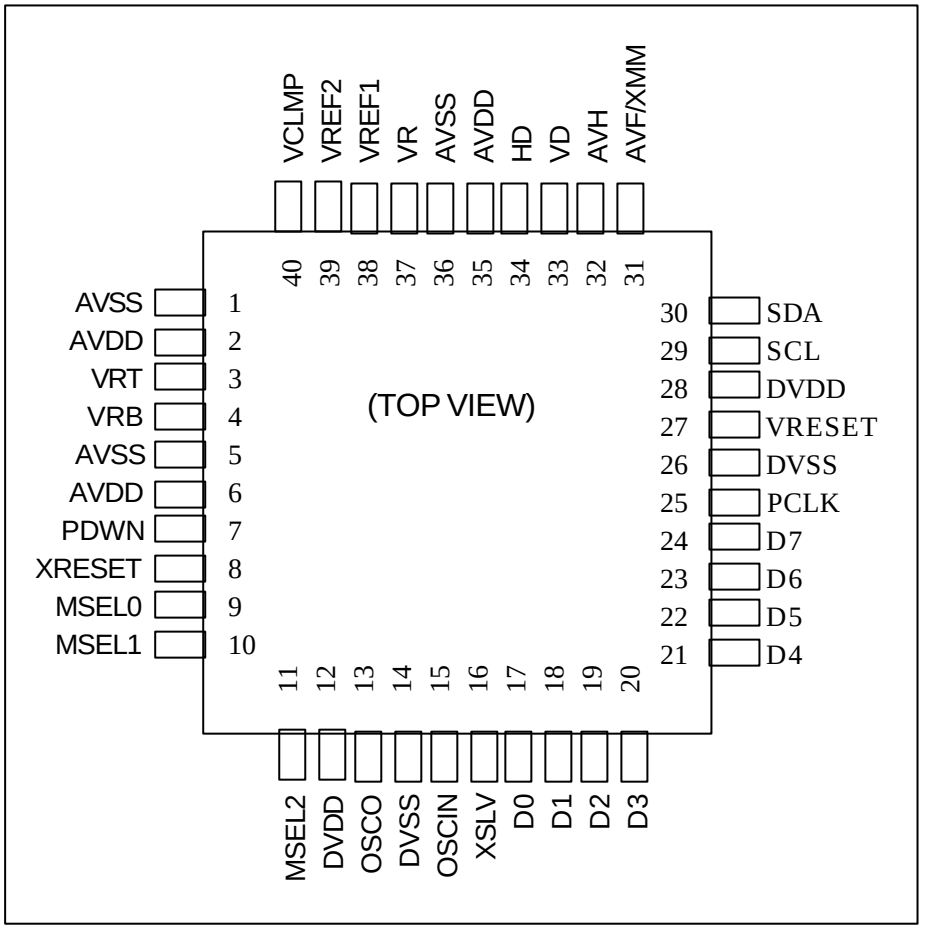
Features

- CIF (352 x 288) compatible image array size
- Additional QCIF-sized output
- Very low power operation
- Power saving operation with intermittent exposure mode
- Primary color mosaic filter and micro lens array
- Digital YUV 422 output
- Support CCIR656 standard headers
- Auto exposure and gain control
- Auto white balance control
- Programmable gamma and aperture correction
- Both horizontal and vertical mirror inversion
- Single 2.8V power supply
- Internal voltage reference
- Progressive scanning up to 30 frame/s
- Start up programming with external I2C EEPROM
- Stand by mode
- I2C serial interface

Specifications

Electrical Specifications	
Total Array Size	373(H) x 301(V)
Pixel Size	5.5 µm x 5.5 µm
Sensitivity	29 mV/lx @ 33 ms
Saturation	600 mV
SN ratio	47 dB
Supply Voltage	2.8 V
Power Consumption (Typical)	30 mW @15 f/s (Decrease to 25 mW on power save mode)
Operating Temperature	-25 to 65 degrees in C.

Pin Assignment

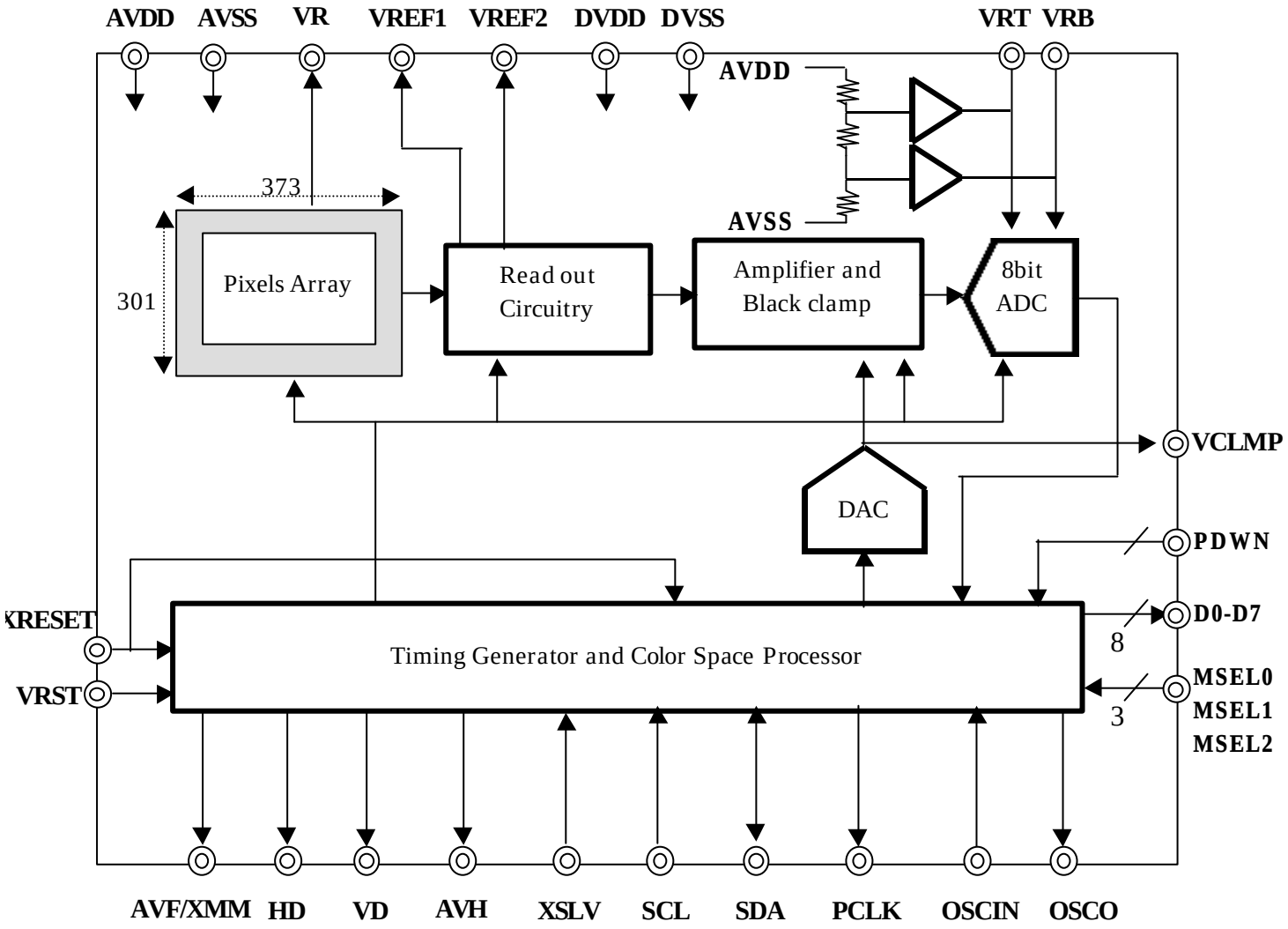


Pin Functions

Pin Name	I/O	Pin Number	Description
AVDD	-	2, 6, 35	Analog power supply.
AVSS	-	1, 5, 36	Analog ground.
VR	O	37	Sensors reference voltage.
VREF1	O	38	Voltage reference No.1.
VREF2	O	39	Voltage reference No.2.
VRT	O	3	Upper level voltage of AD converter.
VRB	O	4	Lower level voltage of AD converter.
VCLMP	O	40	Black clamp voltage.
DVDD	-	12, 28	Digital power supply.
DVSS	-	14, 26	Digital ground.
D7	O	24	Video data output. D7 is MSB and D0 is LSB.
D6	O	23	
D5	O	22	
D4	O	21	
D3	O	20	
D2	O	19	
D1	O	18	
D0	O	17	
OSCIN	I	15	Oscillator input
OSCO	O	13	Oscillator output.
PCLK	O	25	Pixel clock output.
HD	O	34	Horizontal sync.
VD	O	33	Vertical sync.
XRESET	I	8	Reset input. “L” for reset.
PDWN	I	7	Power down. “H” for power down.
AVH	O	32	Horizontal active video.
AVF/XMM	O	31	Active frame or master mode indicator
SCL	I/O	29	I2C clock.
SDA	I/O	30	I2C data.
XSLV	I	16	I2C mode. L: slave mode. H: master mode (*Note1)
MSEL0	I	9	Mode select. L: normal operation. H: test mode
MSEL1	I	10	EEPROM I2C address. L: A1h, H: A3h
MSEL2	I	11	The I2C slave address. L: C2h(write), C3h(read); H: C0h(write), C1h(read)
VRESET	I	27	Vertical timing reset.

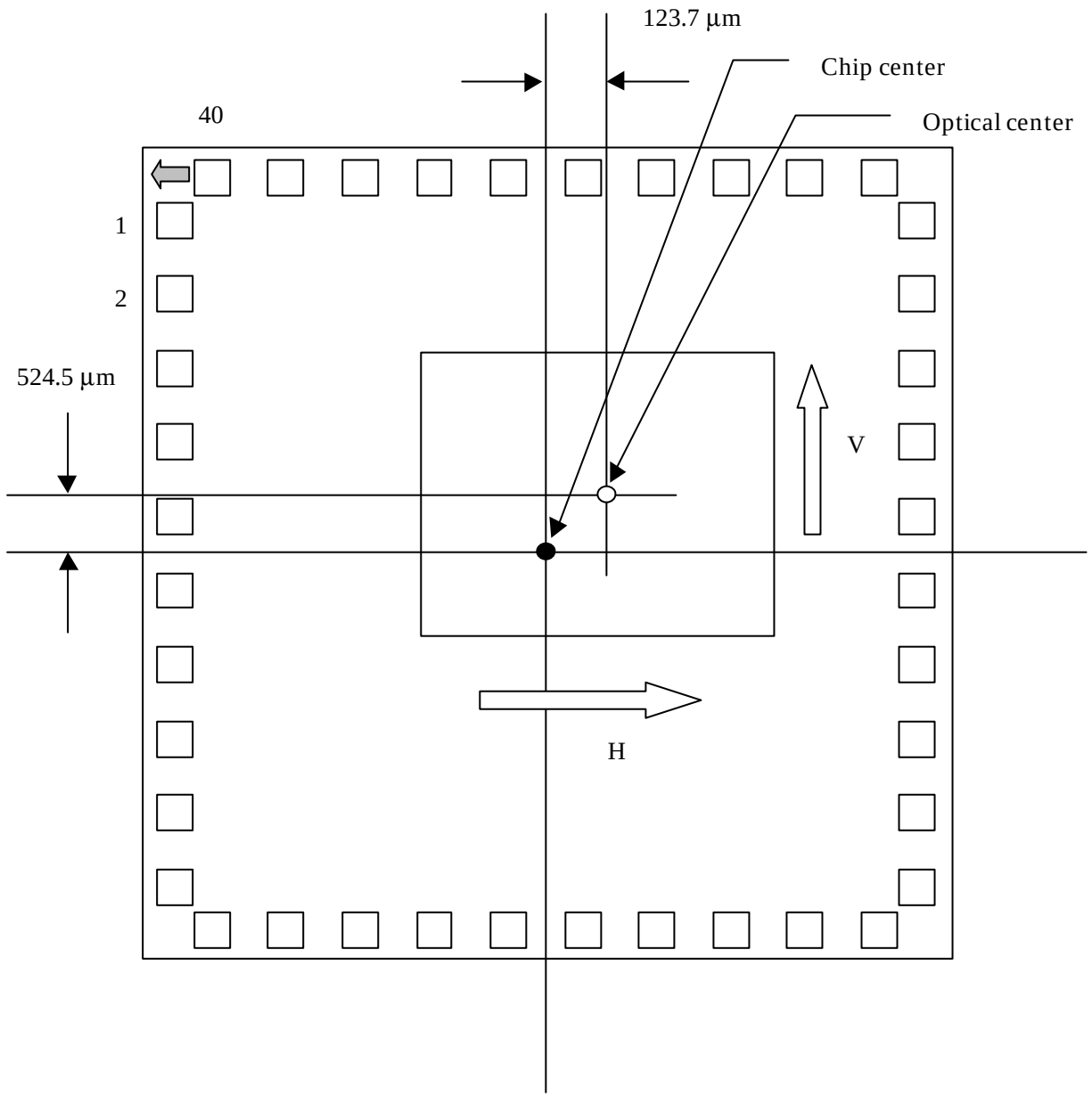
*Note1: When XSLV is connected to DVDD, MB86S02 set the I2C interface to master mode during the loading of the EEPROM data. After all data is stored, the I2C interface turns to slave mode.

Block Diagram

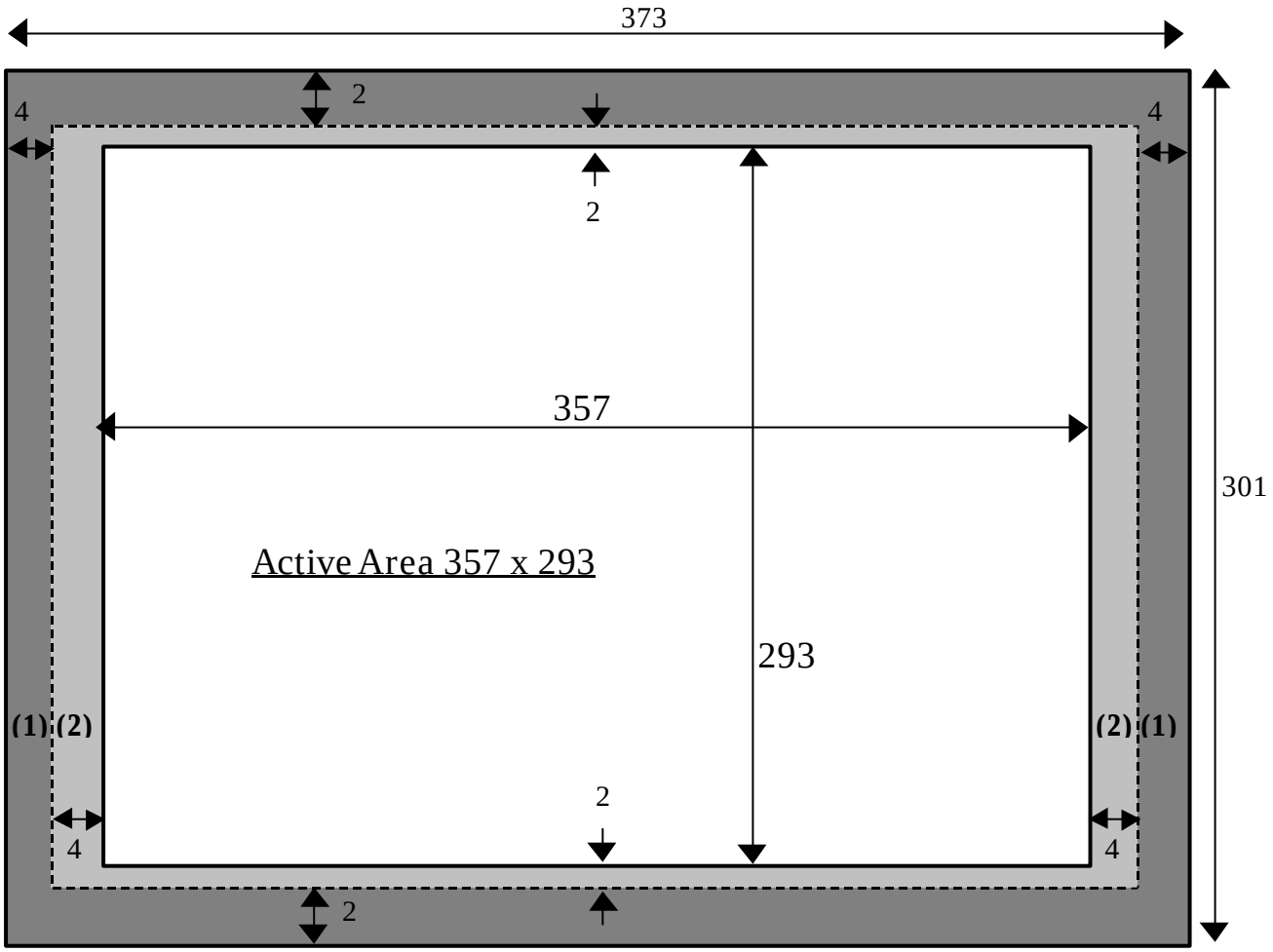


Optical Center and Scan Direction

The optical center of the pixel array is show in below and the default scan directions are indicated by arrows. (Top View)



Pixel Array Format



(1) Optical Black1
(2) Optical Black2 (for internal test use)

Color filters in active area are formatted as follows.

	1	2	3	4	---	353	354	356	357
293	R	G	R	G	---	G	R	G	R
292	G	B	G	B	---	B	G	B	G
291	R	G	R	G	---	G	R	G	R
290	G	B	G	B	---	B	G	B	G
---	---	---	---	---	---	---	---	---	---
4	G	B	G	B	---	B	G	B	G
3	R	G	R	G	---	G	R	G	R
2	G	B	G	B	---	B	G	B	G
1	R	G	R	G	---	G	R	G	R

Electrical Characteristics

Absolute maximum ratings

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	AVDD, DVDD	-0.3	4.0	V
Input and output voltage	VR, VREF1, VREF2, VRT, VRB, VCLMP	-0.3	AVDD+0.3	V
	D0 to D7, OSCIN, OSCO, PCLK, HD, VD, XRESET, PDWN, AVH, AVF/XMM, MSEL0, MSEL1, MSEL2, VRESET	-0.3	DVDD+0.3	V
Storage temperature	Tstg	-35	85	C

Recommended operating conditions

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage		AVDD, DVDD	2.6	2.8	3.0	V
Oscillator frequency		fOSCIN	8	9	20	MHz
Digital “H” input voltage	OSCIN, XRESET, PDWN, XSLV, MSEL0, MSEL1, MSEL2, VRESET	VIHD	DVDD-0.5	DVDD		V
Digital “L” input voltage		VILD		0	0.5	V
Digital "H" input voltage	SDA, SCL	VIHI2C	0.7DVDD			
Digital "L" input voltage		VILI2C			0.3DVDD	
Digital input current		IID	-20		5	µA
Operating temperature		Ta	-25		65	°C
SCL input frequency		Fscl			400	KHz

DC electrical characteristics

(AVDD=2.8V, DVDD=2.8V, Ta=25°C)

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Analog power supply current		IAVDD		7		mA
Digital power supply current		IDVDD		3.5		mA
Digital “H” output voltage (Ioh=800µA)	PCLK, HD, VD, D0-D7, OSCO	VOHD	DVDD-0.4			V
Digital “L” output voltage (Iol=1mA)		VOLD			0.4	V
Digital "L" output voltage (Iol=3mA)	SDA, SCL	VOLI2C			0.4	V
Digital input current		IID	-20		5	µA
Standby current		Istb		8		µA

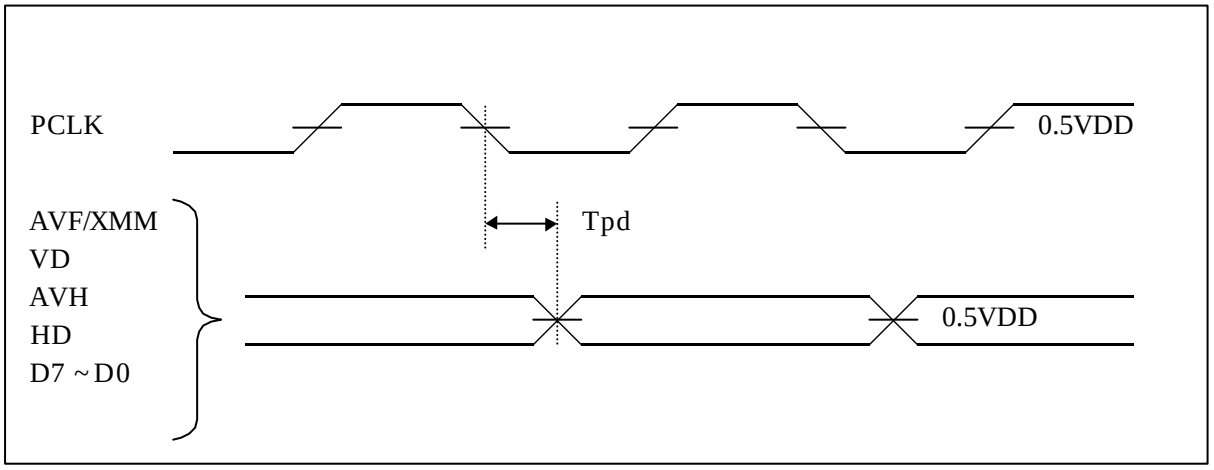
AC electrical characteristics

(AVDD=2.8V, DVDD=2.8V, Ta=25°C)

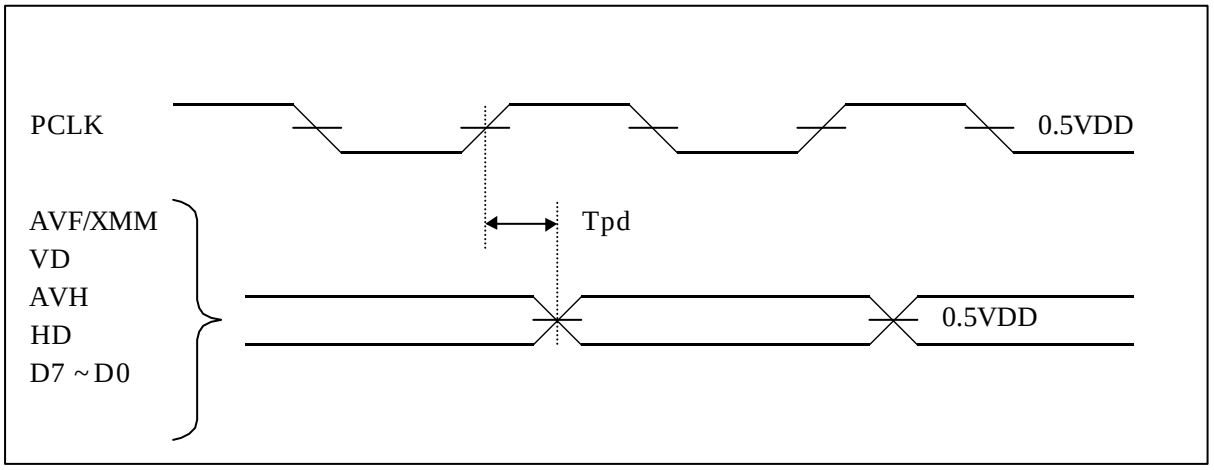
Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Output clock frequency	IDR bit01 = 0	fPCLK		fOSCIN/2		Hz
	IDR bit01 = 1			fOSCIN/4		Hz
PCLK to digital output delay	AVF/XMM, VD, AVH, HD, D7-D0	Tpd		2		ns

Timing diagram

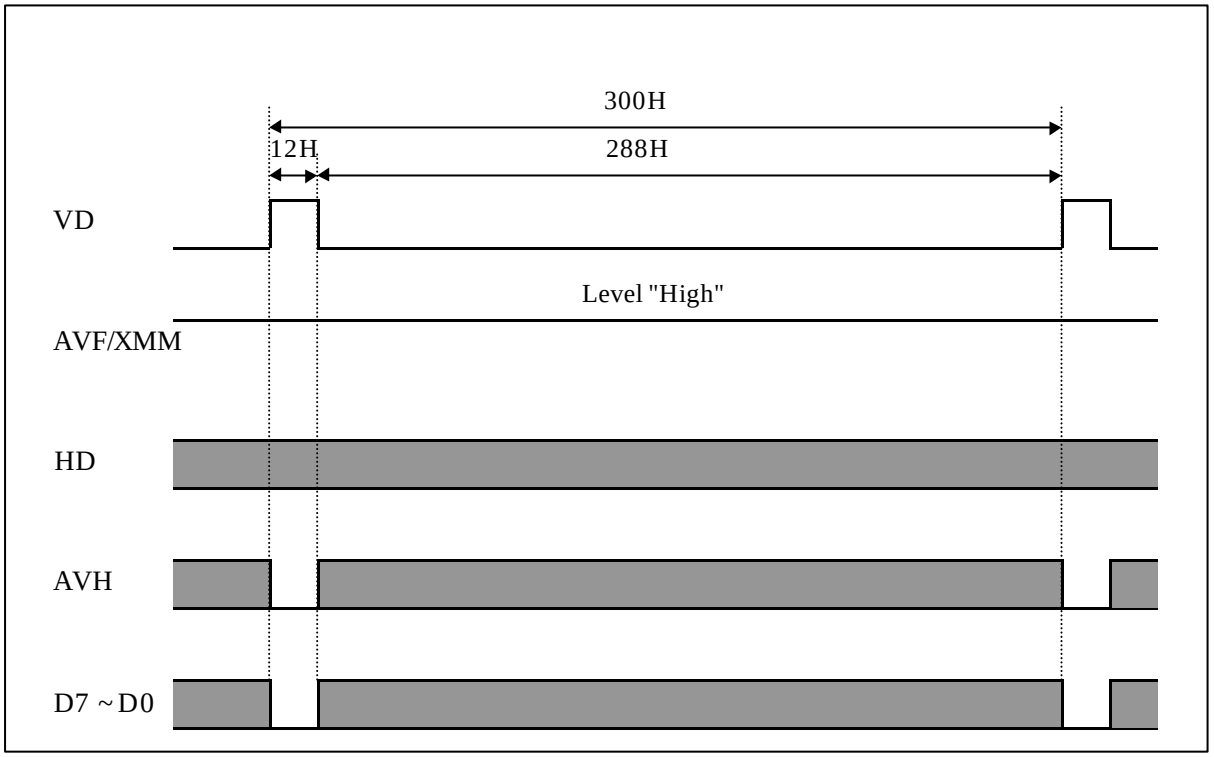
1. Digital outputs (POLR bit03 = 0)



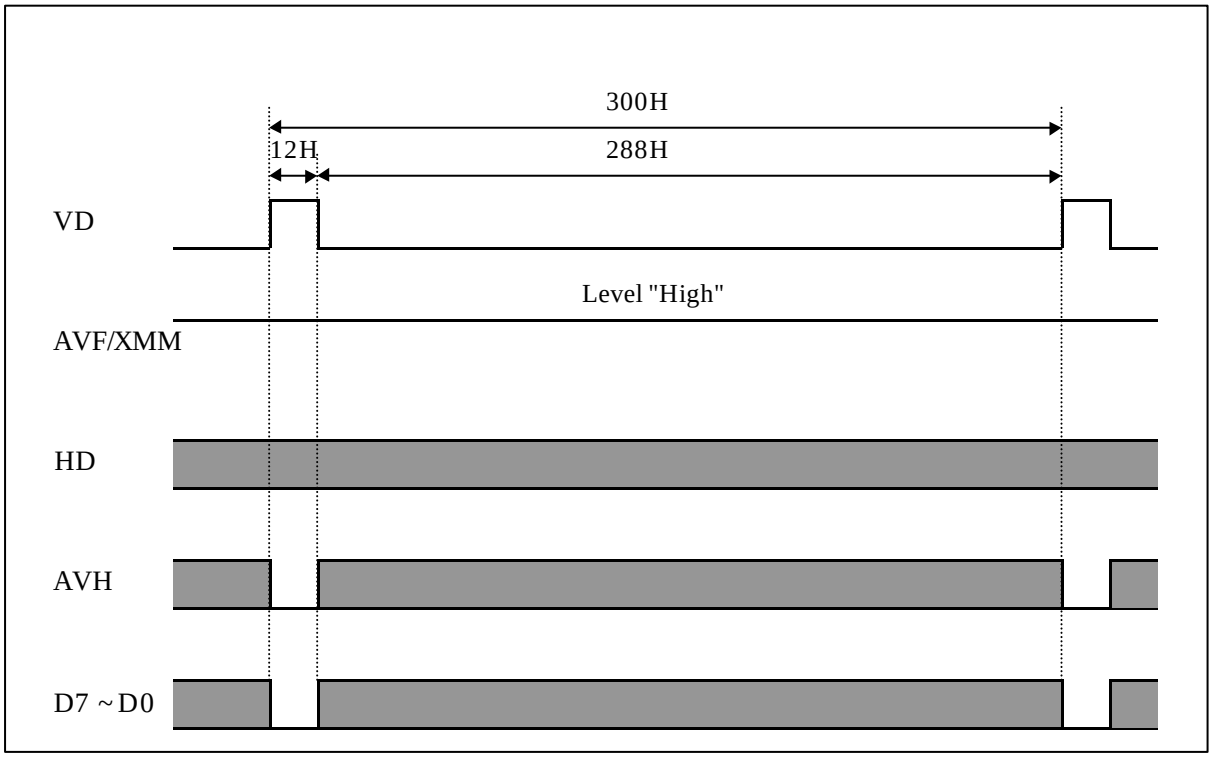
2. Digital outputs (POLR bit03=1)



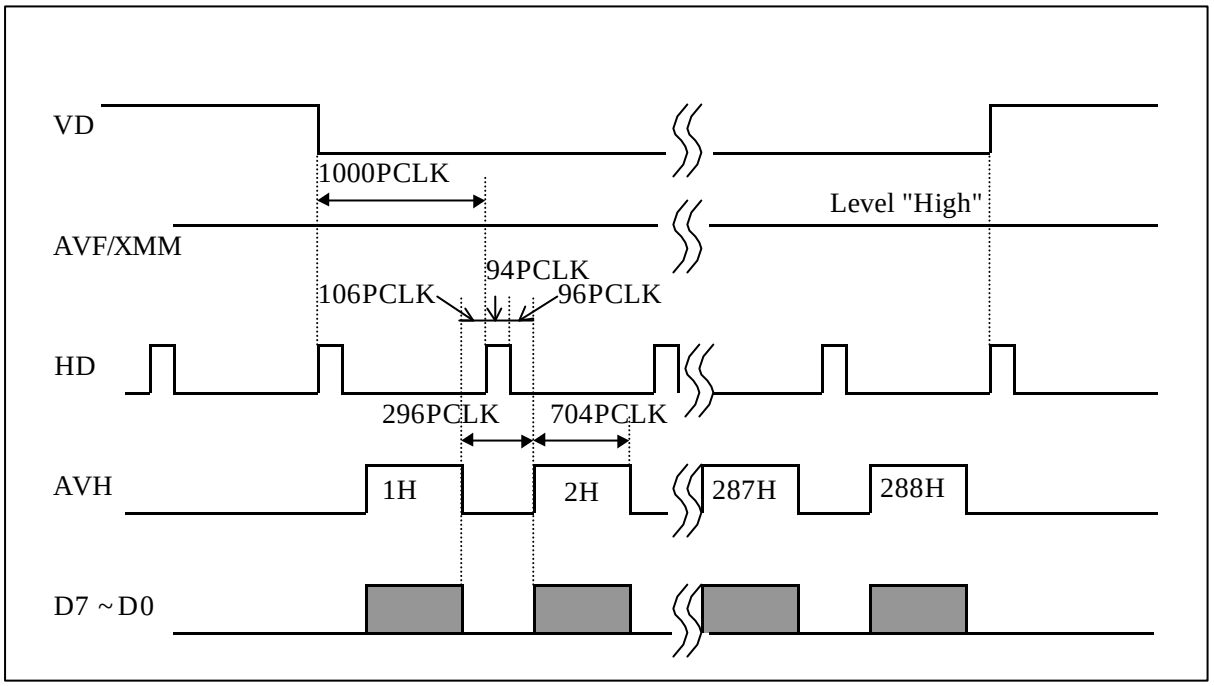
3. Vertical timing (default)



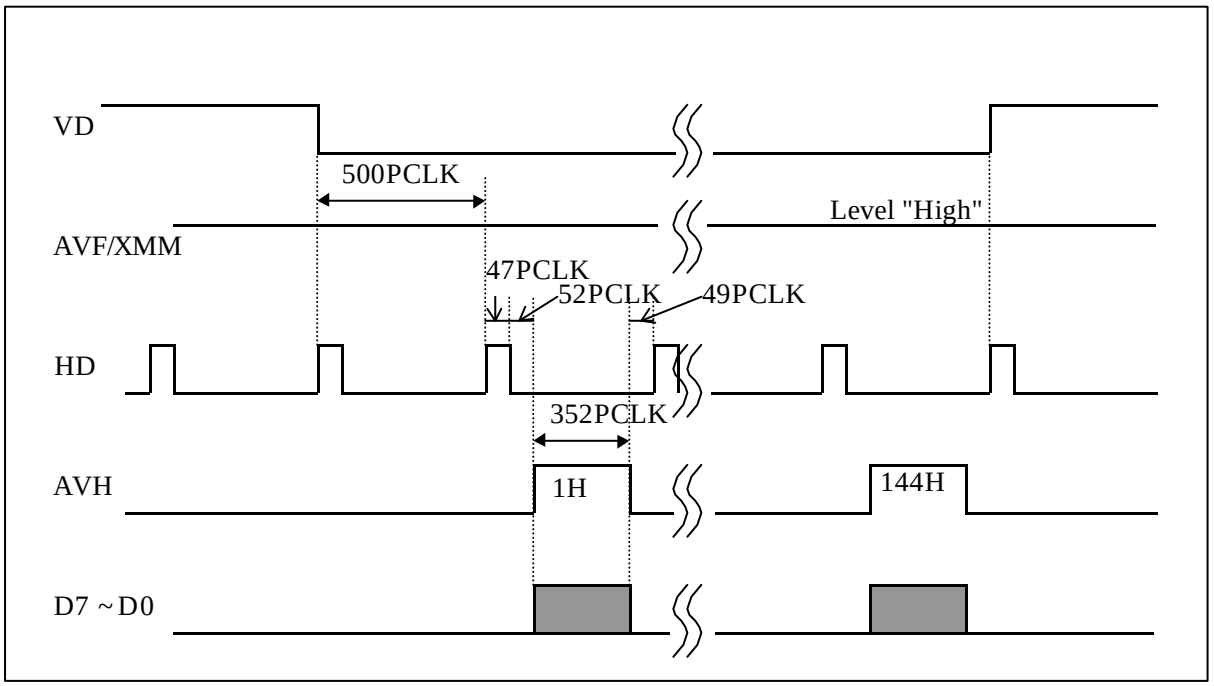
4. Vertical timing (QCIF default, MD1 bit02= 1)



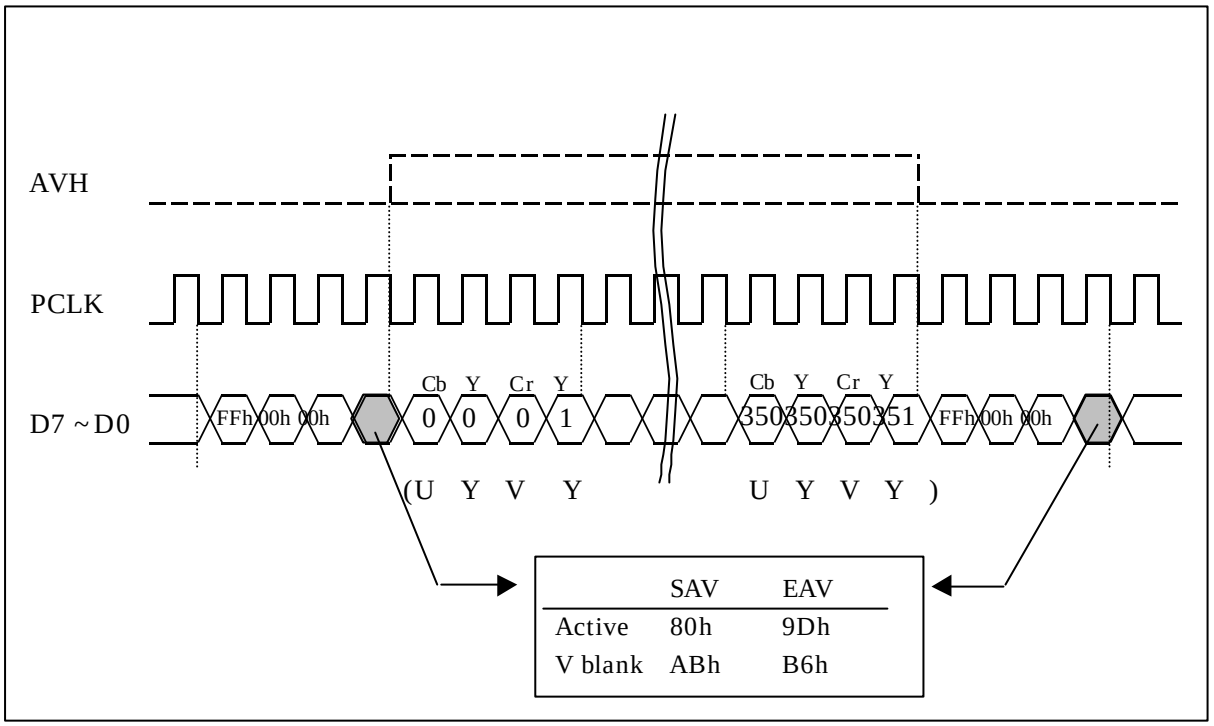
5. Horizontal timing (default)



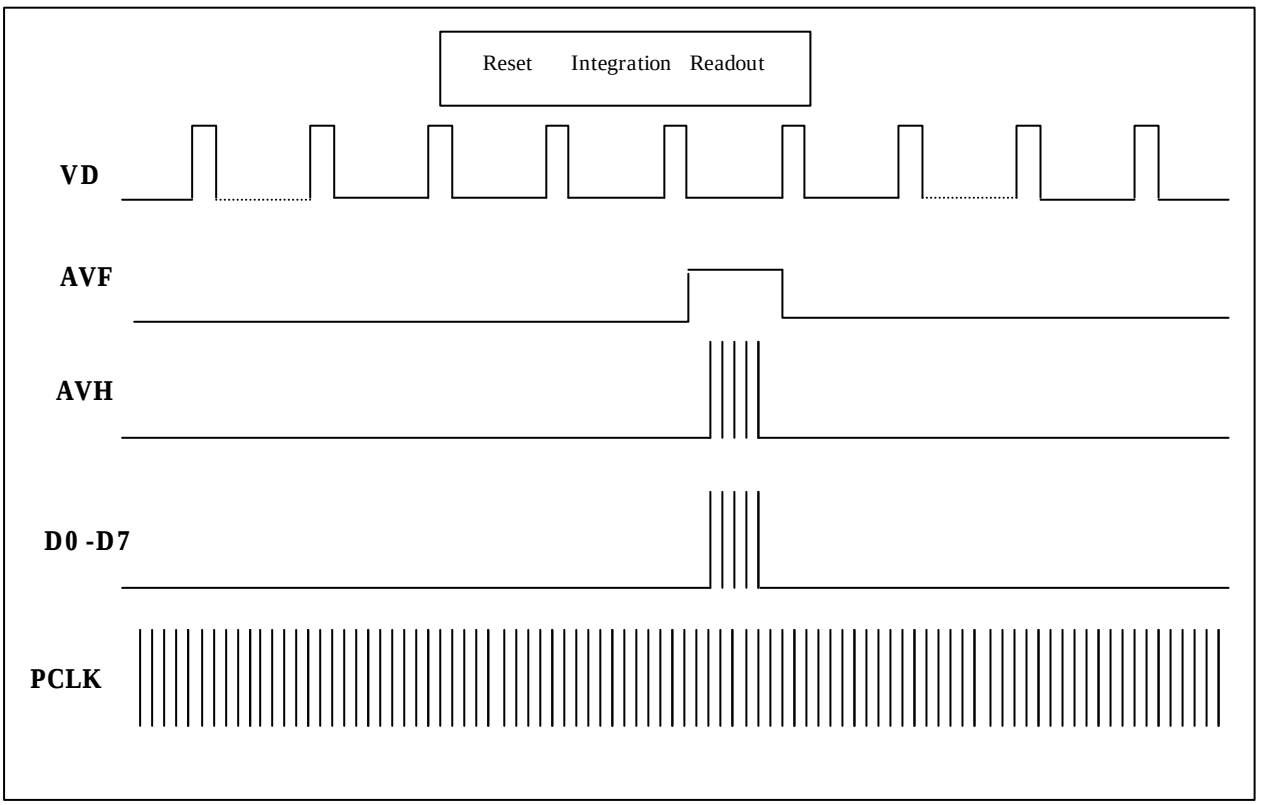
6. Horizontal timing (QCIF default, MD1 bit02=1)



7. Video data output timing (default)

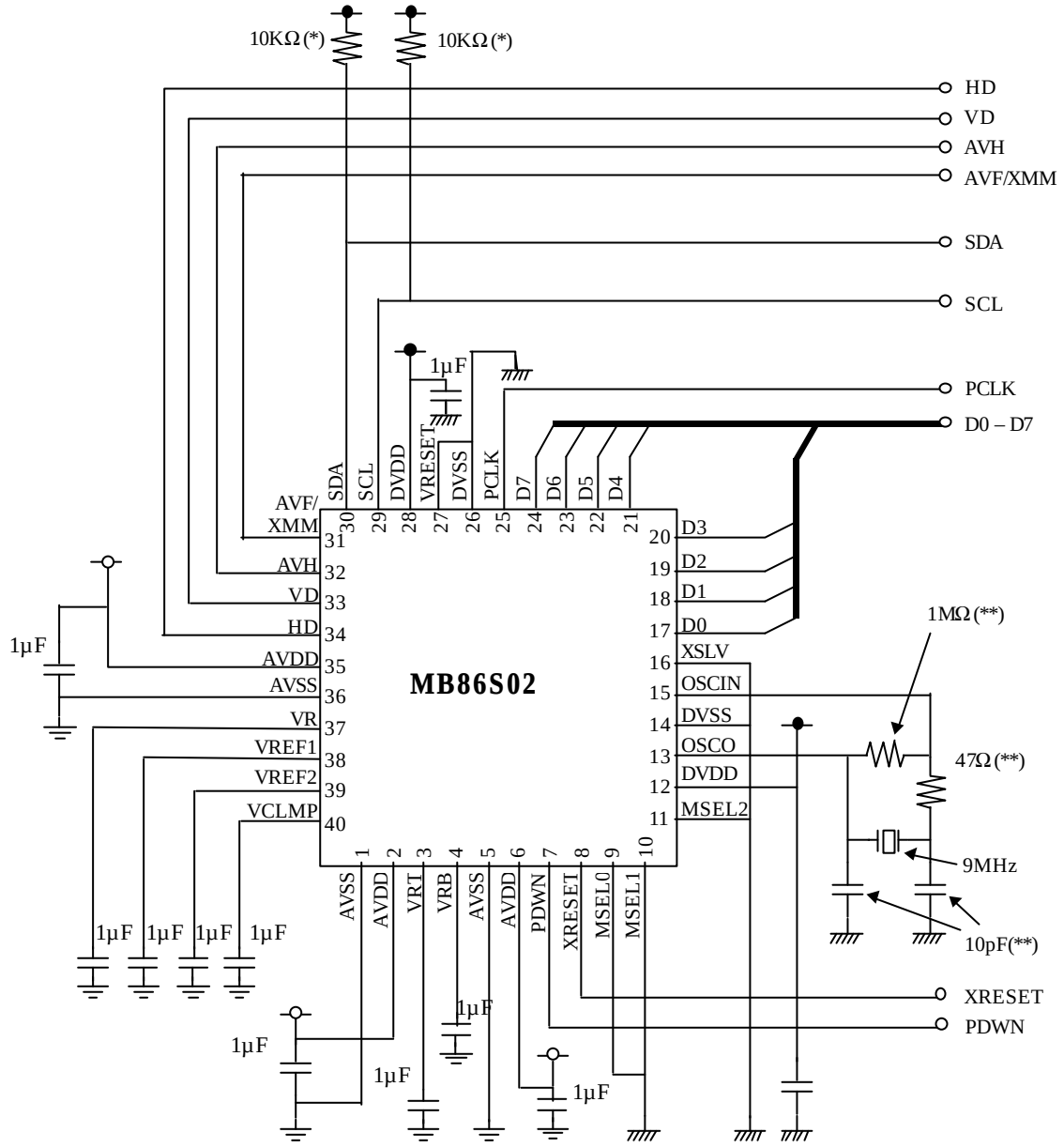


8. Power save mode

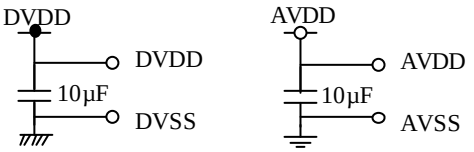


Application Diagram

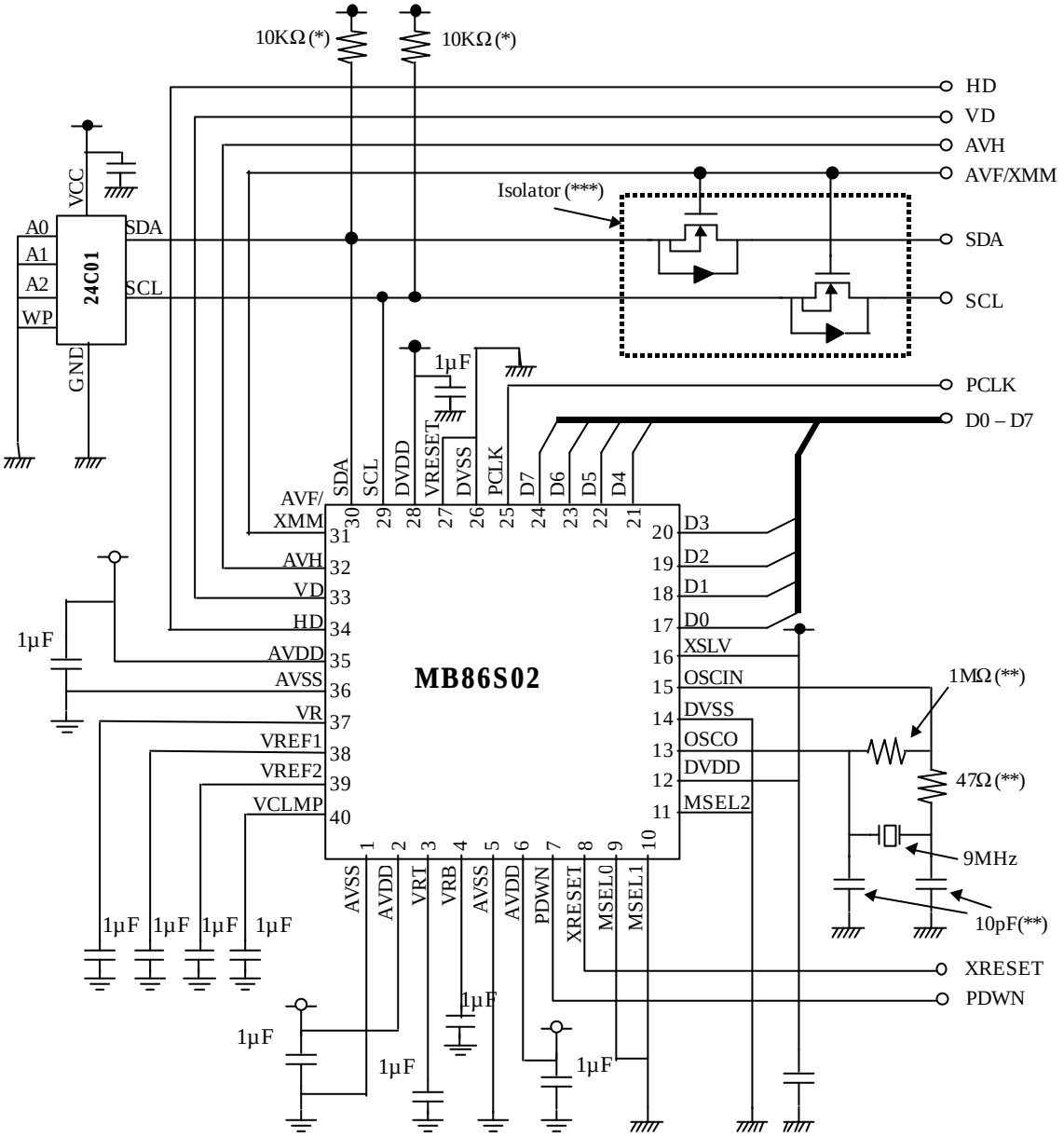
Slave mode (XSLV=L)



(*) The value of pull-up resistors depend on the following parameters:
Supply voltage, bus capacitance, number of connected devices and maximum I2C frequency.
(**) The value of resistors and capacitors must be optimized for stable oscillation.



Auto load mode (XSLV=H)



(*) The value of pull-up resistors depend on the following parameters: Supply voltage, bus capacitance, number of connected devices and maximum I2C frequency.

(**) The value of resistors and capacitors must be optimized for stable oscillation.

(***) If it is necessary to isolate the bus from the other part of system when MB86S02 operate in master mode, XMM signal can control MOS-FET isolators. The requirements of MOS FET characteristics depend on the supply voltage and bus speed.

Register Definitions

Register Map

Address	Name	Bit	Type	Default	Description
00	VER	07-00	R		Hardware version information
01	IDR	07	R		EEPROM data loading status 0: Read fail, 1:Read completed
		06-03	R/W		Reserved
		02	R/W		Reserved
		01	R/W	0	Clock divider 0: divided by 2, 1: divided by 4
		00	W	0	Internal counter reset 1: Counter reset
02	MD1	07	R/W	0	CCIR656 headers 0: with SAV/EAV, 1: no headers
		06	R/W	0	Gamma adjustment 0: apply the gamma, 1: no adjustment
		05	R/W	0	Aperture correction 0: apply aperture correction, 1: no correction
		04	R/W	0	Mosaic into GBR 0: Color, 1: G=B=R
		03	R/W	1	Median filter 0: apply median filter, 1: no filter
		02	R/W	0	QCIF mode 0: CIF, 1:QCIF
		01	R/W	0	Vertical scan direction 0: Normal, 1: Up side down
		00	R/W	0	Horizontal scan direction 0: Normal, 1: Mirror
03	MD2	07-06	R/W	00	Auto gain control mode select 00: Auto, 10: Number of line is fixed, 11: Manual
		05-04	R/W	00	White balance coefficient 00: Auto, 01, 10, 11: Fixed coefficients
		03	R/W	0	Auto white balance 0: On, 1:Off
		02	R/W	0	Binary code of YUV and YCbCr 0: Offset binary, 1: Straight binary
		01	R/W	0	Video output mode 0: UV or CbCr leading, 1: Y leading
		00	R/W	0	Video output format 0: YCbCr, 1: YUV

Address	Name	Bit	Type	Default	Description
04	POL	07	R/W	0	Polarity of AVF 0: Active high, 1: Active low
		06	R/W	0	Polarity of AVH 0: Active high, 1: Active low
		05	R/W	0	Polarity of HD 0: Active high, 1: Active low
		04	R/W	0	Polarity of VD 0: Active high, 1: Active low
		03	R/W	0	Polarity of PCLK 0: Normal, 1: Inverse
		02	R/W	0	Polarity of DATA0-7 0: Normal, 1: Inverse
		01	R/W	0	Reserved
		00	R/W	0	Output disable 0: Enable, 1: High impedance
05	RSV05	07-00	R/W		Reserved
06	T_HSTT	07-00	R/W	14(d)	Horizontal start position of output data (in unit of 2*PCLK)
07	T_HWID	07-00	R/W	176(d)	Output valid pixels per line (in unit of 2*PCLK)
08	T_VSTT	07-00	R/W	8(d)	Vertical start position of output data (line)
09	T_VWID	07-00	R/W	160(d)	Output valid lines per frame (Set the valid line – 128)
0A	L_I1G	07-00	R/W	16(d)	Black level adjustment (Green)
0B	L_I1B	07-00	R/W	16(d)	Black level adjustment (Blue)
0C	L_I1R	07-00	R/W	16(d)	Black level adjustment (Red)
0D	L_G1G	07-00	R/W	9(d)	Gain adjustment of low signal level (Green)
0E	L_G1B	07-00	R/W	98(d)	Gain adjustment of low signal level (Blue)
0F	L_G1R	07-00	R/W	49(d)	Gain adjustment of low signal level (Red)
10	L_I2G	07-00	R/W	128(d)	Threshold level of high signal level (Green)
11	L_I2B	07-00	R/W	128(d)	Threshold level of high signal level (Blue)
12	L_I2R	07-00	R/W	128(d)	Threshold level of high signal level (Red)
13	L_G2G	07-00	R/W	9(d)	Gain adjustment of high signal level (Green)
14	L_G2B	07-00	R/W	98(d)	Gain adjustment of high signal level (Blue)
15	L_G2R	07-00	R/W	49(d)	Gain adjustment of high signal level (Red)

Address	Name	Bit	Type	Default	Description
16	C_GG	07-00	R/W	19(d)	Matrix elements of color correction GO=GI+(GI*C_GG)+(BI*C_GB)+(RI*C_GR) BO=BI+(GI*C_BG)+(BI*C_BB)+(RI*C_BR) RO=RI+(GI*C_RG)+(RI*C_RB)+(RI*C_RR) GI, BI, RI, GO, BO, RO are input and output RGB signals
17	C_GB	07-00	R/W	-7(d)	
18	C_GR	07-00	R/W	-12(d)	
19	C_BG	07-00	R/W	-35(d)	
1A	C_BB	07-00	R/W	36(d)	
1B	C_BR	07-00	R/W	-1(d)	
1C	C_RG	07-00	R/W	-11(d)	
1D	C_RB	07-00	R/W	5(d)	
1E	C_RR	07-00	R/W	6(d)	
1F	RSV1F	07-00	R/W		Reserved
20	A_KG	07-00	R/W	32(d)	Gain of aperture sharpness (Green)
21	A_KB	07-00	R/W	32(d)	Gain of aperture sharpness (Blue)
22	A_KR	07-00	R/W	32(d)	Gain of aperture sharpness (Red)
23	G_I2	07-00	R/W	4(d)	Gamma curve adjustment (low level of medium range)
24	G_I3	07-00	R/W	150(d)	Gamma curve adjustment (high level of medium range) 0 < = I2 < = I3 < 256
25	G_G1	07-00	R/W	16(d)	Gamma curve adjustment (gain of low level)
26	G_C2	00	R/W	0(d)	Gamma coefficient (select 0.45 or 1) 0: 0.45, 1: 1
27	G_G2	07-00	R/W		Gain of medium level (gamma curve)
28	G_G3	07-00	R/W		Gamma curve adjustment (gain of high level)
29	G_OFF2	07-00	R/W		Gamma curve adjustment (offset of medium level)
2A	Y_GU	07-00	R/W	126(d)	Gain of chrominance (U)
2B	Y_GV	07-00	R/W	225(d)	Gain of chrominance (V)
2C	Y_LIM_YL	07-00	R/W	0(d)	Lower limit of Y
2D	Y_LIM_YH	07-00	R/W	255(d)	Upper limit of Y
2E	Y_LIM_UL	07-00	R/W	0(d)	Lower limit of U
2F	Y_LIM_UH	07-00	R/W	255(d)	Upper limit of U
30	Y_LIM_VL	07-00	R/W	0(d)	Lower limit of V
31	Y_LIM_VH	07-00	R/W	255(d)	Upper limit of V
32	A_HSTT	07-00	R/W	29(d)	Horizontal start position of the AGC window Set the number of clock / 2
33	A_VSTT	07-00	R/W	27(d)	Vertical start position of the AGC window Set the number of line / 2
34	A_WID	07-04	R/W	1011	Vertical width of the AGC window 0110: 32 lines, 1010: 128 lines, 1011: 192 lines, 1100: 256 lines
		03-00	R/W	1100	Horizontal width of the AGC window 0110: 32 pixels, 1010: 128 pixels, 1011: 192 pixels, 1100: 256 pixels
35	A_INTVL	07-00	R/W	0(d)	AGC frame interval
36	A_DEAD	05-00	R/W	20(d)	Dead band width of the AGC feed-back loop
37	A_GAIN	07-00	R/W	32(d)	Gain of AGC feed-back loop

Address	Name	Bit	Type	Default	Description
38	A_LINEU	07-00	R/W	149(d)	Upper limit of the number of integration lines Set the number of line / 2
39	A_LINEB	07-00	R/W	1(d)	Lower limit of the number of integration lines Set the number of line / 2
3A	A_INTG	05-00	R/W	12(d)	Initial gain of video amplifier (dB) 24(d) max.
3B	A_MAXG	05-00	R/W	21(d)	Gain limit of video amplifier (dB) 24(d) max.
3C	A_LEVEL	07-00	R/W	120(d)	AGC target of averaged Y level
3D	A_AVRG	07-00	R		Average of Y level
3E	AI_INTGL	07-00	R		Number of integration line
3F	AI_INTGH	07-01	R/W		Not used.
		00	R		Number of integration line (MSB)
40	AI_AGAIN	07-06	R/W		Not used
		05-00	R		Gain of video amplifier
41	FMD	07	R		Flicker sensing status
		06	R	0	Flicker detected result 0: 60 Hz, 1: 50 Hz
		05-02	R/W		Reserved
		01	W		Restart flicker detection 1: Restart
		00	R/W	0	Auto flicker detection 0: On, 1: Off
42	FTHR	07-04	R/W	2(d)	Counter setting of flicker detection
		03-00	R/W	5(d)	Threshold of flicker detection
43	FACT	07-04	R/W	8(d)	Delay for starting auto flicker detection
		03-00	R/W	10(d)	Maximum frame number of AFD
44	W_HSTT	07-00	R/W	29(d)	Horizontal start position of the AWB window Set the number of clock / 2
45	W_VSTT	07-00	R/W	27(d)	Vertical start position of the AWB window Set the number of line / 2
46	W_WID	07-04	R/W	1011	Vertical width of the AWB window 0110: 32 lines, 1010: 128 lines, 1011: 192 lines, 1100: 256 lines
		03-00	R/W	1100	Horizontal width of the AWB window 0110: 32 lines, 1010: 128 lines, 1011: 192 lines, 1100: 256 lines
47	W_INTVL	07-00	R/W	0	AWB frame interval
48	W_LIMB	07-00	R/W	25(d)	Limit of blue signal of white area
49	W_LIMR	07-00	R/W	25(d)	Limit of red signal of white area
4A	W_DEADB	07-00	R/W	2(d)	Dead band width of AWB feed-back (Blue)
4B	W_DEADR	07-00	R/W	2(d)	Dead band width of AWB feed-back (Red)
4C	W_GAIN	07-00	R/W	16(d)	Gain of AWB feed-back loop
4D	W_GB0	07-00	R/W	0(d)	Initial gain of AWB (Blue)
4E	W_GR0	07-00	R/W	0(d)	Initial gain for AWB (Red)
4F	W_GB1	07-00	R/W	-32(d)	Fixed gain set No. 1 (Blue)

Address	Name	Bit	Type	Default	Description
50	W_GR1	07-00	R/W	26(d)	Fixed gain set No. 1 (Red)
51	W_GB2	07-00	R/W	-16(d)	Fixed gain set No. 2 (Blue)
52	W_GR2	07-00	R/W	6(d)	Fixed gain set No. 2 (Red)
53	W_GB3	07-00	R/W	27(d)	Fixed gain set No. 3 (Blue)
54	W_GR3	07-00	R/W	-54(d)	Fixed gain set No. 3 (Red)
55	W_AVGB	07-00	R		Average of B - Y
56	W_AVGR	07-00	R		Average of R - Y
57	RSV57	07-00	R/W		Reserved
58	HTC	07-00	R/W	0(d)	Horizontal total count 0: 500 pixels, 255(d): 1010 pixels
59	HSYS	07-00	R/W	50(d)	Start position of HD 0: 0 pixel, 50: 50 pixels
5A	HSYE	07-00	R/W	46(d)	End position of HD from the rising edge of AVH 0: 0 pixel, 46: 46 pixels
5B	RSV5B	07-00			Not used
5C	VSYS	07-06			Not used
		05-03	R/W	1(d)	Start position of VD
		02-00	R/W	0(d)	End position of VD
5D	VSYHADJ	07-06	R/W	00	VD edge alignment 00: Align both rising and falling edge to the rising edge of HD 01: Align rising edge to the falling edge of AVH, and falling edge to the rising of AVH 10: Align rising edge to the rising edge of AVH, and falling edge to the falling of AVH 11: Align rising edge to the falling edge of AVH, and falling edge to the falling of AVH
		05-03	R/W	101	VD rising edge timing adjustment 000: 5 clocks, 101: just, 111: -2 clocks (1 clock= PCLK/2)
		02-00	R/W	101	VD falling edge timing adjustment 000: 5 clocks, 101: just, 111: -2 clocks (1 clock= PCLK/2)
5E	AV_HS	07			Not used
		06-00	R/W	1(d)	Horizontal start position of AVH in pixels
5F	AV_HE	07			Not used
		06-00	R/W	1(d)	Horizontal end position of AVH in pixels

Address	Name	Bit	Type	Default	Description
60	AV_VS	07			Not used
		06-00	R/W	0(d)	Vertical start line of AVH
61	AV_VE	07			Not used
		06-00	R/W		Vertical end line of AVH
62	PWRSV	07			Not used
		06	R/W	0	Power save mode control 0: Continuous operation, 1: Power saving
		05	R/W	0	Accumulation mode (please fix to 0) 0: 1 frame, 1: Reserved
		04-00	R/W	2(d)	Interval on power save mode 2-31 frames
63	BKLVL	07-00	R/W	16(d)	Black clamp level
64	BKCLP	07	R/W	0	Black clamp on/off 0: on 1: off (please fix to 0)
		06	R/W	1	Black clamp mode 0: clamping on every lines, 1: clamping on every frames
		05-03	R/W	1(d)	Start pixel of black clamp
		02-00	R/W	4(d)	End pixel of black clamp
65	ANLG1	07-00	R/W	0(d)	Reserved for timing adjustment (Please use the default)
66	ANLG2	07-00	R/W	0(d)	CDS timing adjustment (Please use the default)
67	ANLG3	07-06			Not used
		05	R/W	0	Reserved (Please use default setting)
		04	R/W	0	Reserved (Please use default setting)
		03	R/W	1	Reserved (Please use default setting)
		02	R/W	0	Reserved (Please use default setting)
		01-00	R/W	00	Reserved (Please use default setting)
68	TEST	07-00	R/W	0(d)	Test mode for image sensor
69	Reserved	07-00	R/W	0(d)	Reserved
6A	Reserved	07-00	R/W	0(d)	Reserved
6B	RSV6B	07-00	R/W	0(d)	Reserved
6C	C_TEST1	07-00	R/W	0(d)	Test mode for DSP
6D	C_TEST2	07-00	R/W	0(d)	Test mode for DSP
6E	C_TEST3	07-00	R/W	0(d)	Test mode for DSP
6F	C_TEST4	07-00	R/W	0(d)	Test mode for DSP

Functional Description

Auto loading from the EEPROM

When the XSLV is connected to DVDD at the reset, the auto loading from the EEPROM can set all register values except the read only bits and IDR. For the successful loading the first byte data of EEPROM must be equal to the value of VER register. The bit 7 of IDR register will set to 1 when the loading is completed. The XMM pin keeps the level low during the MB86S02 is in master mode.
MB86S02 will turn to the slave mode if following conditions are occurred.

1. XSLV is connected to GND at the reset.
2. The first byte data of EEPROM dose not correspond to the VER.
3. The bus collision of SDA line will occur.
4. Not detect the data acknowledgement.

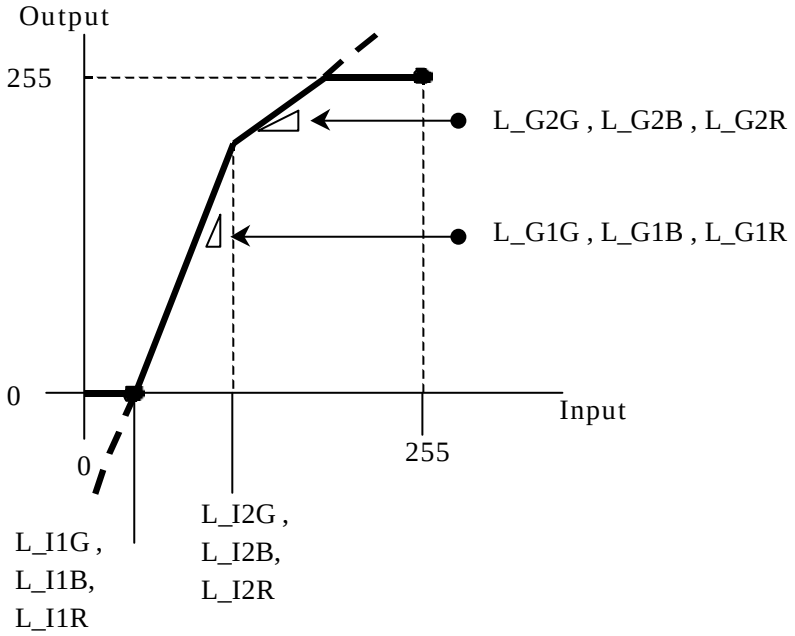
Median filter

The digital output signals from the AD converter can be performed with the three taps of median filter for the same color pixels of horizontal direction. Setting the bit 3 of MD1 register activates the median filter.

Offset and gain adjustment

The offset and gain of each color can be adjusted independently for GBR signals. The adjustment curve is shown in below.

Input-output relation
(For each G/B/R)



Color adjustment

The output color space is widely adjustable. The color is calculated by following equations.

$$G_o = (1+Cgg)*G_i + Cgb*B_i + Cgr*R_i$$
$$B_o = Cbg*G_i + (1+Cbb)*B_i + Cbr*R_i$$
$$R_o = Crg*G_i + Crb*B_i + (1+Crr)*R_i$$

, where G_i, B_i, R_i are gain-offset corrected signals and G_o, B_o, R_o are output.

The matrix coefficients Cgg, Cgb, …, Crr are defined by the register values of C_GG, C_GB, …, C_RR by the relationship of Cxx=C_XX/64.

Aperture correction

The aperture response of GBR signals is corrected by the following equations.

$$G_a = G_o - P_e * Gain\_G$$
$$B_a = B_o - P_e * Gain\_B$$
$$R_a = R_o - P_e * Gain\_R$$

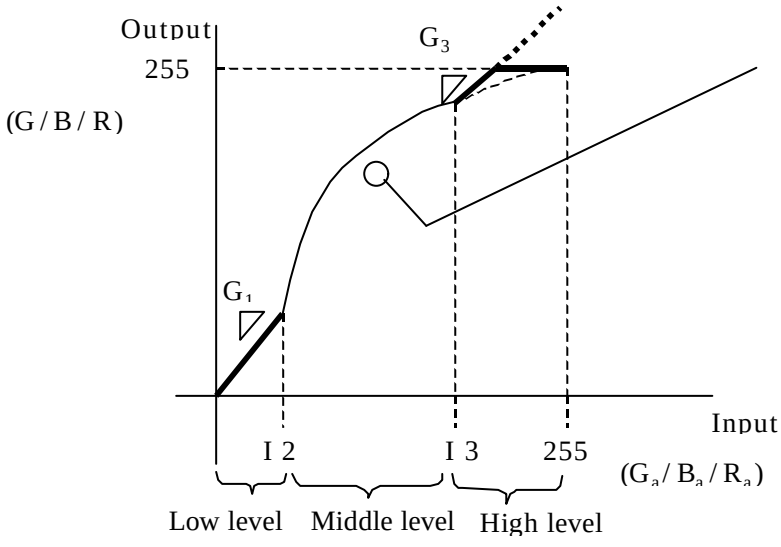
, where Gain_G, Gain_B, Gain_R are defined by the register values of A_KG, A_KB, AKR by the relationship of Gain_X=A_KX/64.

The edge component, P_e, for the (i, j) pixel is obtained from the G_o signal by calculating the following expression.

$$P_e(i,j) = \frac{1}{4}[G_o(i,j+1) + G_o(i,j-1) + G_o(i-1,j) + G_o(i+1,j)] - G_o(i,j)$$

Gamma correction

The gamma correction is applied to the three part of input signal. The middle level part uses a gamma curve. The low and high-level region uses the straight line. The correction curve is shown in below.



The middle level curve is defined by the following equations.

$$Output = f(x) * gain2 - off2$$

$$f(x) = \left(\frac{x}{255}\right)^g * 255$$

, where

$$gain2 = 1 + \frac{G\_G2}{128}$$
$$off2 = G\_OFF2$$

RGB to YCbCr or YUV encoding

The RGB signals are encoded to the YCbCr or YUV using the following transformations.

YCbCr:

$$Y = 16 + \frac{1}{512}(131 * R + 257 * G + 50 * B)$$

$$Cb = 128 + \frac{1}{512}(-153 * R - 301 * G + 454 * B) * \frac{127}{256}$$

$$Cr = 128 + \frac{1}{512}(359 * R - 301 * G - 58 * B) * \frac{160}{256}$$

YUV:

$$Y = \frac{1}{512}(153 * R + 301 * G + 58 * B)$$

$$U = \frac{1}{512}(-153 * R - 301 * G + 454 * B) * \frac{G_U}{256}$$

$$V = \frac{1}{512}(359 * R - 301 * G - 58 * B) * \frac{G_V}{256}$$

The range of RGB signals is 0 to 255. G_U and G_V are defined by the register Y_GU and Y_GV, respectively.

White balance control

White balance control is performed using the mean value of the chrominance in the active window pixels. The width, height, start position of the window are defined by the registers of W_WID, W_HSTT and W_VSTT respectively. The calculated average value of chrominance is set into W_AVGB and W_AVGR registers.

The stability of automatic white balance control is adjustable by two functions.

1. The register W_INTVL defines the interval of feed back loop in the unit of frame. The feed back control is performed for every frame when this register is set to 0 otherwise the appropriate interval time defined by the register value.
2. The registers W_DEADB and W_DEADR define the width of dead band for Y-B and Y-R values. The feedback only performed when the change of chrominance exceeds these values, so that the intensity based stability will keep desired level.

The registers W_GB1, W_GR1, W_GB2, W_GR2, W_GB3 and W_GB3 set the default white balance coefficients. The defaults are selected by bit 05-04 of the register MD2.

Automatic gain control

The automatic gain control is activate when the bit 07-06 of register MD2 are set to 00 (default) or 10. The difference of two modes is the control behavior for the bright condition. Mode 00 can decrease the exposure time for the very bright condition but mode 01 fixes the exposure time. For the dark condition the register A_MAXG can limit the maximum gain.

The mean value of the Y level is calculated for the pixels in the window in an image. The registers A_WID, A_HSTT and A_VSTT define the width, height and position of the window. The calculated result is set into the register A_AVRG.

The stability of automatic gain control is adjustable by two functions.

1. The register A_INTVL defines the interval of feed back loop in the unit of frame. The feed back control is performed for every frame when this register is set to 0 otherwise the appropriate interval time defined by the register value.
2. The register A_DEAD defines the width of dead band for Y level. The feedback only performed when the change of illumination exceeds these values, so that the intensity based stability will keep desired level.

Flicker detection

Resetting the IC or setting the bit 01 of the register FMD triggers the flicker detection. The MB86S02 try to detect the flicker fluctuation on an image and judge the frequency of light illumination if possible. The result is set into the bit 06 of FMD register when the detection success. Then the exposure time is adapted to minimize the flicker fluctuation. The bit 07 of FMD register is set during the flicker detection. If the brightness is not enough for the detection or the flicker fluctuation dose not exceeds the detection threshold, the detected result will be set to the default (60 Hz). The flicker detection is effective only for the frame rate of 15 and 30 f/s. The bit 00 of FMD register can enable and disable the flicker detection.

Power save mode

MB86S02 run into the power save mode when the bit 06 of PWRSV register is set. The power save mode is the intermittent exposure of the image sensor. The most of power supply is cut off except for the time of exposing. Using this mode reduces the average power consumption if the continuous data stream is not necessary. The bit 04-00 of PWRSV register sets the interval of exposure on the unit of frame. The table in below shows an example of the reduction on power save mode.

(FOSCIN=9MHz)

Frame interval (frame)	Bit 04-00 of the PWRSV	Relative power consumption (%)
Continuous	---	100
3	2	70
5	4	60
10	9	53

The output data is flashed intermittently except for the timing signals such as HD, VD and PCLK. The timing schematic is shown in the section 8th of timing diagram part.

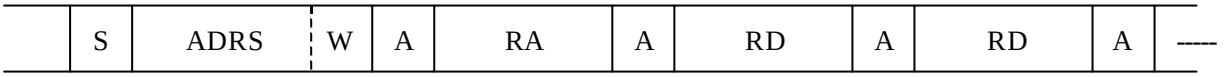
Read and write sequence on the slave mode

The figures in below illustrate the read and write sequence through I2C interface on the slave mode. In each figure the symbols represent the following status.

S: Start condition, P: Stop condition, ADRS: Slave address except read and write bit,
A: Data acknowledgement, RA: Register address, RD: Register data,
R: Read bit ("1"), W: Write bit ("0").

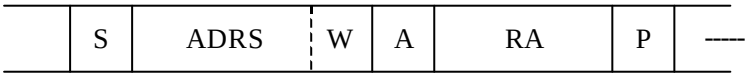
1. Write sequence

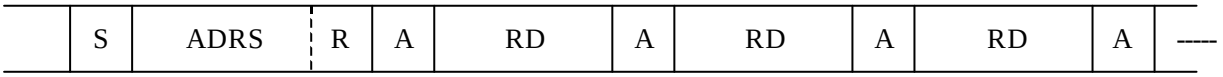
Following the start condition write the slave address with the write bit and register address. The registers data are sent after this sequence. The register address is automatically incremented.



2. Read sequence

First, following the start condition write the slave address with the write bit, register address and the stop condition. Then following the start condition write the slave address with read bit. After the acknowledgement, it can read the data sequentially. The register address is automatically incremented by this sequence.





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