Dual, High Voltage, Isolated MOSFET Driver

Features

- ±400V input to output isolation
- ±700V isolation between outputs
- No external voltage supply required
- Dual isolated output drivers
- Option of internal or external clock

Applications

- Telecommunications
- Modems
- Solid state relays
- High side switches
- High end audio switches
- Avionics
- ATE

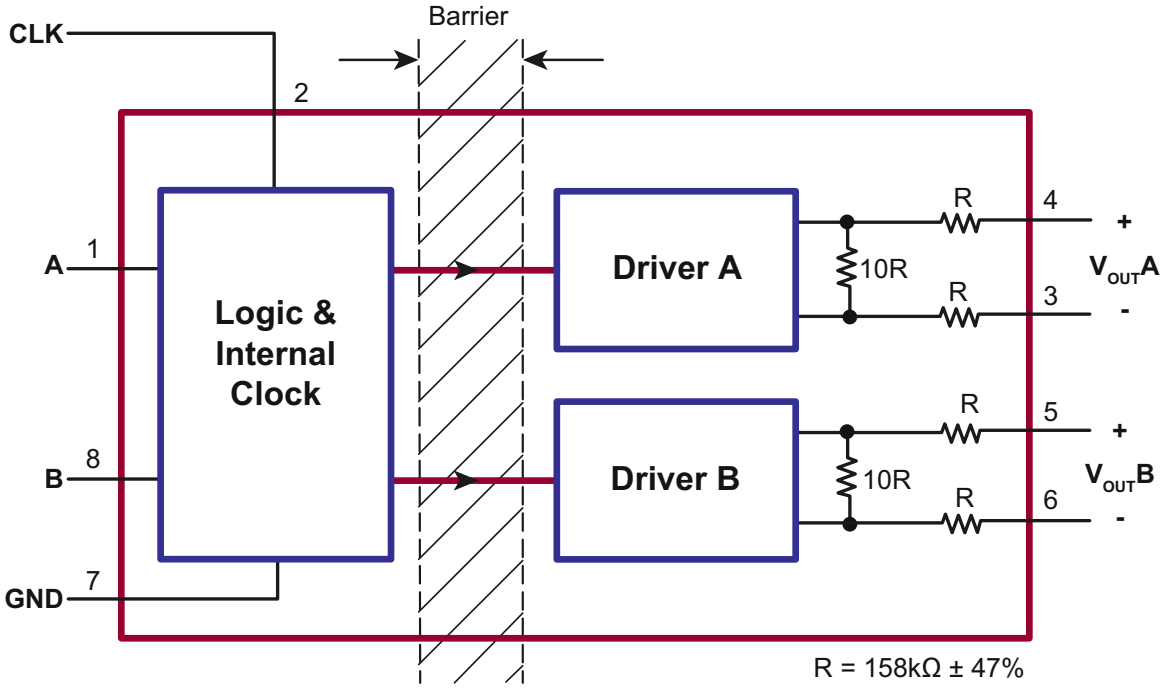
General Description

The Supertex HT0440 is a dual, high voltage, isolated MOSFET driver utilizing Supertex's proprietary HVCMOS® technology. It is designed to drive discrete MOSFETs configured as bidirectional or unidirectional switches. It can drive N-channel MOSFETs as high-side switches up to 400V. The HT0440 generates two independent DC isolated voltages to the outputs, $V_{OUT}A$ and $V_{OUT}B$ when logic inputs A and B are at logic high.

The internal clock of the HT0440 can be disabled by applying an external clock signal to the CLK pin. This allows the power dissipation and AC characteristics to be tailored to meet specific needs. The CLK pin should be connected to ground when not in use. The HT0440 does not require any external power supplies, the internal supply voltage is supplied by either of the two logic inputs, A or B, when they are at logic high.

For detailed circuit application information, please refer to application note AN-D26.

Block Diagram



Ordering Information

Part Number	Package Options	Packing
HT0440K6-G	10-Lead (3x4) DFN	3000/Reel
HT0440LG-G	8-Lead SOIC (Narrow Body)	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

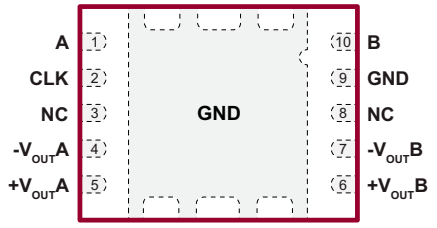
Parameter	Value
Input to output isolation voltage, V_{ISO}	±400V
Logic input voltage, V_A, V_B	-0.5 to +7.0V
Maximum junction temperature	+125°C
Storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

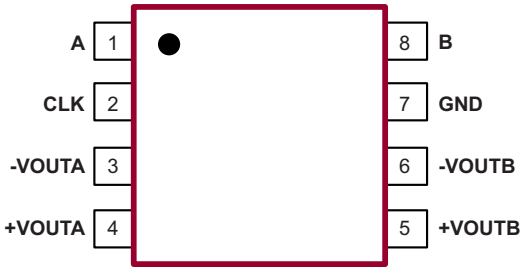
Typical Thermal Resistance

Package	θ_{ja}
10-Lead DFN	40°C/W
8-Lead SOIC (Narrow Body)	101°C/W

Pin Configurations



10-Lead DFN
(top view)



8-Lead SOIC (Narrow Body)
(top view)

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
___ = "Green" Packaging

Package may or may not include the following marks: Si or

10-Lead DFN

YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (Narrow Body

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
CLK	External clock frequency	0.5	-	2.0	MHz	---
V_{IHCLK}	Clock input high voltage	3.15	-	5.5	V	---
V_{ILCLK}	Clock input low voltage	0	-	0.5	V	---
V_{IH}	Logic input high voltage	3.15	-	5.5	V	---
V_{IL}	Logic input low voltage	0	-	0.5	V	---
T_A	Operating temperature	-40	-	+85	°C	---

DC Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{HA} + I_{HB}$	Total logic high input current	-	-	300	µA	V_A = 3.5V, V_B = 3.5V, CLK = 0V
		-	-	500	µA	V_A = 3.5V, V_B = 3.5V, CLK = 500kHz
		-	-	2.0	mA	V_A = 3.5V, V_B = 3.5V, CLK = 2.0MHz
		-	-	1.0	mA	V_A = 5.5V, V_B = 5.5V, CLK = 0V
		-	-	2.0	mA	V_A = 5.5V, V_B = 5.5V, CLK = 500kHz
V_{OUTA}, V_{OUTB}	Output voltage	6.0	-	-	V	V_A = 3.15V, V_B = 3.15V, CLK = 0V, no load
		5.0	-	-	V	V_A = 3.15V, V_B = 3.15V, CLK = 500kHz, no load
		6.0	-	-	V	V_A = 3.15V, V_B = 3.15V, CLK = 2.0MHz, no load
		10.0	-	-	V	V_A = 4.5V, V_B = 4.5V, CLK = 0V, no load
		8.0	-	-	V	V_A = 4.5V, V_B = 4.5V, CLK = 500KHz, no load
I_{ILA}	Logic low input A current	-	-	10	µA	V_A = 0.5V, V_B = high
I_{ILB}	Logic low input B current	-	-	10	µA	V_A = high, V_B = 0.5V
I_{ILQ}	Quiescent current	-	-	10	µA	V_A = 0.5V, V_B = 0.5V
V_{ISO}	Input to output isolation voltage	±400	-	-	V	---
V_{CISO}	Output to output isolation voltage	±700	-	-	V	---

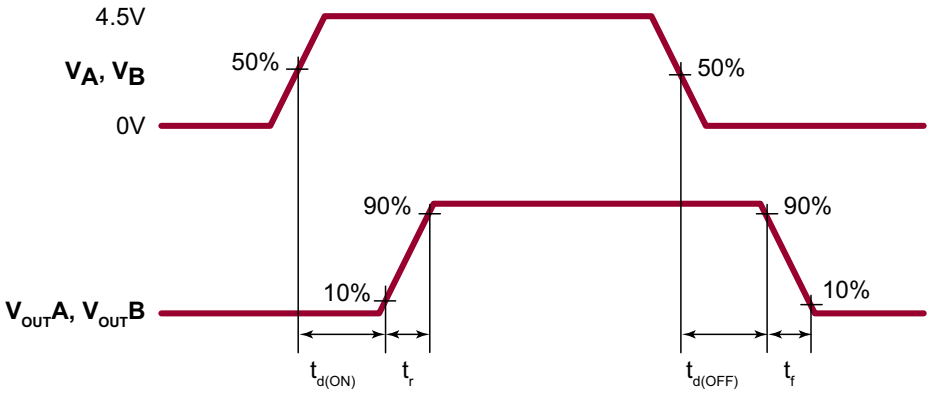
AC Electrical Characteristics *(T_A =25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
$t_{d(ON)}$	Turn-ON delay time	-	-	50	µs	See timing diagram and test circuit CLK = 0V, CL = 600pF
t_r	Rise time	-	-	650	µs	
$t_{d(OFF)}$	Turn-OFF delay time	-	-	150	µs	
t_f	Fall time	-	-	3.0	ms	

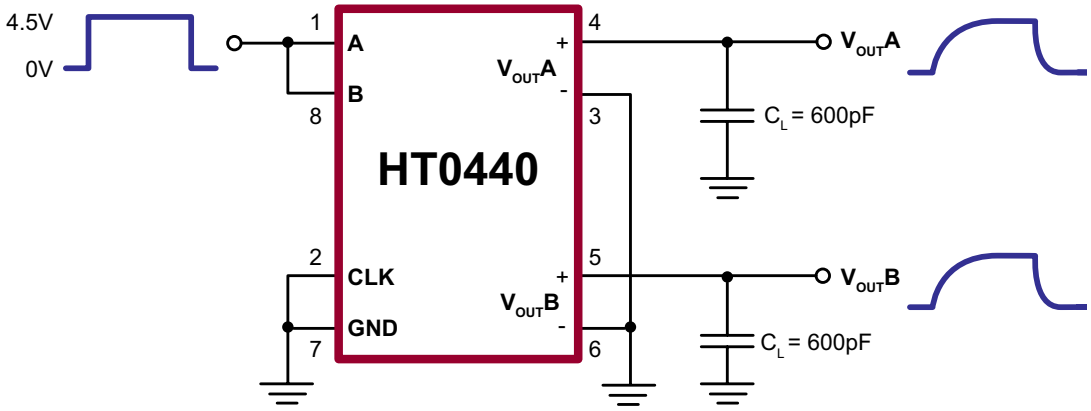
Truth Table

A	B	CLK	V_{OUT}A	V_{OUT}B	Internal Clock
0	0	0	OFF	OFF	OFF
0	⌐	0	OFF	ON	ON
⌐	0	0	ON	OFF	ON
1	1	0	ON	ON	ON
0	0	CLK	OFF	OFF	OFF
0	⌐	CLK	OFF	ON	OFF
⌐	0	CLK	ON	OFF	OFF
1	1	CLK	ON	ON	OFF

Timing Diagram

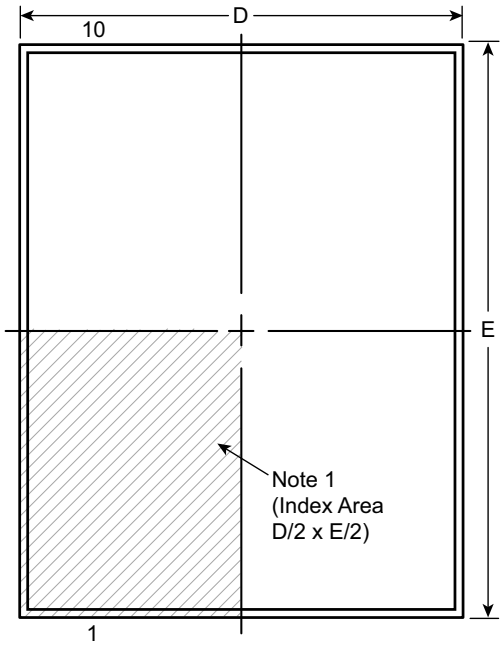


Test Circuit

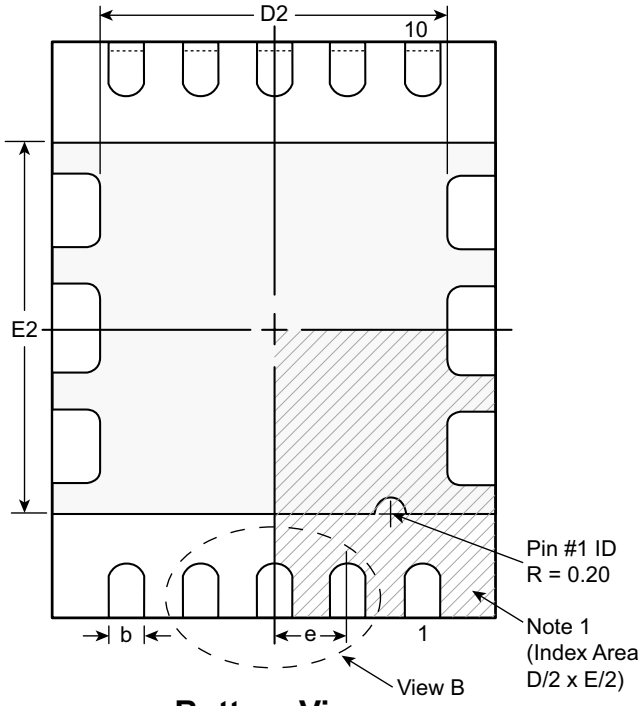


10-Lead DFN Package Outline (K6)

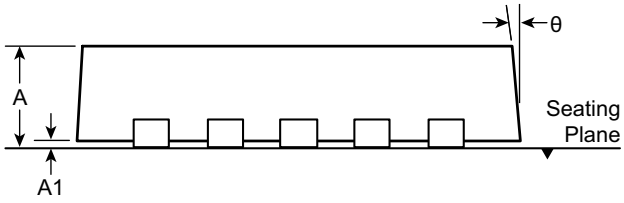
3.00x4.00mm body, 1.00mm height (max), 0.50mm pitch



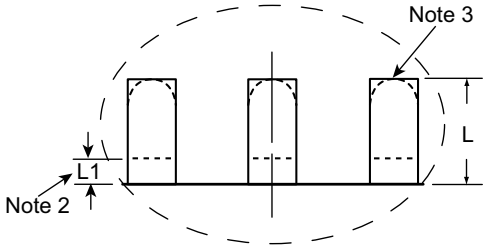
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

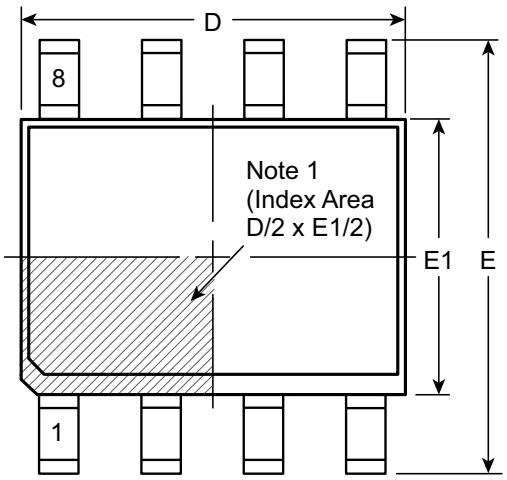
Symbol		A	A1	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.18	2.95	2.20	3.95	2.50	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02	0.25	3.00	2.35	4.00	2.65		0.40	-	-
	MAX	1.00	0.05	0.30	3.05	2.45	4.05	2.75		0.50	0.15	14°

Drawings not to scale.

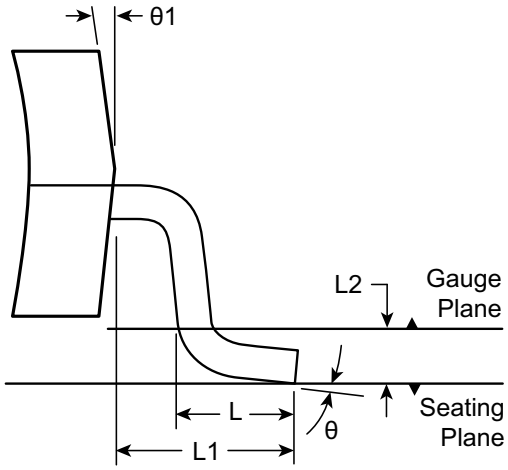
Supertex Doc. #: *DSPD-10DFNK63X4P050, Version A072611*

8-Lead SOIC (Narrow Body) Package Outline (LG)

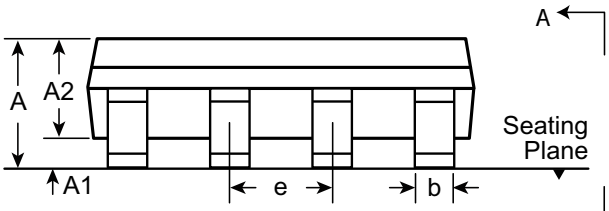
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



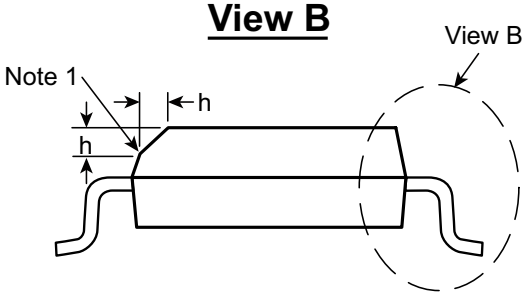
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-8SOLGTG, Version I041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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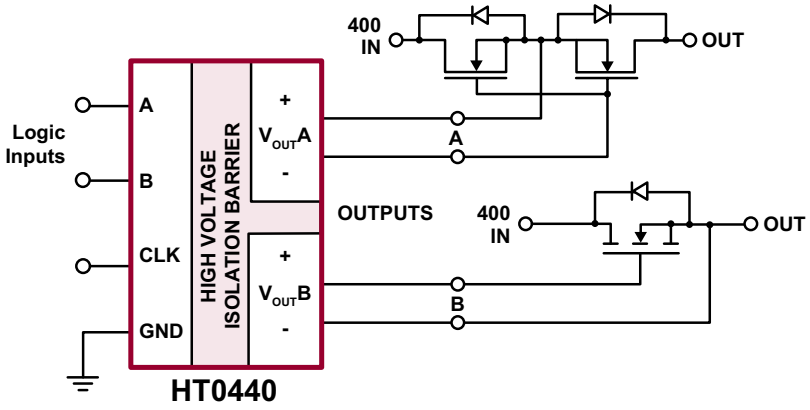
High Voltage Isolated MOSFET Driver

Features

- Switches up to ±400V from ground referenced logic
- Provides ±700V isolation between outputs
- No floating power supplies required to bias MOSFETs
- Operates isolated MOSFETs from 3.15V min., 5.5V max. logic inputs
- 1.0mA max. input operating current per channel
- No biasing current required from high voltage rails
- Low profile, surface-mount packaging
- Not recommended for applications with AC across input - output

The Supertex HT0440 is a dual, high voltage isolated driver utilizing Supertex's proprietary HVCMOS technology. It is designed to drive discrete MOSFETs configured as bi-directional or unidirectional switches. It can drive N-channel MOSFETs as high side switches up to 400V. The HT0440 has an internal clock which generates two independent DC isolated voltages to the outputs, V_{OUTA} and V_{OUTB}, when logic inputs A and B are at logic high. The internal clock can be disabled by applying an external clock signal to the CLK pin. This allows the power dissipation and AC characteristics to be tailored to meet specific needs. The HT0440 does not require any external power supplies. The internal supply voltage is supplied by either of the two logic inputs A or B when they are at logic high.

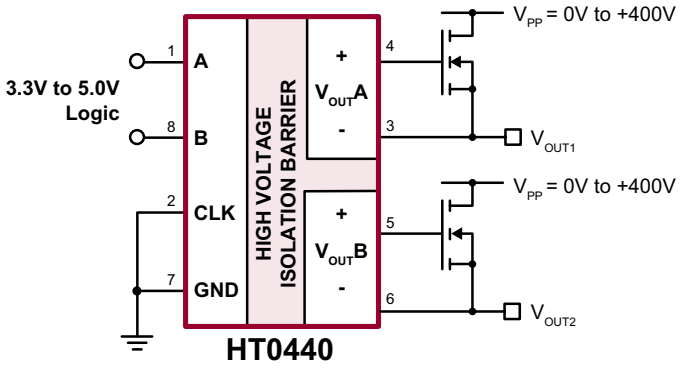
Figure 1



N-Channel High Side Switches

Driving high side N-channel MOSFETs from ground referenced logic requires a separate power supply that is 10 to 15V higher in potential than the high side rail. This is necessary to provide the gate bias to control the MOSFETs. Alternatively, a P-channel MOSFET can be used with a voltage level translation scheme that maintains a safe 10 to 15V differential between gate to source. As shown in Figure 2, an N-channel MOSFET can be driven from a floating gate drive provided by the HT0440. As shown in the circuit, the input to the HT0440 is connected to the output of a microprocessor, thereby providing a convenient and safe interface. Another advantage is the lower cost of an N-channel MOSFET compared to a P-channel device, especially if low ON-resistance is necessary. This two chip solution is cost effective, since the component count is much lower than any other previously used method.

Figure 2

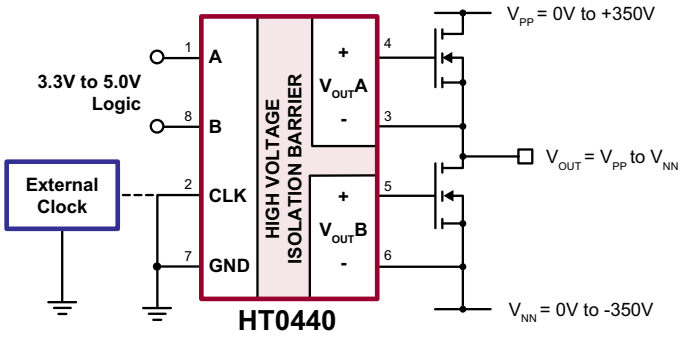


Totem Pole High Voltage Output

The high side, or “top-side,” switch in a totem pole configuration requires complicated drive and level translation schemes as mentioned earlier in this application note. A simple way of switching an output between positive and negative voltage rails directly from 5.0V logic is to use 2 N-channel MOSFETs with a single HT0440. Again, the floating and isolated outputs of the HT0440 are used to directly drive the top and bottom side N-channel MOSFETs. The logic control inputs can be exercised to produce break-before-make switching that eliminates potential short circuiting of the positive and negative rails. This easy technique enables the output to be switched between +350 and -350V by simply applying a +5.0V logic control to both logic inputs of the HT0440. No other interfacing is required. The circuit is ideal for lower switching speed applications. An external clock can be used at a lower frequency than the on-chip clock of 1MHz to reduce current input demand into the logic control pins. In this case, Pin 2 is simply connected to the external clock instead of ground.

Compared to previously used schemes for driving MOSFETs, e.g. pulse transformers and optical isolators, this technique utilizes smaller and less costly components, thereby saving board space and cost.

Figure 3



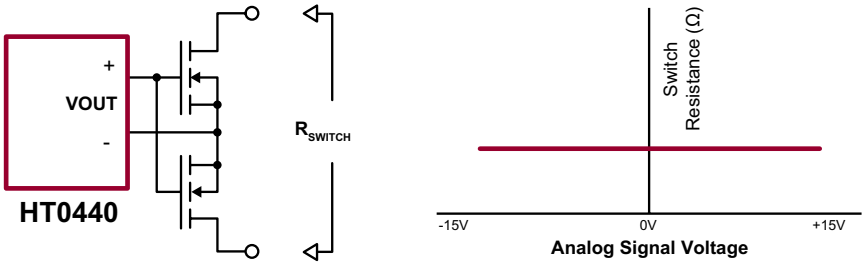
Constant Resistance Analog Switch

Applications that require a constant ON-resistance over a wide range of analog signals will benefit considerably from the HT0440. Any MOSFET used in conjunction with a HT0440 will exhibit a fixed “ON” state resistance due to the constant value of voltage across the gate and source of the MOSFET switch (see Figure 5). This gate-source voltage differential will remain independent of the voltage level and polarity of the analog signal through the switch. Some examples of applications that benefit from this technique are high-end audio, sample and hold, and data conversion circuits.

Figure 4 shows a commonly used scheme for most Analog Switch ICs that utilizes an N- and P-channel MOSFET. A major disadvantage of this configuration is that the ON-resistance of the analog switch changes with variations in the amplitude of the signal voltage.

Figure 4 - Conventional Approach

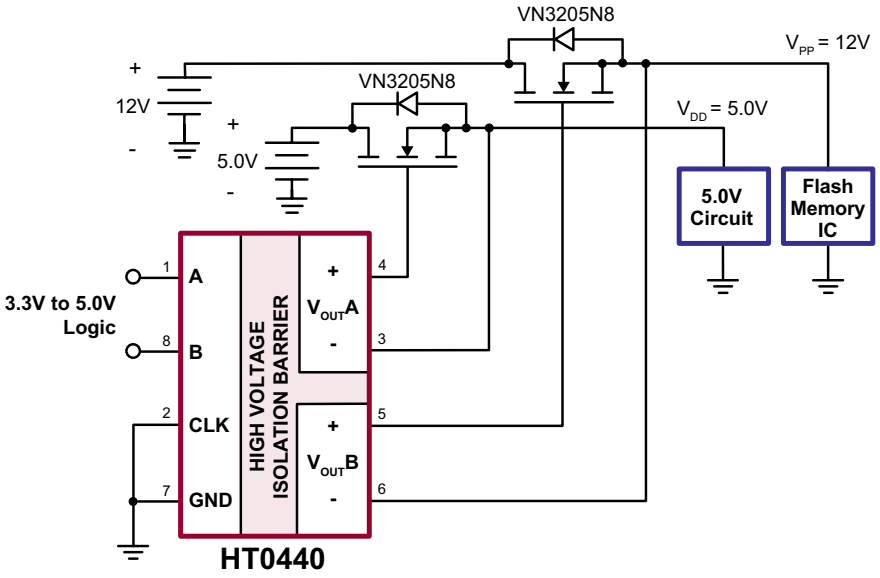
Figure 5 - HT0440 Solution



Power Management Circuits

With outputs that are not only electrically isolated from each other but also isolated from the logic controls and the ground reference, the HT0440 is useful in a variety of power management circuits. The simple application of input logic allows for power rails to directly switch up to 400V via high voltage N-channel MOSFETS. The HT0440 structure, which has a high degree of galvanic isolation, independently controls two separate power circuits. These power loops need not even have the same ground reference as the logic signals; they can be totally floating systems with their own “ground” references.

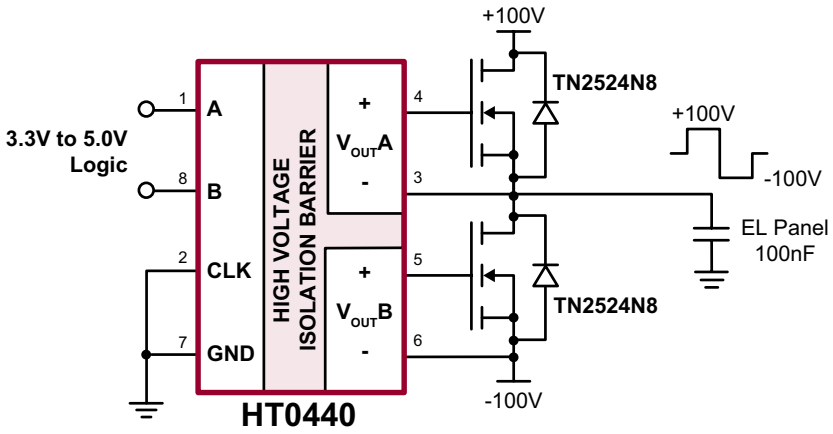
Figure 6



Electroluminscent Backlight Driver

The isolation feature of the HT0440 driver outputs make them ideal for driving Totem Pole N-channel MOSFETS between both positive and negative voltage rails. The low input logic current of the HT0440, together with the fact that it need not be driven from a power supply, conserves power from batteries in portable systems. The low profile height and package size of the surface mounted HT0440 make it ideal for use in backlight systems in a portable application.

Figure 7

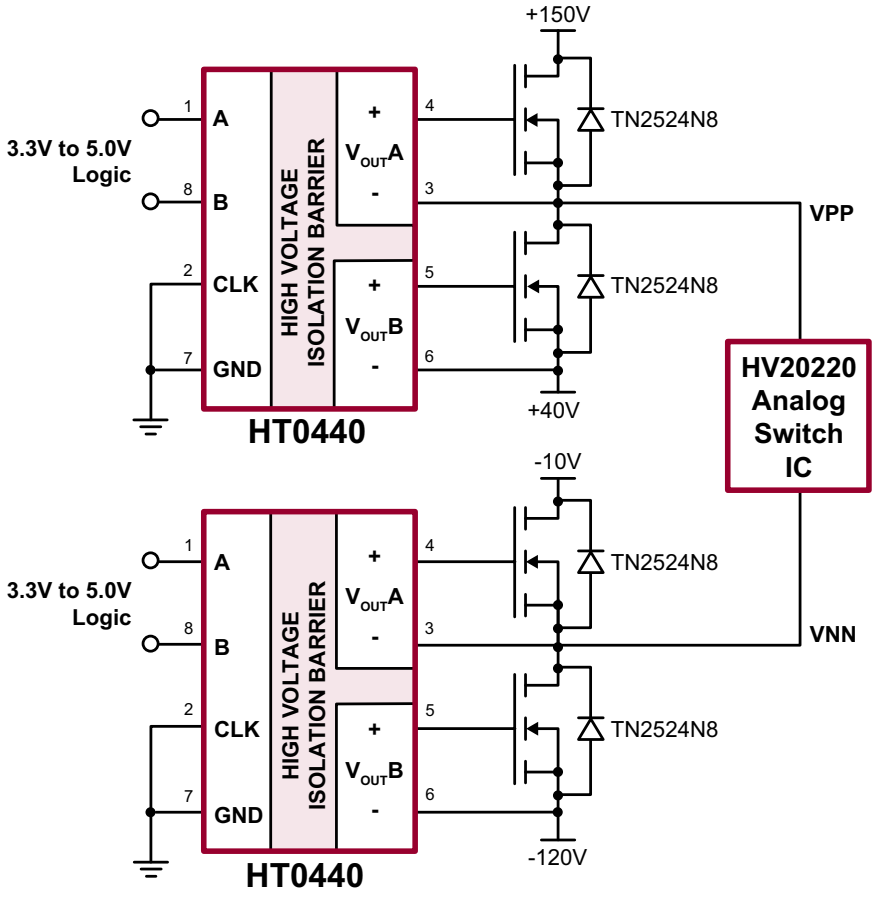


High Voltage Selector Switch

The HT0440 is compatible in voltage capability with the wide range of high voltage driver ICs from Supertex. Figure 8 shows an HV20220 Analog Switch used in a typical ultrasound detection system.

To exercise the required control on piezoelectric transducer connected to the outputs of the HV20220, different levels of high voltages need to be applied to the analog switch. The HT0440 driver offers a simple and cost affective way to achieve this control. In applications where high board density is required, the low power dissipation and surface mount packaging of the HT0440 make it an ideal solution.

Figure 8

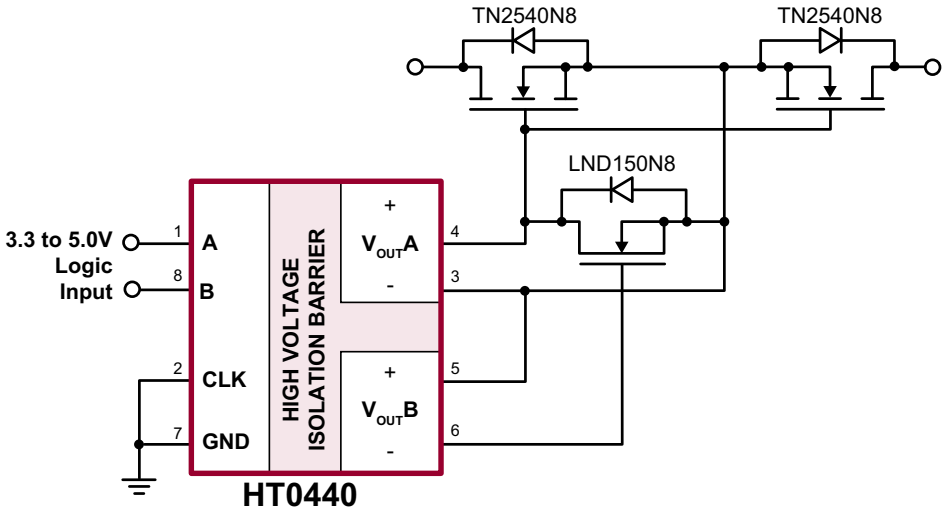


Fast Turn-off Break-Before-Make Switch

The turn-on time of a typical driver is related to the input capacitance of the MOSFET it is driving. T_{ON} is 0.25 x 10^6 x (MOSFET $C_{ISS)}$. Similarly, the turn-off time of the driver is 10^6 x (MOSFET C_{ISS}).

In this situation, t_{OFF} is greater than t_{ON}. For a system using multiple switches, however, there may be a problem since some switches will close before others open. Using the HT0440 as shown in Figure 9 will provide a solution to this problem and ensure that the correct switches open before others close. To achieve turn-off time that is less than turn-on time, a small depletion-mode MOSFET placed on the output of the HT0440 (as shown) will slow t_{ON} such that the circuit exhibits break-before-make switching.

Figure 9

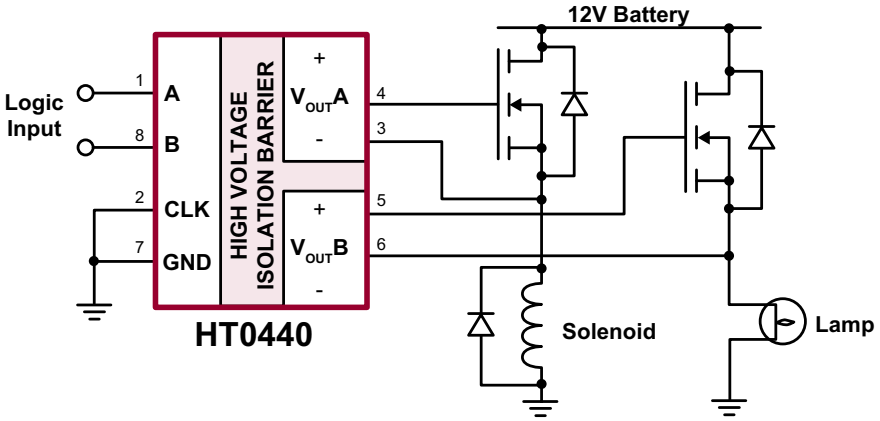


Automotive High Side Switches

In automotive applications requiring large MOSFETs, an N-Channel MOSFET with the same R_{ON} and BV_{DSS} as a P-channel will be half the size of the P-channel device and, cost-wise, would be a more effective solution.

The floating gate drive of the HT0440 allows direct interface of a 5.0V microprocessor output to an N-channel MOSFET. An important advantage of using the HT0440 is that isolation is provided between the load, which is usually in a high transient voltage environment, and the low voltage control circuitry.

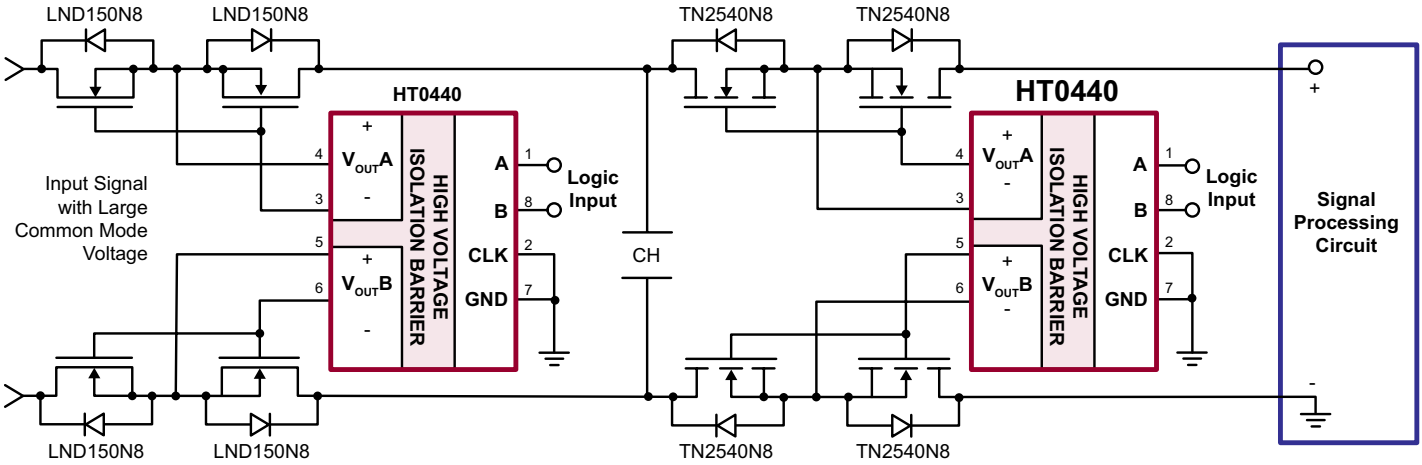
Figure 10



Data Acquisition Using Flying Capacitor

Present solutions for collecting and routing analog data into data acquisition systems usually use relays or opto-coupled systems. Although these solutions provide the necessary isolation from the analog line to the control line, they have significant drawbacks. They are typically large, high profile devices that draw considerable power and exhibit slow switching speeds. With the HT0440, higher speeds are achieved in routing the signals, and there is no degradation of the isolation voltage. Additionally, higher board density and a lower profile solution is provided with the HT0440 in the SO-8 package. Another advantage is greatly reduced power consumption. Figure 11 shows a solution using the HT0440, LND150N8 (depletion-mode MOSFETs) and TN2540N8 (enhancement mode MOSFETs) all manufactured by Supertex in surface mount packages.

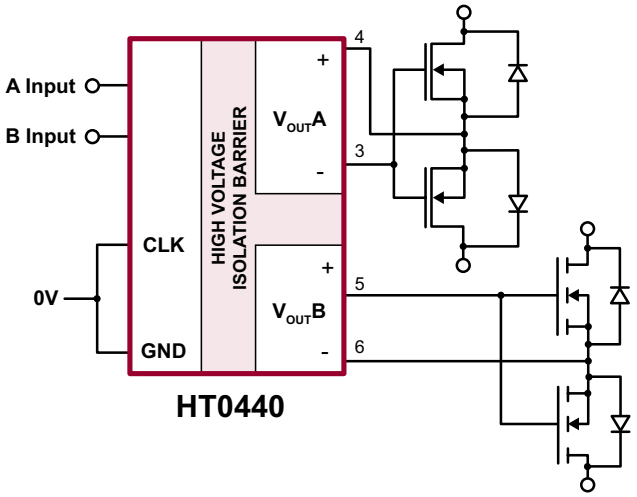
Figure 11



Solid State Relay

The HT0440 technology allows multiple channel drives to be integrated in a monolithic IC. The 2 channel HT0440 has galvanic ±400V isolation between the outputs and logic inputs, and ±700V isolation between output channels. The HT0440 driver along with the MOSFET switches is analogous to a relay. The HT0440 will drive both depletion-mode and enhancement-mode bidirectional MOSFETs, thereby giving either normally open and normally closed "contacts." The low profile SO-8 surface mount HT0440 gives this solution an added advantage over the single channel high profile opto packages, and is also lower in cost.

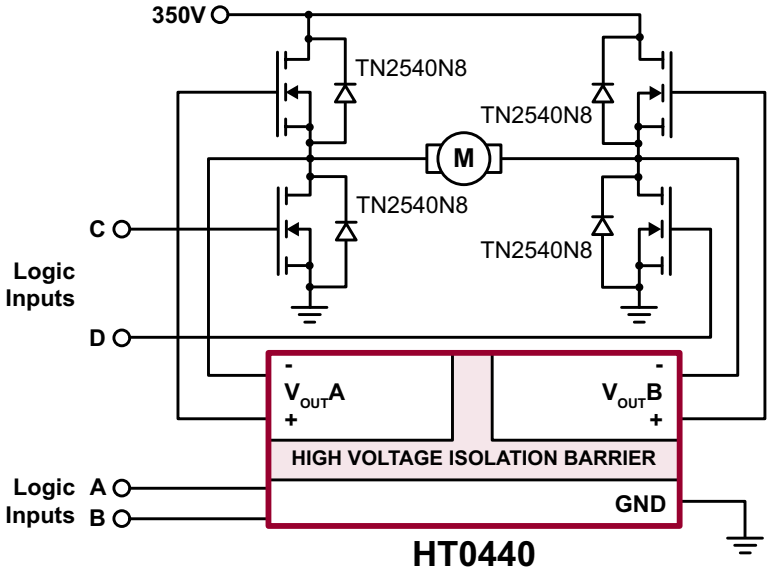
Figure 12



High and Low Side Motor Drivers

Motor drive that requires on/off as well as reverse control often use P-channel, MOSFET switches in the top end of H-bridge configurations. With the HT0440, these P-channel FETs can be replaced by less expensive N-channel switches. This solution is particularly attractive where it is only necessary to have a forward/reverse control without any critical speed control. Shown below are 4 N-channel MOSFETS configured with a HT0440 driver to provide a cost effective solution.

Figure 13



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