CD4070B, CD4077B

CMOS Quad Exclusive-OR and Exclusive-NOR Gate

Data sheet acquired from Harris Semiconductor
SCHS055C

January 1998 - Revised July 2002

Features

- **High-Voltage Types (20V Rating)**
- **CD4070B - Quad Exclusive-OR Gate**
- **CD4077B - Quad Exclusive-NOR Gate**
- **Medium Speed Operation**
  - **t_{PHL}, t_{PLH} = 65ns (Typ) at V_{DD} = 10V, C_L = 50pF**
- **100% Tested for Quiescent Current at 20V**
- **Standardized Symmetrical Output Characteristics**
- **5V, 10V and 15V Parametric Ratings**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range**
  - **100nA at 18V and 25°C**
- **Noise Margin (Over Full Package Temperature Range)**
  - **1V at V_{DD} = 5V, 2V at V_{DD} = 10V, 2.5V at V_{DD} = 15V**
- **Meets All Requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices**

Applications

- **Logical Comparators**
- **Adders/Subtractors**
- **Parity Generators and Checkers**

Description

The Harris CD4070B contains four independent Exclusive-OR gates. The Harris CD4077B contains four independent Exclusive-NOR gates.

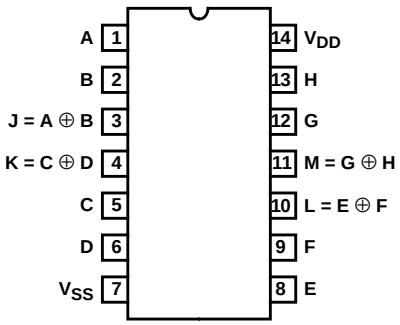
The CD4070B and CD4077B provide the system designer with a means for direct implementation of the Exclusive-OR and Exclusive-NOR functions, respectively.

Ordering Information

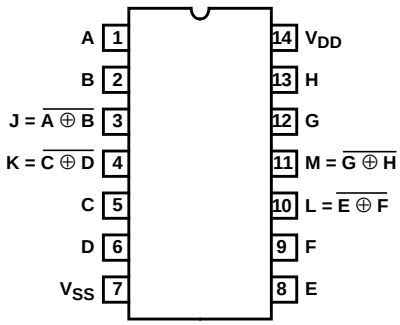
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4070BE	-55 to 125	14 Ld PDIP
CD4070BF	-55 to 125	14 Ld CERDIP
CD4070BM	-55 to 125	14 Ld SOIC
CD4070BNSR	-55 to 125	14 Ld SOP
CD4070BPWR	-55 to 125	14 Ld TSSOP
CD4077BE	-55 to 125	14 Ld PDIP
CD4077BF	-55 to 125	14 Ld CERDIP
CD4077BM	-55 to 125	14 Ld SOIC
CD4077BM96	-55 to 125	14 Ld SOIC
CD4077BNSR	-55 to 125	14 Ld SOP
CD4077BPWR	-55 to 125	14 Ld TSSOP

Pinouts

CD4070B
(PDIP, CERDIP, SOIC, SOP, TSSOP)
TOP VIEW



CD4077B
(PDIP, CERDIP, SOIC, SOP, TSSOP)
TOP VIEW

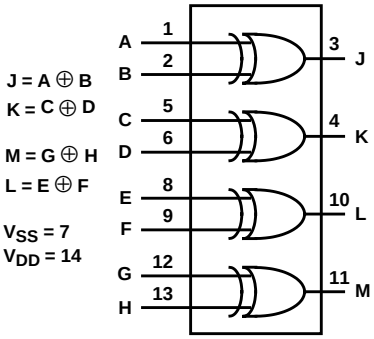


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

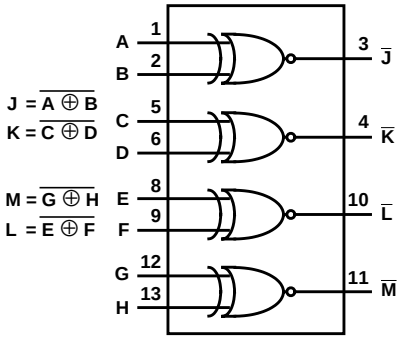
File Number **910.1**

Functional Diagrams

CD4070B



CD4077B



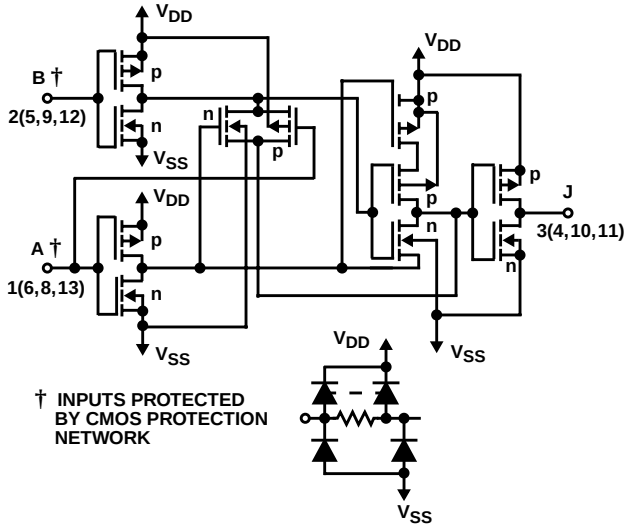


FIGURE 1. SCHEMATIC DIAGRAM FOR CD4070B (1 OF 4 IDENTICAL GATES)

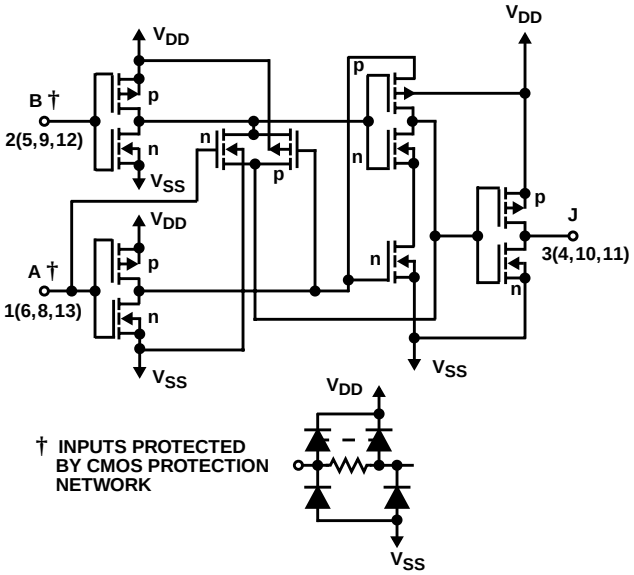


FIGURE 2. SCHEMATIC DIAGRAM FOR CD4077B (1 OF 4 IDENTICAL GATES)

CD4070B TRUTH TABLE (1 OF 4 GATES)

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

NOTE:
1 = High Level
0 = Low Level
J = A ⊕ B

CD4077B TRUTH TABLE (1 OF 4 GATES)

A	B	J
0	0	1
1	0	0
0	1	0
1	1	1

NOTE:
1 = High Level
0 = Low Level
J = $\overline{A \oplus B}$

Absolute Maximum Ratings

DC Supply Voltage Range (V_{DD}) . . . . . -0.5V to 20V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} 0.5V
DC Input Current . . . . . ± 10mA

Operating Conditions

Temperature Range (T_A) . . . . . -55^oC to 125^oC
Supply Voltage Range (Typical) . . . . . 3V to 18V

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
PDIP Package . . . . . $80^oC/W$
SOIC Package . . . . . $86^oC/W$
SOP Package . . . . . $76^oC/W$
TSSOP Package . . . . . $113^oC/W$
Maximum Junction Temperature (Hermetic Package or Die) . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (^oC)							UNITS
								25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	85	125	MIN	TYP	MAX	
Quiescent Device Current I_{DD} Max	-	0, 5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	µA
	-	0, 10	10	0.5	0.5	15	15	-	0.01	0.5	µA
	-	0, 15	15	1	1	30	30	-	0.01	1	µA
	-	0, 20	20	5	5	150	150	-	0.02	5	µA
Output Low (Sink) Current I_{OL} Min	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	mA
	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	-	mA
Output High (Source) Current I_{OH} Min	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	mA
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	mA
	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	mA
Output Voltage: Low Level, V_{OL} Max	-	0, 5	5	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0, 10	10	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0, 15	15	0.05	0.05	0.05	0.05	-	0	0.05	V
Output Voltage: High Level, V_{OH} Min	-	0, 5	5	4.95	4.95	4.95	4.95	4.95	5	-	V
	-	0, 10	10	9.95	9.95	9.95	9.95	9.95	10	-	V
	-	0, 15	15	14.95	14.95	14.95	14.95	14.95	15	-	V
Input Low Voltage, V_{IL} Max	0.5, 4.5	-	5	1.5	1.5	1.5	1.5	-	-	1.5	V
	1, 9	-	10	3	3	3	3	-	-	3	V
	1.5, 13.5	-	15	4	4	4	4	-	-	4	V
Input High Voltage, V_{IH} Min	0.5, 4.5	-	5	3.5	3.5	3.5	3.5	3.5	-	-	V
	1, 9	-	10	7	7	7	7	7	-	-	V
	1.5, 13.5	-	15	11	11	11	11	11	-	-	V
Input Current, I_{IN} Max	-	0, 18	18	±0.1	±0.1	±1	±1	-	$\pm 10^{-5}$	±0.1	µA

AC Electrical Specifications

$T_A = 25^oC$, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS ON ALL TYPES		UNITS
		V_{DD} (V)	TYP	MAX	
Propagation Delay Time	t_{PHL}, t_{PLH}	5	140	280	ns
		10	65	130	ns
		15	50	100	ns
Transition Time	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	ns
		15	40	80	ns
Input Capacitance	C_{IN}	Any Input	5	7.5	pF

Typical Performance Curves

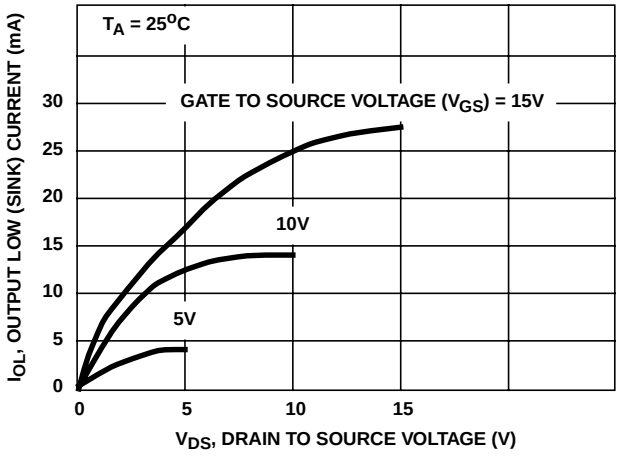


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

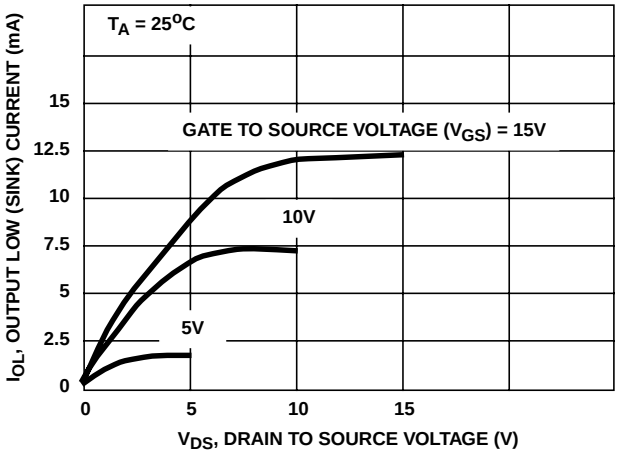


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

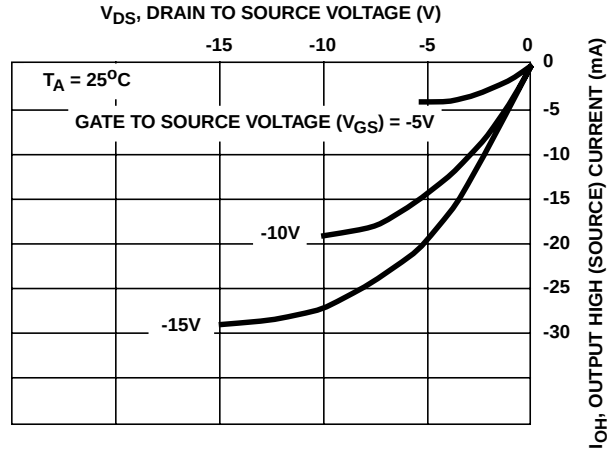


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

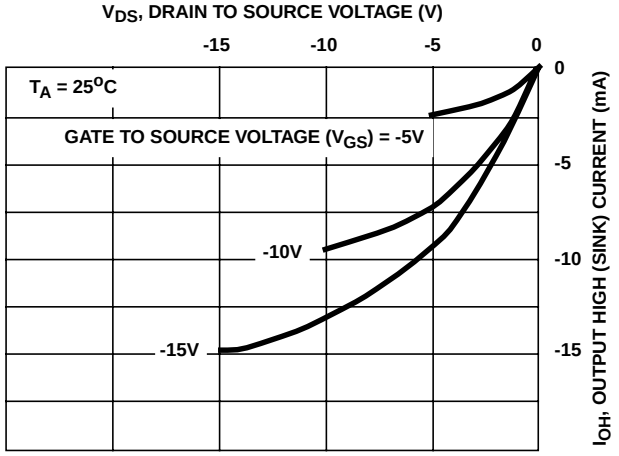


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Curves (Continued)

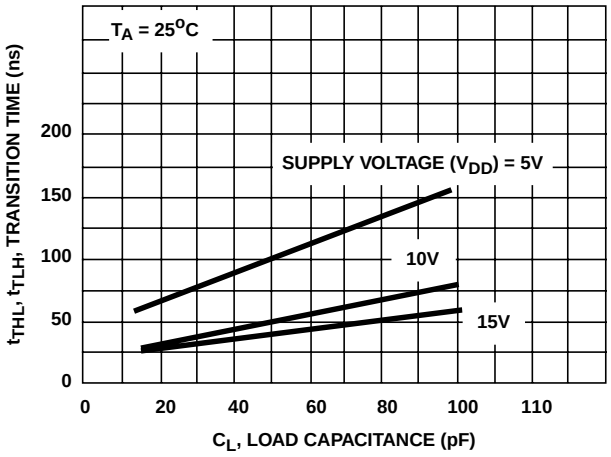


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

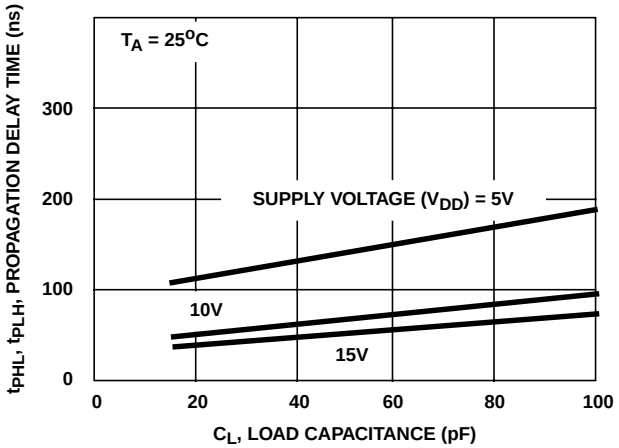


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

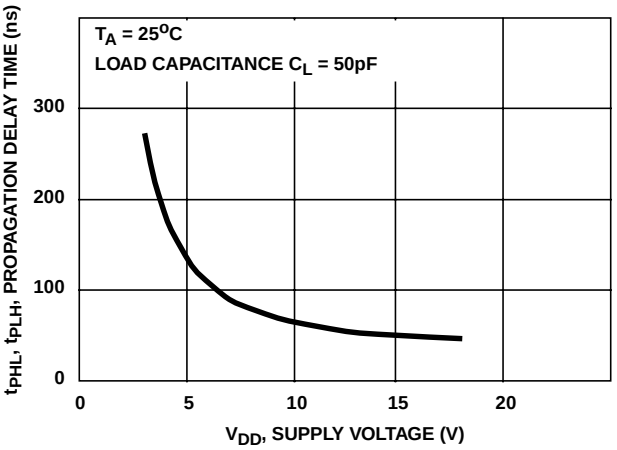


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE

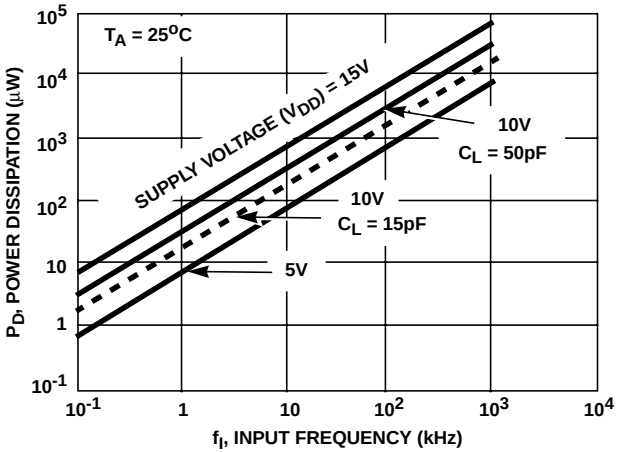


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

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