CMOS LDO Regulator Series for Portable Equipments

Versatile Package FULL CMOS LDO Regulator

BUxxUC3WG series

●General Description

BUxxUC3WG series is high-performance FULL CMOS regulator with 300-mA output, which is mounted on versatile package SSOP5 (2.9 mm × 2.8 mm × 1.25 mm). It has excellent noise characteristics and load responsiveness characteristics despite its low circuit current consumption of 50μA. It is most appropriate for various applications such as power supplies for logic IC, RF, and camera modules ROHM's.

●Features

- High accuracy detection
- low current consumption
- Compatible with small ceramic capacitor (Cin=Co=1.0uF)
- With built-in output discharge circuit
- High ripple rejection
- ON/OFF control of output voltage
- With built-in over current protection circuit and thermal shutdown circuit
- Package SSOP5 is similar to SOT-23-5 (JEDEC)
- Low dropout voltage

●Key Specifications

- Output voltage: 1.0V to 4.0V
- Accuracy output voltage: ±1.0% (±25mV)
- Low current consumption: 50μA
- Operating temperature range: -40°C to +85°C

●Applications

Battery-powered portable equipment, etc.

●Package

SSOP5: 2.90mm x 2.80mm x 1.25mm

●Typical Application Circuit

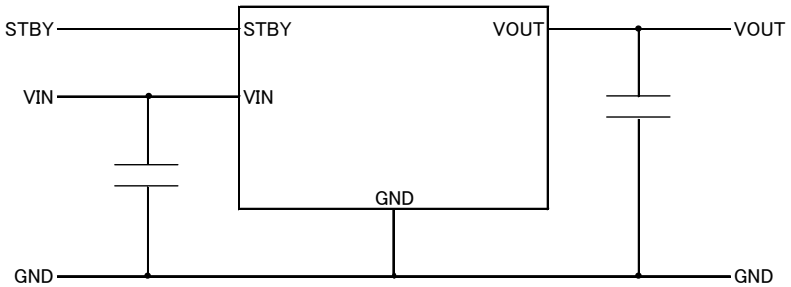
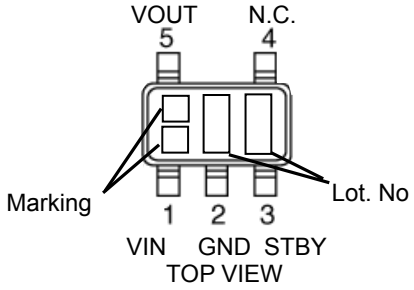


Figure 1. Application Circuit

●Connection Diagram

SSOP5



●Pin Descriptions

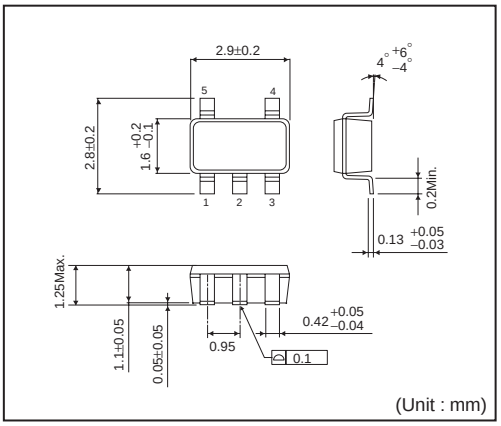
SSOP5		
PIN No.	Symbol	Function
1	VIN	Power Supply Voltage
2	GND	Grounding
3	STBY	ON/OFF control of output voltage (High: ON, Low: OFF)
4	N.C.	Unconnected Terminal
5	VOUT	Output Voltage

●Ordering Information

B U x x U C 3 W G − x x

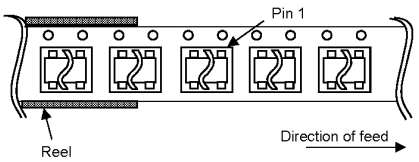
Part Number	Output Voltage 10 : 1.0V ⇩ 40 : 4.0V	Low Dropout Voltage Maximum Output Current 300mA	with switch	Package G : SSOP5	Packageing and forming specification Embossed tape and reel TR : The pin number 1 is the upper right TL : The pin number 1 is the lower left

SSOP5



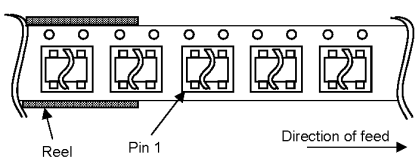
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TL (The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand)



●**Lineup**

Marking	Q0	Q1	Q2	Q3	Q4	Q5	Q6	TBD (*)	TBD (*)	TBD (*)
Output Voltage	1.0V	1.05V	1.1V	1.15V	1.2V	1.25V	1.3V	1.35V	1.4V	1.45V
Part Number	BU10	BU1A	BU11	BU1B	BU12	BU1C	BU13	BU1D	BU14	BU1E

Q7	TBD (*)	TBD (*)	TBD (*)	TBD (*)	TBD (*)	Q8	Q9	R0	TBD (*)	R1
1.5V	1.55V	1.6V	1.65V	1.7V	1.75V	1.8V	1.85V	1.9V	1.95V	2.0V
BU15	BU1F	BU16	BU1G	BU17	BU1H	BU18	BU1J	BU19	BU1K	BU20

R2	R3	TBD (*)	R4	TBD (*)	R5	TBD (*)	TBD (*)	TBD (*)	R6	TBD (*)
2.05V	2.1V	2.15V	2.2V	2.25V	2.3V	2.35V	2.4V	2.45V	2.5V	2.55V
BU2A	BU21	BU2B	BU22	BU2C	BU23	BU2D	BU24	BU2E	BU25	BU2F

R7	TBD (*)	R8	R9	Y0	Y1	Y2	Y3	Y4	TBD (*)	Y5
2.6V	2.65V	2.7V	2.75V	2.8V	2.85V	2.9V	2.95V	3.0V	3.05V	3.1V
BU26	BU2G	BU27	BU2H	BU28	BU2J	BU29	BU2K	BU30	BU3A	BU31

TBD (*)	Y6	TBD (*)	Y7	TBD (*)	Y8	TBD (*)	TBD (*)	TBD (*)	TBD (*)	TBD (*)
3.15V	3.2V	3.25V	3.3V	3.35V	3.4V	3.45V	3.5V	3.55V	3.6V	3.65V
BU3B	BU32	BU3C	BU33	BU3D	BU34	BU3E	BU35	BU3F	BU36	BU3G

Y9	TBD (*)	TBD (*)	TBD (*)	TBD (*)	TBD (*)	TBD (*)
3.7V	3.75V	3.8V	3.85V	3.9V	3.95V	4.0V
BU37	BU3H	BU38	BU3J	BU39	BU3K	BU40

(*)Under development

●**Absolute Maximum Ratings (Ta=25°C)**

PARAMETER	Symbol	Limit	Unit
Power Supply Voltage	VMAX	-0.3 ～ +6.0	V
Power Dissipation	Pd	540(*1)	mW
Maximum junction temperature	TjMAX	+125	℃
Operating Temperature Range	Topr	-40 ～ +85	℃
Storage Temperature Range	Tstg	-55 ～ +125	℃

(*1)Pd deleted at 5.4mW/℃ at temperatures above Ta=25℃, mounted on 70×70×1.6 mm glass-epoxy PCB.

●**RECOMMENDED OPERATING RANGE (not to exceed Pd)**

PARAMETER	Symbol	Limit	Unit
Power Supply Voltage	VIN	1.7～5.5	V
Maximum Output Current	IMAX	300	mA

●**OPERATING CONDITIONS**

PARAMETER	Symbol	MIN.	TYP.	MAX.	Unit	CONDITION
Input Capacitor	Cin	0.47(*2)	1.0	-	μF	Ceramic capacitor recommended
Output Capacitor	Co	0.47(*2)	1.0	-	μF	

(*2)Make sure that the output capacitor value is not kept lower than this specified level across a variety of temperature, DC bias, changing as time progresses characteristic.

●Electrical Characteristics

(Ta=25℃, VIN=VOUT+1.0V (*3), STBY=VIN, Cin=1.0μF, Co=1.0μF, unless otherwise noted.)

PARAMETER	Symbol	Limit			Unit	Conditions
		MIN.	TYP.	MAX.		
Overall Device						
Output Voltage	VOUT	VOUT×0.99	VOUT	VOUT×1.01	V	IOUT=10μA,VOUT≧2.5V
		VOUT-25mV		VOUT+25mV		IOUT=10μA,VOUT＜2.5V
Operating Current	IIN	-	50	90	μA	IOUT=0mA
Operating Current (STBY)	ISTBY	-	-	1.0	μA	STBY=0V
Ripple Rejection Ratio	RR	45	70	-	dB	VRR=-20dBv,fRR=1kHz,IOUT=10mA, VIN=3.6V
Dropout Voltage	VSAT	-	470	700	mV	1.0V≦VOUT＜1.2V(IOUT=300mA)
		-	350	500	mV	1.2V≦VOUT＜1.5V(IOUT=300mA)
		-	280	380	mV	1.5V≦VOUT＜1.7V(IOUT=300mA)
		-	250	320	mV	1.7V≦VOUT＜2.1V(IOUT=300mA)
		-	220	260	mV	2.1V≦VOUT＜2.5V(IOUT=300mA)
		-	200	220	mV	2.5V≦VOUT(IOUT=300mA)
Line Regulation	VDL	-	2	20	mV	VIN=VOUT+1.0V to 5.5V(*4), IOUT=10μA
Load Regulation	VDLO	-	25	45	mV	IOUT=0.01mA to 300mA
Over-current Protection (OCP)						
Limit Current	ILMAX	370	550	-	mA	Vo=VOUT*0.95
Short Current	ISHORT	50	150	300	mA	Vo=0V
Standby Block						
Discharge Resistor	RDSC	20	50	80	Ω	VIN=5.5V, STBY=0V, VOUT=2.6V
STBY Pin Pull-down Current	ISTB	0.1	0.9	8.0	μA	STBY=1.5V
STBY Control Voltage ON	VSTBH	1.2	-	5.5	V	
STBY Control Voltage OFF	VSTBL	-0.3	-	0.3	V	

○This product is not designed for protection against radioactive rays.

(*3) VIN=2.5V for VOUT≦1.5V

(*4) VIN=2.5V to 3.6V for VOUT≦1.5V

●Block Diagrams

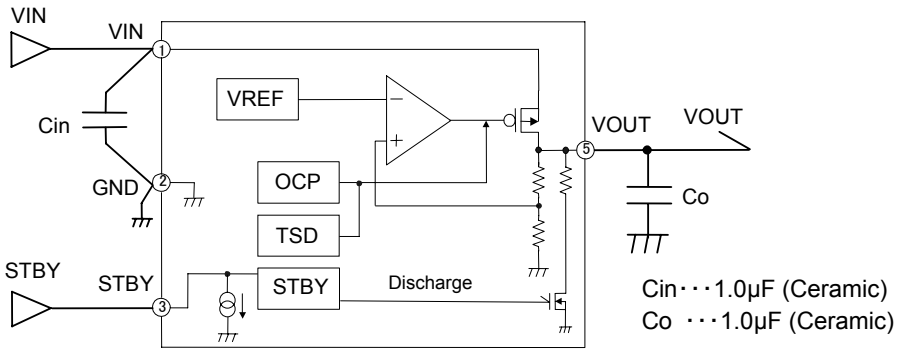


Figure 2. Block Diagrams

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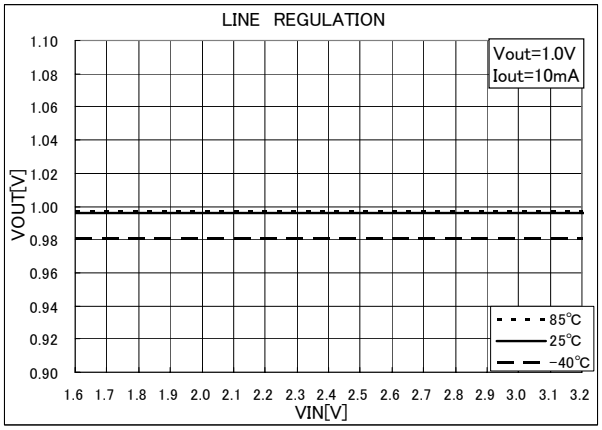

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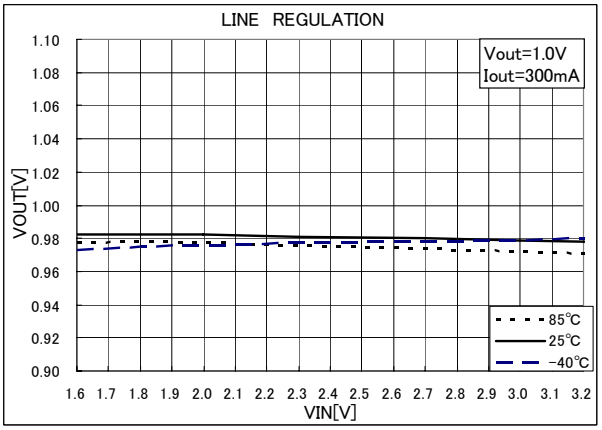

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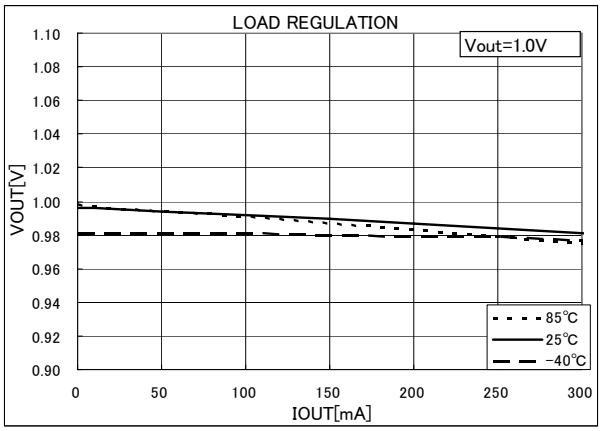

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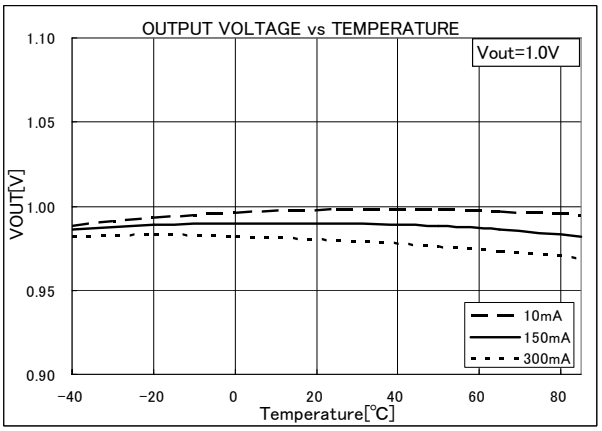

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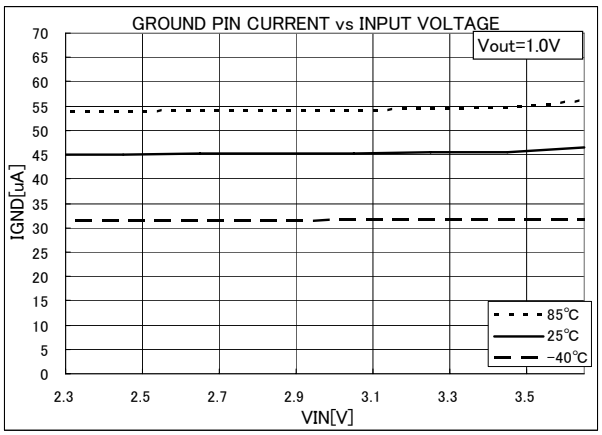

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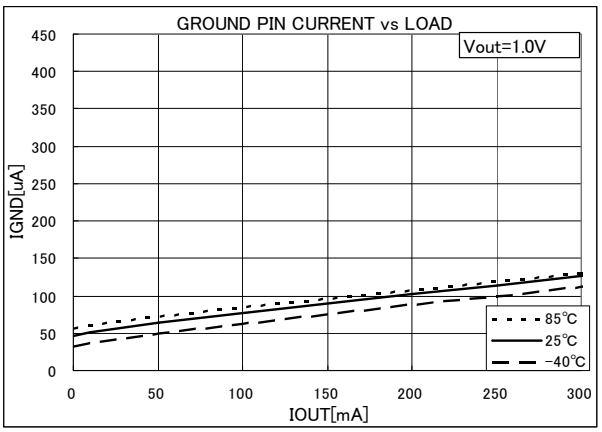

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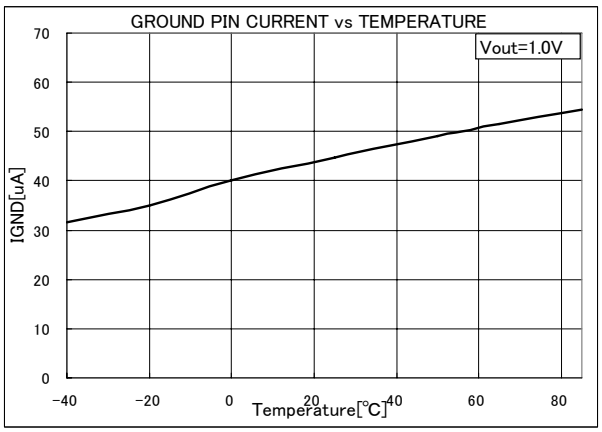

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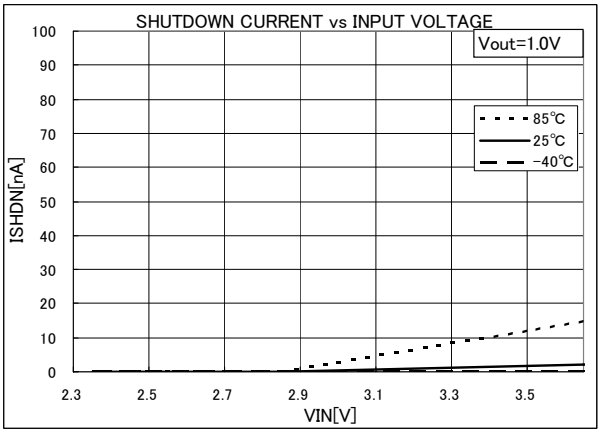

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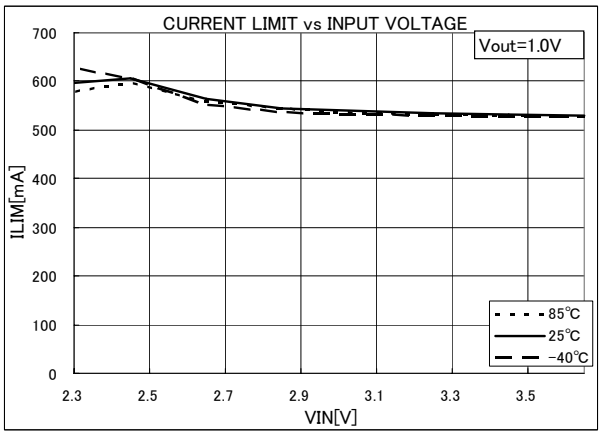

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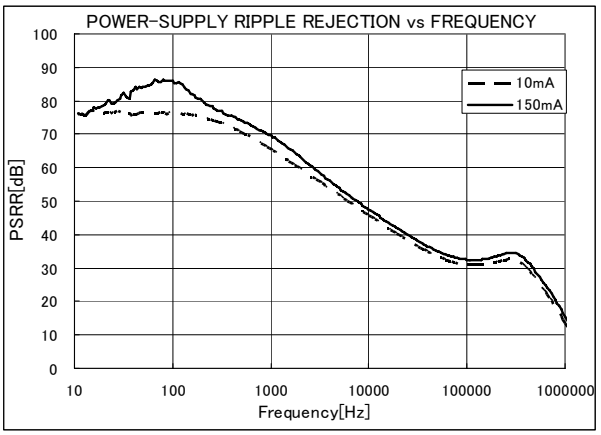

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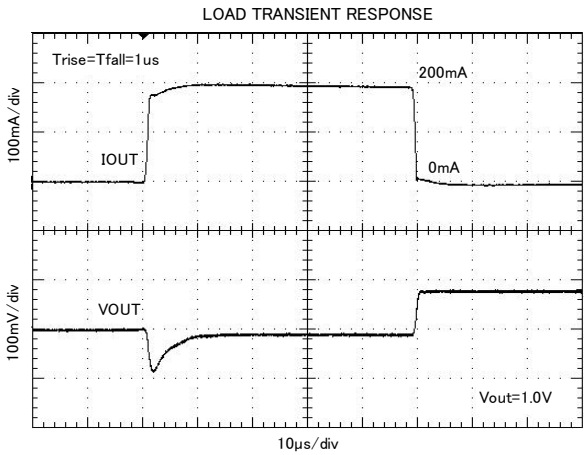

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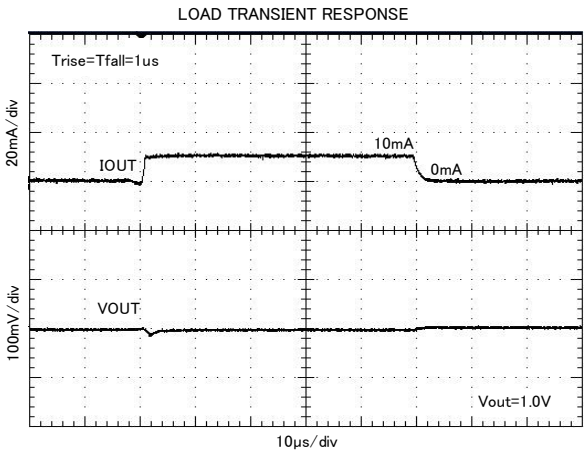

Figure 14.

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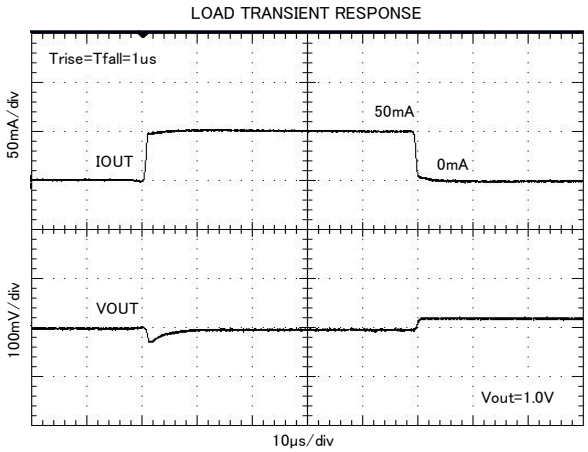

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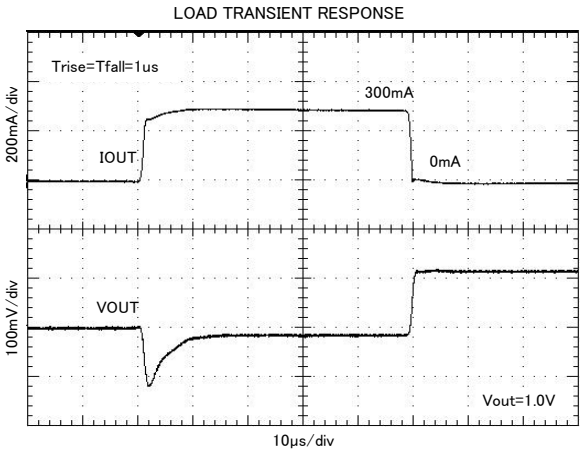

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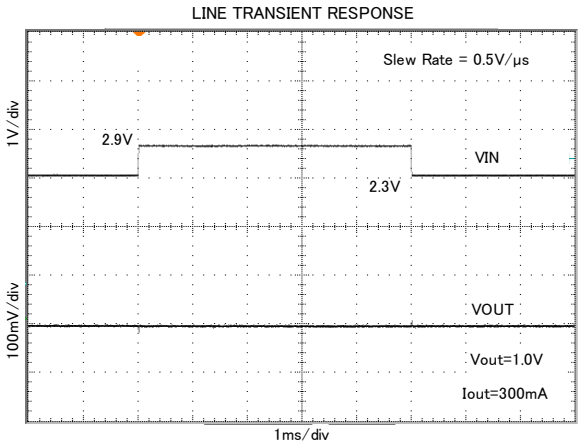

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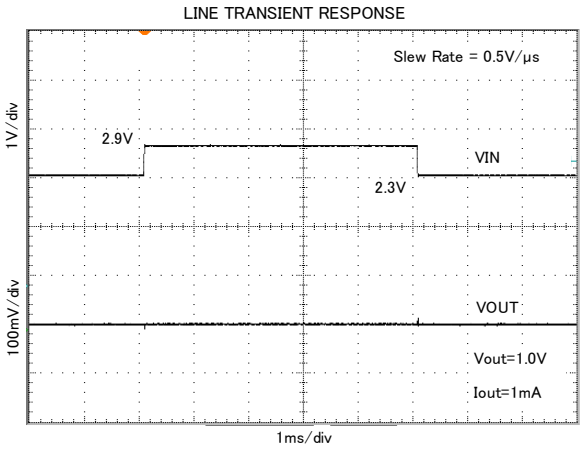

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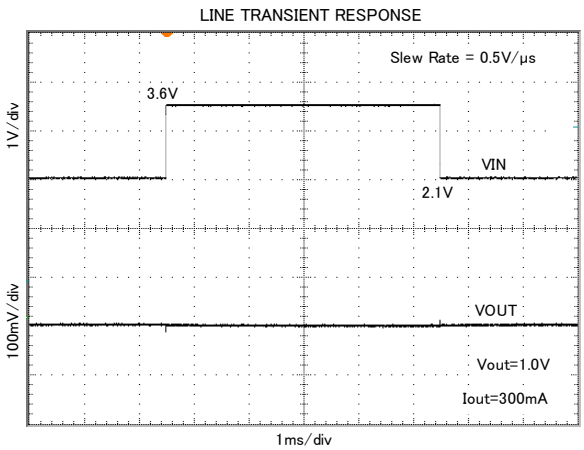

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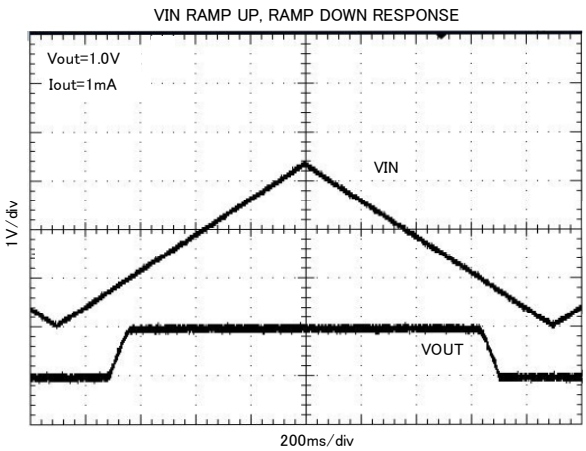

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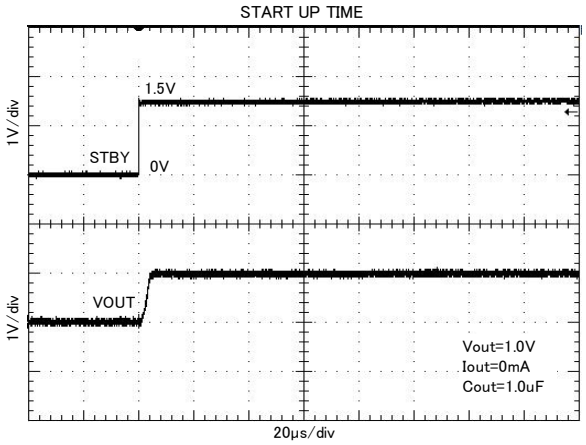

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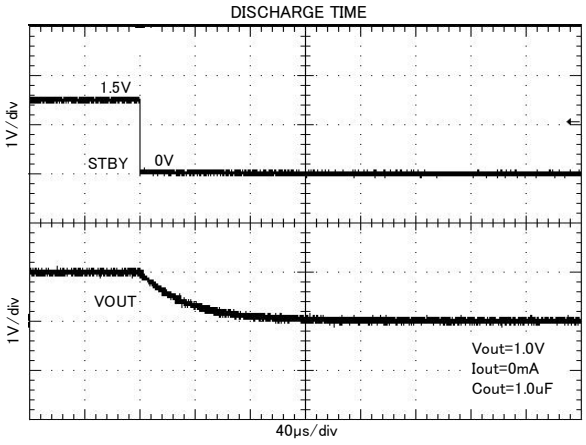

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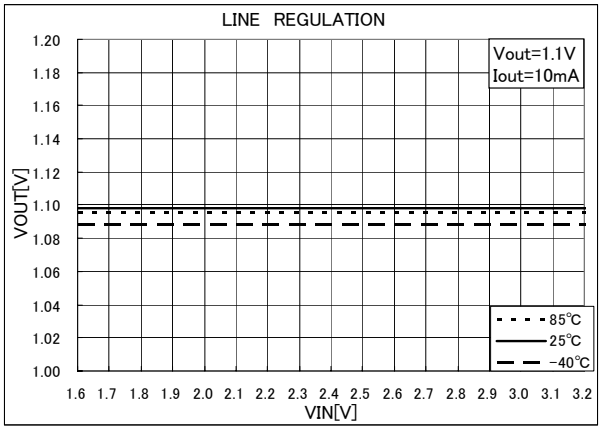

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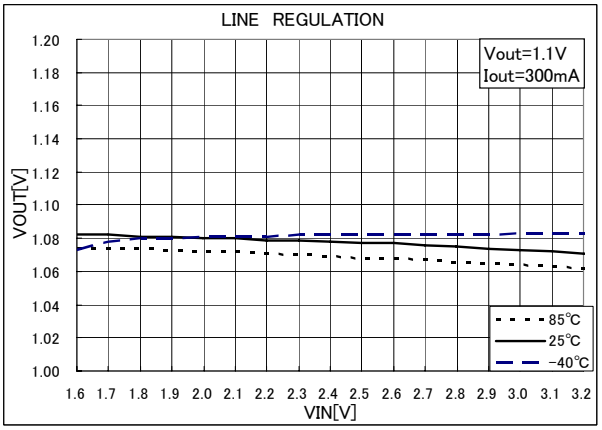

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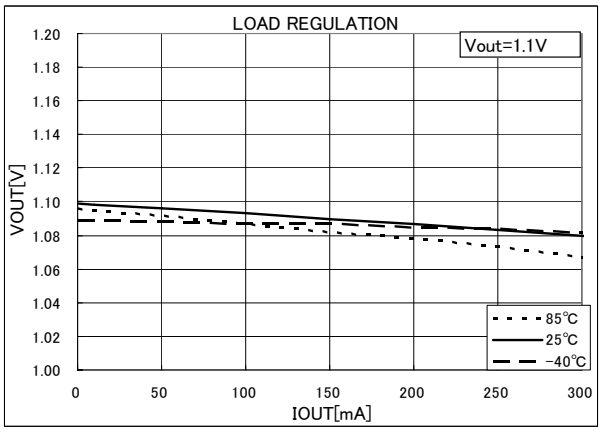

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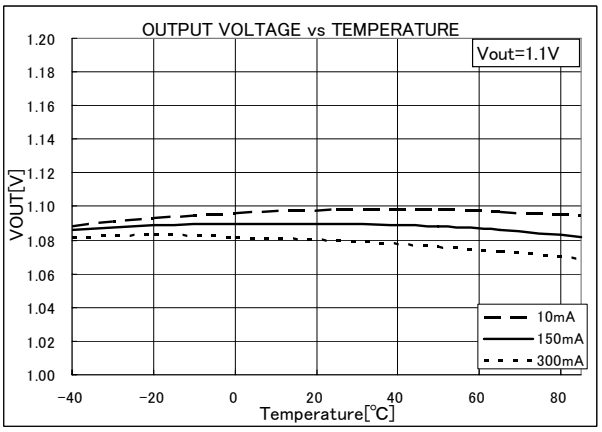

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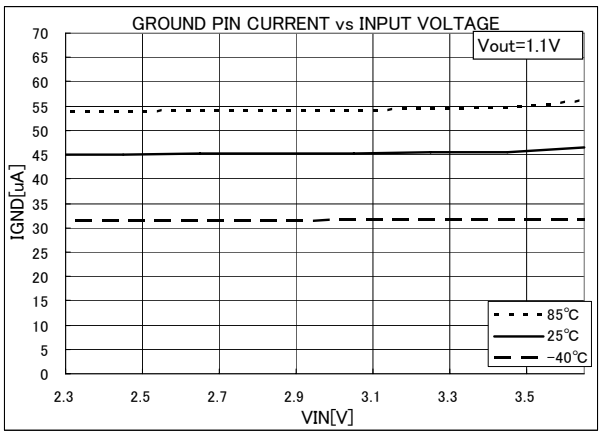

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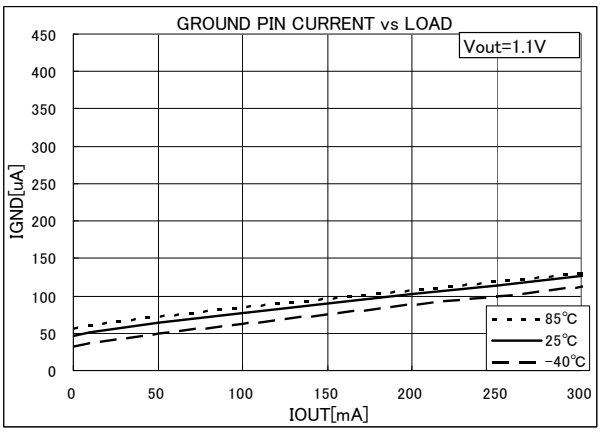

Figure28.

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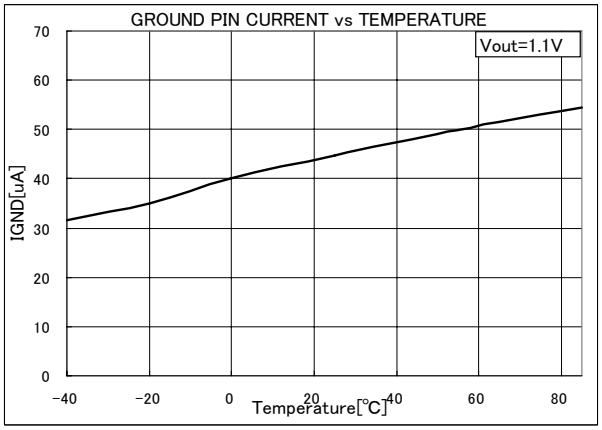

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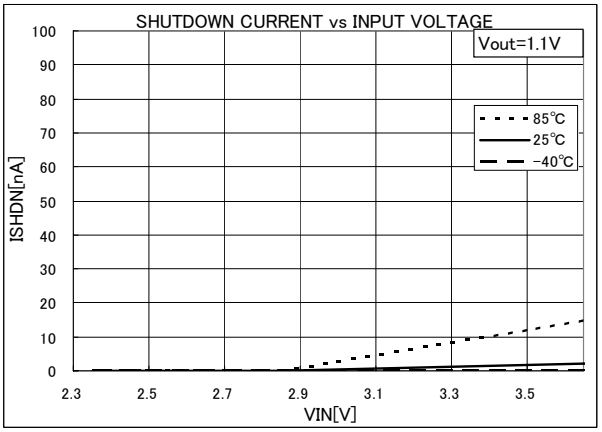

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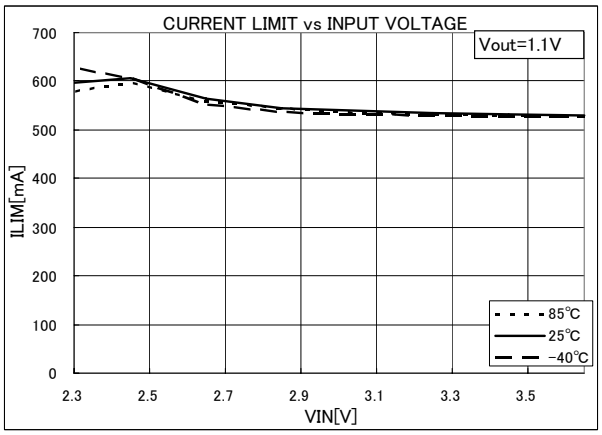

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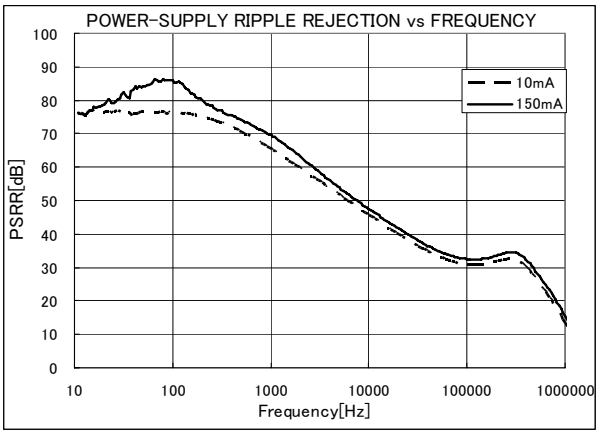

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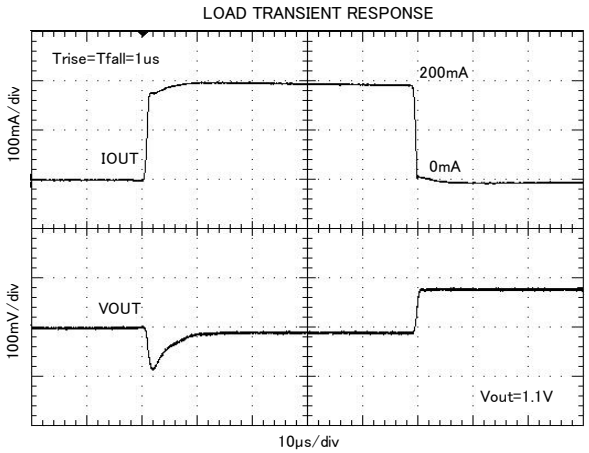

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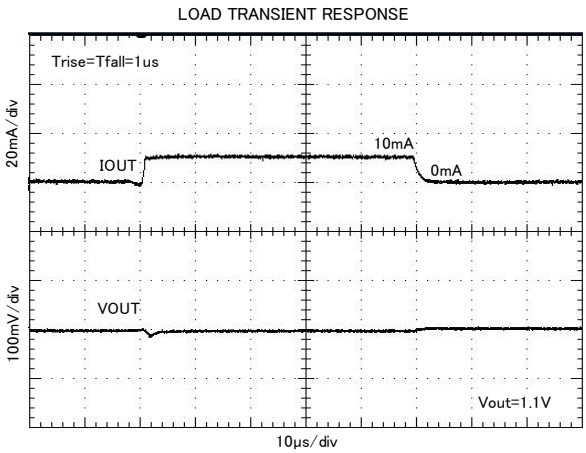

Figure 34.

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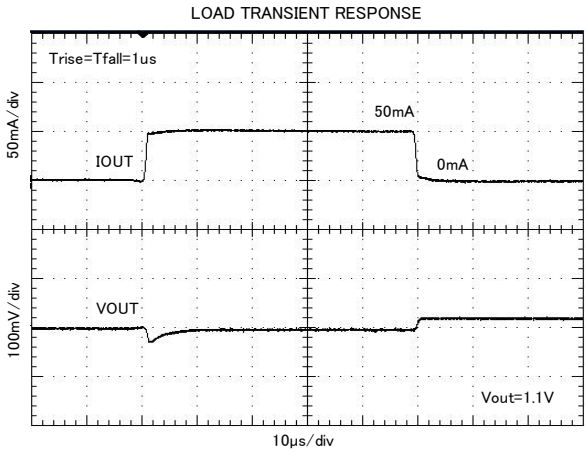
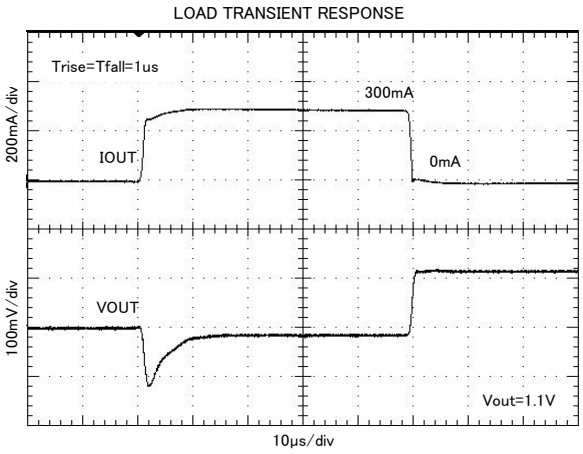


Figure 35.



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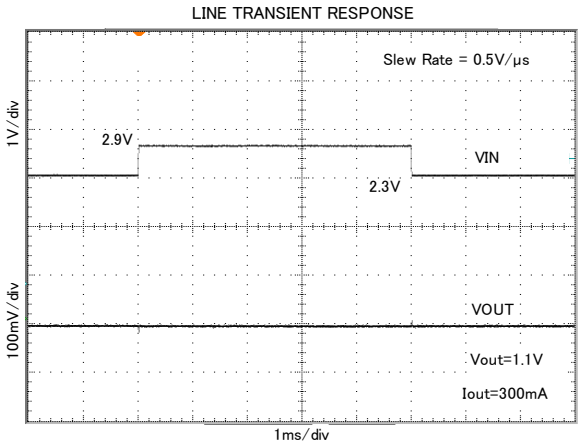

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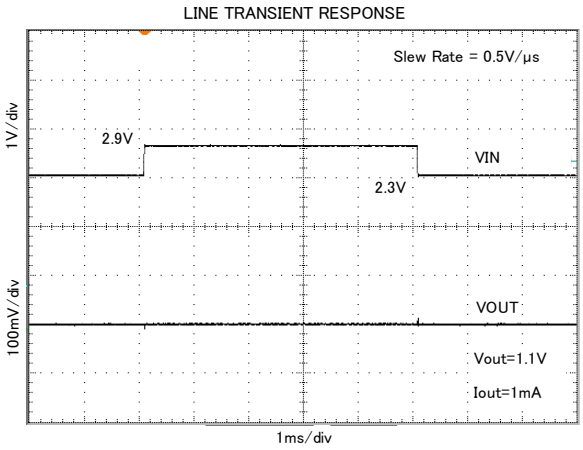
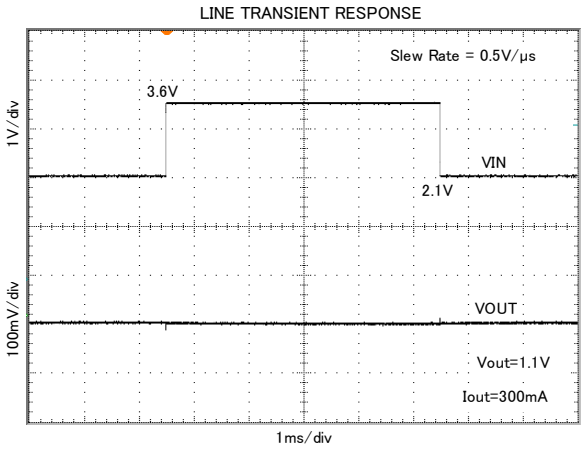


Figure 38.



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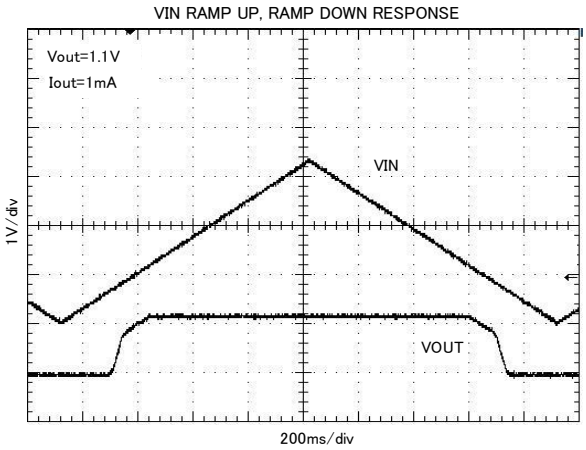
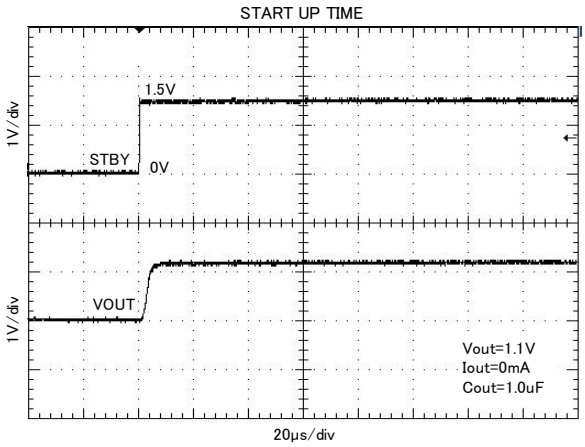


Figure 40.

● **Reference data** **BU11UC3WG** (Ta=25ºC unless otherwise specified.)



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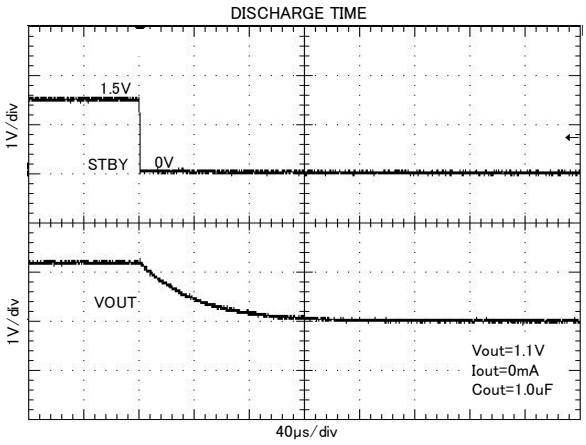

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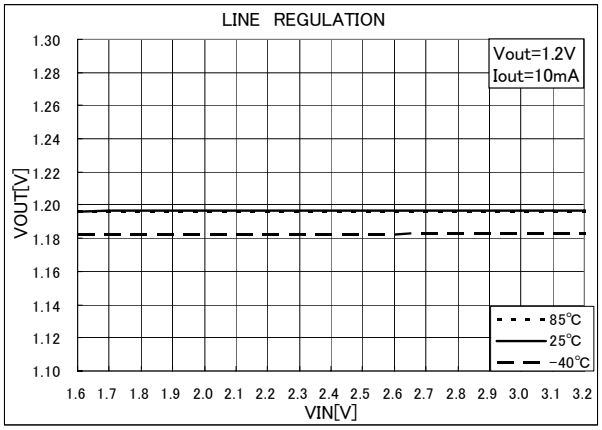

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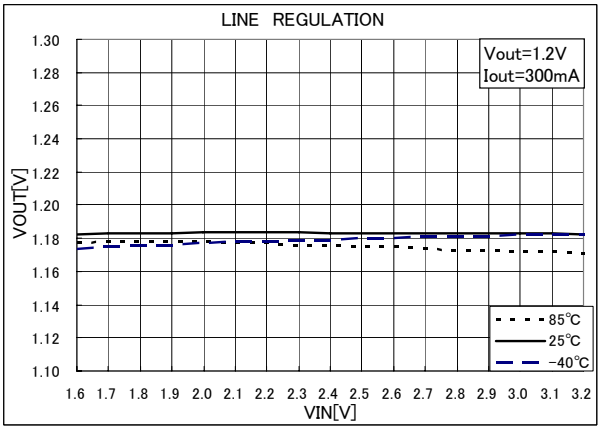

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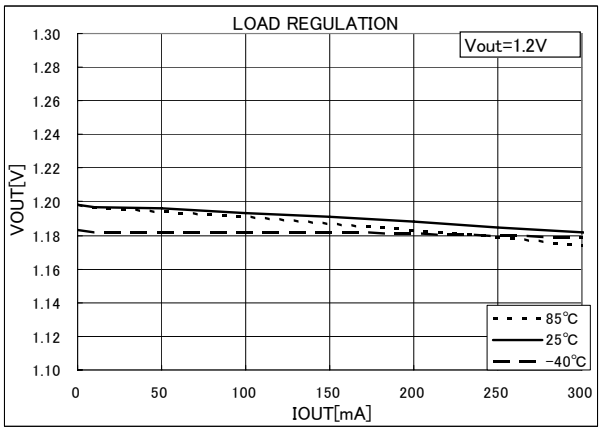

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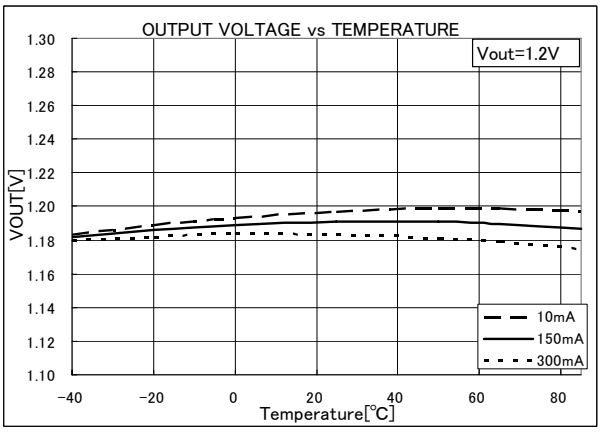

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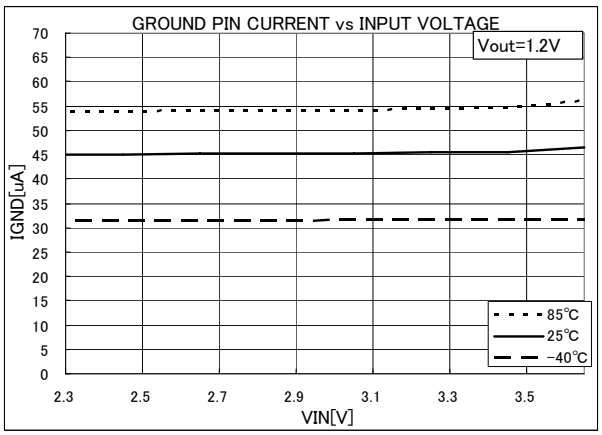
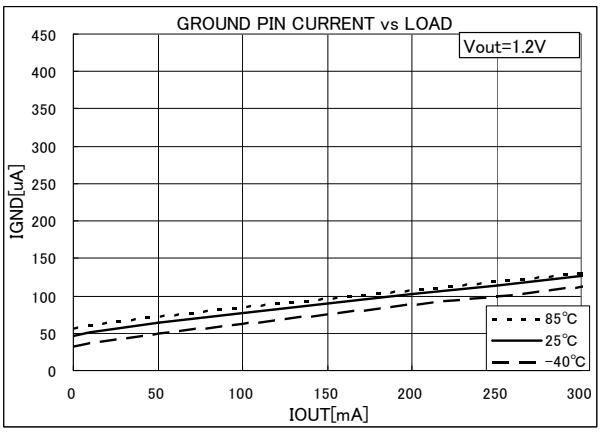


Figure 47.



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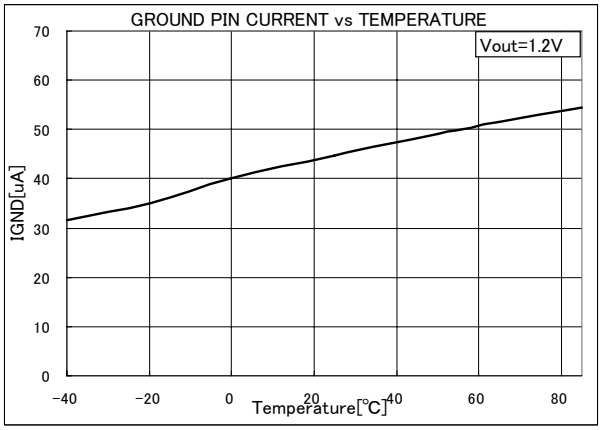

Figure 49.

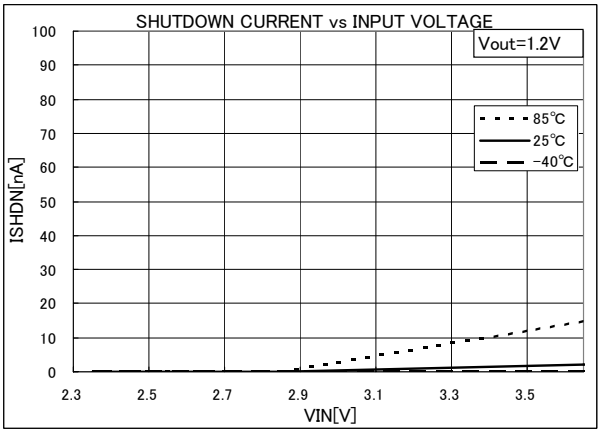

Figure 50.

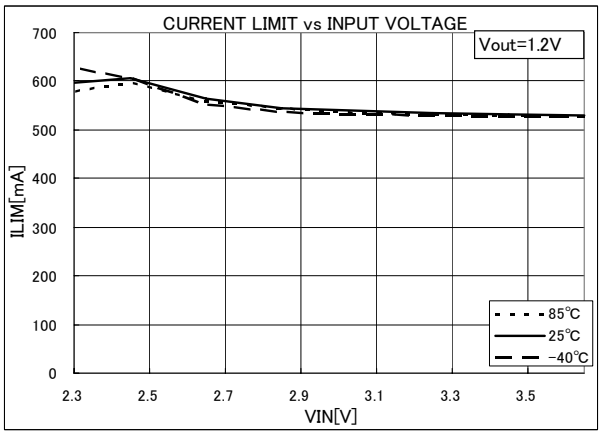

Figure 51.

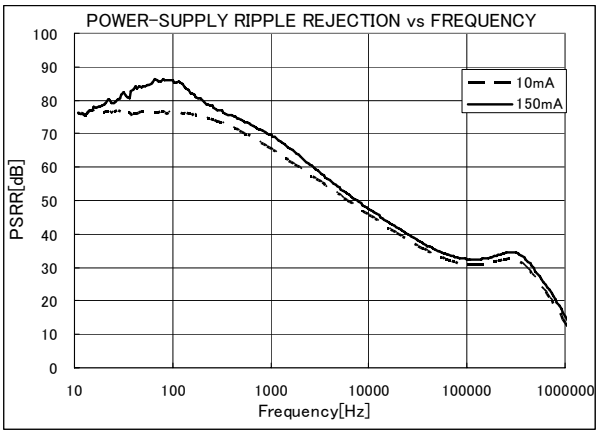

Figure 52.

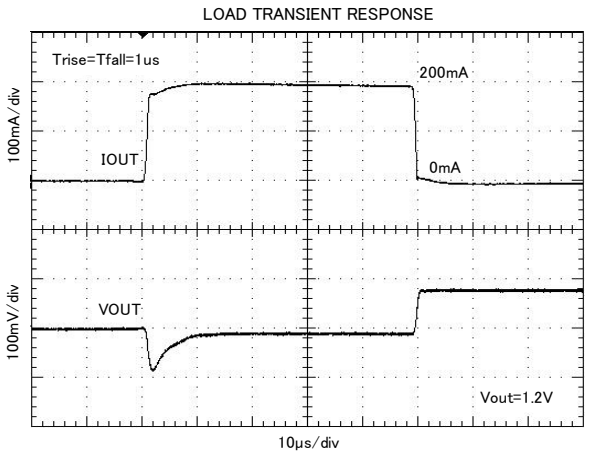

Figure 53.

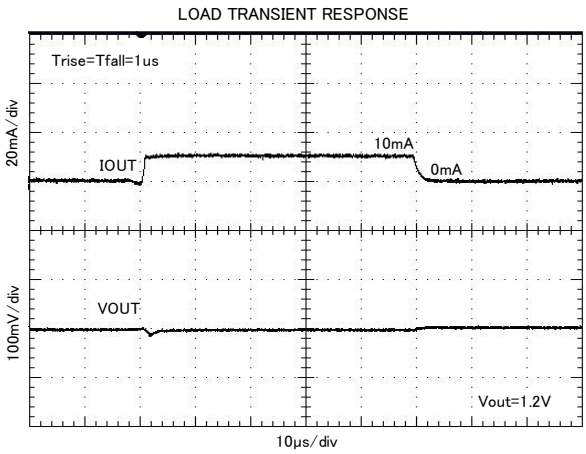

Figure 54.

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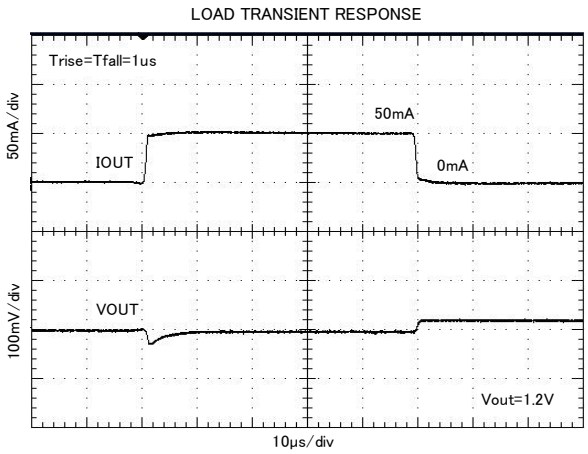

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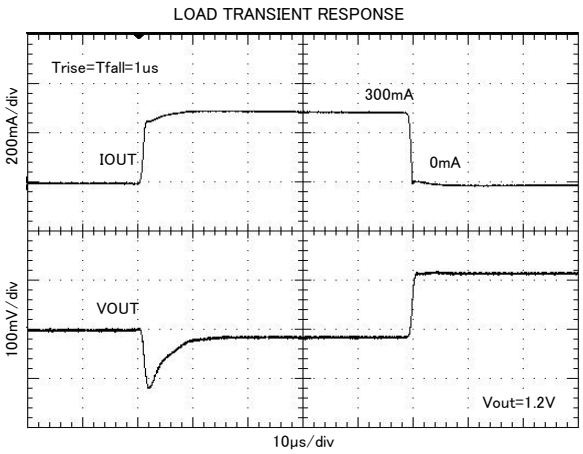
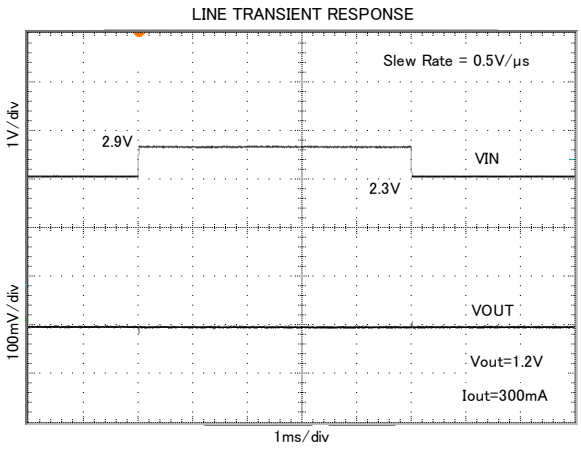


Figure 56.



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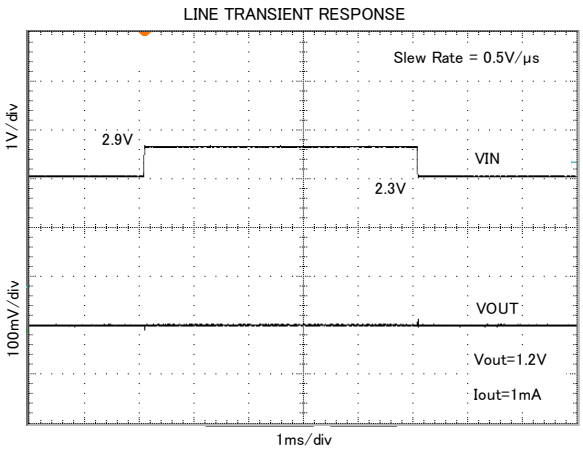
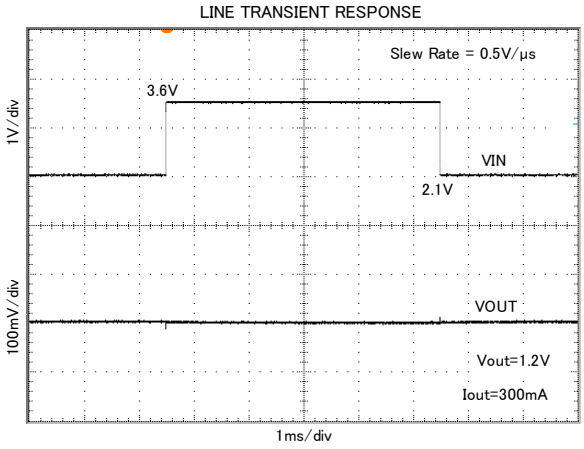


Figure 58.



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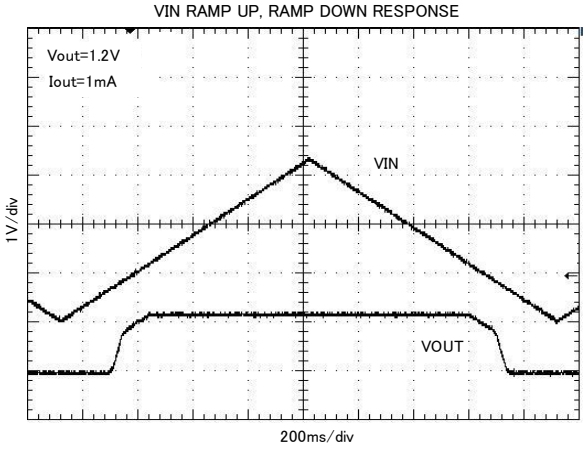

Figure 60.

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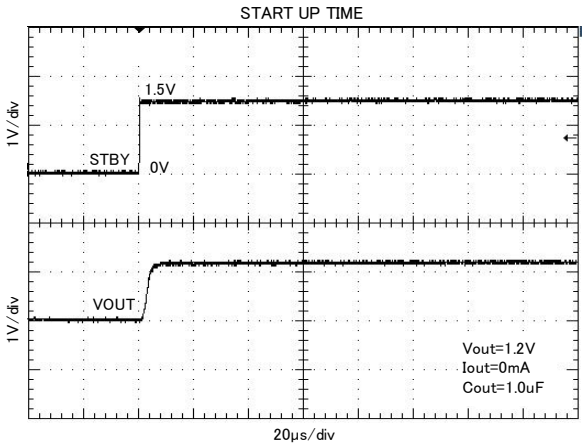

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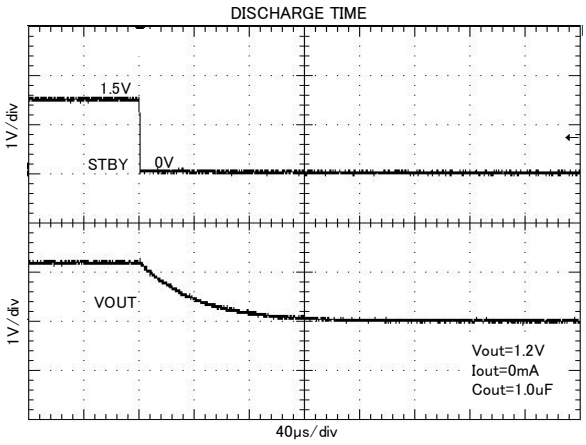


Figure 62.

● **Reference data** **BU18UC3WG** (Ta=25ºC unless otherwise specified.)

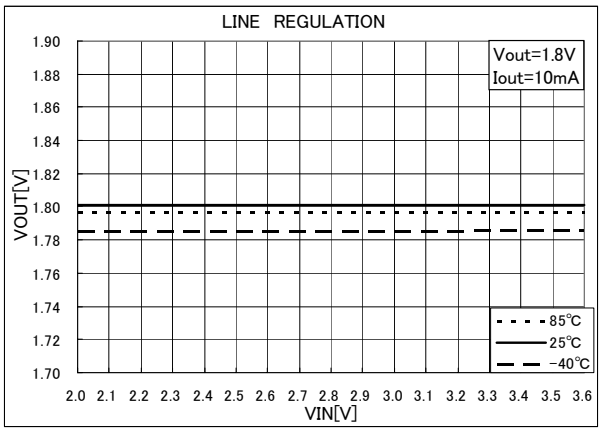


Figure 63.

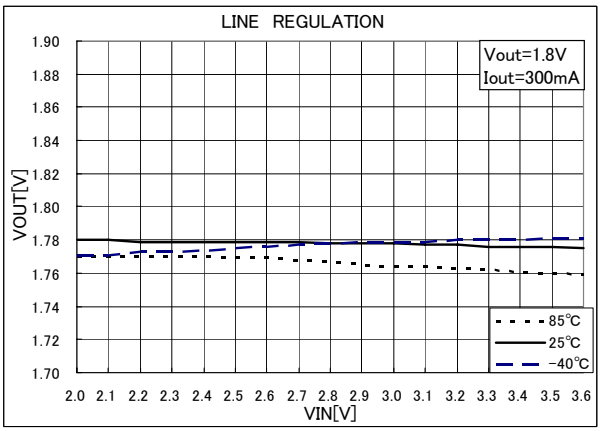


Figure 64.

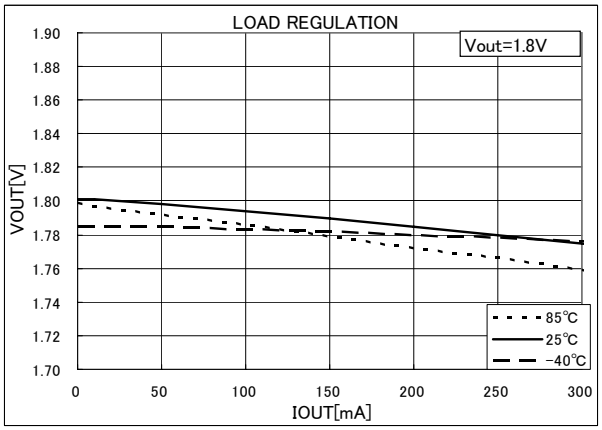


Figure 65.

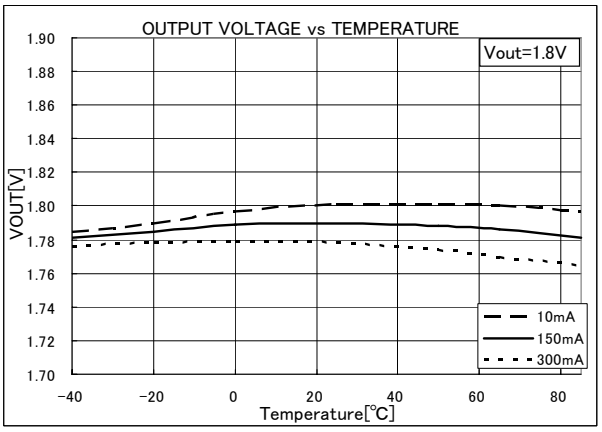
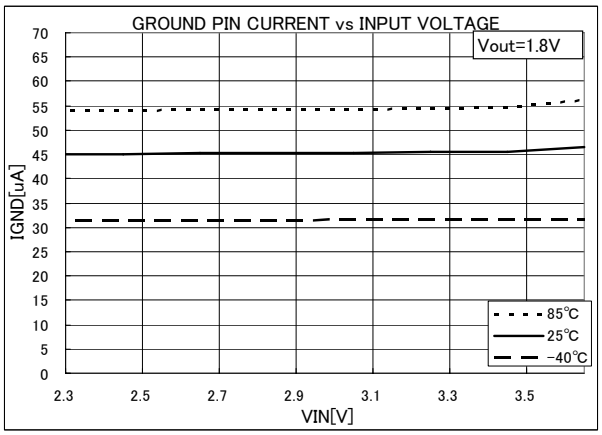


Figure 66.



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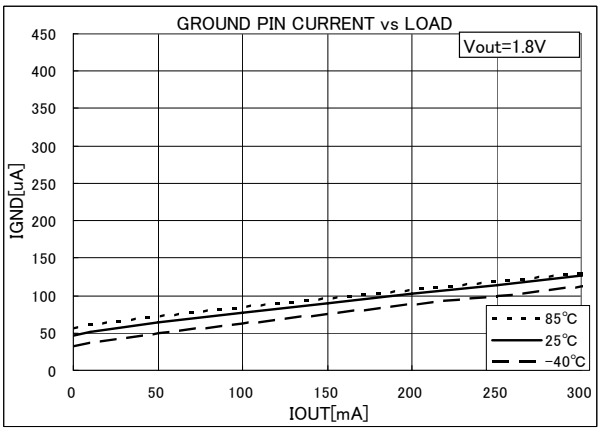


Figure 68.

● **Reference data** **BU18UC3WG** (Ta=25ºC unless otherwise specified.)

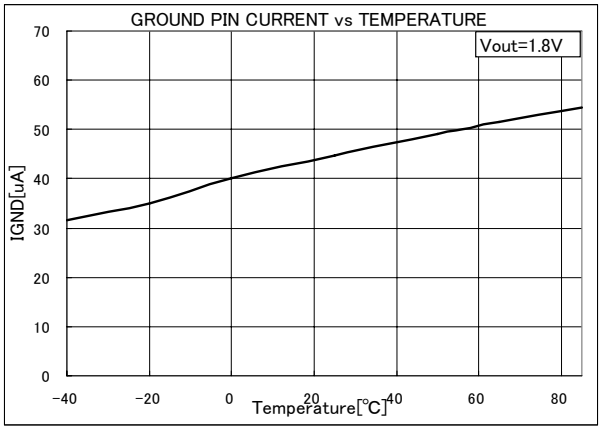


Figure 69.

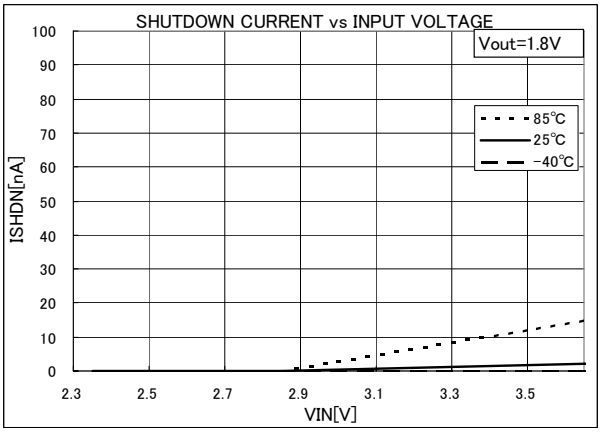


Figure 70.

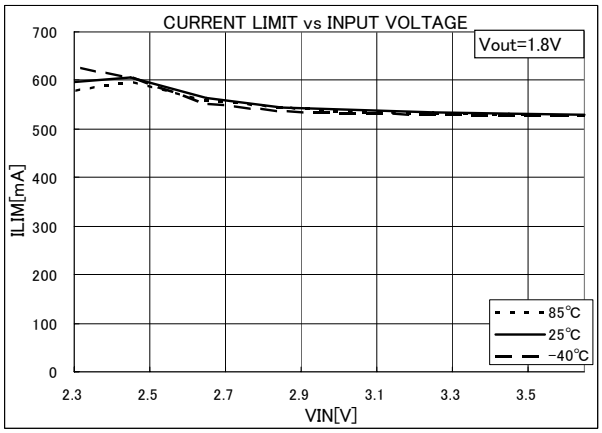


Figure 71.

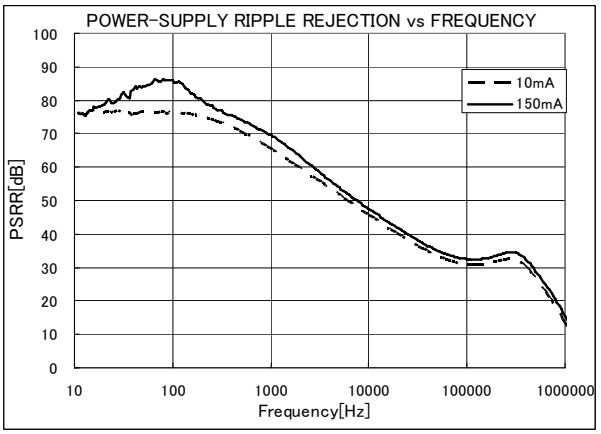
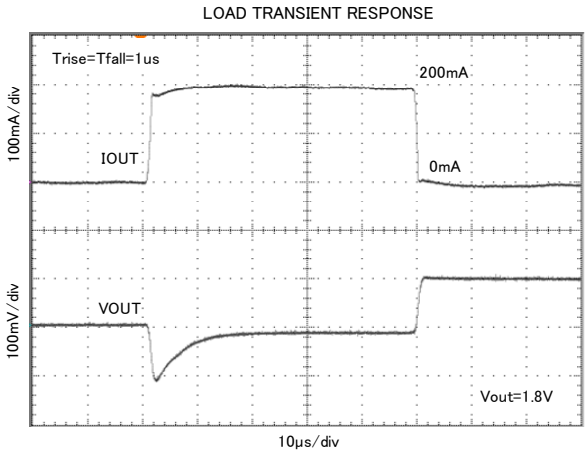


Figure 72.



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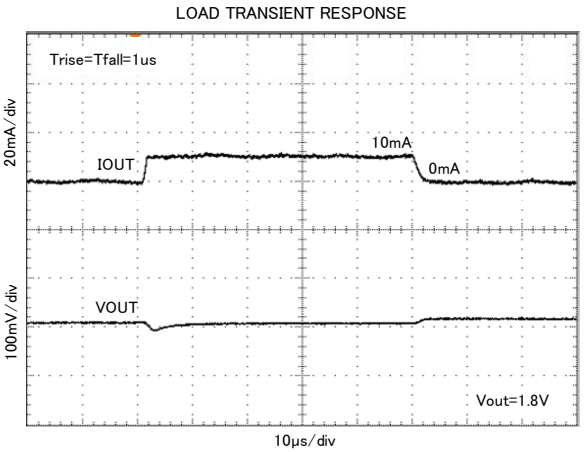


Figure 74.

● **Reference data** **BU18UC3WG** (Ta=25ºC unless otherwise specified.)

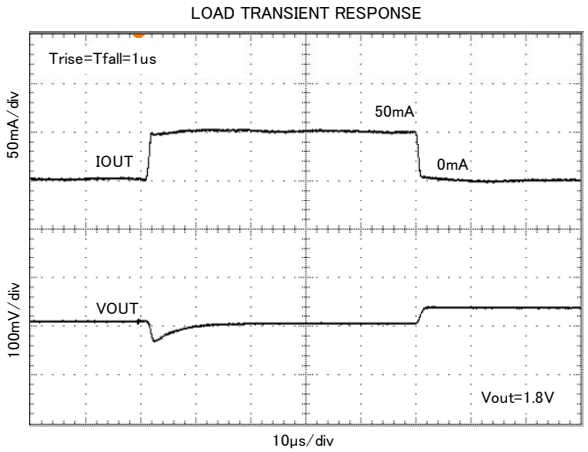
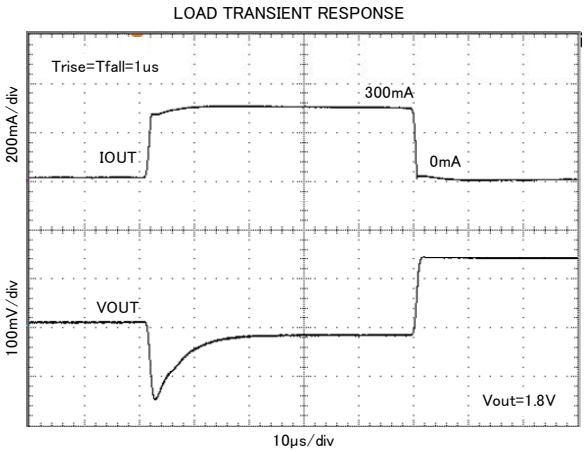


Figure 75.



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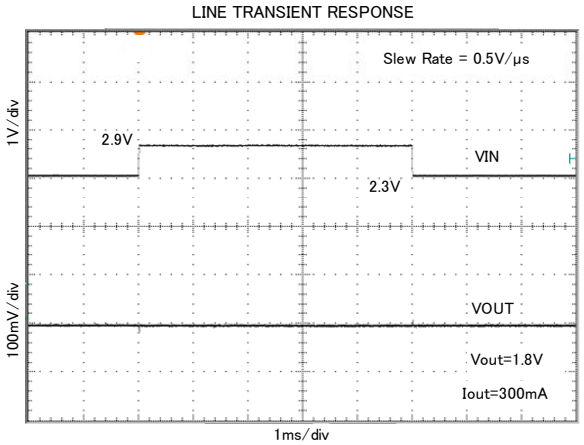

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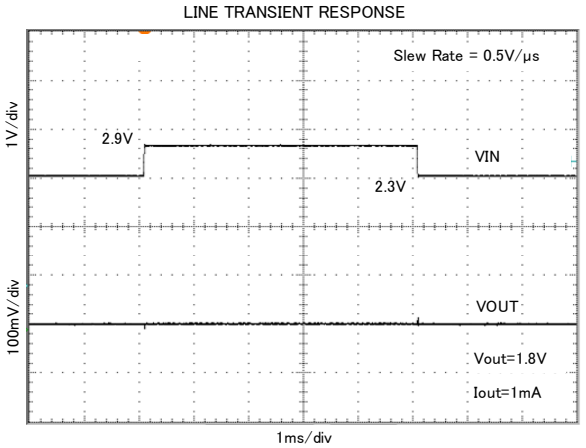

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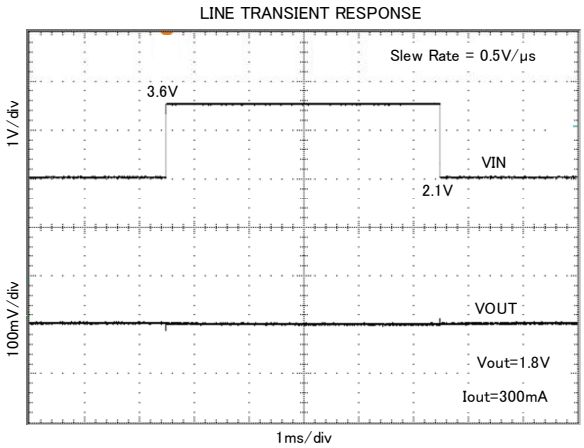


Figure 79.

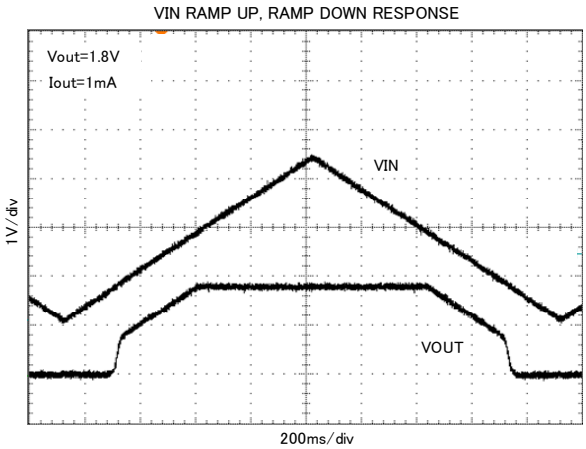


Figure 80.

● **Reference data** **BU18UC3WG** (Ta=25ºC unless otherwise specified.)

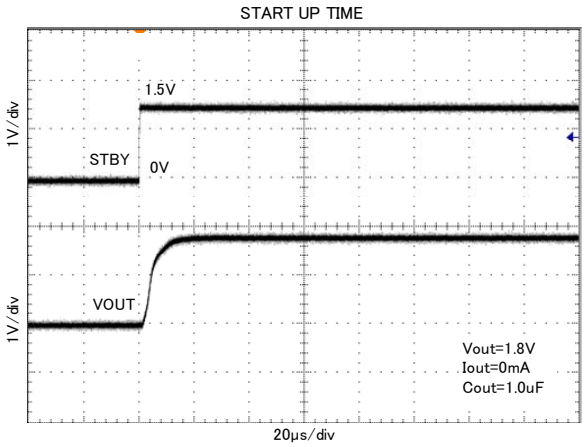


Figure 81.

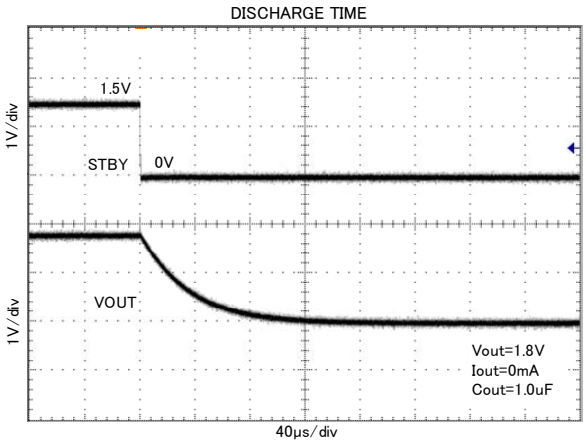


Figure 82.

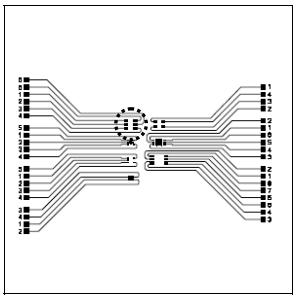
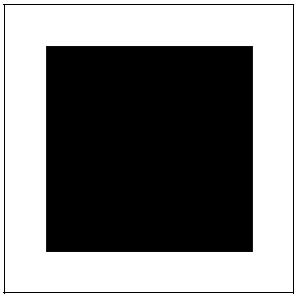
●About power dissipation (Pd)

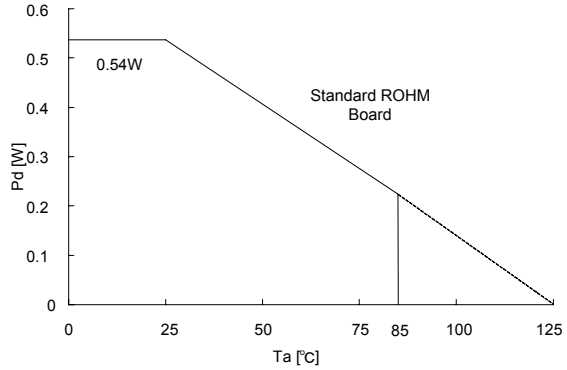
As for power dissipation, an approximate estimate of the heat reduction characteristics and internal power consumption of IC are shown, so please use these for reference. Since power dissipation changes substantially depending on the implementation conditions (board size, board thickness, metal wiring rate, number of layers and through holes, etc.), it is recommended to measure Pd on a set board. Exceeding the power dissipation of IC may lead to deterioration of the original IC performance, such as causing operation of the thermal shutdown circuit or reduction in current capability. Therefore, be sure to prepare sufficient margin within power dissipation for usage.

Calculation of the maximum internal power consumption of IC (PMAX)

PMAX=(VIN-VOUT)×IOUT(MAX.) (VIN： Input voltage VOUT： Output voltage IOUT(MAX)： Maximum output current)

○ Measurement conditions

		Standard ROHM Board
Layout of Board for Measurement IC Implementation Position		 Top Layer (Top View)  Bottom Layer (Top View)
Measurement State		With board implemented (Wind speed 0 m/s)
Board Material		Glass epoxy resin (Double-side board)
Board Size		70 mm x 70 mm x 1.6 mm
Wiring Rate	Top layer	Metal (GND) wiring rate: Approx. 0%
	Bottom layer	Metal (GND) wiring rate: Approx. 50%
Through Hole		Diameter 0.5mm x 6 holes
Power Dissipation		0.54W
Thermal Resistance		θja=185.2°C/W



* Please design the margin so that PMAX becomes is than Pd (PMAX<Pd) within the usage temperature range

Figure 83. SSOP5 Power dissipation heat reduction characteristics (Reference)

●**Operation Notes**

1.) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

2.) GND potential

The potential of the GND pin must be the minimum potential in the system in all operating conditions.
Never connect a potential lower than GND to any pin, even if only transiently.

3.) Thermal design

Use a thermal design that allows for a sufficient margin for that package power dissipation rating (Pd) under actual operating conditions.

4.) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting or shorts between pins may result in damage to the IC.

5.) Operation in strong electromagnetic fields

Strong electromagnetic fields may cause the IC to malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.

6.) Common impedance

Wiring traces should be as short and wide as possible to minimize common impedance. Bypass capacitors should be use to keep ripple to a minimum.

7.) Voltage of STBY pin

To enable standby mode for all channels, set the STBY pin to 0.3 V or less, and for normal operation, to 1.2 V or more. Setting STBY to a voltage between 0.3 and 1.2 V may cause malfunction and should be avoided. Keep transition time between high and low (or vice versa) to a minimum.

Additionally, if STBY is shorted to VIN, the IC will switch to standby mode and disable the output discharge circuit, causing a temporary voltage to remain on the output pin. If the IC is switched on again while this voltage is present, overshoot may occur on the output. Therefore, in applications where these pins are shorted, the output should always be completely discharged before turning the IC on.

8.) Over-current protection circuit (OCP)

This IC features an integrated over-current and short-protection circuitry on the output to prevent destruction of the IC when the output is shorted. The OCP circuitry is designed only to protect the IC from irregular conditions (such as motor output shorts) and is not designed to be used as an active security device for the application. Therefore, applications should not be designed under the assumption that this circuitry will engage.

9.) Thermal shutdown circuit (TSD)

This IC also features a thermal shutdown circuit that is designed to turn the output off when the junction temperature of the IC exceeds about 150℃. This feature is intended to protect the IC only in the event of thermal overload and is not designed to guarantee operation or act as an active security device for the application. Therefore, applications should not be designed under the assumption that this circuitry will engage.

10.) Input/output capacitor

Capacitors must be connected between the input/output pins and GND for stable operation, and should be physically mounted as close to the IC pins as possible. The input capacitor helps to counteract increases in power supply impedance, and increases stability in applications with long or winding power supply traces. The output capacitance value is directly related to the overall stability and transient response of the regulator, and should be set to the largest possible value for the application to increase these characteristics. During design, keep in mind that in general, ceramic capacitors have a wide range of tolerances, temperature coefficients and DC bias characteristics, and that their capacitance values tend to decrease over time. Confirm these details before choosing appropriate capacitors for your application.(Please refer the technical note, regarding ceramic capacitor of recommendation)

11.) About the equivalent series resistance (ESR) of a ceramic capacitor

Capacitors generally have ESR (equivalent series resistance) and it operates stably in the ESR-IOUT area shown on the right. Since ceramic capacitors, tantalum capacitors, electrolytic capacitors, etc. generally have different ESR, please check the ESR of the capacitor to be used and use it within the stability area range shown in the right graph for evaluation of the actual application.

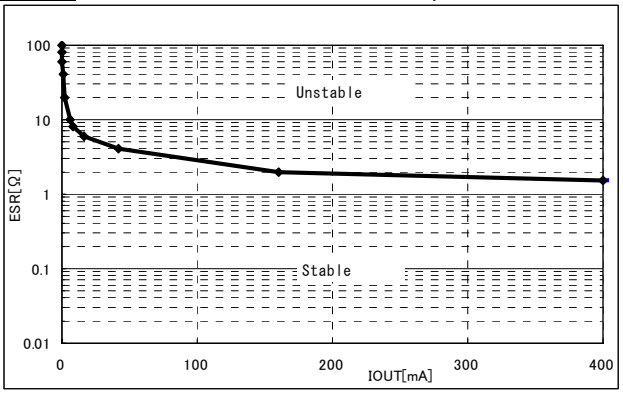


Figure 84. Stable region (example)

●**Revision History**

Date	Revision	Changes
27.Jun.2013	001	New Release
02.Jul.2013	002	Absolute Maximum Ratings of Power Supply Voltage is changed. Adding reference data.