

# Triacs logic level

## BT136 series D

### GENERAL DESCRIPTION

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

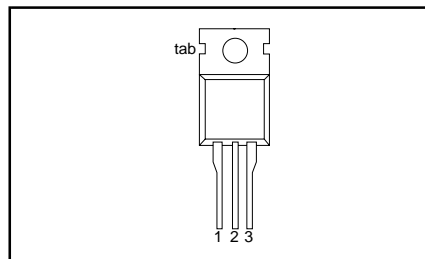
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DRM}$	Repetitive peak off-state voltages	<b>600D</b> 600	V
$I_{T(RMS)}$	RMS on-state current	4	A
$I_{TSM}$	Non-repetitive peak on-state current	25	A

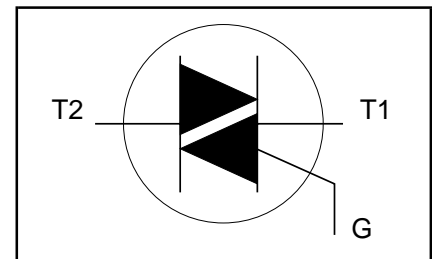
### PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

### PIN CONFIGURATION



### SYMBOL



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DRM}$	Repetitive peak off-state voltages		-	<b>-600D</b> 600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107^\circ\text{C}$	-	4	A
$I_{TSM}$	Non-repetitive peak on-state current	full sine wave; $T_j = 25^\circ\text{C}$ prior to surge $t = 20\text{ ms}$	-	25	A
		$t = 16.7\text{ ms}$	-	27	A
		$t = 10\text{ ms}$	-	3.1	A <sup>2</sup> s
$I^2t$	$I^2t$ for fusing		-		
$dl_t/dt$	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 6\text{ A}$ ; $I_G = 0.2\text{ A}$ ; $dl_G/dt = 0.2\text{ A}/\mu\text{s}$			
		T2+ G+	-	50	A/ $\mu\text{s}$
		T2+ G-	-	50	A/ $\mu\text{s}$
		T2- G-	-	50	A/ $\mu\text{s}$
		T2- G+	-	10	A/ $\mu\text{s}$
$I_{GM}$	Peak gate current		-	2	A
$V_{GM}$	Peak gate voltage		-	5	V
$P_{GM}$	Peak gate power		-	5	W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5	W
$T_{stg}$	Storage temperature		-40	150	$^\circ\text{C}$
$T_j$	Operating junction temperature		-	125	$^\circ\text{C}$

### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

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### STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
$I_{GT}$	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	T2+ G+	-	2.0	5	mA
			T2+ G-	-	2.5	5	mA
			T2- G-	-	2.5	5	mA
			T2- G+	-	5.0	10	mA
$I_L$	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	T2+ G+	-	1.6	10	mA
			T2+ G-	-	4.5	15	mA
			T2- G-	-	1.2	10	mA
			T2- G+	-	2.2	15	mA
$I_H$	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	1.2	10	mA	
$V_T$	On-state voltage	$I_T = 5\text{ A}$	-	1.4	1.70	V	
$V_{GT}$	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.7	1.5	V	
$I_D$	Off-state leakage current	$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125\text{ °C}$	0.25	0.4	-	V	
		$V_D = V_{DRM(max)}; T_j = 125\text{ °C}$	-	0.1	0.5	mA	

### DYNAMIC CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$dV_D/dt$	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$ exponential waveform; $R_{GK} = 1\text{ k}\Omega$	-	5	-	V/ $\mu$ s
$t_{gt}$	Gate controlled turn-on time	$I_{TM} = 6\text{ A}; V_D = V_{DRM(max)}; I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	$\mu$ s

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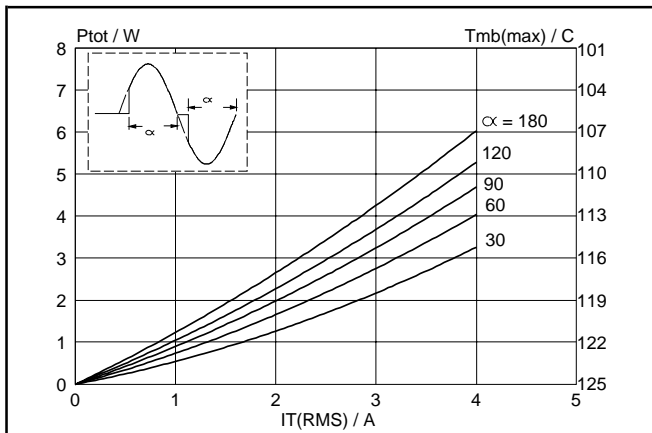


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , versus rms on-state current,  $I_{T(RMS)}$ , where  $\alpha =$  conduction angle.

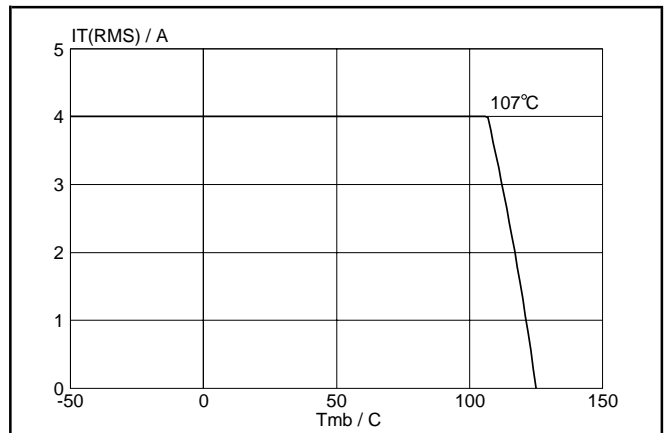


Fig.4. Maximum permissible rms current  $I_{T(RMS)}$ , versus mounting base temperature  $T_{mb}$ .

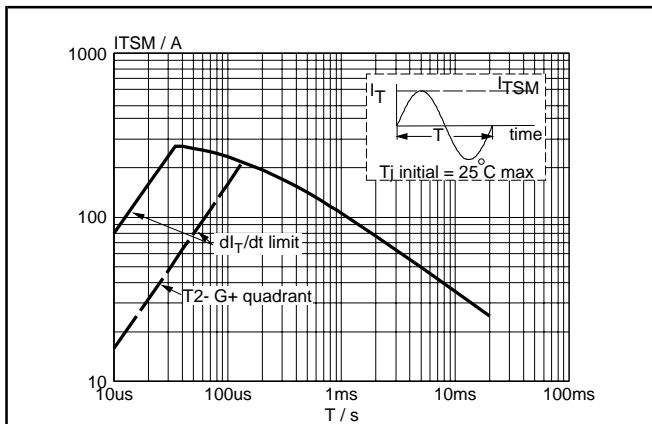


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 20\text{ms}$ .

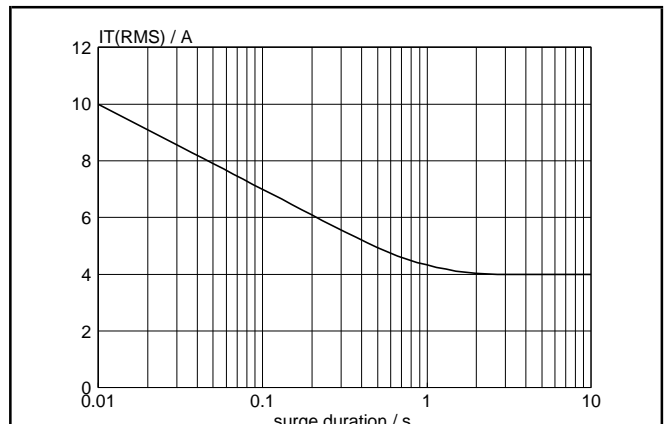


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50\text{ Hz}$ ;  $T_{mb} \leq 107^\circ\text{C}$ .

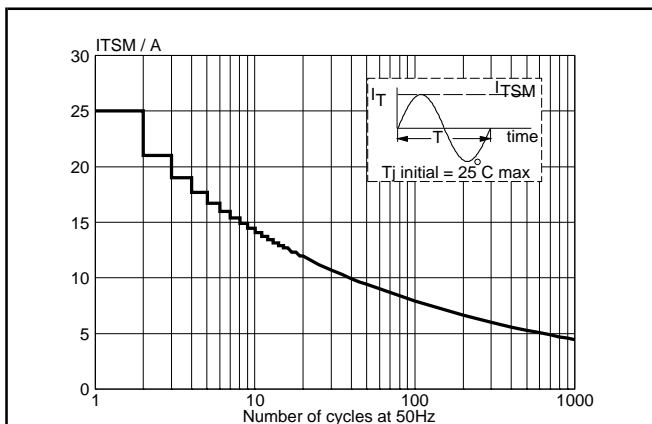


Fig.3. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50\text{ Hz}$ .

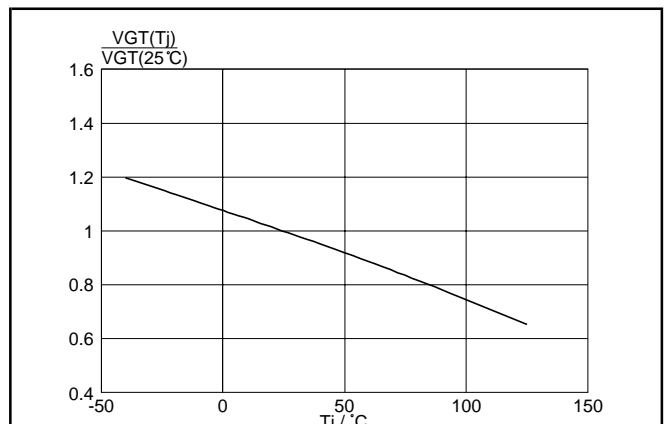
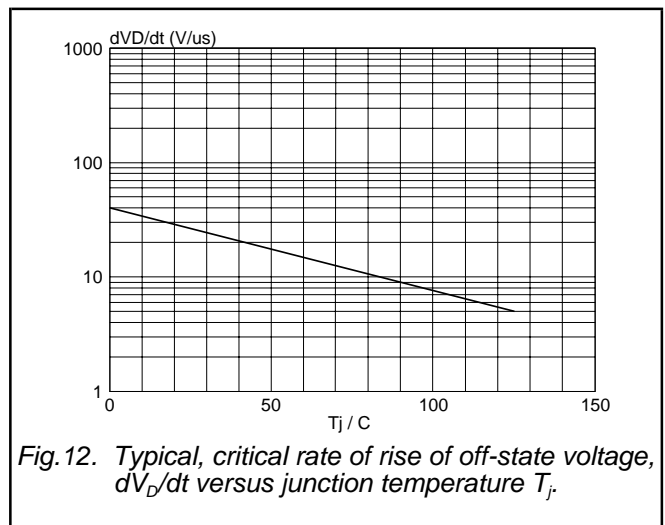
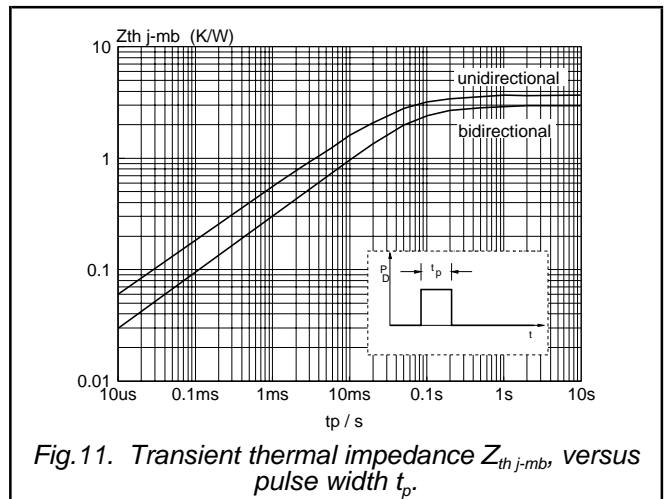
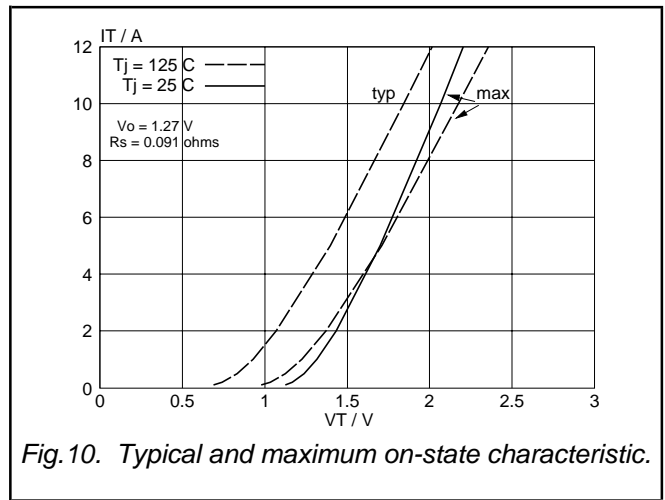
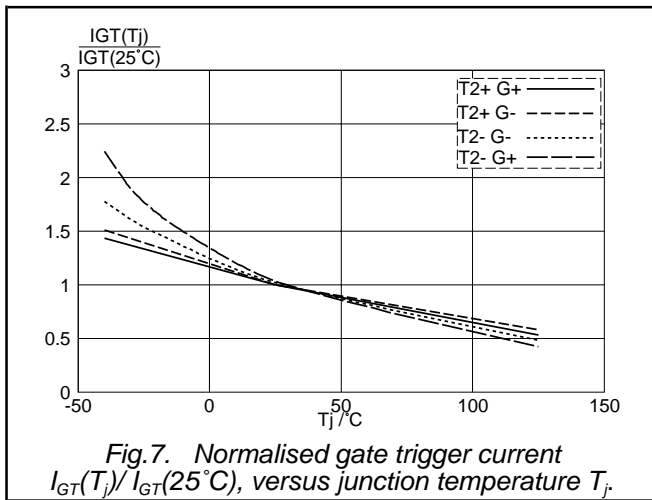


Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

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**MECHANICAL DATA**



**Notes**

1. Refer to mounting instructions for SOT78 (TO220) envelopes.
2. Epoxy meets UL94 V0 at 1/8".

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## DEFINITIONS

<b>DATA SHEET STATUS</b>		
<b>DATA SHEET STATUS<sup>1</sup></b>	<b>PRODUCT STATUS<sup>2</sup></b>	<b>DEFINITIONS</b>
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A
<b>Limiting values</b>		
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
<b>Application information</b>		
Where application information is given, it is advisory and does not form part of the specification.		
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