AC/DC Drivers

AC/DC Controller IC for LED Lighting Included 650V MOSFET

BM520Q19F

●Description

The quasi-resonant controller typed LED driver IC BM520Q19F for AC/DC can be applied to a non-isolated application, and make the designs for various types of low power convertor easily.

Owing to the start-up circuit with 650V withstand voltage, the low power consumption and high-speed start are achieved.

Owing to the quasi-resonant mode, the soft switching is achieved, and by the alterable operating frequency, the EMI is also improved. And owing to the external current setting resistance, a power supply design with a high degree of freedom can be achieved.

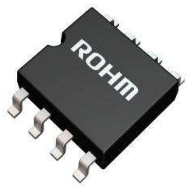
With the built-in MOSFET with 650V withstand voltage, a low-cost application can be achieved, and it makes the application design easily.

●Features

- Quasi-resonant switching mode
- Built-in 650V starter circuit
- Built-in 650V switching MOSFET
- Maximum frequency 200kHz
- VCC pin: under voltage protection
- VCC pin: over voltage protection (latch)
- SOURCE pin: Leading-Edge-Blanking function
- ZT pin: trigger mask function
- ZT pin: over voltage protection (latch)
- NTC pin: temperature detecting protection (automatic recovery)

●Package

SOP8	5.00mm × 4.40mm (Typ.)	(Typ.)	pitch 1.27mm (Typ.)



●Key Specifications

■Operating power supply voltage range:

VCC 8.9V to 26.0V DRAIN: ～650V

■Operating current: Normal operation: 0.35mA (Typ.)

■Operating temperature range: - 40deg. to +105deg.

■MOSFET ON resistance: 8.5Ω (Typ.)

●Application

LED bulb, sealed-type LED lighting

Electrical machineries for LED lighting

●Application Circuit

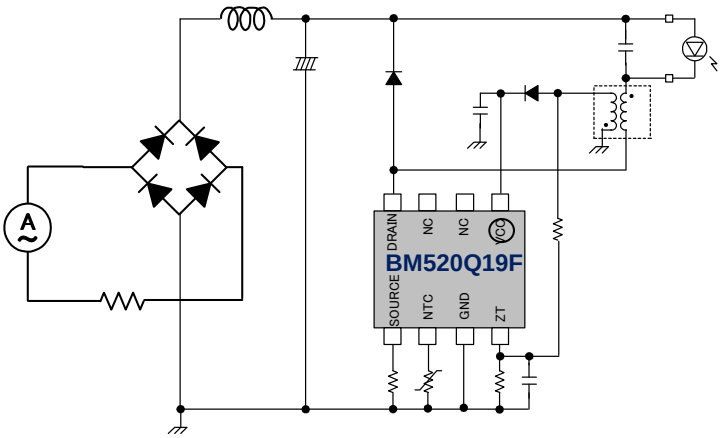


Figure 1. Application circuit

●**Absolute Maximum Ratings（Ta=25℃）**

Item	Symbol	Rating	Unit	Condition
Input voltage range 1	Vmax1	-0.3～30	V	VCC
Input voltage range 2	Vmax2	-0.3～6.5	V	SOURCE, NTC, ZT
Input voltage range 3	Vmax3	650	V	DRAIN
Drain current pulse	I_{DP}	2.60	A	P_W=10us, Duty cycle=1%
Maximum power dissipation	Pd	563 (Note1)	mW	
Operating temperature range	Topr	-40 ～ +105	°C	
Maximum junction temperature	Tjmax	150	°C	
Storage temperature range	Tstr	-55 ～ +150	°C	

(Note1) When mounted (on 70 mm × 70 mm, 1.6 mm thick, glass epoxy on single-layer substrate). Reduce to 4.563 mW/°C when Ta = 25°C or above.

●**Operating Conditions（Ta=25℃）**

Item	Symbol	Rating	Unit	Condition
Input voltage range 1	VCC	8.9～26.0	V	VCC voltage
Input voltage range 2	V_{DRAIN}	～650	V	DRAIN voltage

●**Electrical Characteristics（Ta=25℃）**

MOSFET（Unless otherwise specified, Ta = 25°C, VCC = 15 V）

Item	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
Drain-Source breakdown voltage	$V_{(BR)DDS}$	650	-	-	V	ID=1mA / VGS=0V
Drain leakage current	I_{DSS}	-	-	100	uA	VDS=650V / VGS=0V
ON resistance	$R_{DS(ON)}$	-	8.5	12.0	Ω	ID=0.25A / VGS=10V

●**Electrical Characteristics**

IC（Unless otherwise specified, Ta = 25°C, VCC = 15 V）

Item	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
[Circuit current]						
Circuit current (ON)1	I_{ON1}	120	250	600	μA	NTC=2.0V(PULSE operating) BM520Q15F
Circuit current (ON)2	I_{ON2}	-	220	400	μA	NTC=0V(PULSE OFF)
[VH pin start up circuit]						
VH starting current 1	I_{START1}	0.20	0.55	0.90	mA	VCC= 0V
VH starting current 2	I_{START2}	1	3	6	mA	VCC=10V
VH OFF current	I_{START3}	-	10	20	uA	VCC UVLO released
						VH pin sink current
VH starting current switching voltage	V_{SC}	0.3	0.7	1.6	V	VCC pin
[VCC pin protection]						
VCC UVLO voltage 1	V_{UVLO1}	12.5	13.5	14.5	V	VCC rising up
VCC UVLO voltage 2	V_{UVLO2}	7.5	8.2	8.9	V	VCC falling down
VCC UVLO hysteresis	V_{UVLO3}	-	5.3	-	V	$V_{UVLO3}= V_{UVLO1}- V_{UVLO2}$
VCC OVP trigger voltage	V_{OVP1}	25.0	27.5	30.0	V	VCC rising up
VCC OVP release voltage	V_{OVP2}	21.0	23.5	26.0	V	VCC falling down
Latch released VCC voltage	V_{LATCH2}	-	V_{UVLO2}-0.5	-	V	VCC falling down
VCC recharge start voltage	V_{CHG1}	7.7	8.7	9.7	V	VCC falling down
VCC recharge end voltage	V_{CHG2}	12	13	14	V	VCC rising up
Latch mask time	T_{LATCH}	60	100	140	us	
[DC/DC comparator（turn-on）]						
ZT comparator voltage 1	V_{ZT1}	40	100	160	mV	ZT falling down
ZT comparator voltage 2	V_{ZT2}	120	200	280	mV	ZT rising up
ZT comparator hysteresis	V_{ZTHYS}	-	100	-	mV	$V_{ZTHYS}= V_{ZT1}- V_{ZT2}$
ZT trigger mask time	T_{ZTMASK}	-	0.8	-	us	VZT H->L, for preventing from noise
ZT trigger timeout	T_{ZTOUT}	50	100	150	us	
[DC/DC comparator（turn-off）]						
Current trigger voltage	V_{CS}	0.582	0.600	0.618	V	no AC compensation
Maximum frequency	F_{SW}	175	200	225	KHz	
Leading edge blank time	T_{LEB}	-	0.2	-	us	
Maximum ON time	T_{max}	5	15	25	us	
[DC/DC protection]						
ZT OVP voltage	V_{ZTL}	3.250	3.500	3.750	V	
[NTC pin protection]						
NTC pin source current	I_{NTC}	45	50	55	uA	NTC voltage=1.0V
NTC trigger voltage	V_{NTC}	0.06	0.12	0.18	V	NTC voltage falling down
NTC hysteresis	V_{NTCHYS}	0.04	0.08	0.12	V	NTC voltage rising up

●Pin Configuration

Table 1. I/O PIN functions

NO.	Pin Name	I/O	Function	ESD protection	
				VCC	GND
1	VCC	I/O	Power supply pin	-	○
2	N.C.	-	Non Connection	-	-
3	N.C.	-	Non Connection	-	-
4	DRAIN	I/O	MOSFET DRAIN pin	-	○
5	SOURCE	I	MOSFET DRAIN pin Inductor current sensing pin	-	○
6	NTC	I/O	NTC detect input pin	-	○
7	GND	I/O	GND pin, input pin for feedback signal	○	-
8	ZT	I	Zero current detecting pin	-	○

●I/O Equivalent Circuit Diagram

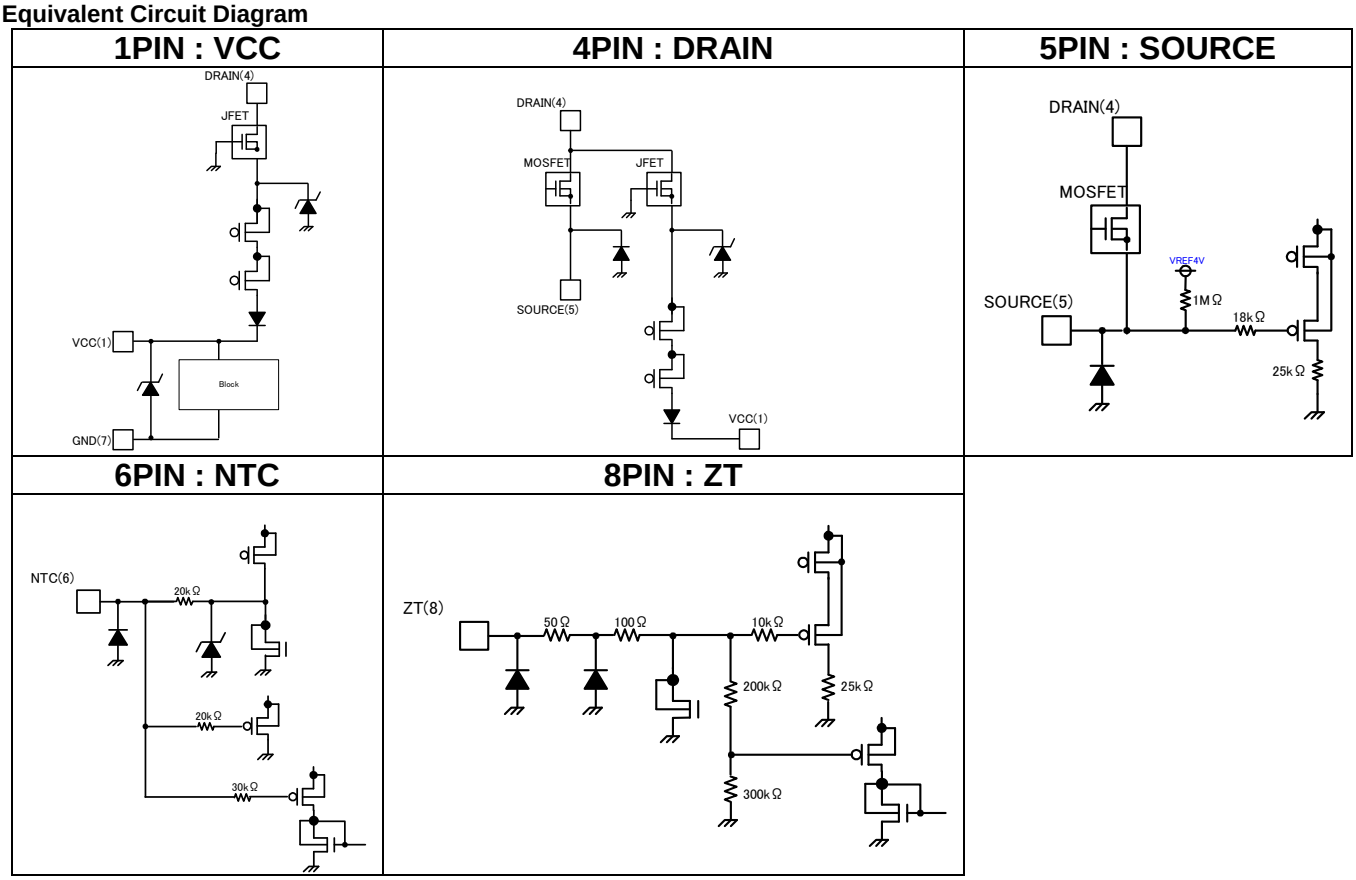


Figure 2. I/O equivalent circuit diagram

●Block Diagram

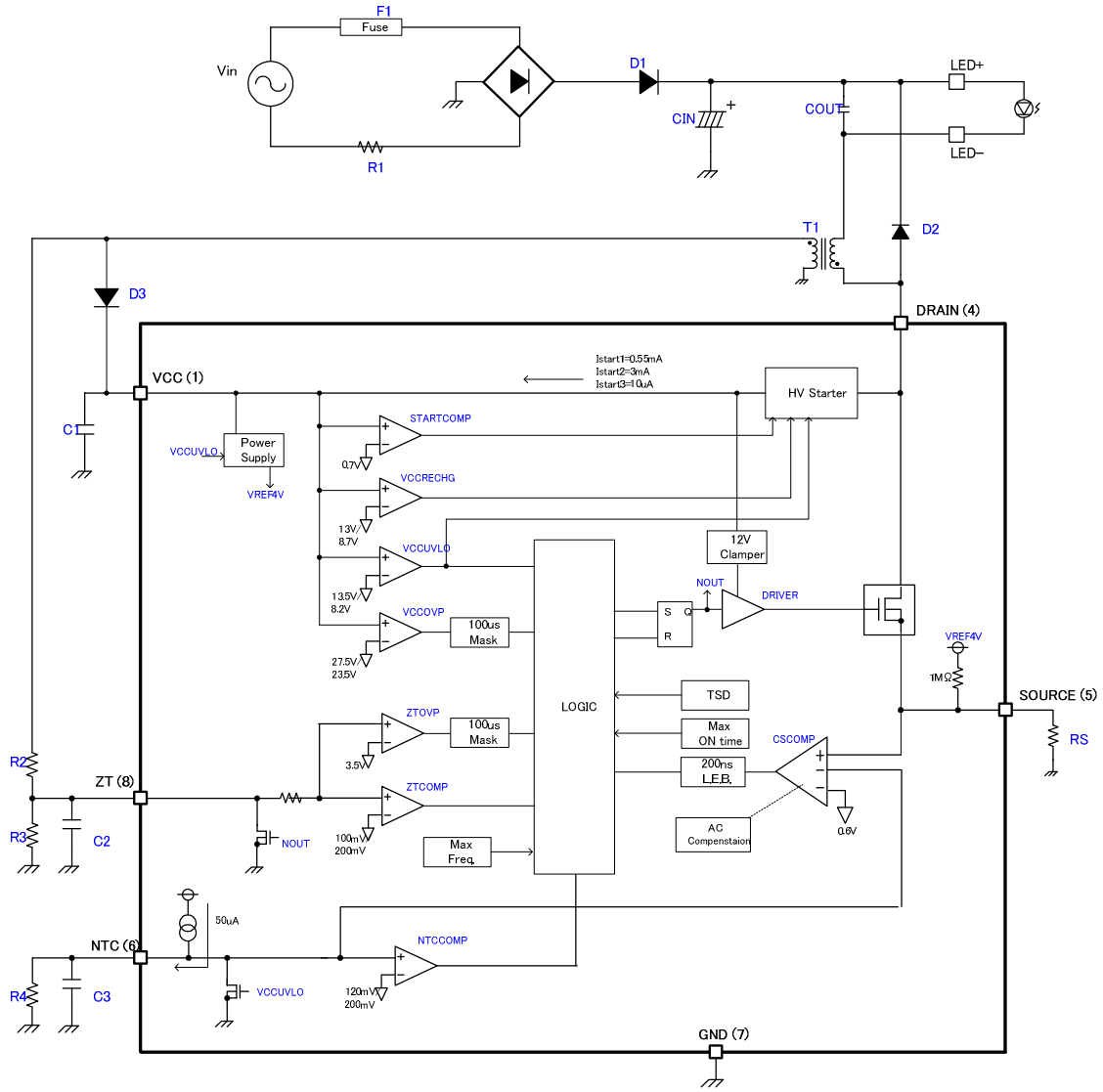


Figure 3. Block diagram

●External Dimensions

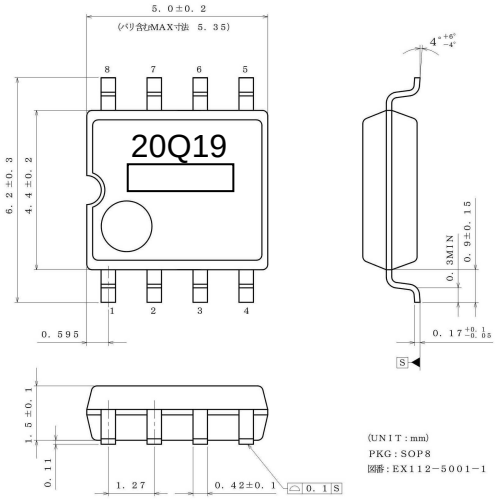


Figure 4. SOP8 package external dimensions

●Block Descriptions

(1) Start-up circuit (DRAIN : 4pin, VCC:1pin)

(1-1)Block Descriptions

A bootstrap circuit with 650V withstand voltage is built in this IC. Owing to this, the low-power standby and high-speed start can be achieved. After the IC was booted up, the power consumption becomes only the idling current（typ=10uA）.The reference value of the start-up time is showed in Figure 7. When C_{VCC}=10uF, the start-up time can be less than 0.1s.

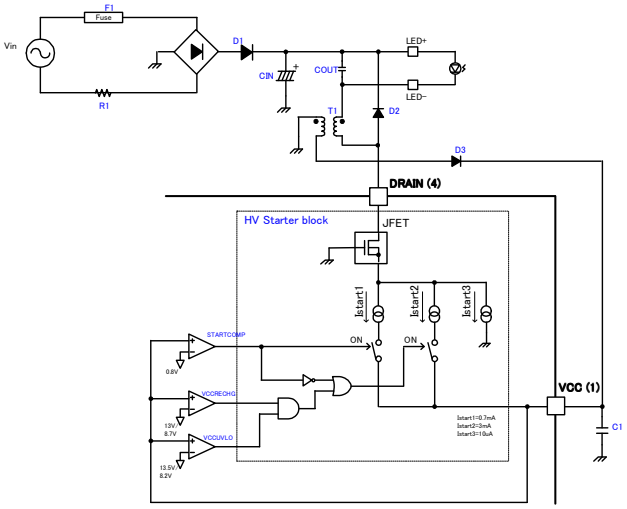


Figure 5. Start-up circuit block diagram

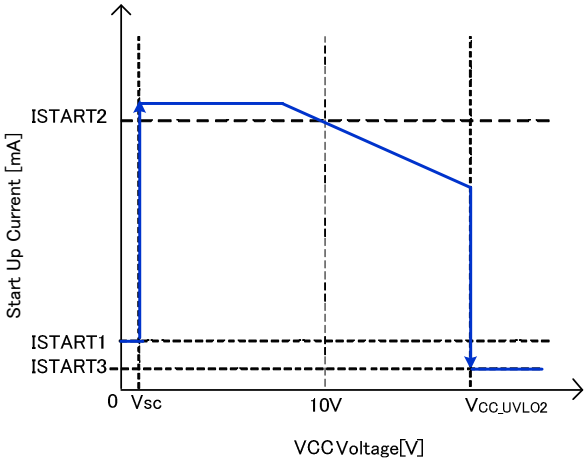


Figure 6. Start-up current－VCC voltage curve

The start-up current means the current from the DRAIN pin.

ex) When Vac=100V, the power consumption of bootstrap circuit is
PVH＝100V*√2*10uA=1.41mW

ex) When Vac=240V, the power consumption of bootstrap circuit is
PVH＝240V*√2*10uA=3.38mW

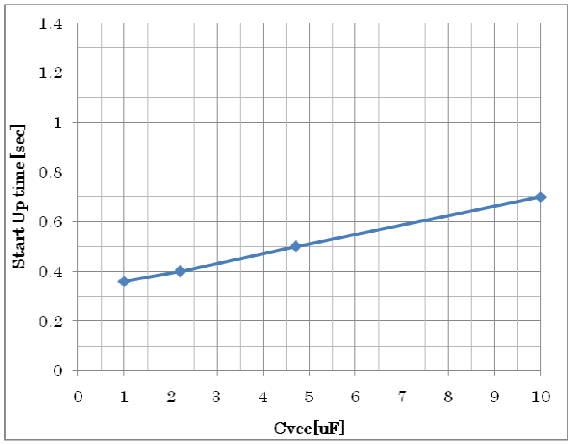


Figure 7. Start-up time－VCC capacitance characteristics

(1-2)Start sequences 1（VCC supply with auxiliary winding）

The time chart of the start sequences are showed in Figure 9. The DC/DC circuit which reduces the power consumption of the IC can be composed by using the auxiliary winding of the transformer.

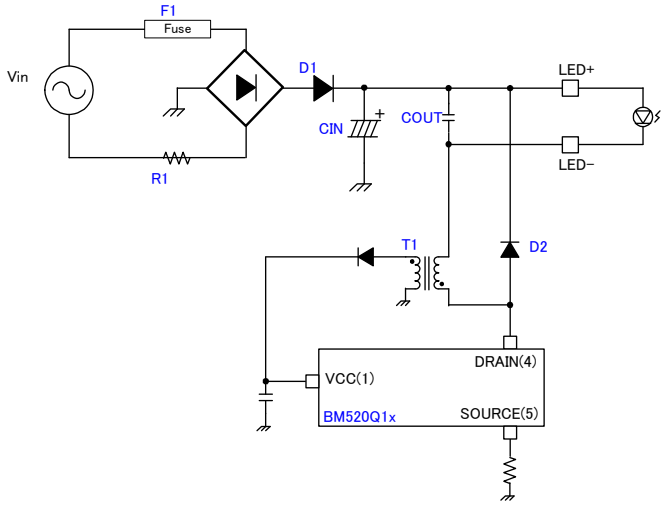


Figure 8. Schematic of the DC/DC Part while Supplying with the Auxiliary Winding

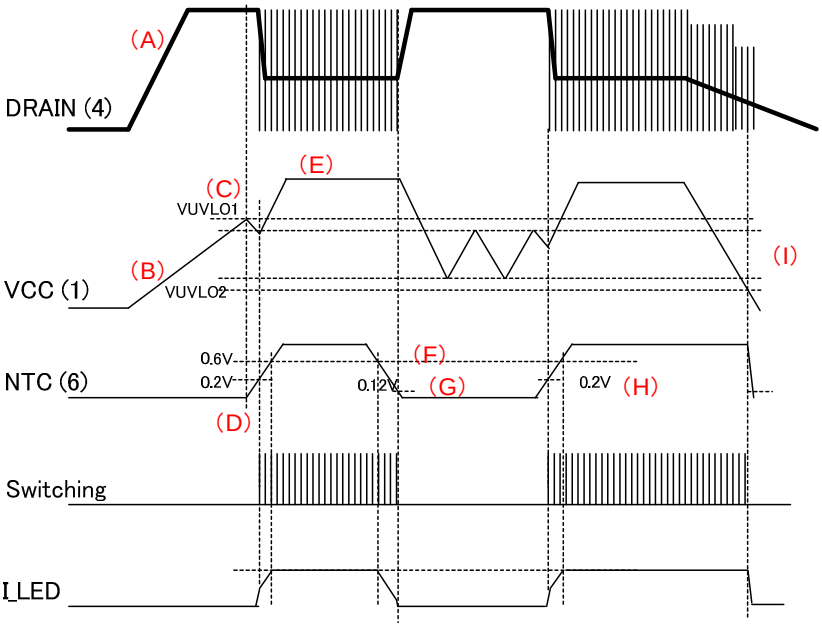


Figure 9. ON/OFF Sequences (supplying VCC with auxiliary winding)

A: Input voltage VH is applied. (Though the LED and the transformer, a high voltage is applied to DRAIN pin from VH.)
B: The capacitor connected to the VCC pin is charged by the start-up current from the DRAIN pin.
C: The IC starts operating when VCC > V_{UVLO1}
D: The soft start is achieved by the voltage rise of the NTC pin.(The switching starts when VNTC>0.2V)
E: The current is supplied to VCC pin from the auxiliary winding by the switching operation.
※The power is supplied by the auxiliary winding, and the VCC voltage is determined by the specification of transformer.
F: While the voltage of NTC pin is falling down, the LED current decreases from VNTC<0.6V.
G: The switching operation stops when V_{NTC}<0.1V. The current supply to VCC pin disappears, the recharge operation of VCC pin is repeated.
H: The switching operation restarts when V_{NTC}>0.2V. The VCC is supplied by the auxiliary winding.
I: When the power supply turns OFF, VCC voltage falls down due to the descend of the voltage of DRAIN pin. The IC turns hen the V_{UVLO2} is triggered.

(1-3)Start sequences 2（no VCC supply with auxiliary winding）

While IC operates after VCCUVLO is released, VCC pin operates by the charge/discharge to the external capacitor. By supplying the VCC with the start-up circuit, a circuit without the auxiliary winding of the transistor can be composed. Figure 10 shows the schematic of the DC/DC part.

It is necessary to pay attention to the heat which caused by the power consumption of the JFET of the start-up circuit, while there is no VCC supply with the auxiliary winding of the transformer.

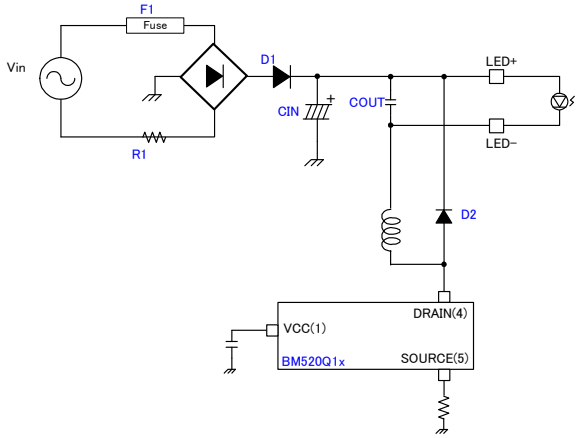


Figure 10. Schematic of the DC/DC Part without Power Supply by Auxiliary Winding

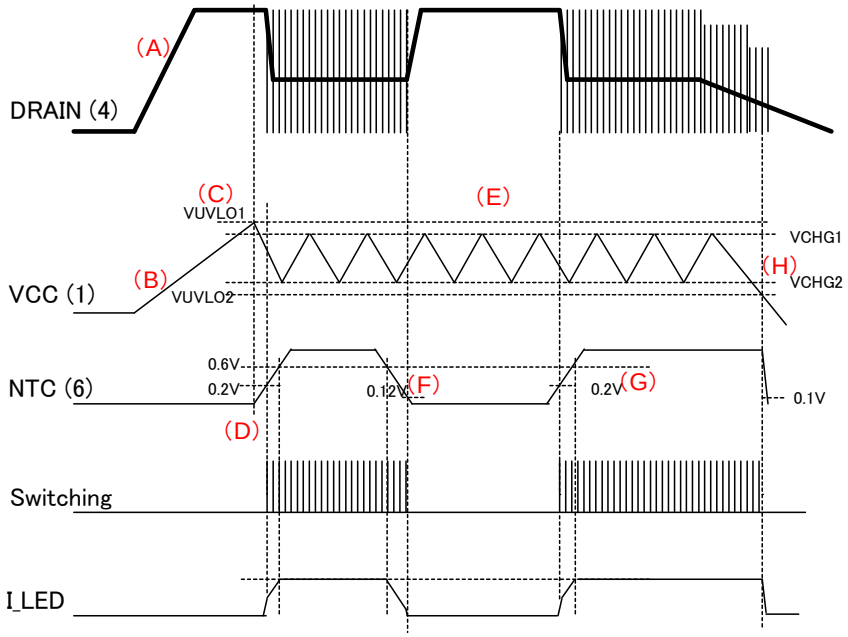


Figure 11. ON/OFF Sequences (no VCC supply with auxiliary winding)

A: Input voltage VH is applied. (Though the LED and the transformer, a high voltage is applied to DRAIN pin from VH.)
B: The capacitor connected to the VCC pin is charged by the start-up current from the DRAIN pin.
C: The IC starts operating when VCC > V_{UVLO1}
D: The soft start is achieved by the voltage rise of the NTC pin.(The switching starts when VNTC>0.2V)
E: The VCC repeats charge/recharge operations between the recharge trigger voltage V_{CHG1} and V_{CHG2}.
F: The switching operation stops when V_{NTC}<0.12V.
G: The switching operation restarts when V_{NTC}>0.2V.
H: When the power supply turns OFF, VCC voltage falls down due to the descend of the voltage of DRAIN pin. The IC turns OFF when the V_{UVLO2} is triggered.

(2) VCC pin protection function

The VCC under voltage protection function VCC UVLO (Under Voltage Lock Out), over voltage protection function VCC OVP (Over Voltage Protection), and a VCC recharge function which operates when a voltage drop occurs at VCC pin are built in this IC. The VCC UVLO and VCC OVP functions are used for preventing the destructions of the switching MOSFET which occurs when the VCC voltage is too high or too low.

Owing to the VCC charge function, the VCC pin is charged from high voltage lines by the start circuit when the VCC voltage drops, and the secondary output voltage is stabilized.

(2-1) VCC UVLO / VCC OVP function

VCC UVLO and VCC OVP are auto recovery comparators which have voltage hysteresis.

VCC OVP has a built-in mask time T_{LATCH}(Typ=100us).

When the VCC voltage is over V_{OVP} (typ=27.5V) ,and this state lasts T_{LATCH} (typ=100us) , the detection is executed.

By this function, the surge which occurs at VCC pin can be masked .

(2-2) VCC charge function

When the VCC pin voltage is over V_{UVLO1}, the IC starts up. In this case, if the VCC pin voltage drops below V_{CHG1}, VCC charge function operates. At this time, the VCC pin is charged from the DRAIN pin through the bootstrap circuit. Owing to this operation, the failure of start-up can be prevented.

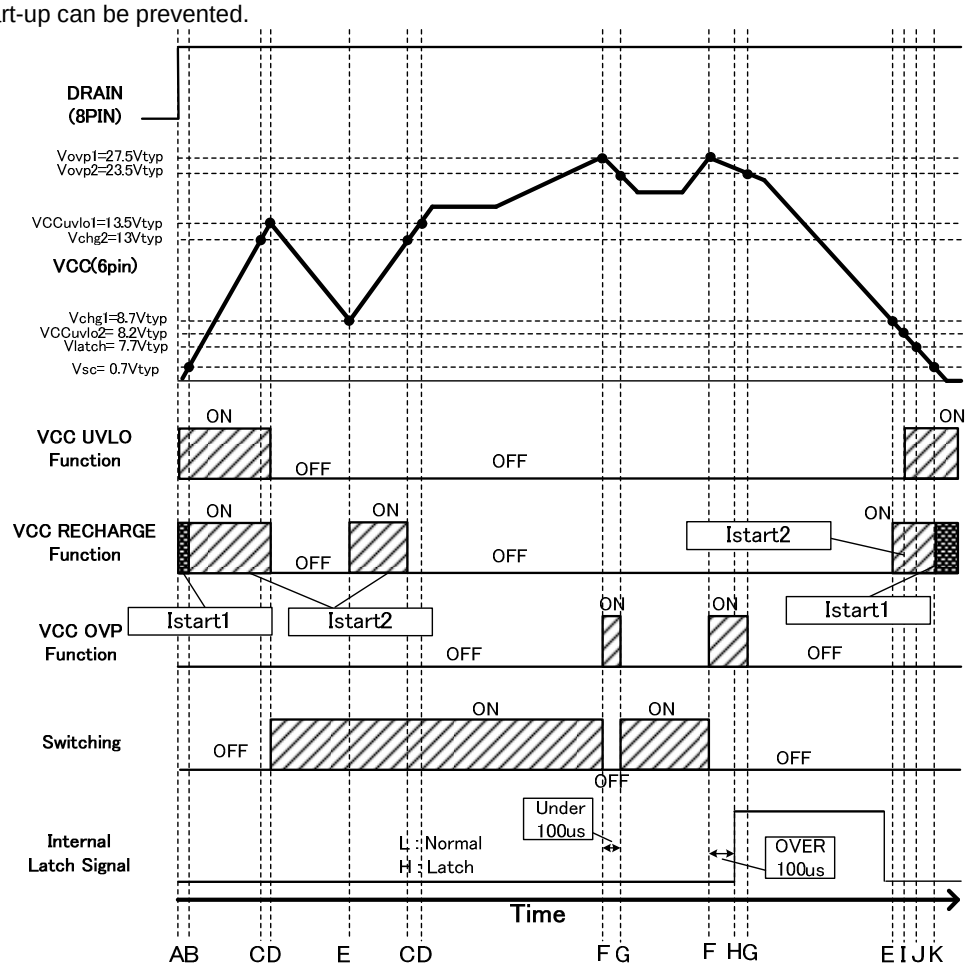


Figure 12. VCC UVLO/ VCC OVP / VCC charge function timing chart

A: DRAIN pin voltage is applied, VCC voltage rises by the charging current Istart1 (550uA typ.).
B: VCC voltage> $V_{SC,}$ the charging current to VCC changes from Istart1(550uA typ.) to Istart2(3mA typ.)
C: VCC voltage> $V_{CHG2,}$ though VCC charge function reacts, due to VCC UVLO is detected, the charge continues.
D: VCC voltage> V_{UVLO1}, the VCC UVLO is released, and DC/DC operation starts, the charge to VCC stops.
E: VCC voltage> V_{CHG1}, the charge to VCC restarts.
F: VCC voltage> V_{OVP1}, VCC OVP is detected.
G: VCC voltage> V_{OVP2}, if VCC voltage drops below V_{OVP2} in 100us, VCC OVP is released, and the latch will not be activated.
H: V_{OVP2}< VCC voltage < $V_{OVP1,}$ if this state is kept longer than 100us, the switching stops by latch.
I: VCC voltage< $V_{UVLO1,}$ VCC UVLO is detected.
J: VCC voltage< V_{LATCH}, the latch state is released.
K: VCC voltage< V_{SC}, the charging current to VCC changes from start2(3mA typ.)⇒Istart1(550uA typ.)

(3) LED peak current sensing

The peak current sensing is proceeded in every switching cycle. The switching turns OFF if the voltage of SOURCE pin exceeds some certain value. An AC compensation function is built in this IC. It is a function which increases the LED peak current sensing level with the increment of time. This operation is showed in Figure 13,14.

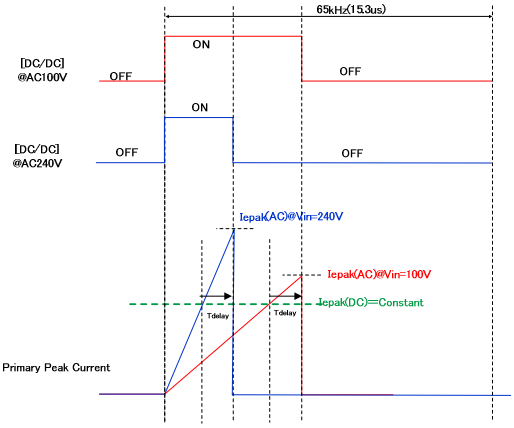


Figure 13. Peak current sensing without AC compensation

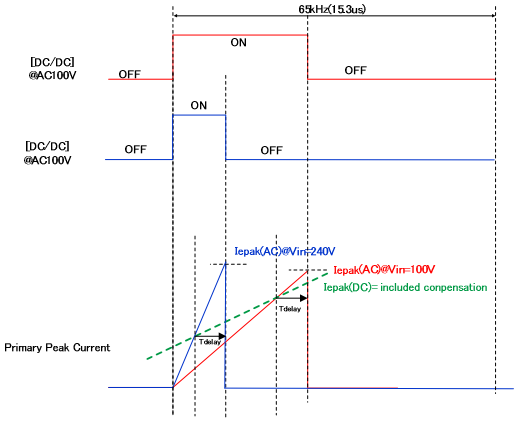


Figure 14. Peak current sensing with AC compensation

(4) L.E.B blanking period

When the MOSFET driver is turned ON, surge current occurs by the capacitive components and drive current. In this case, if the SOURCE pin voltage rises temporarily, false detections may occur in the over current limiter circuit. For preventing from the false detections, a L.E.B function（Leading Edge Blanking function）which masks the SOURCE voltage during the 200nsec after the OUT pin switches form L→H is built in.

(5) SOURCE pin open protection

When the SOURCE pin (pin 5) becomes open, the IC may be damaged by overheats. For preventing from this, an open protection circuit is built in this IC. (automatic recovery protection)

(6) NTC pin temperature detecting protection

There occurs a voltage which is caused by a 50uA source current from the NTC pin on the thermistor. When NTC pin voltage is lower than 0.67V, the LED peak current reduces gradually, and when this voltage is lower than 0.12V, the switching operation stops. When NTC voltage rises up to higher than 0.2V, the switching operation recovers.

●**Operation mode of protection circuit**

Operation mode of protection functions are shown in Table 2.

Table 2. Operation mode of protection circuit

Abnormal state detection		Detect	Release	Protection operations
VCC	UVLO	<= 8.2V	>= 13.5V	Automatic recovery
	OVP	>= 27.5V	Before latch：<= 23.5V Latched：VCC<= 7.7V	100us timer latch
TSD		>= 175℃	Before latch：<= 155℃ Latched：VCC<= 7.7V	100us timer latch
ZT	OVP	>= 3.50V	Before latch：<= 3.33V Latched：VCC<= 7.7V	100us timer latch
NTC	LED TEMP	<= 0.12V	>= 0.2V	Switching OFF

●**Sequences**

The sequences diagram of all states of this IC is showed in Figure 15.

In all states, when VCC<8.2V, the states change to OFF mode.

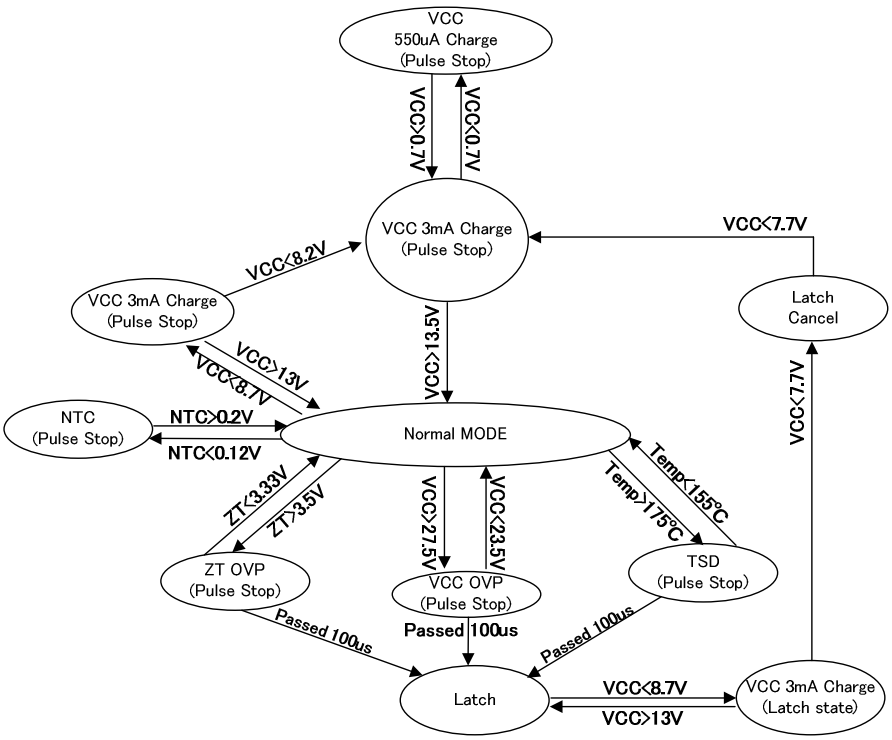


Figure 15. Transition diagram of all states

●**Thermal loss**

According to the thermal design, please observe the conditions below when use this IC.

1. The ambient temperature Ta must be 105℃ or less.
2. The consumption of the IC must be within the allowable dissipation P_d.

The thermal dissipation characteristics are as follows.
(PCB: 70 mm × 70mm × 1.6 mm, mounted on glass epoxy substrate)

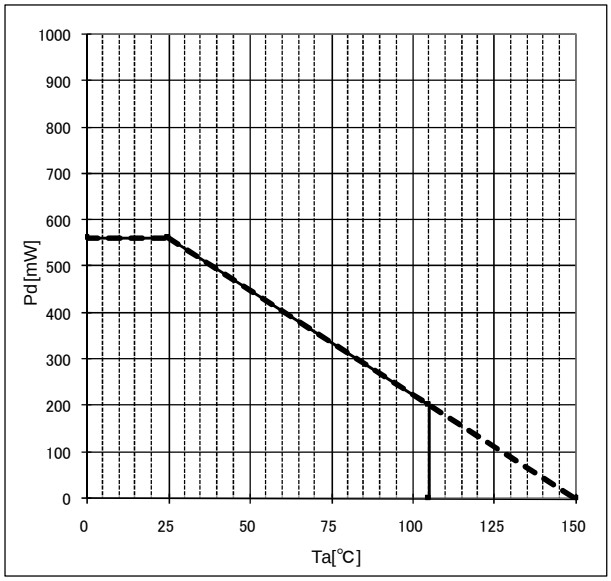


Figure 16. Thermal dissipation characteristics

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors**.**

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

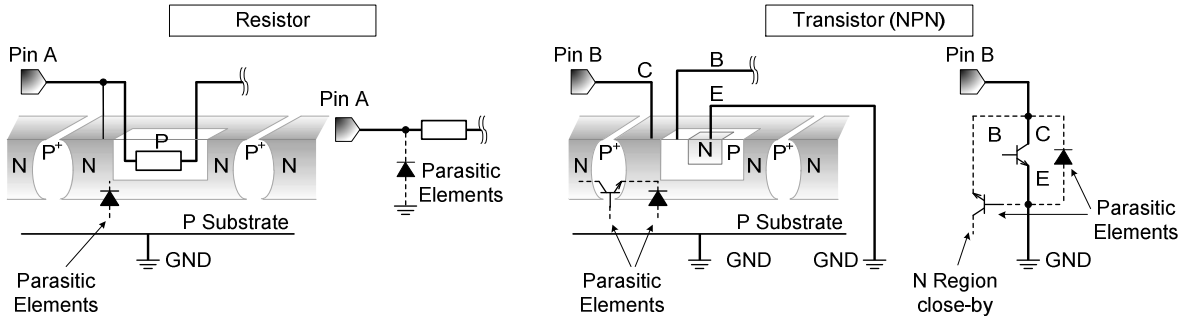
Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

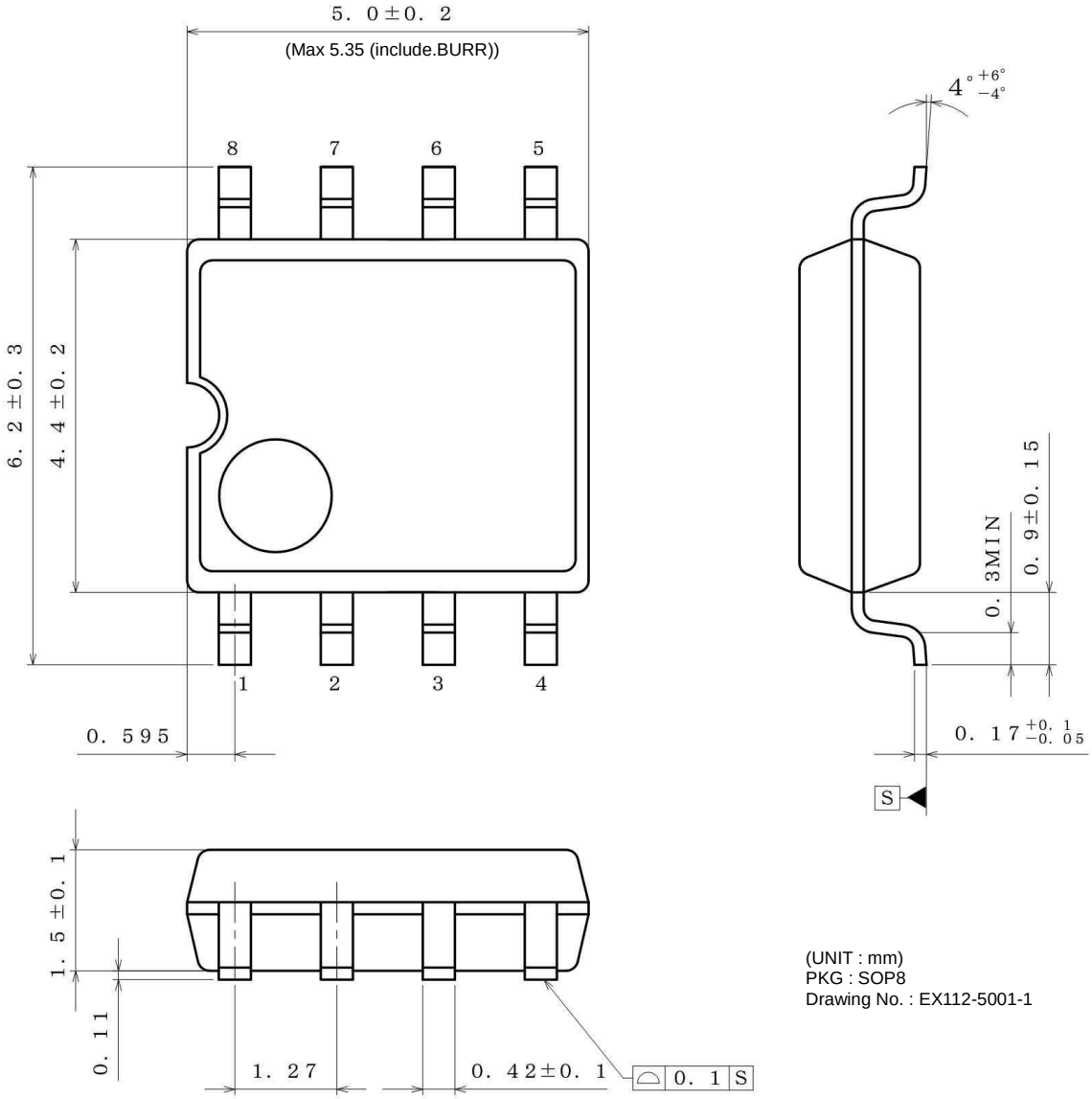
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

●Physical Dimension, Tape and Reel Information

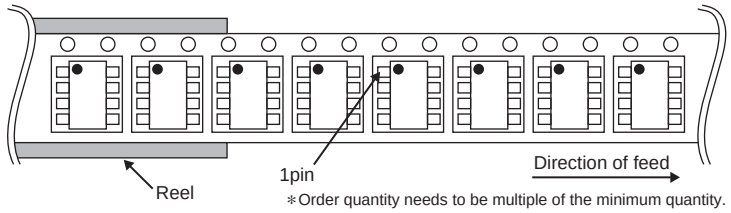
Package Name	SOP8



(UNIT : mm)
PKG : SOP8
Drawing No. : EX112-5001-1

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

●**Ordering Information**

B M 5 2 0 Q 1 9 F	-	XX

Product name

Package
F : SOP8

Packaging and forming specification

XX: Please confirm the formal name with our salesmen.

●**Marking Diagram**