Quasi-Resonant Control DC/DC converter and Power Factor Correction converter IC for AC/DC Converter

BM1050AF-G

● General Description
BM1050AF is compounded LSI of Power Factor Correction converter (PFC) for harmonic solution and DC/DC converter (DC/DC). Because DC/DC operates on Quasi-resonant method, DC/DC contributes to Low EMI.
BM1050AF built in a HV starter circuit that tolerates 650V. Because of putting the current sense resistors externally both the PFC part and the DC/DC part, IC enables power supply design free.

In the PFC part, IC adopts peak current control operation. Suitable application is proposed by a various protection circuit, such as the multiplier with a revision circuit on the AC voltage falls, the load regulation revision circuit, and the maximum power feed-forward circuit, etc. Moreover, the frequency hopping function is built in and it contributes to Low EMI.

The Quasi-resonant system of a DC/DC part contributes to low EMI because PFC operates by soft switching. A burst mode is built in, so the power is reduced at light load. Various protection functions, such as a soft start function, a burst function, an over-current limiting for every cycle, overvoltage protection, and over current protection, are built in. The pin for communicated control with a controller and the external stop pin are prepared; it proposes the system that can be adapted for various applications.

● Basic specifications
- Operating Power Supply Voltage Range: VCC: 8.5 to 24.0V
- Operating Current:
  - QR ON (PFC OFF): 1.20mA (pulse on)
  - QR ON (PFC OFF): 1.00mA (pulse off)
  - QR ON (PFC ON): 1.80mA (pulse on)
- Oscillation Frequency QR part: 120kHz (FB=2.0V typ)
- Operating Temperature: -40°C to +85°C

● Typical Application Circuit(s)

![Application circuit](Image)

Figure 1. Application circuit

● Features
- Quasi-resonant circuit + PFC circuit
- Built-in HV Starter circuit
- Low consumption current (typ.10μA) when starter circuit is OFF.
- Quasi resonant circuit
  - Max operating frequency (120kHz)
  - Frequency reduction function
  - Over-current limiting variable function
  - Pulse-by-pulse over-current protection circuit
  - Built-in Soft start
  - Voltage protection function (brown out) during low input
  - ZT pin Over Voltage Protection
  - Output overload protection (auto recovery / latch switching enabled)
- 250nsec Leading-Edge Blanking
- Power Factor Correction circuit
  - Peak current control (65kHz)
  - Frequency hopping function
  - Per-cycle over current protection circuit
  - Maximum power revision the multiplier with a revision circuit when the AC voltage falls
  - the load change measure circuit
- Selectable protection method by LATCH/AUTOR terminal.
  - LATCH/AUTOR=H: Latch
  - LATCH/AUTOR=L: Auto recovery
- External stop function (COMP pin)
- AC input voltage stop detected function (ACDET)
- Built-in PFC stop terminal (PFCON/OFF)

● Package(s)
SOP24: 15.0mm × 5.40mm × 1.80mm pitch1.27mm

● Applications
TV, AC adapters, printers, LED lighting

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### Absolute Maximum Ratings (Ta = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum applied voltage 1</td>
<td>V\text{max}_1</td>
<td>650</td>
<td>V</td>
<td>VH\text{_IN}</td>
</tr>
<tr>
<td>Maximum applied voltage 2</td>
<td>V\text{max}_2</td>
<td>30</td>
<td>V</td>
<td>VCC, P\text{_QR_SEL}</td>
</tr>
<tr>
<td>Maximum applied voltage 3</td>
<td>V\text{max}_3</td>
<td>5.5</td>
<td>V</td>
<td>P_BO, P_VSE0, P_VS, P_BOPK, P_CS, P_FC0\text{_OFF}, P_COMP, P_AD\text{_DET}, P_ACT\text{_IMER}, P_QR_CS, P_QR_ZT, P_QR_FB, P_LATCH, P_AUTOR, P_VREF</td>
</tr>
<tr>
<td>Maximum applied voltage 4</td>
<td>V\text{max}_4</td>
<td>15</td>
<td>V</td>
<td>G\text{_CLAMP}, P_OUT, P_QR_OUT</td>
</tr>
<tr>
<td>Output peak current 1</td>
<td>I\text{_O}</td>
<td>-0.5</td>
<td>A</td>
<td>QR_OUT, P_OUT</td>
</tr>
<tr>
<td>Output peak current 2</td>
<td>I\text{_L}</td>
<td>1.0</td>
<td>A</td>
<td>QR_OUT, P_OUT</td>
</tr>
<tr>
<td>QR_ZT pin current 1</td>
<td>I\text{_Sz\text{_T1}}</td>
<td>-2.0</td>
<td>mA</td>
<td>QR_OUT, P_OUT</td>
</tr>
<tr>
<td>QR_ZT pin current 2</td>
<td>I\text{_Sz\text{_T2}}</td>
<td>3.0</td>
<td>mA</td>
<td>QR_OUT, P_OUT</td>
</tr>
<tr>
<td>Allowable dissipation</td>
<td>P_d</td>
<td>687.6 (Note1)</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>T\text{_opr}</td>
<td>-40 ~ +85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Maximum junction temperature</td>
<td>T\text{_jmax}</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature range</td>
<td>T\text{_str}</td>
<td>-55 ~ +150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(Note1) When mounted (on 70 mm × 70 mm, 1.6 mm thick, glass epoxy on single-layer substrate). Reduce to 5.5 mW/°C when Ta = 25°C or above.

### Operating Conditions (Ta = 25°C)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage range 1</td>
<td>VCC</td>
<td>8.5~24.0</td>
<td>V</td>
<td>VCC</td>
</tr>
<tr>
<td>Power supply voltage range 2</td>
<td>VH_IN</td>
<td>80~600</td>
<td>V</td>
<td>VH_IN</td>
</tr>
<tr>
<td>Power supply voltage range 3</td>
<td>P_BO</td>
<td>0.0~1.8</td>
<td>V</td>
<td>P_BO</td>
</tr>
</tbody>
</table>
### Electrical Characteristics (Unless otherwise noted, Ta=25, VH_IN=320Vdc, VCC=12V)

#### [Circuit current]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Specifications</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit current (ON) 1</td>
<td>$I_{ON1}$</td>
<td>0.700</td>
<td>1.200</td>
<td>1.700 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VCC=12.0V (QR=ON, PFC=OFF) QR_FB=1.0V (during pulse operation)</td>
</tr>
<tr>
<td>Circuit current (ON) 2</td>
<td>$I_{ON2}$</td>
<td>0.700</td>
<td>1.000</td>
<td>1.300 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VCC=12.0V (QR =ON, PFC=OFF) QR_FB=VREF (during pulse operation when OFF)</td>
</tr>
<tr>
<td>Circuit current (ON) 3</td>
<td>$I_{ON3}$</td>
<td>0.800</td>
<td>1.800</td>
<td>2.800 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VCC=12.0V (QR =ON, PFC=ON) QR_FB=1.0V (during pulse operation)</td>
</tr>
</tbody>
</table>

#### [Start circuit Block]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Specifications</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start current 1</td>
<td>$I_{S1}$</td>
<td>0.100</td>
<td>0.500</td>
<td>1.000 mA</td>
</tr>
<tr>
<td>Start current 2</td>
<td>$I_{S2}$</td>
<td>1.000</td>
<td>3.000</td>
<td>5.000 mA</td>
</tr>
<tr>
<td>OFF Current</td>
<td>$I_{S3}$</td>
<td>-</td>
<td>10</td>
<td>16 uA</td>
</tr>
<tr>
<td>VH voltage switched start current</td>
<td>$V_{Sc}$</td>
<td>0.400</td>
<td>0.800</td>
<td>1.400 V</td>
</tr>
</tbody>
</table>

#### [VREF Block]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Specifications</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREF output voltage</td>
<td>$V_{REF}$</td>
<td>3.500</td>
<td>4.000</td>
<td>4.500 V</td>
</tr>
<tr>
<td>VREF output capacitor</td>
<td>$C_{REF}$</td>
<td>0.68</td>
<td>1.00</td>
<td>2.20 uF</td>
</tr>
<tr>
<td>GCLAMP voltage 1</td>
<td>$GCL1$</td>
<td>11.0</td>
<td>12.5</td>
<td>14.0 V</td>
</tr>
<tr>
<td>GCLAMP voltage 2</td>
<td>$GCL2$</td>
<td>11.0</td>
<td>12.5</td>
<td>14.0 V</td>
</tr>
<tr>
<td>VREF UVLO 1</td>
<td>$V_{UVLO1}$</td>
<td>77.5</td>
<td>87.5</td>
<td>97.5% (3.100V, 3.500V, 3.900V)</td>
</tr>
<tr>
<td>VREF UVLO 2</td>
<td>$V_{UVLO2}$</td>
<td>52.5</td>
<td>62.5</td>
<td>72.5% (2.100V, 2.500V, 2.900V)</td>
</tr>
<tr>
<td>VREF UVLO hysteresis</td>
<td>$V_{UVLO3}$</td>
<td>-</td>
<td>25</td>
<td>%</td>
</tr>
<tr>
<td>VCC UVLO voltage 1</td>
<td>$V_{UVLO1}$</td>
<td>12.50</td>
<td>13.50</td>
<td>14.50 V</td>
</tr>
<tr>
<td>VCC UVLO voltage 2</td>
<td>$V_{UVLO2}$</td>
<td>5.50</td>
<td>7.00</td>
<td>8.50 V</td>
</tr>
<tr>
<td>VCC UVLO hysteresis</td>
<td>$V_{UVLO3}$</td>
<td>-</td>
<td>6.50</td>
<td>%</td>
</tr>
<tr>
<td>VCC OVP voltage 1</td>
<td>$V_{OVP1}$</td>
<td>24.0</td>
<td>27.0</td>
<td>30.0 V</td>
</tr>
<tr>
<td>VCC OVP voltage 2</td>
<td>$V_{OVP2}$</td>
<td>20.0</td>
<td>23.0</td>
<td>26.0 V</td>
</tr>
<tr>
<td>VCC OVP hysteresis</td>
<td>$V_{OVP3}$</td>
<td>-</td>
<td>4.0</td>
<td>%</td>
</tr>
<tr>
<td>Brown out detection voltage 1</td>
<td>$V_{BO1}$</td>
<td>0.350</td>
<td>0.400</td>
<td>0.450 V</td>
</tr>
<tr>
<td>Brown out detection voltage 2</td>
<td>$V_{BO2}$</td>
<td>-</td>
<td>0.200</td>
<td>%</td>
</tr>
<tr>
<td>Brown out detection hysteresis</td>
<td>$V_{BO3}$</td>
<td>-</td>
<td>0.200</td>
<td>%</td>
</tr>
<tr>
<td>Brown out detection delay time 1</td>
<td>$T_{BO1}$</td>
<td>21.8</td>
<td>32.0</td>
<td>42.2 ms</td>
</tr>
<tr>
<td>Brown out detection delay time 2</td>
<td>$T_{BO2}$</td>
<td>87.0</td>
<td>128.0</td>
<td>169.0 ms</td>
</tr>
<tr>
<td>Brown out detection delay time 3</td>
<td>$T_{BO3}$</td>
<td>170</td>
<td>250</td>
<td>330 ms</td>
</tr>
</tbody>
</table>

**Note:** Times until ACDET logic change (ACTIMER=L) and Times until PFC and QR stop.
### Electrical Characteristics

(Unless otherwise noted, \( Ta=25 \), \( VH_{IN}=320\text{Vdc} \), \( VCC=12\text{V} \))

<table>
<thead>
<tr>
<th>Parameter</th>
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<th>Unit</th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>[ACDET pin characteristics]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ACDET pin ON resister</td>
<td>( R_{ACDET} )</td>
<td>50</td>
<td>100</td>
<td>200 ( \Omega )</td>
</tr>
<tr>
<td><strong>[ACTIMER pin characteristics]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ACTIMER pin input L level</td>
<td>( V_{ACTIMEL} )</td>
<td>-</td>
<td>-</td>
<td>0.3 ( V )</td>
</tr>
<tr>
<td>ACTIMER pin input H level</td>
<td>( V_{ACTIMEH} )</td>
<td>1.2</td>
<td>-</td>
<td>- ( V )</td>
</tr>
<tr>
<td>ACTIMER pin pull-down resistor</td>
<td>( R_{ACTIMEH} )</td>
<td>165</td>
<td>330</td>
<td>500 ( \text{k}\Omega )</td>
</tr>
<tr>
<td><strong>[PFCON/OFF pin characteristics]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PFCON/OFF pin input L level</td>
<td>( V_{PON/OFFL} )</td>
<td>-</td>
<td>-</td>
<td>0.3 ( V )</td>
</tr>
<tr>
<td>PFCON/OFF pin input H level</td>
<td>( V_{PON/OFFH} )</td>
<td>1.2</td>
<td>-</td>
<td>- ( V )</td>
</tr>
<tr>
<td>PFCON/OFF pin pull-down resistor</td>
<td>( R_{PON/OFFH} )</td>
<td>50</td>
<td>100</td>
<td>150 ( \text{k}\Omega )</td>
</tr>
<tr>
<td>PFCON/OFF pin timer time</td>
<td>( T_{PON/OFF} )</td>
<td>0.50</td>
<td>1.50</td>
<td>3.00 ( \text{ms} )</td>
</tr>
<tr>
<td><strong>[LATCH/AUTOR pin characteristics]</strong></td>
<td></td>
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</tr>
<tr>
<td>LATCH/AUTOR pin input L level</td>
<td>( V_{MODEL} )</td>
<td>-</td>
<td>-</td>
<td>0.3 ( V )</td>
</tr>
<tr>
<td>LATCH/AUTOR pin input H level</td>
<td>( V_{MODEH} )</td>
<td>1.2</td>
<td>-</td>
<td>- ( V )</td>
</tr>
<tr>
<td>LATCH/AUTOR pin pull-down resistor</td>
<td>( R_{MODEH} )</td>
<td>50</td>
<td>100</td>
<td>150 ( \text{k}\Omega )</td>
</tr>
<tr>
<td><strong>[COMP pin characteristics]</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>COMP pin detection voltage</td>
<td>( V_{COMP} )</td>
<td>0.370</td>
<td>0.500</td>
<td>0.630 ( V )</td>
</tr>
<tr>
<td>COMP pin pull-up resistor</td>
<td>( R_{COMP} )</td>
<td>19.4</td>
<td>25.9</td>
<td>32.3 ( \text{k}\Omega )</td>
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<tr>
<td>External Thermistor resistor</td>
<td>( R_{T} )</td>
<td>3.32</td>
<td>3.70</td>
<td>4.08 ( \text{k}\Omega )</td>
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<tr>
<td>Latch release voltage (VCC pin voltage)</td>
<td>( V_{LATCHOFF} )</td>
<td>-</td>
<td>( V_{UVLO} - 0.5 )</td>
<td>- ( V )</td>
</tr>
<tr>
<td>Latch mask time</td>
<td>( T_{COMP} )</td>
<td>70</td>
<td>150</td>
<td>240 ( \text{us} )</td>
</tr>
</tbody>
</table>
### Electrical Characteristics (Unless otherwise noted Ta=25, VH_IN=320Vdc, VCC=12V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Specifications</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Minimum</td>
<td>Standard</td>
</tr>
<tr>
<td>[Quasi-resonant Control Block]</td>
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<tr>
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<tr>
<td>[Quasi-resonant DC/DC converter Block (turn off)]</td>
<td></td>
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<tr>
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<tr>
<td>[Quasi-resonant DC/DC converter Block (turn on)]</td>
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<tr>
<td>[Quasi-resonant DC/DC converter protection functions]</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
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<tr>
<td>[QR_OUT pin]</td>
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<tr>
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</tr>
<tr>
<td>[QR_SEL pin]</td>
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</tr>
</tbody>
</table>

*1 Pulse is applied to QR_CS pin

*2 Pulse is applied to QR_ZT pin
Electrical Characteristics (Unless otherwise noted Ta=25, VH_IN=320Vdc, VCC=12V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Specifications</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Power Factor Correction (PFC) controller block]</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>[Power Factor Correction (PFC) Gm amplifier block]</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>P_VS pin pull-up current</td>
<td>I_P_VS</td>
<td>-</td>
<td>0.50</td>
<td>-</td>
</tr>
<tr>
<td>Gm amplifier normal voltage</td>
<td>V_GSAMP</td>
<td>2.460</td>
<td>2.500</td>
<td>2.540</td>
</tr>
<tr>
<td>Gm amplifier trans-conductance</td>
<td>V_GSAMP</td>
<td>30.8</td>
<td>44.0</td>
<td>57.2</td>
</tr>
<tr>
<td>Maximum Gm amplifier source current</td>
<td>I_GSAMP1</td>
<td>15</td>
<td>25</td>
<td>35</td>
</tr>
<tr>
<td>Maximum Gm amplifier sink current</td>
<td>I_GSAMP2</td>
<td>24</td>
<td>40</td>
<td>56</td>
</tr>
<tr>
<td>[Power Factor Correction (PFC) input voltage monitor block]</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>P_BO input voltage range</td>
<td>V_P_BOIN</td>
<td>0.000</td>
<td>-</td>
<td>1.800</td>
</tr>
<tr>
<td>P_BO pin leak current</td>
<td>I_BOLEAK</td>
<td>-1.00</td>
<td>0.00</td>
<td>1.00</td>
</tr>
<tr>
<td>[Power Factor Correction (PFC) input voltage peak detect block]</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>P_BOPK max charge current</td>
<td>I_BOPKCHG</td>
<td>36</td>
<td>72</td>
<td>144</td>
</tr>
<tr>
<td>P_BOPK max discharge current</td>
<td>I_BOPKDIS</td>
<td>0.1</td>
<td>0.2</td>
<td>0.4</td>
</tr>
<tr>
<td>[Power Factor Correction (PFC) multiplier block]</td>
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</tr>
<tr>
<td>Multiplier constant</td>
<td>K_MULTI</td>
<td>0.37</td>
<td>0.54</td>
<td>0.71</td>
</tr>
<tr>
<td>P_VSEO stop voltage 1</td>
<td>V_PSEO1</td>
<td>181</td>
<td>226</td>
<td>271</td>
</tr>
<tr>
<td>P_VSEO stop voltage 2</td>
<td>V_PSEO2</td>
<td>88</td>
<td>128</td>
<td>168</td>
</tr>
<tr>
<td>[Power Factor Correction (PFC) Oscillation frequency block]</td>
<td></td>
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<tr>
<td>PFC Oscillation frequency</td>
<td>F_PSW1</td>
<td>60</td>
<td>65</td>
<td>70</td>
</tr>
<tr>
<td>PFC Frequency hopping width</td>
<td>F_PSWEL</td>
<td>-</td>
<td>4.0</td>
<td>-</td>
</tr>
<tr>
<td>PFC hopping frequency</td>
<td>F_PCH</td>
<td>75</td>
<td>125</td>
<td>175</td>
</tr>
<tr>
<td>Minimum Pulse width</td>
<td>T_MIN</td>
<td>-</td>
<td>500</td>
<td>-</td>
</tr>
<tr>
<td>Maximum DUTY</td>
<td>D_MAX</td>
<td>90.0</td>
<td>94.0</td>
<td>98.0</td>
</tr>
<tr>
<td>[Power Factor Correction (PFC) Driver block]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_OUT pin PMOS ON resistor</td>
<td>R_POUT</td>
<td>5</td>
<td>15</td>
<td>30</td>
</tr>
<tr>
<td>P_OUT pin NMOS ON resistor</td>
<td>R_NOUT</td>
<td>2</td>
<td>5</td>
<td>10</td>
</tr>
</tbody>
</table>
### Electrical Characteristics (Unless otherwise noted Ta=25, VH_IN=320Vdc, VCC=12V)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Specifications</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leading Edge Blanking time</td>
<td>T_{PLEB}</td>
<td>-</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>P_CS over current limit voltage 1</td>
<td>V_{PCS1}</td>
<td>0.93</td>
<td>1.16</td>
<td>1.40 V</td>
</tr>
<tr>
<td>P_CS over current limit voltage 2</td>
<td>V_{PCS2}</td>
<td>0.48</td>
<td>0.60</td>
<td>0.72 V</td>
</tr>
<tr>
<td>P_VS short protection voltage</td>
<td>V_{P_SHORT}</td>
<td>0.200 (-92%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.300 (-88%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.400 (-84%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QR power-limit P_VS voltage 1</td>
<td>V_{PFCON}</td>
<td>1.800 (-28%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.000 (-20%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.200 (-12%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QR power limit P_VS voltage 2</td>
<td>V_{PFCON}</td>
<td>1.100 (-56%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.250 (-50%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.400 (-44%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_VS QR power limit hysteresis</td>
<td>V_{PFCHYS}</td>
<td>- 0.750 (30%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_VS gain rise voltage</td>
<td>V_{PGUP}</td>
<td>2.050 (-18%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.250 (-10%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.450 (-2%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_VS gain fall voltage</td>
<td>V_{POVP1}</td>
<td>- 2.625 (+5%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_VS over voltage protection voltage</td>
<td>V_{POVP2}</td>
<td>- 2.725 (+9%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_VS over voltage protection timer</td>
<td>T_{POVP2}</td>
<td>16</td>
<td>32</td>
<td>48 ms</td>
</tr>
</tbody>
</table>

*Figure of () is comparison with P_VS standard voltage 2.5V*

---

**TSZ22111**

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- **TSZ22111 - 15 - 001**
- **10.Apr.2015 Rev.003**
### Table 1. I/O Pin Functions

<table>
<thead>
<tr>
<th>NO</th>
<th>PIN</th>
<th>I/O</th>
<th>Function</th>
<th>ESD protection system</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>P_BO</td>
<td>I</td>
<td>Input AC Voltage monitor pin</td>
<td>○</td>
</tr>
<tr>
<td>2</td>
<td>P_VSEO</td>
<td>I/O</td>
<td>PFC gm amplifier output pin</td>
<td>○</td>
</tr>
<tr>
<td>3</td>
<td>P_VS</td>
<td>I</td>
<td>PFC Output voltage monitor pin</td>
<td>○</td>
</tr>
<tr>
<td>4</td>
<td>P_BOPK</td>
<td>O</td>
<td>Connected capacitor to the pin</td>
<td>○</td>
</tr>
<tr>
<td>5</td>
<td>P_CS</td>
<td>I</td>
<td>PFC Coil current monitor pin</td>
<td>○</td>
</tr>
<tr>
<td>6</td>
<td>PFCON/OFF</td>
<td>I</td>
<td>PFC ON/OFF control input pin</td>
<td>○</td>
</tr>
<tr>
<td>7</td>
<td>COMP</td>
<td>I</td>
<td>External latch stop pin</td>
<td>○</td>
</tr>
<tr>
<td>8</td>
<td>ACDET</td>
<td>O</td>
<td>Input AC voltage state communication pin</td>
<td>○</td>
</tr>
<tr>
<td>9</td>
<td>ACTIMER</td>
<td>I</td>
<td>Brown out detection time setting input pin</td>
<td>○</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>I/O</td>
<td>GND</td>
<td>-</td>
</tr>
<tr>
<td>11</td>
<td>P_OUT</td>
<td>O</td>
<td>PFC Output drive pin</td>
<td>○</td>
</tr>
<tr>
<td>12</td>
<td>GCLAMP</td>
<td>I/O</td>
<td>Gate H level clamp pin</td>
<td>○</td>
</tr>
<tr>
<td>13</td>
<td>VCC</td>
<td>I</td>
<td>Power supply pin</td>
<td>-</td>
</tr>
<tr>
<td>14</td>
<td>QR_OUT</td>
<td>O</td>
<td>Quasi-resonant Output drive pin</td>
<td>○</td>
</tr>
<tr>
<td>15</td>
<td>QR_SEL</td>
<td>O</td>
<td>Quasi-resonant Mask pin</td>
<td>-</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>I/O</td>
<td>GND</td>
<td>-</td>
</tr>
<tr>
<td>17</td>
<td>QR_CS</td>
<td>I</td>
<td>Quasi-resonant Over current detected pin</td>
<td>○</td>
</tr>
<tr>
<td>18</td>
<td>QR_FB</td>
<td>I</td>
<td>Quasi-resonant Feedback detected pin</td>
<td>○</td>
</tr>
<tr>
<td>19</td>
<td>QR_ZT</td>
<td>I</td>
<td>Quasi-resonant Zero cross detected pin</td>
<td>-</td>
</tr>
<tr>
<td>20</td>
<td>LATCH/AUTOR</td>
<td>I</td>
<td>Protection mode switched input pin</td>
<td>○</td>
</tr>
<tr>
<td>21</td>
<td>VREF</td>
<td>O</td>
<td>Internal power supply pin</td>
<td>○</td>
</tr>
<tr>
<td>22</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>23</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>24</td>
<td>VH_IN</td>
<td>I</td>
<td>AC Input voltage applied pin</td>
<td>-</td>
</tr>
</tbody>
</table>

*Notes:* ESD protection system indicates the presence or absence of protection for VCC and GND.
Figure 2. I/O Equivalent Circuit Diagram
Figure 3. Block Diagram
Figure 3-2. Block Diagram
●Explanation of each block

(1) Starter block (24pin)
BM1050AF built in the starter circuit that withstands 650V. For that, application used the IC is enabled faster start time and low standby power. After start-up, consumption power is idling current $I_{\text{START3}}$ (typ=10μA) only. Reference of start-up time is shown in Figure 6. It can start-up less than 0.1sec when $C_{\text{VCC}}=10\mu\text{F}$.

![Start Circuit Block Diagram](image)

![Start-up current vs VCC voltage](image)

![Start time vs $C_{\text{VCC}}$ (Reference values)](image)

*Start current flows from VH_IN pin to VCC pin.

ex) When $V_{\text{ac}}=100V$; consumption power of start-up circuit only.
$P_{\text{VH}}=100V \times \sqrt{2} \times 10\mu\text{A}=1.41\text{mW}$

ex) When $V_{\text{ac}}=240V$; consumption power of start-up circuit only.
$P_{\text{VH}}=240V \times \sqrt{2} \times 10\mu\text{A}=3.38\text{mW}$
(2) Start sequence

The start sequence of IC operates DC/DC part, next PFC part (See the figure 7).

A : Input voltage VH is applied.
B : Charge current flows from VH_IN pin to the VCC pin capacitor. Then VCC pin voltage rises.
C : Monitor the AC voltage by P_BO pin. And confirm normal state by releasing brown out.
D : When \( V_{\text{SOLO}} \) (typ=13.5V) < VCC pin, release the inside UVLO and ON the inside regulator VREF.
E : When \( V_{\text{BAND}} \) (typ=87.5%) < VREF pin, release the inside VREFUVLO.
F : If the ‘E’ state continues constant period, DC/DC part starts because it recognizes normal state.
   When the switching starts, VOUT voltage rises.
   When the DC/DC start-up, please set external parts to be regulated output voltage within the \( T_{\text{FOLP}} \) period (64ms typ).
[QR start-up operation]
G : This IC adjusts over current limiter of DC/DC by operation of soft start 1 against over voltage and current rising.
   That term continues \( T_{ss1} \) (typ=1ms).
H : This IC adjusts over current limiter of DC/DC by operation of soft start 2 against over voltage and current rising.
   Soft start 2 operation continues power limiter operation until \( P_{\text{VS}} \) pin voltage > \( V_{\text{PFCON}} \) (2.00V typ) and \( T_{ss2} \) (typ=4ms).
   This IC operates the state that maximum power of QR is 50% at this state.
I : If secondary voltage is setting value, QR_FB pin voltage is constant value corresponded load by current from photo coupler.
   At normal state, QR_FB voltage is QR_FB<\( V_{\text{PFCON}} \) (2.60V typ).
[PFC start up operation]
J : At the point in I time, This IC recognizes that the part of DC/DC operation is normal, Part of PFC starts operation.
K : If P_VS pin voltage is upper \( V_{\text{PFCON}} \) (typ = 0.3V), this IC judges short detection normal.
L : P_VSEO voltage rises from 0V to prevent from over rising voltage and current at PFC part.
   At this time P_OUT pin DUTY increase from 0% with P_VSEO voltage increasing.

Figure 7. Start sequences Timing chart
About figure 7, condition is PFCON/OFF=L.
Start up operation is shown at figure 8, 9 by the state shift figure.
Figure 8 is LATCH/AUTOR=L (auto return operation), and figure 9 is LATCH/AUTOR=H (LATCH operation).

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside.

Figure 8. Diagram of state machine (LATCH/AUTOR=L)
Figure 9. Diagram of state machine (LATCH/AUTOR=H)
(3) VCC protection function and VREF pin function
(3-1) VCC pin protection function (13pin)
BM1050AF built in VCC low voltage protection function of VCCUVLO (Under Voltage Lock Out) and over voltage protection function of VCC OVP (Over Voltage Protection).
This function monitors VCC pin and prevent VCC pin from destroying switching MOSFET at abnormal voltage. VCCUVLO is auto recovery comparator that has voltage hysteresis. VCCOVP operates as latch mode comparator in the LATCH/AUTOR=H and as auto return comparator in the LATCH/AUTOR=L. VCC<Vuvlo1 (typ = Vuvlo1 - 0.5) is condition of latch release (reset) after detection of latch operation by VCCOVP. Refer to the operation figure 10.
VCCOVP built in mask time TCOMP (typ=150us), in case of continuing VCCOVP 150us, operates over voltage detection. By this function, this IC masks pin generated surge etc.
(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside.

Figure 10. VCC UVLO / OVP (LATCH/AUTOR=H at Latch stop)

A: VH input, VCC voltage rise
B: VCC>Vuvlo1, DC/DC operation start
C: VCC<Vuvlo2, DC/DC operation stop
D: VCC>Vuvlo1, DC/DC operation start
E: VCC voltage decreases until starting DC/DC switching
F: VCC rise
G: When VCC>Vovp1, DC/DC operation is stopped. Switching is stopped by internal latch signal.
H: Then DC/DC operation is stopped, power supply is lost from auxiliary. VCC voltage downs.
I: When VCC>Vuvlo1, this IC dose not operate DC/DC for latch operation. VCC voltage drops because of dropping of IC's consumption current.
J: same of H
K: same of I
L: same of J
M: VH is open (the state is outlet out). VCC drops.
N: VCC < VCOMP, latch releases.
(3-2) VREF pin function(21pin)
VREF pin is internal regulator output pin.
The use of VREF pin is IC's internal supply and connection of LATCH/AUTOR pin changing.
This pin needs an external capacitance, please use the capacitance following table.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Specification</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREF Output Capacitor</td>
<td>C&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>0.68 1.00 2.20</td>
<td>μF</td>
</tr>
</tbody>
</table>

Table 2. VREF pin output capacitor capacitance

(3-3) VREF pin protection function(21pin)
VREF pin built in low voltage protection function VREF UVLO (Under Voltage Protection).
This IC prevents from error operating at the time, VREF starts up and VREF is low, by this function.

Figure11. VREF UVLO Function
(3-4) Blown out function (1 pin)

BM1050AF is built in blown out function. This function is that this IC stops DCDC operating at the time when input AC voltage is low. Show the example figure 12. This IC divides input voltage by the resistance, and input P_BO pin.

This IC detects from circuit normal state, and starts DC/DC operation the time when P_BO pin exceeds Vbo1 (0.4V typ). ACDET=L after Tbo1 (typ. 32ms) or Tbo2 (typ. 128ms) from P_BO pin drops from Vbo2 (0.2V typ). Moreover, if Tbo3 (typ. 250ms) passes from P_BO < Vbo2, DC/DC part and PFC part is stopped.

About every resistance of figure 12, because P_BO pin is used PFC operation, please set Rbo1=4Mohm, Rbo2=16kohm for operating the range of P_BO pin voltage 0~1.8V. In this case, by the following formula, P_BO=0V~0.56V at the case AC100V, P_BO=0V~1.237V at the case AC220V.

\[
P_{BO} = \left(2 \times V_{AC}\right) \left(2 \times V_{F1}\right) \times \frac{R_{BO2}}{R_{BO1} + R_{BO2}}
\]

Then

\[
\sqrt{2} \times V_{AC} >> V_{F1}
\]

\[
P_{BO} = \sqrt{2} \times V_{AC} \times \frac{R_{BO2}}{R_{BO1} + R_{BO2}}
\]

![Figure 12. Block Diagram of Blown out Function](image)

A : P_BO > Vbo1 (typ. 0.4V) → ACDET=L→H
B : After 150us from A DC/DC part starts up.
C : QRF_FB < V_REF (typ. 2.6V) → PFC part starts up.
D : If PFC output is larger than constant voltage, ACTIMER=L→H.
E : P_BO < Vbo2 (typ. 0.2V) Timer start operation by detection blown out protection.
F : After Tbo1 (typ. 32ms) or Tbo2 (typ. 128ms) from E, ACDET=H→L. It is possible to set Tbo1 and Tbo2 at ACTIMER pin.
G : After Tbo3 (typ. 250ms) from E, DC/DC part and PFC part are OFF.

![Figure 13. Detection Way of Blown out Function](image)
(4) Controller part
(4-1) ACDET pin (8pin)
ACDET pin is NMOS open drain output. It monitors AC voltage, and is used for controlling secondary micon.
Show the using example figure 14, 15. Please set VIN is H voltage of micon.
ACDET=L : Abnormal state (P_BO < 0.2V)
ACDET=H : Normal state

Figure 14. Using Example of ACDET Pin

Figure 15. Explanation of ACDET Pin
Next, show an easy sequence.

Because P_BO < 0.4V, DC/DC part is OFF. VCC voltage > 13.5V

Figure 16. At applied AC Input Voltage (P_BO voltage < 0.4V)

Figure 17. At applied AC Input Voltage (P_BO voltage > 0.4V)
A: Detect $P_{BO}>0.4V$, Quasi resonance starts operation after 150μs
B: PFC start up
C: PFC output stabilized

*About PFC operation, by the micro, is able to be controlled using PFCON/OFF pin.

Figure 18. At AC Power Supply OFF

A: Detect $P_{BO}<0.2V$, internal ACDET timer operates. At this time, output of PWC downs.
B: After 32ms (ACTIMER=L) from the point A, ACDET pin voltage is H->L, send to the μ-controller abnormal signals.
C: After 250ms from the point of A, PFC and Quasi Resonant are stopped

Figure 19. At AC Power Supply the case of operation moment stop

The case of AC voltage is OFF suddenly, constant area is masked.
The time of constant area of masking is depends on ACTIMER pin.
The case of ACTIMER pin=L, Mask time=32ms, the case of ACTIMER pin=H, mask time=128ms.
The moment of AC voltage momentary power interruption, because PFC output voltage is down by corresponding to load, please watch out.
(4-3) PFCON/OFF pin

PFCON/OFF pin is NMOS gate input pin. Refer to following the functions.

An internal timer is integrated for noise protection on PFCON/OFF pin.
After $T_{PFCON/OFF}$ (typ. 1ms) from PFCON/OFF H→L, PFCON/OFF L operation starts. At PFCON/OFF L→H, internal timer is not integrated.

function1) PFC circuit operation is OFF control.

In order to reduce standby power, IC controls PFC part operation at PFCON/OFF pin.
function2) QR_SEL pin is Hi-z→L

Refer to example of using at figure 20.

PFCON/OFF=L : DC/DC part=ON, PFC part=ON, QR_SEL=Hi-Z
PFCON/OFF=H : DC/DC part=ON, PFC part=OFF, QR_SEL=L

---

Figure 20. Using example of PFCON/OFF pin
(4-4) LATCH/AUTOR pin

LATCH/AUTOR pin is NMOS gate input pin. Refer to example of using at figure21.

Table3. List of Protection Function Operation Setting by LATCH/AUTOR pin

<table>
<thead>
<tr>
<th>ITEM</th>
<th>Contents</th>
<th>LATCH/AUTOR=GND</th>
<th>LATCH/AUTOR=VREF</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREFUVLO</td>
<td>VREF PIN Low voltage protection function</td>
<td>VREF&lt;2.5V (VREF falling)</td>
<td>VREF&lt;2.5V (VREF falling)</td>
</tr>
<tr>
<td>VCCUVLO</td>
<td>VCC PIN Low voltage protection function</td>
<td>VCC&lt;7.0V (VCC falling)</td>
<td>VCC&lt;7.0V (VCC falling)</td>
</tr>
<tr>
<td>VCCOVP</td>
<td>VCC PIN Over voltage protection function</td>
<td>VCC&gt;27V state continues between 50us (VCC rising)</td>
<td>VCC&gt;27V state continues between 50us (VCC rising)</td>
</tr>
<tr>
<td>Blown out</td>
<td>Low voltage protection function</td>
<td>P_BO&lt;0.2V state continues between 200ms</td>
<td>P_BO&lt;0.2V state continues between 200ms</td>
</tr>
<tr>
<td>GR_FB OLPI</td>
<td>Over current protection function</td>
<td>GR_FB&lt;2.6V state continues between 200ns (GR_FB)</td>
<td>GR_FB&lt;2.6V state continues between 200ns (GR_FB)</td>
</tr>
<tr>
<td>GR_FB OLPI2</td>
<td>Over current protection function</td>
<td>P_FB&lt;0.2V state continues between 10us (P_FB)</td>
<td>P_FB&lt;0.2V state continues between 10us (P_FB)</td>
</tr>
<tr>
<td>QR, ZT OVP</td>
<td>Over voltage protection function</td>
<td>QR_ZT&lt;3.5V state continues between 150us (QR_ZT)</td>
<td>QR_ZT&lt;3.5V state continues between 150us (QR_ZT)</td>
</tr>
<tr>
<td>P, VS short protection</td>
<td>Short protection function</td>
<td>P, VS&lt;0.3V (P, VS)</td>
<td>P, VS&lt;0.3V (P, VS)</td>
</tr>
<tr>
<td>P, VS GAIN increasing</td>
<td>Low voltage gain increasing function</td>
<td>P, VS&lt;2.2V (P, VS)</td>
<td>P, VS&lt;2.2V (P, VS)</td>
</tr>
<tr>
<td>P, VS OVP2</td>
<td>Over voltage protection function</td>
<td>P, VS&lt;2.75V (P, VS)</td>
<td>P, VS&lt;2.75V (P, VS)</td>
</tr>
<tr>
<td>COMP function</td>
<td>COMP pin Protection function</td>
<td>COMP&lt;0.5V state continues between 150us (COMP)</td>
<td>COMP&lt;0.5V state continues between 150us (COMP)</td>
</tr>
</tbody>
</table>

*Comparator level of protection function is shown by TYP value.
(4-5) ACTIMER pin

ACTIMER pin is NMOS gate input pin. Show example of using figure 22, 23
Set the detect timer of AC voltage drop. (please refer to ACDET pin page)

ACTIMER=VREF : 128ms Timer
ACTIMER=GND : 32ms Timer

Figure 22. Using example of ACTIMER pin

![Diagram of ACTIMER pin configurations]

32ms (ACTIMER=GND) × Toff
128ms (ACTIMER=VREF) × Toff

AC Voltage

P_BO

[DC/DC] ON

[DQ/DC] ON

Constant Voltage

DC/DC Output Voltage 390V

PFC Output Voltage

Figure 23. AC power at the case momentary power interruption OFF
(4-6) COMP pin (external stop control function)

COMP pin is stop control pin. When COMP pin voltage drops from \( V_{\text{COMP}} \) (0.5V. typ), COMP pin stops PFC and DC/DC part operation.

This IC built in \( T_{\text{COMP}} \) (150us typ) until stopping switching, prevent from stopping by noise.

COMP pin in pull-up resistor \( R_{\text{COMP}} \) (25.9k\( \Omega \). typ), When COMP pin in the state of pull-down with lower resistance than \( R_r \) (3.70k\( \Omega \).typ), COMP pin detects abnormal. Show application examples at the figure 24, 25, and 26.

Temperature protection by NTC thermistor

By putting a thermister at the COMP pin, it is possible to stop latch on temperature rising.

The case of this application, please design thermister resistor is \( R_r \) (3.70k\( \Omega \).typ) on temperature detection. (Figure 24 and 25 is application circuit that latch on \( T_a=110^\circ\text{C} \))

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside.

Secondary over-voltage protection

This IC can detect secondary over-voltage by putting photo coupler to COMP pin.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside.

![Temperature Protection Application](image1)

![Temperature-Thermistor Resistor characteristic](image2)

![Output Over Voltage Protection Application](image3)

Table 4. Changes of COMP function Operation by LATCH/AUTOR pin

<table>
<thead>
<tr>
<th>ITEM</th>
<th>contents</th>
<th>LATCH/AUTOR=GND</th>
<th>LATCH/AUTOR=VREF</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>detection method</td>
<td>operation at detection</td>
</tr>
<tr>
<td>COMP function</td>
<td>COMP pin protection function</td>
<td>COMP-0.5V state continues between 150us (COMP falling)</td>
<td>PFC part, DC/DC part operation stops</td>
</tr>
</tbody>
</table>
(5) Quasi-Resonant DC/DC converter function

Part of quasi-resonant DC/DC uses PFM (Pulse Frequency Modulation) mode control. The QR_FB pin, QR_ZT pin and QR_CS pin are monitored to provide a system optimized for DC/DC. The switching MOSFET ON width (turn OFF) is controlled via the QR_FB pin and QR_CS pin, and the OFF width (turn ON). Show following detail explanation. (refer to figure27).

Figure27. Diagram of Quasi-resonant DC/DC Operation
(5-1) Determination of ON width (turn OFF)
ON width is controlled via the QR_FB pin and QR_CS pin. The QR_FB pin voltage is compared with the IC internal voltage \( V_{\text{lim1}} \) (1.0V typ) and, as is shown in Figure 28. And the comparator level changes linearly.

The QR_CS pin is also used for the pulse-by-pulse over current limiter circuit. By changing voltage at the QR_FB pin, DC/DC results in changes of the maximum blanking frequency and over-current limiter level.
- mode1: Burst operation
- mode2: Frequency reduction operation (reduces maximum frequency)
- mode3: Maximum frequency operation (operates at maximum frequency)
- mode4: Overload operation (pulse operation is stopped when overload is detected)

**Figure 28. Relation of QR_FB pin, over current limiter and maximum frequency**

The over current limiter level is adjusted when the input voltage is changed, operate the soft start function. In this case, the \( V_{\text{lim1}} \) and \( V_{\text{lim2}} \) values are as listed below.*

<table>
<thead>
<tr>
<th>Soft start</th>
<th>AC=100V</th>
<th>AC=230V</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( V_{\text{lim1}} )</td>
<td>( V_{\text{lim2}} )</td>
</tr>
<tr>
<td>Start~1ms</td>
<td>0.250V (25.0%)</td>
<td>0.039V (3.9%)</td>
</tr>
<tr>
<td>1ms~PFC Start &amp;4ms</td>
<td>0.750V (75.0%)</td>
<td>0.113V (11.3%)</td>
</tr>
<tr>
<td>PFC Start &amp; 4ms</td>
<td>1.000V (100.0%)</td>
<td>0.150V (15.0%)</td>
</tr>
</tbody>
</table>

*( ) is AC=100V, these show relative value of compare with \( V_{\text{lim1}} \) (1.0V typ) of normal operation. This table is separated AC100V and AC230V for the function of QR_CS current changing function that is shown \( 4-3 \).
(5-2) LEB (Leading Edge Blanking) function
When the switching MOSFET is turned ON, surge current occurs at each capacitor charge /discharge or drive current.
For that, QR_CS voltage rise temporarily, over current limiter may be detected errors.
To prevent detection errors blanking time is built in to mask T_LEB (typ=250ns).
This blanking function enables a reduction of CS pin filtering.

(5-3) CS over current protection function
When the AC input voltage (VHIN) is high, the ON time is reduced and the operating frequency increases. As a result, the maximum rated power is increased for a constant over current limiter level. As a countermeasure, DC/DC is switched over current detected level.
AC input voltage detection method is that monitoring QR_ZT current.
When MOSFET is turn ON, the auxiliary voltage (Va) is the minus voltage that depends on input voltage (VH).
QR_ZT pin is clamped about 0V internal IC.
Following is the formula for that case.
Refer to the block figure29. See the graph figure30 and 31.
$$I_{ZT} = \frac{(V_a - V_{zt1})}{R_{zt1}} \Rightarrow V_a/R_{zt1} = \frac{VH \cdot N_a/N_p}{R_{zt1}}$$
$$R_{zt1} = \frac{V_a}{I_{zt}}$$
For that, VH voltage is set by the resistance value of $R_{zt1}$. Then, QR_ZT bottom detection voltage is decided, Please set timing by $C_{zt}$.

![Diagram of CS switching current](image-url)
Figure 30. QR_CS Switching QR_FB Voltage VS QR_CS Voltage

Figure 31. QR_CS Switching Izt Current VS QR_CS Voltage

ex) setting method (operate changing AC100V and AC220V)
AC100V 141V±42V (±30% margin)
AC220V 308V±62V (±20% margin)
The case of above, Between 182V~246V, operates changing of CS current => Operate VH=214VH
Np=100, Na=15

V_a = V_x*N_a/N_p = 214V*15/100 *(-1) = -32.1V
R_zc = V_a/I_z = -32.1V/-1mA = 32.1kΩ

By the above explanation, R_zc=32KΩ

Figure 32. Example of Over current limiter of CS switching
(5-4) Determination of OFF width (turn ON)

OFF width is controlled at the QR\_ZT pin.
When switching is OFF, the power stored in the coil is supplied to the secondary-side output capacitor.
When this power supply ends there is no more current flowing to secondary side, so the switching MOS drain pin voltage drops.
Consequently, the voltage on the auxiliary coil side also drops.
A voltage that was resistance-divided from the QR\_ZT pin by $R_{zt1}$ and $R_{zt2}$ is applied. When this voltage level drops to $V_{zt1}(100\text{mV typ})$ or below, switching is turned ON the QR\_ZT comparator. Since bottom status is detected at the QR\_ZT pin, time constants are generated using $C_{zt}$, $R_{zt1}$, and $R_{zt2}$.
Additionally, a QR\_ZT trigger mask function (described in section 5-5) and a QR\_ZT time out function (described in section 5-6) are built in.

(5-5) QR\_ZT trigger mask function

The QR\_ZT trigger mask function is shown below figure33.
When switching is set ON -> OFF, super position of noise may occur at the QR\_ZT pin.
At such times, the QR\_ZT comparator is masked for the $T_{ztmask}$ time to prevent QR\_ZT comparator operation errors.

![Figure 33. ZT trigger mask Function](image)

A: QR\_OUT OFF=>ON
B: QR\_OUT ON=>OFF
C: Because of generation of QR\_ZT pin noise, $T_{ztmask}$ doesn’t operate the QR\_ZT comparator.
D: Same as A
E: Same as B
F: Same as C
G: Same as A
(5-6) ZT timeout function (Figure 34)

After the ZT comparator is detected, this function forcibly turns switching ON if the following is not detected, even when \( T_{\text{ztout}} \) (15us typ) has elapsed.

If, the secondary output voltage is low, the auxiliary coil voltage VA is reduced, and the QR\_ZT pin voltage drops below \( V_{\text{zt1}} \) (100mVtyp).

In such cases, this function turns switching ON forcibly.

As for \( T_{\text{ztout}} \), since 15 us (typ) = 66.7kHz, when the maximum frequency is in frequency reduction mode, the QR\_ZT timeout time depends on the frequency reduction mode.

Figure 34. ZT Time out Function

A: QR\_ZT < \( V_{\text{zt1}} \), DC/DC is ON. Count maximum frequency at this point.
B: DC/DC ON => OFF
C: Because noise is generated at QR\_ZT pin, \( T_{\text{ztmax}} \) doesn’t operate QR\_ZT comparator.
D: DC/DC OFF => ON
E: Same as B
F: Same as C
G: Count maximum frequency
H: Because 1cycle > \( T_{\text{ztout}} \), forcibly be DC/DC OFF => ON

(5-7) Soft start operations

Normally, when the power supply is turned ON, a large current flows to the AC/DC power supply. The BM1050AF builds-in a soft start function to prevent large changes in the output voltage and output current during startup.

This function is reset when the VCC pin voltage is at \( V_{\text{UVLO2}} \) (7.0V typ) or below, soft start is performed again at the next AC power-on.

During a soft start, the following post-startup operations are performed. (See turn OFF described in section 5-1)

Start to 1ms -> Set to 25% when CS limiter value is normal
1ms PFC normal status -> Set to 75% when CS limiter value is normal
(5-8) Overload protection function/Overload protection mode switching

The overload protection function monitors the overload status of the secondary output current at the FB pin, and fixes the OUT pin at low level when overload status is detected. During overload status, current no longer flows to the photocoupler, so the QR_FB pin voltage rises. When this status continues for the T_FOLP time (64ms typ), it is considered an overload, and the OUT pin is fixed at low level. Once the QR_FB pin voltage exceeds V_FOLP1 (2.8V typ), if it drops to lower than V_FOLP2 (2.6V typ) during the T_FOLP time (64ms typ), the overload protection timer is reset. At startup, the QR_FB voltage is pulled up to the internal voltage by pull-up resistor, and operation starts once the voltage reaches V_FOLP1 (2.8V typ) or above. Therefore, the design must set the QR_FB voltage at or below the V_FOLP1 (2.6V typ) voltage within the T_FOLP (64ms typ) time. In other words, the secondary output voltage start time must be set to within T_FOLP (64ms typ) after IC startup.

When an overload is detected, either auto recovery mode or latch mode can be selected for the BM1050AF. When pull-down resistance R_FOLP (100kΩ typ) is attached to QR_FB pin, latch mode is set. Do not attach any R_FOLP value other than 100kΩ typ, since that would prevent latching due to the IC7s internal resistance ratio.

To release latching after selecting latch mode, first unplug the power supply, and then set VCC<V_LATCH (typ=6.5V) to release latching.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside.

(5-9) QR_ZT pin OVP (Over Voltage Protection)

An OVP (Over Voltage Protection) function is built in for the QR_ZT pin. When the QR_ZT pin voltage reaches V_ZT (TYP=3.5V) overvoltage status is detected. QR_ZT pin OVP protection performed latch mode.

A mask time defined as T_LATCH (TYP=150us) is built in for the QR_ZT pin OVP function. When QR_ZT OVP status continues for 150us, overvoltage is detected. This function masks any surges (etc.) that occur at the pin. See the illustration in Figure 35. (Like VCC OVP, T_LATCH (TYP=150us) is built in)

(5-10) Quasi-resonant DC/DC block protection operation mode

Show every protection function operation mode table 6.

FB pin over load protection function is able to change LATCH/AUTOR by FB pin pull down resistance.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside.

<table>
<thead>
<tr>
<th>ITEM</th>
<th>Contents</th>
<th>Detection method</th>
<th>Operation at detection</th>
<th>Release method</th>
<th>Operation at detection</th>
</tr>
</thead>
<tbody>
<tr>
<td>QR_FB_OLP1</td>
<td>QR_FB pin over current protection function</td>
<td>QR_FB&gt;2.8V state continues 250ms (QR_FB rising)</td>
<td>DC/DC part operation stop</td>
<td>QR_FB&lt;2.6V (QR_FB falling)</td>
<td>normal operation</td>
</tr>
<tr>
<td>QR_FB_OLP2</td>
<td>QR_FB pin over current protection function</td>
<td>QR_FB&gt;3.6V (QR_FB rising)</td>
<td>DC/DC part operation stop</td>
<td>QR_FB&lt;3.4V (QR_FB falling)</td>
<td>normal operation</td>
</tr>
<tr>
<td>QR_ZT OVP</td>
<td>QR_ZT pin over voltage protection function</td>
<td>QR_ZT&gt;3.5V state continues 150us (QR_ZT rising)</td>
<td>DC/DC part operation stop</td>
<td>QR_ZT&lt;3.5V (QR_ZT falling)</td>
<td>normal operation</td>
</tr>
</tbody>
</table>

Table 6. Protection Circuit Operation Mode of Quasi-resonant DC/DC
(6) Power Factor Correction Circuit (PFC: Power Factor Correction) Part

Power Factor Correction Circuit is peak current control method of fixed frequency.

It is possible to supply proper system as PFC by monitoring P_VS pin, P_CS pin, and P_BO. It is possible to control the MOSFET ON width by monitoring output voltage at P_VS pin, AC input voltage at P_BO pin, and MOSFET current at P_CS pin.

The switching frequency is F_{PFC} (typ=65kHz), built in frequency hopping function (±4kHz), and contribute to low EMI. Following is detail explanation of PFC (reference figure 36).

Figure 36. Diagram of PFC block
(6-1) gm AMP

P_VS pin monitors a divide voltage between resistors of PFC output voltage. P_VS pin is piled up ripple voltage of AC frequency (50kHz/60kHz).

The gmAMP filters this ripple voltage and controls the voltage level of P_VSEO, by responding to error of P_VS pin voltage P_VS pin voltage and internal reference voltage V_{VSAMP} (typ 2.5V).

Please set cut-off frequency of filter at P_VSEO pin showed in figure 37, to about 5~10Hz.

Gm constant is designed 44[uA/V].

![Figure 37. Diagram of gmAMP](image)

(6-2) Monitor of input voltage

PFC is monitored AC input voltage at the P_BO pin.

Because the range of input voltage at P_BO pin is 0~1.8V, please select R_{bo1} and R_{bo2} to set P_BO voltage in the range.

Refer to block figure at figure38.

![Figure 38. Diagram of Input Voltage Monitor](image)
(6-3) Maximum power limiting function

PFC maximum power is also larger as input voltage is larger. To compensate this maximum power, PFC built-in Maximum power limiting. Maximum power is in proportion to the square of output of multiplier V_MULT, so it is possible to correct that maximum power depends on input voltage by dividing P_BO voltage by P_BOPK voltage which is peak voltage of P_BO pin.

Figure 39. Diagram of Maximum Power Restriction Function

(6-4) Multiplier

A multiplier is calculated gmAMP output voltage and P_BO pin voltage, and P_BOPK pin voltage. Following is formula of Multiplier output.

\[
V_{MULT} = \frac{K_1 \times V(P_{BO}) \times K_2 \times V(P_{VSEO})}{K_3 \times V(P_{BOPK})}
= K \times \frac{V(P_{BO}) \times V(P_{VSEO})}{V(P_{BOPK})}
\]

V_max: Multiplier output voltage  K: Multiplier constant

(6-5) Switching frequency

Switching frequency is averaged typ. 65kHz. MAX DUTY is D_max (typ 94%), always the period has OFF width. PFC built in frequency hopping function, frequency changes every 500us. The amplitude is F_{paxl} (typ=±4kHz) The cycle is F_{ch} (typ = 125Hz) (figure40). By this function, frequency spectrums are diffused, and contribute to low EMI.

Figure 40. Frequency Hopping Function
(6-6) LEB (Leading Edge Blanking) function

When the switching MOSFET is turned ON, surge current occurs at each capacitor charge/discharge or drive current. For that, P_CS voltage rise temporarily, over current limiter may be detected errors. To prevent detection errors blanking time is built in during T_{PLEB} (typ=250ns) from P_OUT pin changing L→H..

This blanking function enables a reduction of P_CS pin noise filter.

(6-7) Over current protection function

P_CS pin built in over current protection function for MOSFET. This function operates in pulse by pulse, and detects over current. Over current detection voltage is changed by P_BOPK pin voltage. Over current detection voltage is V_{PCS1} (typ = 1.16V) at P_BOPK voltage =0.56V, V_{PCS2} (typ = 0.60V) at P_BOPK voltage = 1.30V.

Show figure41 changing of over current detection voltage by P_BOPK pin voltage.

Over-current detection value I_{fcs} is decided I_{fcs} = V_{fcs}/R_s by external resistance R_s at figure42.

![Figure 41. Over-current detection Voltage - P_BOPK Voltage Peculiarity](image1)

![Figure 42. Diagram of Over current Protection](image2)

(6-8) P_VS short protection function

PFC built in short protection function at P_VS. Switching is stopped at P_VS voltage<V_{P_SHORT} (0.30Vtyp).

![Figure 43. P_VS Short Protection Operation](image3)
(6-9) Gain increase function in P_VS low voltage
Dropping output voltage by suddenly load change, because PFC voltage response is slow, output voltage is low for a long time. Therefore, PFC is speed up voltage control loop gain when P_VS pin voltage is low up to V_PGUP (typ = 2.25V)(Output voltage - 10%). In the operation, ON-duty at P_OUT pin increases, PFC prevents from output voltage dropping for a long time. This operation is stopped when P_VS pin voltage is upper than V_OUP (typ=2.25V).

(6-10) P_VS first over voltage protection function
In case of output voltage is rise by starting up or output load suddenly change, because PFC voltage response is slow, output voltage is high for a long time. Therefore, PFC is speed up voltage control loop gain when P_VS pin voltage is rise V_P_OVP1 (typ=2.625). In this operation, ON-duty at P_OUT pin decrease, PFC prevents from output voltage rising for a long time. This operation is stopped when P_VS pin voltage is lower than V_P_OVP1 (typ=2.625V).

(6-11) P_VS second over voltage protection function
PFC built in second over voltage protection, for the case that P_VS voltage exceeds over first over voltage protection voltage V_P_OVP1. It is possible to switch Latch protection (LATCH/AUTOR=H) or auto recovery (LATCH/AUTOR=L) by LATCH/AUTOR pin. In case of latch operation, P_VS pin voltage exceeds V_P_OVP2 (typ=2.725V)(output voltage pulse 9%) during T_P_OVP2 (Typ=32ms), PFC switching is stopped.

In case of auto recovery, P_VS pin voltage is exceeded V_P_OVP2 (typ=2.725V), switching is stopped instantly. When P_VS pin voltage decrease lower than V_P_OVP2 (typ=2.725V), switching operation is re-start. Refer to figure44.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside.

Figure 44. VS Second Over Voltage Protection (at auto recovery mode)

Figure 45. Operation of P_VS Second Over Voltage Protection (at latch mode)

Switching is stopped by second over voltage protection in the case that the P_VS pin loop of output voltage is open loop.
(6-12) PFC burst operation

PFC built-in burst operation for preventing PFC output voltage from rising at light load. This function is that PFC monitors $P_{\text{VSEO}}$ pin at light load, switched burst operation or not. Burst operation voltage depends on $P_{\text{BOPK}}$ voltage.

In case of $P_{\text{BOPK}}$ voltage = 0.56V, burst function operates when $P_{\text{VSEO}}$ voltage is lower than $V_{\text{SEO}}=V_{\text{P_BURST}}$ (0.266V typ). In case of $P_{\text{BOPK}}$ voltage = 1.30V, burst function operates when $P_{\text{VSEO}}$ voltage is lower than $V_{\text{SEO}}=V_{\text{P_BURST1}}$ (0.128V typ).

Refer to the change of burst voltage for $P_{\text{BOPK}}$ voltage figure46.

![Figure 46. Diagram of $P_{\text{VSEO}}$ burst voltage by $P_{\text{BOPK}}$ voltage](image)

(6-13) Operation mode of PFC block protection

Show operation mode every protection function at Table7.

(Note) When the latch mode is used, it is necessary to apply 3.5V~4.5V to VREF terminal from the outside.

Table 7. Protection Circuit Operation mode of PFC

<table>
<thead>
<tr>
<th>ITEM</th>
<th>contents</th>
<th>LATCH/AUTOR=GND</th>
<th>LATCH/AUTOR=VREF</th>
</tr>
</thead>
<tbody>
<tr>
<td>P_VS SHORT PROTECTION</td>
<td>$P_{\text{VSM}}$ short protection function</td>
<td>$P_{\text{VSM}}&lt;0.30V$ ($P_{\text{VSM}}$ falling)</td>
<td>$P_{\text{VSM}}$ operation stop</td>
</tr>
<tr>
<td>P_VS GAIN INCREASING</td>
<td>$P_{\text{VSM}}$ low voltage gain increasing function</td>
<td>$P_{\text{VSM}}&lt;2.25V$ ($P_{\text{VSM}}$ falling)</td>
<td>$P_{\text{VSM}}$ gain INCREASE</td>
</tr>
<tr>
<td>P_VS OVP1</td>
<td>$P_{\text{VSM}}$ over voltage protection function1</td>
<td>$P_{\text{VSM}}&lt;2.725V$ ($P_{\text{VSM}}$ falling)</td>
<td>$P_{\text{VSM}}$ operation stop</td>
</tr>
<tr>
<td>P_VS OVP2</td>
<td>$P_{\text{VSM}}$ over voltage protection function2</td>
<td>$P_{\text{VSM}}&lt;2.725V$ ($P_{\text{VSM}}$ falling)</td>
<td>$P_{\text{VSM}}$ operation stop</td>
</tr>
</tbody>
</table>
- Basic Characteristics  (This data is for reference only and is not guaranteed.)

Fig-47-1 Circuit current (ON) 1
Fig-47-2 Circuit current (ON) 2
Fig-47-3 Circuit current (ON) 3

Fig-47-4 Start current 1
Fig-47-5 Start current 2
Fig-47-6 OFF Current

Fig-47-7 VH voltage switched start current
Fig-47-8 VREF output voltage
Fig-47-9 GCLAMP voltage 1

Fig-47-10 VCC UVLO voltage 1
Fig-47-11 VCC UVLO voltage 2
Fig-47-12 VCC OVP voltage 1

Fig-47-13 VCC OVP voltage 2
Fig-47-14 Brown out detection voltage 1
Fig-47-15 Brown out detection voltage 2
### Basic Characteristics

This data is for reference only and is not guaranteed.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Brown out hysteresis</td>
<td><img src="image1" alt="Graph" /></td>
</tr>
<tr>
<td>Brown out detection delay time</td>
<td><img src="image2" alt="Graph" /></td>
</tr>
<tr>
<td>Brown out detection delay time 2</td>
<td><img src="image3" alt="Graph" /></td>
</tr>
<tr>
<td>Brown out detection delay time 3</td>
<td><img src="image4" alt="Graph" /></td>
</tr>
<tr>
<td>ACDet ON resistor</td>
<td><img src="image5" alt="Graph" /></td>
</tr>
<tr>
<td>ACTimer input level</td>
<td><img src="image6" alt="Graph" /></td>
</tr>
<tr>
<td>Latch/Autor input level</td>
<td><img src="image7" alt="Graph" /></td>
</tr>
<tr>
<td>COMP pin detection voltage</td>
<td><img src="image8" alt="Graph" /></td>
</tr>
<tr>
<td>COMP pin pull-up resistor</td>
<td><img src="image9" alt="Graph" /></td>
</tr>
<tr>
<td>External Thermistor resistor</td>
<td><img src="image10" alt="Graph" /></td>
</tr>
</tbody>
</table>
Basic Characteristics (This data is for reference only and is not guaranteed.)

- Latch mask time
- QR_FB pin pull-up resistance
- CS over-current detect voltage 1A
- CS over-current detect vol. 1B
- CS over-current detect vol. 1C
- CS over-current detect vol. 1D
- Minimum ON width
- Maximum operating frequency 1
- Maximum operating frequency 2
- Freq. reduction start FB voltage
- Freq. reduction end FB voltage
- Voltage gain
• Basic Characteristics  (This data is for reference only and is not guaranteed.)

Fig-47-46  ZT comparator voltage 1  
Fig-47-47  ZT trigger timeout period  
Fig-47-48  Soft start time

Fig-47-49  FB OLP  Voltage 1a  
Fig-47-50  FB OLP  Voltage 2a  
Fig-47-51  FB OLP timer

Fig-47-52  ZT OVP Voltage  
Fig-47-53  QR_OUT pin PMOS ON resistor  
Fig-47-54  QR_OUT pin NMOS ON resistor

Fig-47-55  P_VS pin pull-up current  
Fig-47-56  Gm amplifier normal voltage  
Fig-47-57  Gm amplifier trans-conductance

Fig-47-58  Max. Gm amplifier source current  
Fig-47-59  Max. Gm amplifier sink current  
Fig-47-60  P_VSEO stop voltage1
● Basic Characteristics  (This data is for reference only and is not guaranteed.)

Fig-47-61  P_VSEO stop voltage 2  
Fig-47-62  PFC Oscillation frequency  
Fig-47-63  PFC Min. Pulse width

Fig-47-64  PFC Maximum DUTY  
Fig-47-65  P_CS over current limit voltage1  
Fig-47-66  P_CS over current limit voltage 2

Fig-47-67  P_VS short protection voltage  
Fig-47-68  P_VS gain rise voltage  
Fig-47-69  P_VS gain fall voltage

Fig-47-70  P_VS over voltage protection voltage  
Fig-47-71  P_VS over voltage protection timer

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43/47
10.Apr.2015 Rev.003
● Thermal loss
The thermal design should set operation for the following conditions.
(Since the temperature shown below is the guaranteed temperature, be sure to take a margin into account.)

1. The ambient temperature $T_a$ must be 85$^\circ$C or less.
2. The IC’s loss must be within the allowable dissipation $P_d$.

The thermal abatement characteristics are as follows. (Figure 47)

![Figure 48. SOP24 Temperature reduction peculiarity]
Use-related cautions

(1) Absolute maximum ratings
Damage may occur if the absolute maximum ratings such as for applied voltage or operating temperature range are exceeded, and since the type of damage (short, open circuit, etc.) cannot be determined, in cases where a particular mode that may exceed the absolute maximum ratings is considered, use of a physical safety measure such as a fuse should be investigated.

(2) Power supply and ground lines
In the board pattern design, power supply and ground lines should be routed so as to achieve low impedance. If there are multiple power supply and ground lines, be careful with regard to interference caused by common impedance in the routing pattern. With regard to ground lines in particular, be careful regarding the separation of large current routes and small signal routes, including the external circuits. Also, with regard to all of the LSI’s power supply pins, in addition to inserting capacitors between the power supply and ground pins, when using capacitors there can be problems such as capacitance losses at low temperature, so check thoroughly as to whether there are any problems with the characteristics of the capacitor to be used before determining constants.

(3) Ground potential
The ground pin’s potential should be set to the minimum potential in relation to the operation mode.

(4) Pin shorting and attachment errors
When attaching ICs to the set board, be careful to avoid errors in the IC’s orientation or position. If such attachment errors occur, the IC may become damaged. Also, damage may occur if foreign matter gets between pins, between a pin and a power supply line, or between ground lines.

(5) Operation in strong magnetic fields
Note with caution that these products may become damaged when used in a strong magnetic field.

(6) Input pins
In IC structures, parasitic elements are inevitably formed according to the relation to potential. When parasitic elements are active, they can interfere with circuit operations, can cause operation faults, and can even result in damage. Accordingly, be careful to avoid use methods that enable parasitic elements to become active, such as when a voltage that is lower than the ground voltage is applied to an input pin. Also, do not apply voltage to an input pin when there is no power supply voltage being applied to the IC. In fact, even if a power supply voltage is being applied, the voltage applied to each input pin should be either below the power supply voltage or within the guaranteed values in the electrical characteristics.

(7) External capacitors
When a ceramic capacitor is used as an external capacitor, consider possible reduction to below the nominal capacitance due to current bias and capacitance fluctuation due to temperature and the like before determining constants.

(8) Thermal design
The thermal design should fully consider allowable dissipation (Pd) under actual use conditions.

Also, use these products within ranges that do not put output Tr beyond the rated voltage and ASO.

(9) Rush current
In a CMOS IC, momentary rush current may flow if the internal logic is undefined when the power supply is turned ON, so caution is needed with regard to the power supply coupling capacitance, the width of power supply and GND pattern wires, and how they are laid out.

(10) Handling of test pins and unused pins
Test pins and unused pins should be handled so as not to cause problems in actual use conditions, according to the descriptions in the function manual, application notes, etc. Contact us regarding pins that are not described.

(11) Document contents
Documents such as application notes are design documents used when designing applications, and as such their contents are not guaranteed. Before finalizing an application, perform a thorough study and evaluation, including for external parts.
BM1050AF-G

**Ordering Information**

<table>
<thead>
<tr>
<th>Product name</th>
<th>Package</th>
<th>Packaging and forming specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>BM 1050 AF</td>
<td>F : SOP24</td>
<td>E2: Embossed tape and reel</td>
</tr>
</tbody>
</table>

**Physical Dimension Tape and Reel Information**

- Tape: Embossed carrier tape
- Quantity: 2000pcs
- Direction of feed: E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

**Marking Diagram**

- 1PIN
- LOT No
<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.Feb.2014</td>
<td>002</td>
<td>Correction of errors</td>
</tr>
<tr>
<td>11.Apr.2015</td>
<td>003</td>
<td>P13, P16, P17, P23, P25, P31, P32, P37, P38</td>
</tr>
<tr>
<td>11.Apr.2015</td>
<td>003</td>
<td>The note external application of VREF when the latch mode is used.</td>
</tr>
<tr>
<td>11.Apr.2015</td>
<td>003</td>
<td>P12 Figure4-&gt;Figure6 (Reference of start-up time)</td>
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<td>11.Apr.2015</td>
<td>003</td>
<td>P25 Figure25-&gt;Figure24</td>
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<tr>
<td>11.Apr.2015</td>
<td>003</td>
<td>P25 Figure26-&gt;Figure25</td>
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</tbody>
</table>
Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM’s Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

<table>
<thead>
<tr>
<th>JAPAN</th>
<th>USA</th>
<th>EU</th>
<th>CHINA</th>
</tr>
</thead>
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<tr>
<td>CLASS III</td>
<td>CLASS III</td>
<td>CLASS II b</td>
<td>CLASS III</td>
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<tr>
<td>CLASS IV</td>
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</tbody>
</table>

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   a. Installation of protection circuits or other protective devices to improve system safety
   b. Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM’s Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc., prior to use, must be necessary:
   a. Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   b. Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   c. Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   d. Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   e. Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   f. Sealing or coating our Products with resin or other coating materials
   g. Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   h. Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification
Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - the temperature or humidity exceeds those recommended by ROHM
   - the Products are exposed to direct sunshine or condensation
   - the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM’s internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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