AS3940

2.4 GHz Low Power Multi-Channel FSK Transceiver

1 General Description

The AS3940 is a highly integrated low power FSK transceiver for wireless communication in the worldwide 2.4 GHz ISM band. It supports data transfer in burst mode and streaming mode at data rates up to 2 Mbit/s.

All communication with a MCU and all configuration of the transceiver can be done using a bidirectional 4 pin serial data interface (SDI).

The integrated timers and link manager enable very low average current consumption in operation and standby and help to reduce overall system cost by eliminating the need for a complex microcontroller (MCU).

Optimum MCU clock frequency can be obtained from a programmable glitch-free clock output derived from the 16 MHz reference crystal oscillator.

The integrated link manager controls all power management modes, like power-down, standby, sleep, wakeup, and data mode, which enable to save power.

The link manager handles all data and frame management in a star network (one master and up to 8 clients) using four separate 256-bit data buffers; two for RX and two for TX. This decreases MCU workload and ensures a smooth data transfer and correct protocol handling. All low level transmission codec and CRC generation is done internally. Microcontroller controlled data transfer (MCDT) mode enables support of proprietary protocols.

Excellent blocking and sensitivity, pseudorandom allocation of communication time slots and the adaptive channel switching enable reliable data transmission and high resistance to interferers like WLAN or Bluetooth.

The high level of integration eliminates the need for external components like battery monitoring circuitry, additional high frequency crystal, and power-on-reset circuitry.

The product is available in a QFN 32 pin (5mm x 5mm) package.

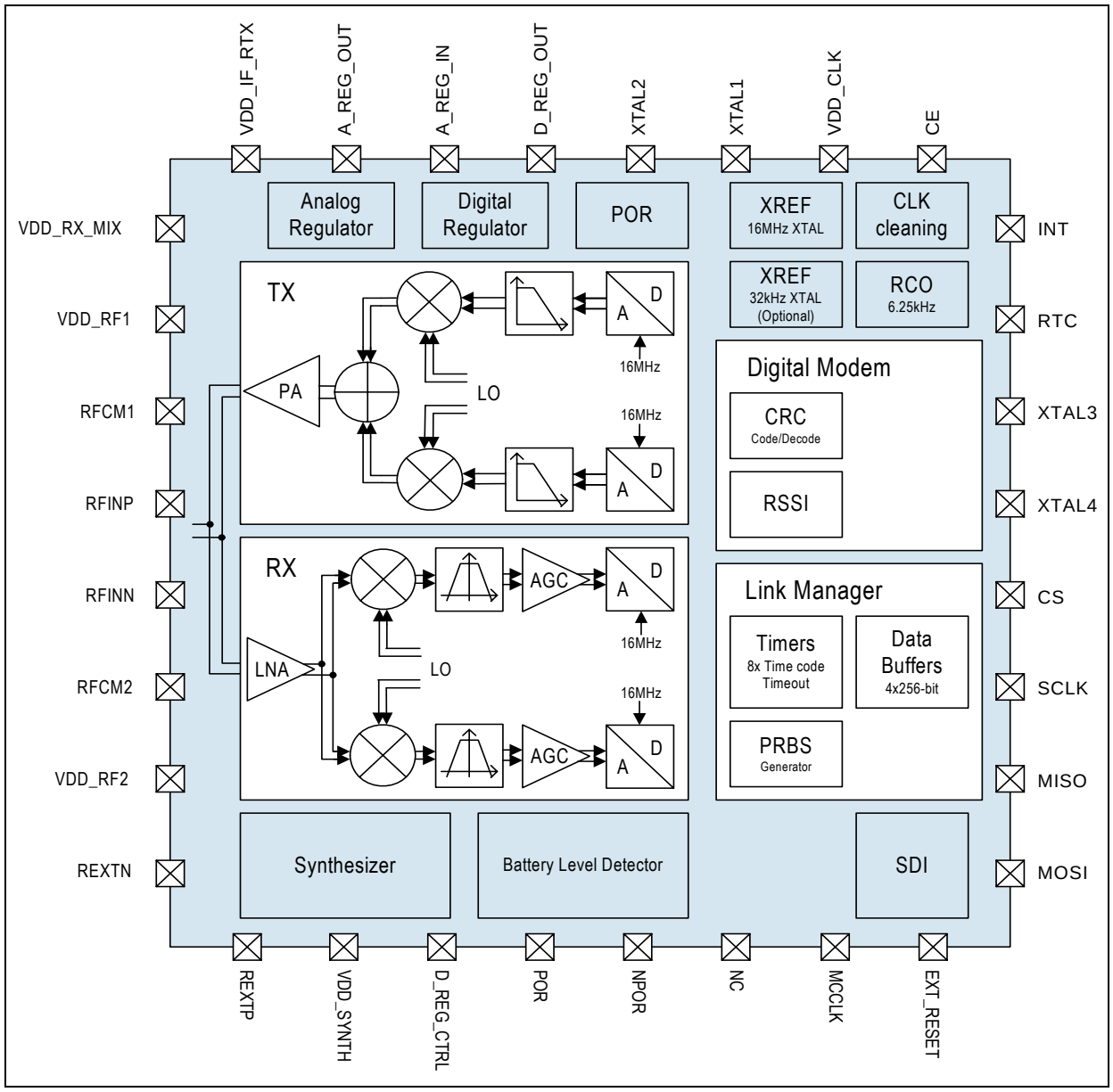
2 Key Features

- Fully integrated FSK transceiver
- Operating frequency 2405 to 2480 MHz
- Minimum channel spacing 1MHz
- Data rates in burst mode 250, 1000, 2000 kbps
- Net data rate in streaming mode up to 1000 kbps
- Sensitivity of -100dBm@250kbps, -95.5dBm@1000kbps, and -92.5dBm@2000kbps
- Excellent adjacent channel rejection and blocking performance
- Package synchronized digital RSSI
- Integrated real-time-clock (RTC), 32 kHz XTAL oscillator / calibrated 6.25 kHz derived from a RCO
- Glitch-free CMOS compatible reference clock output 8/4/2/1 MHz or 6.25 kHz
- Output power programmable in 3dB steps (-24 dBm to 0 dBm)
- Integrated Gaussian filter, PLL and loop filter
- 4 separate 256-bit user data buffers (2 x RX, 2 x TX)
- Power on reset (POR, NPOR) for reliable system start
- Battery voltage detection
- Link manager for reliable control of star network (up to 8 clients)
- Device ID recognition and 16-bit CRC computation
- Pairing and automatic (re-)synchronization
- Power-optimized wakeup modes
- Programmable auto-acknowledgement and re-transmit
- Adaptive channel switching / support of frequency hopping
- Programmable timers to define time slots for communication
- Pseudorandom allocation of time slots

3 Applications

The AS3940 is ideal for low-power short range devices, body area networks (health, fitness), simple control networks (industry, home), and interactive remote controls.

Figure 1. Block diagram AS3940



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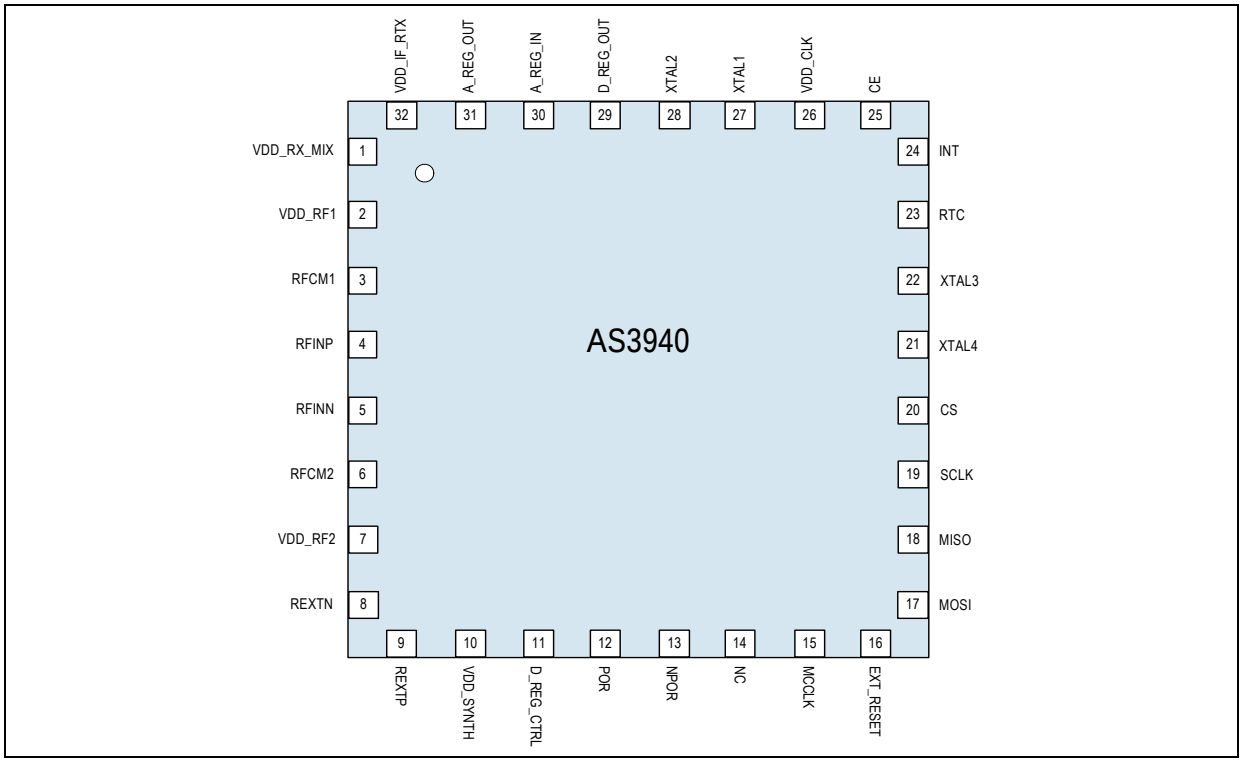
4 Pin Assignment

Figure 2. Pin Assignment



4.1 Pin Description

Table 1. Pin Description

Pin Name	Pin Number	Pin Type	Supply	Description
VDD_RX_MIX	1	S	Voltage input 1.9V ± 0.1V	VDD for IF part of RX and BB part of TX
VDD_RF1	2	S	Voltage input 1.9V ± 0.1V	VDD for LNA and PA
RFCM1	3	AIO	Voltage output TX: 1.9V RX: ≈170mV	Common Mode voltage output for matching network
RFINP	4	AIO	200Ω differential	Antenna input/output
RFINN	5	AIO	200Ω differential	Antenna input/output
RFCM2	6	AIO	Voltage output TX: 1.9V RX: ≈170mV	Common Mode voltage output for matching network
VDD_RF2	7	S	Voltage input 1.9V ± 0.1V	VDD for LNA and PA
REXTN	8	AIO	560 Ω	External resistor for biasing
REXTP	9			
VDD_SYNTH	10	S	Voltage input 1.9V ± 0.1V	VDD for synthesizer

Table 1. Pin Description

Pin Name	Pin Number	Pin Type	Supply	Description
D_REG_CTRL	11	S	Voltage input If GND --> D_REG_OUT= 1.6V	When tied to ground, the digital regulator is forced to 1.6V typ. supply voltage even during the device read access.
			If NC or A_REG_OUT --> D_REG_OUT= 1.65Vmin during the device read	When left unconnected or tied high to the analog regulator output (1.9V typ.), the digital regulator will increase its voltage to at least 1.65V worst case (1.7V typ.) during the device read access.
POR	12	AIO		Digitally delayed POR active high
NPOR	13	AIO		Digitally delayed POR active low
NC	14			
MCCLK	15	DO		Clock for MCU (8/4/2/1 MHz or 6.25 kHz)
EXT_RESET	16	DI		Reset signal from MCU, active low
MOSI	17	DI		SPI Master out slave in
MISO	18	DO_T		SPI Master in slave out
SCLK	19	DI		SPI clock
CS	20	DI		SPI chip select, active low
XTAL4	21	AIO		XTAL
XTAL3	22	AIO		XTAL
RTC	23	DO		Real time clock/RCO (32/6.25 kHz)
INT	24	DO		Interrupt to MCU, active low
CE	25	DI		Chip enable, active high
VDD_CLK	26	S	Voltage input 1.9V ± 0.1V	VDD for XTAL oscillator or clock divider, and ADC
XTAL1	27	AIO		XTAL sense 27pF to ground
XTAL2	28	AIO		XTAL drive 33pF to ground
D_REG_OUT	29	S	1.6V	decoupling pin for digital VDD
A_REG_IN	30	S	2.2 → 3.6V	Positive Supply voltage
A_REG_OUT	31	S	Voltage output 1.9V ± 0.1V	Stabilized analog supply voltage output
VDD_IF_RTX	32	S	Voltage input 1.9V ± 0.1V	VDD for IF strip, TX mixers and both I/Q dividers
Exposed Pad			GND	Exposed Pad must me grounded

Note: The following are the Pin Types

- S: supply pad
- AIO: analog I/O
- DI: digital input
- DO_T: digital output / tristate
- DO: digital output

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 8 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Note
DC supply voltage (V_{DD})	-0.5	3.6	V	Only a_reg_in
Input pin voltage (V_{IN})	-0.5	3.6	V	Only digital I/O, XTAL3, XTAL4, POR, NPOR. The rating for the remaining analog I/O's is 2V. V_{in} should not exceed V_{DD} + 0.5V.
Input current (latchup immunity) I_{scr}	-100	100	mA	Norm: Jedec 78
ESD for digital pins (ESDO)	±2		kV	Norm: MIL 883 E method 3015 (Human Body Model)
ESD for analog pins (ESDA)	±2		kV	Norm: MIL 883 E method 3015 (Human Body Model)
ESD for RF pins (ESDRF)	±2		kV	Norm: MIL 883 E method 3015 (Human Body Model)
Storage temperature (T_{strg})	-55	125	ºC	
Package body temperature (T_{body})		260	ºC	Norm: IPC/JEDEC J-STD-020C [1,2]
Humidity non-condensing	5	85	%	

1. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices”.
2. The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn).

6 Electrical Characteristics

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Recommended Operating Conditions						
V_{DD}	Positive Supply voltage[1]		2.2	3.0	3.6	V
$V_{DDRIPPLE}$	Positive Supply voltage ripple				2	mV_{pp}
T_{AMB}	Ambient temperature		-40		85	°C
	Chip temperature		-40		95	°C
f_{clk}	System clock frequency		16			MHz
Current Consumption Specifications						
I_{PD}	POWER-DOWN mode	Leakage currents, weak digital regulator running		1.5		µA
I_{SLEEP}	SLEEP mode, 32kHz XTAL	If clock provided to the RTC pin, additional current is 0.3µA + 0.1µA/pF		4.1		µA
I_{SLEEP}	SLEEP mode, RCO	If clock provided to the RTC pin, additional current is 0.3µA + 0.1µA/pF		2.9		µA
I_{SB}	STANDBY mode	Weak digital regulator, strong digital regulator, analog regulator and 16MHz XTAL are active		2.0		mA
I_{RX}	RX mode			20.9		mA
I_{TX} @ 0dBm	TX mode, 0dBm			21.5		mA
I_{TX} @ -3dBm	TX mode, -3dBm			19.3		mA
I_{TX} @ -24dBm	TX mode, -24dBm			14.7		mA
Characteristics for Digital Inputs and Outputs						
CMOS input						
V_{IH}	High level input voltage		2		3.6	V
V_{IL}	Low level input voltage		-0.3		0.8	V
I_{LEAK}	Input leakage current	At V_I = 3.3V or 0V	-10		10	µA
CMOS output						
V_{OH}	High level output voltage	At I_{LOAD}= 1mA	V_{DD} - 0.6			V
V_{OL}	Low level output voltage	At I_{LOAD}= 1mA			0.4	V
C_L	Capacitive load				50	pF
Tristate CMOS output						
V_{OH}	High level output voltage		V_{DD} - 0.6			V
V_{OL}	Low level output voltage				0.4	V
I_{OZ}[2]	Tristate leakage current	At V_O = 3.3V or 0 V	-10		10	µA

1. The AS3940 is functional down to minimum positive supply voltage of 2.0V, but specifications are not guaranteed
2. The input voltage and the voltage forced on a tristate output should not exceed V_{DD} + 0.3 V in order to meet the 10µA leakage requirement at low supply voltages.

6.1 Electrical System Specifications

Table 4. Electrical System Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
Modulation						
	Modulation method	BT=0.5		GFSK		
	Frequency range		2405		2480	MHz
	Bit rate			250		kbps
				1000		kbps
				2000		kbps
	Frequency deviation			160		kHz
				320		kHz
				400		kHz
				800		kHz
	Payload data size	Programmable with 1-Byte steps	8		256	bits
Receiver[1]						
Sensitivity						
	@ 250kbps	f_dev = 160kHz		-100.0		dBm
	@ 1Mbps	f_dev = 160kHz		-89.0		dBm
		f_dev = 400kHz		-95.5		dBm
	@ 2Mbps	f_dev = 320kHz		-85.5		dBm
		f_dev = 800kHz		-92.5		dBm
Blocking[2]		C/I C = Sensitivity + 3dB				
DR = 250kbps, f_dev = 160kHz						
	0 MHz	CW interferer		10.0		dB
	0 MHz	Modulated interferer		10.0		dB
	± 1MHz	CW interferer		-25.0		dB
	± 1MHz	Modulated interferer		-25.0		dB
	± 2MHz	CW interferer		-45.0		dB
	± 2MHz	Modulated interferer		-30.0		dB
	± 3MHz	CW interferer		-40.0		dB
	± 3MHz	Modulated interferer		-45.0		dB
DR = 1000kbps, f_dev = 160kHz						
	0 MHz	CW interferer		3.0		dB
	0 MHz	Modulated interferer		13.0		dB
	± 1MHz	CW interferer		-20.0		dB
	± 1MHz	Modulated interferer		0.0		dB
	± 2MHz	CW interferer		-30.0		dB
	± 2MHz	Modulated interferer		-20.0		dB
	± 3MHz	CW interferer		-40.0		dB

Table 4. Electrical System Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
	± 3MHz	Modulated interferer		-25.0		dB
DR = 1000kbps, f_dev = 400kHz						
	0 MHz	CW interferer		10.0		dB
	0 MHz	Modulated interferer		10.0		dB
	± 2MHz	CW interferer		-40.0		dB
	± 2MHz	Modulated interferer		-20.0		dB
	± 4MHz	CW interferer		-25.0		dB
	± 4MHz	Modulated interferer		-20.0		dB
	± 6MHz	CW interferer		-55.0		dB
	± 6MHz	Modulated interferer		-55.0		dB
DR = 2000kbps, f_dev = 320kHz						
	0 MHz	CW interferer		3.0		dB
	0 MHz	Modulated interferer		12.0		dB
	± 2MHz	CW interferer		-20.0		dB
	± 2MHz	Modulated interferer		0.0		dB
	± 4MHz	CW interferer		-30.0		dB
	± 4MHz	Modulated interferer		-20.0		dB
	± 6MHz	CW interferer		-45.0		dB
	± 6MHz	Modulated interferer		-35.0		dB
DR = 2000kbps, f_dev = 800kHz						
	0 MHz	CW interferer		10.0		dB
	0 MHz	Modulated interferer		10.0		dB
	± 3MHz	CW interferer		-15.0		dB
	± 3MHz	Modulated interferer		-15.0		dB
	± 6MHz	CW interferer		-50.0		dB
	± 6MHz	Modulated interferer		-30.0		dB
	± 9MHz	CW interferer		-55.0		dB
	± 9MHz	Modulated interferer		-55.0		dB
	Maximum input signal			10.0		dBm
	IP3	Measured at the balun input with two carriers of -33dBm		-15		dBm
RSSI						
	RSSI start			-95.0		dBm
	RSSI stop			-35.0		dBm
	RSSI accuracy			±2		dB
	RSSI linearity			±0.5		dB
	RSSI resolution			0.2		dB

Table 4. Electrical System Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
Transmitter[3]						
	TX output power	Programmable in 3dB steps down to -24dBm	-24	0	1.5	dBm
Spurious Emissions according to ETSI EN 300 440						
	25MHz…1000MHz (RBW=1MHz)	max -36dBm (operation)		-85		dBm
		max -57dBm (standby)		-85		
	47MHz…74MHz, 87,5MHz…118MHz, 174MHz…230MHz, 470MHz…862MHz (RBW=100kHz)	max -54dBm (operation)		-85		dBm
		max -57dBm (standby)		-85		
	Otherwise >1000MHz	max -30dBm (operation)		-75 @2nd Harm		dBm
				-55 @3rd Harm		
		max -47dBm (standby)		-70		
Spurious Emissions according to FCC CFR47 Section 15.249						
	Forbidden bands <960MHz (RBW=120kHz)	max -49 dBm		-85		dBm
	Forbidden bands 960-1000 MHz (RBW=120kHz)	max -41 dBm		-85		dBm
	Forbidden bands 1000MHz...2400MHz (RBW=1MHz)	max -41dBm fc=2405MHz (modulated signal)		-45 @2389 MHz		dBm
	Forbidden bands 2483.5MHz...∞ (RBW=1MHz)	max -41dBm fc=2480MHz (modulated signal, CW for harmonics)		-45 @2496 MHz		dBm
				-75 @2nd Harm		
				-55 @3rd Harm		
Spurious Emissions according to ARIB STD-T66						
	<2387MHz (RBW=1MHz)	max -26dBm fc=2405MHz (CW signal)		-60		dBm
	2387-2400MHz (RBW=1MHz)	max -16dBm fc=2405MHz (CW signal)		-70		dBm
	2483.5-2496.5MHz (RBW=1MHz)	max -16dBm fc=2480MHz (CW signal)		-65		dBm
	>2496.5MHz (RBW=1MHz)	max -26dBm fc=2480MHz (CW signal)		-75 @2nd Harm		dBm
				-55 @3rd Harm		
Synthesizer						
F_{synth}	Frequency range		2405		2480	MHz
	Synthesizer Resolution			1		MHz

Table 4. Electrical System Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
CNR@100kHz	LO Phase noise			-71		dBc/Hz
CNR@1MHz				-91		dBc/Hz
CNR@4MHz				-103		dBc/Hz
CNR@10MHz				-111		dBc/Hz
t_{lock}	PLL Lock time	From channel change or RX/TX switch		120		µs
Crystal Oscillator 32 kHz						
	Recommended crystal accuracy (initial)	-0.034 ppm/K^2 temperature coefficient not assumed			±20	p.p.m.
	Recommended frequency			32.768		kHz
	Maximum contribution of the oscillator to the frequency error			±10		p.p.m
	Minimum Start-up Time			100		ms
	Typical Start-up Time			384		
	Maximum Start-up Time			1000		
	Duty cycle			50		%
	Duty cycle Variation			±20		%
Crystal Oscillator 16 MHz						
	Recommended crystal accuracy	(initial + temp + ageing)			±40	p.p.m.
	Recommended frequency			16		MHz
	Maximum contribution of the oscillator to the frequency error			±9		p.p.m
	Phase noise at 10kHz distance (noise floor)	simulated at the output of a noiseless pulse former that only responds to the rising edge		-126		dBc/Hz
	Duty cycle, full settled			50		%
	Duty cycle Variation, full settled			±5		%
	Start-up time, full settled	Depends on crystal properties[4]		700		µs
	Maximum Start-up time, full settled			2000		
RC Oscillator 6.25 kHz						
	Frequency, calibrated			6.25		kHz
	Maximum frequency error of the calibrated RC Oscillator (without the 16MHz crystal error)			100		p.p.m
	Typical temperature coefficient of the period time	Specified over 10°C sub-ranges near 25°C and near the temperature extremes		-20		ppm/K
	Maximum temperature coefficient of the period time			±200		
	Maximum Start-up time			700		µs

1. All RX measurements have been performed with external matching network (see Figure 18).
2. The level of the wanted signal C is set 3dB above the sensitivity level.
3. All TX measurements have been performed with external matching network (see Figure 18).

4. When the AS3940 wakes up, first the analog voltage regulator is enabled, after it settles the digital regulator is enabled and after that settles the crystal oscillator is enabled. When the AS3940 powers down, all three are disabled simultaneously. Therefore, the crystal oscillator is always started from a well-defined state: the low-to-high transition at its enable input always occurs at a moment when the analog supply voltage has already been there for some time. When the oscillator is disabled, the output going to the digital part must shut down immediately, because the strong digital supply is also disabled and circuitry running at 16MHz should not load the weak digital supply.

6.2 POR

Power-on reset signals, active low (NPOR) and active high (POR), are available for reliable system start-up. Digitally generated delay (tPOR_DELAY) before the POR is released ensures that the system power supply has stabilized at the appropriate levels and the MCCLK has settled. The POR function can be overwritten by an external RESET signal (default behavior of the EXT_RESET pin after power-up) from the MCU.

Figure 3. POR

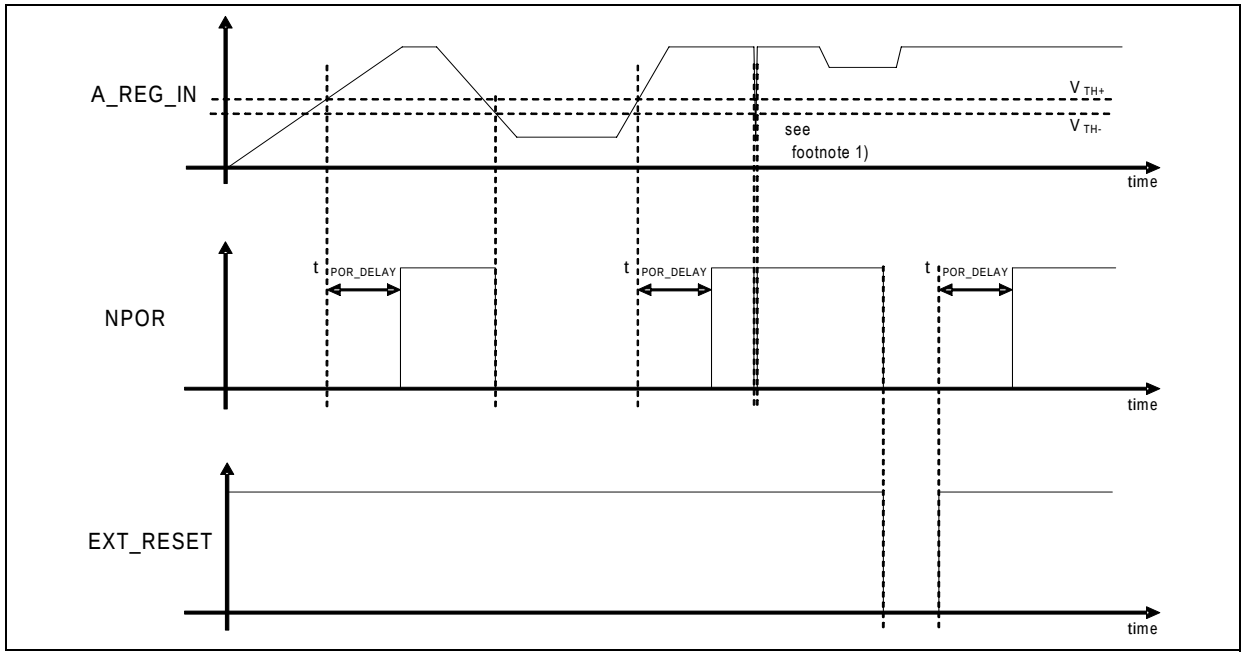


Table 5. Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	V_{TH+}			1.144		V
	V_{TH-}			1.130		V
	Hysteresis			14		mV
	t_{POR_DELAY}	1	150	200	650	ms
	Minimum Supply voltage fall time	2		1		ns
	Minimum Supply voltage rise time			1		ns
	Minimum Supply voltage notch width			1		ns
	Output impedance @ POR, NPOR			10		kΩ

1. When the voltage drops from 3.6V to 0V in 144µs (25kV/s) and then immediately rises to 3.6V with a 1µs rise time (3.6A charge current for a 1µF total decoupling capacitance), a POR is generated on the rising edge of battery voltage.
2. 1ns narrow dips on V_{DD} are rather unlikely. For example 1µF of decoupling on the power supply and 25mA total supply current, the voltage will not drop faster than by 25kV/s even when the battery gets disconnected.

7 Detailed Description

The major parts of AS3940 are receiver (RX), transmitter (TX), synthesizer, digital modem, supporting blocks, and a link manager, these are briefly described below.

- Receiver: The receiver consists of LNA, I/Q down-converting mixers, IF filtering, and two A/D converters.
- Transmitter: The TX consists of DSP generating baseband I/Q-signals, two D/A converters, interpolation filters, I/Q up-converting mixers, and Linear PA.
- Synthesizer: The synthesizer consists of VCO with I/Q output, 16MHz XTAL oscillator, and integrated loop filter.
- Digital Modem: The digital modem consists of modulation/demodulation, CRC, and RSSI.
- Supporting Blocks: The supporting blocks are voltage/current reference, regulator for analog supply, regulator for digital supply, 32.768kHz XTAL oscillator, RC-oscillator with 6.25kHz output, clock cleaning, Power On Reset, bidirectional serial digital interface (SDI), and battery level detector.
- Link Manager: The Link Manager manages the link parameters, the timings, and the adaptive channel switching in order to set-up and to maintain up to 8 communication links simultaneously. All these actions are done automatically and are transparent to the user.

7.1 Link Manager

The transceiver is optimized for applications where low power consumption is very critical, and therefore the data transmission is done in small bursts at high data rate which allows the devices to be active only a short period of time and therefore save power.

For a Client transmitting payload data (programmable between 1 and 32 Bytes) every 2s with auto-acknowledgement enabled, the typical average current consumption values are presented in Table 6. The current includes all timing and network administration done internally by the AS3940 Link Manager.

Table 6. Current Consumption

Data Rate	Average Current Consumption
250kbps	12.2µA + Payload Bytes * 0.35µA
1Mbps	5.8µA + Payload Bytes * 0.087µA
2Mbps	4.8µA + Payload Bytes * 0.045µA

The link manager has a critical role in receiving and transmitting of the data.

Data transmission: The microcontroller (MCU) supplies data via SDI to an integrated TX data buffer from where the link manager takes the data, adds the needed network management bits (preamble, device ID, time code, and CRC), and enables the transmitter for transmitting the data package at a correct time slot.

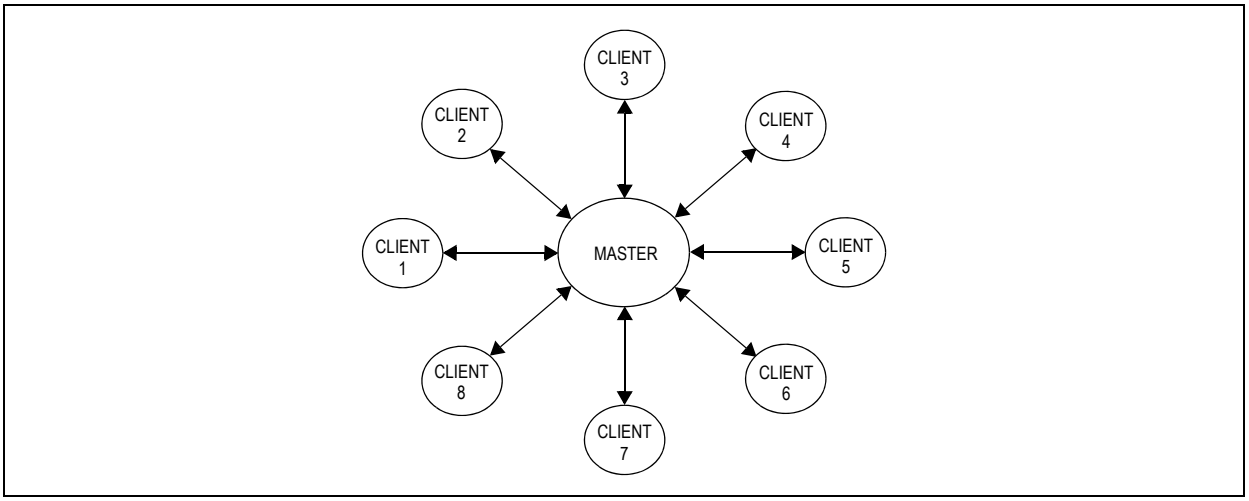
Data receiving: The link manager wakes up the receiver at a correct time slot. It checks the CRC of the payload data and if that is correct, it removes all network management bits and stores the data to a RX data buffer. The link manager gives an interrupt to the MCU, which can then retrieve data via SDI.

When the link manager is by-passed (except AS3940 physical layer, framer/de-framer, RX/TX buffering, and CRC computation), all tasks of the link manager must be made by the MCU via commands (see Commands on page 39).

7.1.1 Network

The Link Manager supports a star network which consists of one master and maximum 8 clients like presented in Figure 4. The master acts as a data processor and collector, the clients act as data producers. The master manages the parameters used for communication such as channel frequency, data rate, auto-acknowledgement, re-transmission of lost data, and adaptive channel switching.

Figure 4. Star Network



All devices in the network have a unique device ID. A communication link between a master and a client can be established if the master receives the device ID from the known device type. Introduction of new clients to a master, when the master stores the device IDs of the clients, is called pairing. In wakeup the master and the client exchange the RF parameters for communication and synchronize their time bases in order to establish next data exchange simultaneously. If the client is already paired with the master, only wakeup is needed prior communication. The pairing and wakeup procedures are done only at certain application specific frequency channels.

7.1.2 Operation Modes

The following different Link Manager operation modes are supported.

7.1.2.1 Power-down

Power-down mode is entered after connecting the battery. Registers have their default values. Lowest current consumption, only a weak regulator is running to keep the register values. No clock is provided at MCCLK and RTC pin (the MCU must have other CLK source).

The CE pin HIGH is needed to switch to standby.

7.1.2.2 Standby

No active communication (idle mode), no connection (no synchronization) established between master and client, SDI operational.

Clock can be provided at MCCLK and/or RTC pin (16MHz XTAL and dividers are active). MCCLK and RTC enable/disable required.

7.1.2.3 Pairing

- Permanent pairing: Device IDs are exchanged and permanently stored (can be overwritten).
- Temporary pairing: done for each temporary session, device ID is not permanently stored.

7.1.2.4 Wakeup

Exchange of time code (or seed) and communication parameters, master synchronizes to client time base.

Synchronization can only be done when the master and the client share the same RF channel and communication mode. The prerequisite for synchronization is that pairing has been done.

7.1.2.5 Active

Transmitting or receiving of sensor data. Different communication types: 1-way data transmit, auto-acknowledge, re-transmit of lost data and channel switching.

For temporary pairing applications, the MCU can set the a temporary master to receive mode in order to get data from an active client which is already permanently paired with its own master, without interfering on the previously established communication between master-client.

7.1.2.6 Sleep

Mode between active communication time slots, timers indicate next active communication time slots. Additionally exit by wakeup event is possible for synchronizing of additional sensors. Weak regulator, timers and RCO/32kHz XTAL are running.

7.2 Link Manager Short Communication Manual

This chapter explains how to set up a data communication link using the Link Manager and relevant registers. Using default register values offers a functional link, but an experienced user has a freedom to further optimize the settings.

Before a data link can be established, some general settings (see General Settings on page 17) have to be done and the devices must be paired (see Pairing on page 18). Only paired devices can exchange data packages. After pairing, wakeup (see Wakeup on page 19) is needed each time to evoke the data link.

7.2.1 General Settings

7.2.1.1 Clock Settings

Default value: 0x00=66 (if no MCCLK/RTC clocks needed and 32.768kHz available for AS3940 timer clock, then set 0x00 = 01)

Default value: 0x01=09 (if no clock needed during sleep, then set 0x01 = 01-07 depending on the used timer tolerance)

RCO, MCCLK, RTC, and AS3940 internal timer clock settings are set via clk_control registers.

The default value of the registers are set after applying the battery to the AS3940 and after a ‘1’ at the CE pin (pin 25). By default, MCCLK is enabled and set to 1 MHz (6.25kHz during sleep), RTC is enabled and set to 6.25 kHz, AS3940 timer clock is set to 6.25 kHz, 32.768 kHz oscillator is disabled, and the timer tolerance is set to +/- 50ppm.

7.2.1.2 Interrupt Masking

Default value: 0x02...0x04=00

Masking of interrupts which can activate the INT pin (pin 24). After the interrupt signal becomes active, additional information on the source of the interrupt can be retrieved via int_status registers (0x05, 0x06, and 0x07).

After reading one of the int_status registers, the content of that specific register is cleared.

7.2.1.3 Device Table

Default value: 0x10...0x23=00

During reception of any type of AS3940 package, the RX data path is only sensitive to information received from the device types set in the device table. In total a table of 10 supported 2-byte device types is available for initial filtering of any incoming packages.

For device types where the level shifts only once or is constant (e.g. 0000, FFFF, 000F) can often be detected in noise and can give a false detection. This may cause non-functional pairing/wakeup and increased packet error rate during the data communication. It is recommended to set non-zero values for all device types in the device type table, even for the unused device type table entries.

7.2.1.4 Device data

Default value: 0xA6...0xAD=FF

The RSSI alignment value must be stored to the device_data register 0xA6, the CRC initial value to 0xA7...0xA8, and the full device ID (2-byte device type and 3-byte serial number) to 0xA9...0xAD after every power up.

7.2.1.5 Pair/wake Table

Default value: 0x90=05

Default value: 0x91=00

Default value: 0x92=10

Default value: 0x93=00

Default value: 0x94=00

Default value: 0x95=0A

Default value: 0x96=0F

The pair/wake table settings, used for pairing (see Pairing on page 18) and wakeup (see Wakeup on page 19), must be the same for the master and all possible own clients. These settings are the pairing/wakeup frequency channel (ICF), communication mode (COM), time code scaling, transmitted power level (PA), timecode, number of wake packages, and trial_max.

7.2.1.6 General Link Manager Settings

Default value: 0x97=1E (for the Client, set 0x97 = 1F for the Master)

Default value: 0x98=8F

Default value: 0x99=80

Default value: 0x9A=00

General purpose link manager settings set the Tpolmax, CRC normal/reverse, receiver on time and duty cycle, device defined as master/client, 16MHZ XTAL startup time, synh_lost, temporary pairing package sensitivity, battery level threshold, battery level above/below the threshold, enabling of RSSI check, enabling of CRC interpretation, enabling of smart_cal, EOC and unpair request, and client selection for EOC/unpair/LIB packages.

For the optimized operation of AS3940, the following addresses must be updated from the default values.

- 0xB1=0A
- 0xE1=69
- 0xE2=24
- 0xE3=58

These settings set the receiver into high gain mode for the highest sensitivity and the transmitter output power to 0dBm. Also, the correlator threshold register 0xB1 is set to avoid false triggering to noise without sacrificing the sensitivity.

7.2.2 Pairing

Pairing is a procedure where master and client exchange their device IDs that is required prior to any data transmission. The pairing command (do_pair = 0C) starts the procedure.

Common frequency channel and communication mode must be set in the Pair/wake Tables (see General Settings on page 17) of all devices which have to be paired. After successful pairing, the device serial number is stored to the first free client table position and the pairing bit is set.

Reading the pairing bit, the device type index, and the corresponding serial number in the SPI register map reveals the paired devices.

7.2.2.1 Pairing bits:

0x33 client_0_6<3>=0 Client 0 not paired

0x33 client_0_6<3>=1 Client 0 paired

0x3D client_1_6<3>=0 Client 1 not paired

0x3D client_1_6<3>=1 Client 1 paired

...

0x79 client_7_6<3>=0 Client 7 not paired

0x79 client_7_6<3>=1 Client 7 paired

7.2.2.2 Device type index:

0x30 client_0_9<7:4> Device type index for Client 0

0x3A client_1_9<7:4> Device type index for Client 1

...

0x76 client_7_9<7:4> Device type index for Client 7

7.2.2.3 Serial numbers:

0x30 client_0_9<3:0> Client 0 serial number<23:20>

0x31 client_0_8<7:0> Client 0 serial number<19:12>

0x32 client_0_7<7:0> Client 0 serial number<11:4>

0x33 client_0_6<7:4> Client 0 serial number<3:0>

0x3A client_1_9<3:0> Client 1 serial number<23:20>

0x3B client_1_8<7:0> Client 1 serial number<19:12>

0x3C client_1_7<7:0> Client 1 serial number<11:4>

0x3D client_1_6<7:4> Client 1 serial number<3:0>

...

0x76 client_0_9<3:0> Client 7 serial number<23:20>

0x77 client_0_8<7:0> Client 7 serial number<19:12>

0x78 client_0_7<7:0> Client 7 serial number<11:4>

0x79 client_0_6<7:4> Client 7 serial number<3:0>

On the master side, the serial number of each paired client is stored. On the client side, the serial number of the master is stored in the client 0 location. One master can be paired with up to 8 clients. A client can be paired with 1 permanent master and with 1 temporary master (the serial number of the temporary master is stored in the client 1 location, the client 1 pairing bit is cleared after a temporary communication session).

7.2.3 Wakeup

Wakeup is a procedure where master determines the used data communication parameters and synchronizes to the client time base. The wakeup command (do_wakeup = 08, do_wakeup_from_client = 09, or do_wakeup_from_master = 0A) starts the procedure.

Common frequency channel and communication mode must be set in the Pair/wake Tables (see General Settings on page 17) of all devices. After successful wakeup, the wake bit and the sync bit are set.

Reading the wake bit and the sync bit in the SPI register map reveals the waked devices.

7.2.3.1 Wake bits:

0x33 client_0_6<0>=0 Client 0 not waked up

0x33 client_0_6<0>=1 Client 0 waked up

0x3D client_1_6<0>=0 Client 1 not waked up

0x3D client_1_6<0>=1 Client 1 waked up

...

0x79 client_7_6<0>=0 Client 7 not waked up

0x79 client_7_6<0>=1 Client 7 waked up

Sync bits:

0x34 client_0_6<7>=0 Client 0 in sync

0x34 client_0_6<7>=1 Client 0 sync lost

0x3E client_1_6<7>=0 Client 1 in sync

0x3E client_1_6<7>=1 Client 1 sync lost

...

0x7A client_7_6<7>=0 Client 7 in sync

0x7A client_7_6<7>=1 Client 7 sync lost

7.2.4 Data Communication

The link manager wakes up the devices at correct time point and, if enabled, automatically re-transmits lost data packages and manages the Adaptive Channel Switching (ACS).

The frame management is done using four separate 32-byte data buffers; 2 for RX and 2 for TX. The link manager switches between the buffers to ensure maximum data throughput (see Communication on page 30). The MCU is responsible to write the TX data buffer before the actual communication time slot, and to read the RX data buffer before the data is overwritten.

7.2.4.1 Data reception:

The MCU is informed about received data packages via the following interrupts (if not masked):

0x05 rx_data_done_1<5>=1 Data received in RX buffer 1

0x05 rx_data_done_0<4>=1 Data received in RX buffer 0

0x05 rx_data_failed<2>=1 Data reception failed

CRC check of the received data is always done (recommended default setting, 0x9A b[6]=0) and the CRC_ok / CRC_not_ok flag is set in the appropriate client table.

0x9A CRC_interpret_disable<6>=0 If the CRC fails, rx_data_0/1 interrupt is not set and the buffer selection stays on the current RX buffer

0x9A CRC_interpret_disable<6>=1 If the CRC fails, rx_data_0/1 interrupt is anyway set and the buffer selection switches to the other RX buffer

7.2.4.2 Data transmission:

The MCU is informed about the success of the transmission via the following interrupts (if not masked):

0x05 tx_data_done_1<7>=1 Data transmitted from TX buffer 1

0x05 tx_data_done_0<6>=1 Data transmitted from TX buffer 0

0x05 tx_data_failed<3>=1 Data transmission failed

If both TX buffers contain old data, the selected buffer is not changed. If the unselected buffer contains new data, it will be used for the next transmission.

Reading the buffer status bits in the SPI register map reveals the usage of the buffers.

0x0A buffer_status<3>=0 TX buffer 0 selected by the link manager

0x0A buffer_status<3>=1 TX buffer 1 selected by the link manager

0x0A buffer_status<2>=0 RX buffer 0 selected by the link manager

0x0A buffer_status<2>=1 RX buffer 1 selected by the link manager
0x0A buffer_status<1>=0 TX buffer 1 can be filled by the MCU
0x0A buffer_status<1>=1 TX buffer 1 should not be filled by the MCU
0x0A buffer_status<0>=0 TX buffer 0 can be filled by the MCU
0x0A buffer_status<0>=1 TX buffer 0 should not be filled by the MCU

7.3 Detailed Link Manager Protocol Description

7.3.1 Time Code

Time code is the time (in units of a known clock) after which the device that transmitted (or received) a data packet will transmit (or receive) again.

The data transmission is done in small bursts at high data rate which allows the devices to be active only a short period of time and therefore save power. In order to avoid collisions between different clients, different time code values can be used. The time code can be a fixed number, or taken randomly from the time code table in order to further decrease the possibility of collisions between different clients.

The client has a timer circuit running indicating the next communication time. The master has as many timers running in parallel as active clients. Each timer gives an interrupt when the appropriate client has to communicate with the master. The delay between the received RF signal and corresponding baseband signal (including the latency of any interrupts) is managed completely by the link manager.

Timers run using the 32.768 kHz XTAL or 6.25 kHz derived from the RCO.

The timer sizes of the different systems are presented in Table 7

Table 7. Timer Sizes

Frequency	Resolution
32.768 kHz	1 / 32768Hz (~ 30µs)
6.25kHz	1 / 6250Hz (~ 160µs)

Clients can transmit data in intervals given in Table 8.

7.3.1.1 Fixed time codes

Fixed time code values presented in Table 8 are hard-coded in a time code table. A programmable multiplier together with the time code number value selects which time code value is used.

The time code equals to time_code_scaling*(895 + time_code)/2048 s. For time_code=FF, a time code is randomly taken with the selected time_code_scaling as described in Pseudo-random time code 7.3.1.2. The random time_code is not supported during pairing and wakeup.

For pairing and wakeup, the time_code is set in register 0x93 PAIRWAKE_TABLE_3<7:0>. The time_code_scaling is set in register 0x92 PAIRWAKE_TABLE_4<5:4>. For data mode, the time_code can be individually set for each client by the master in CLIENT_n_3<7:0> register. The time_code_scaling is set in CLIENT_n_0<4:3> register.

Table 8. Time Code Values

Time code number	Time code value [s]			
	time_code_scaling = 0.5	time_code_scaling = 1	time_code_scaling = 2	time_code_scaling = 4
0	0.5 * 895 / 2048	1 * 895 / 2048	2 * 895 / 2048	4 * 895 / 2048
1	0.5* 896 / 2048	1* 896 / 2048	2 * 896 / 2048	4 * 896 / 2048
2	0.5* 897 / 2048	1* 897 / 2048	2 * 897 / 2048	4 * 897 / 2048
…	…	…	…	…
126	0.5* 1021 / 2048	1* 1021 / 2048	2 * 1021 / 2048	4 * 1021 / 2048
127	0.5* 1022 / 2048	1* 1022 / 2048	2 * 1022 / 2048	Reserved
…	…	…	…	…
254	0.5* 1149 / 2048	1* 1149 / 2048	2 * 1149 / 2048	Reserved
255	8-bit PRBS	8-bit PRBS	8-bit PRBS	7-bit PRBS

Note: If two clients use time code values that are close to each other and there is a collision, it takes long time until they get apart. It is recommended to select appropriate (ideally with largest possible difference) time code values so that the system can recover faster from collisions.

7.3.1.2 Pseudo-random time code

A pseudo-random bit sequence (PRBS) generator is used to provide a pointer to the time code table in order to get the next time code value. The client and the master use the known seed (exchanged during wakeup or temporary pairing) for calculation of the next random time slot. In presence of disturbers or lost data packages, the next time slot is calculated independently.

For each active client a separate PRBS generator is running independently.

If the multiplier of 4 is used, a 7-bit PRBS value is used in order to be compatible with 16-bit timers. Otherwise, 8-bit PRBS value is used.

7.3.2 Communication Mode

The communication mode defines the various combinations of modulation parameters (data rate and frequency deviation) in order to achieve the optimum RF performance. The supported communication modes are presented in Table 9.

Table 9. Supported Communication Modes

Communication Mode	Data Rate	Frequency deviation	Channel spacing
0	250kbit/s	160 kHz	1MHz
1	1Mbit/s	160 kHz	1MHz
2	1Mbit/s	400 kHz	2MHz
3	2Mbit/s	320 kHz	2MHz
4	2Mbit/s	800 kHz	3MHz
5	Reserved	Reserved	Reserved
6	Reserved	Reserved	Reserved
7	Reserved	Reserved	Reserved

Note: Channel spacing is only a recommendation for optimum behavior. Frequency channels can be selected with 1MHz resolution without any restrictions within the operation range.

7.3.3 Frequency Channels

Channel frequencies from 2405MHz to 2480MHz supported.

7.3.4 RSSI

The RSSI value indicates the level of the last correctly received packet (DATA, PAIR0/1, LMB, TEMP_LMB, LIB, or MCDT_RX). After the reception of the packet, the actual value LOG_RSSI_ACT_VALUE<9:0> in address 0xB4 and 0xB5 is updated.

7.3.4.1 RSSI Calibration

If a RSSI value of a certain input power level is needed, a reference measurement has to be done to calibrate the RSSI value. The RSSI calibration can be enabled by setting the RSSI alignment mode bit high (0b1) in register 0xE4. Known RF level (e.g. middle of dynamic range) must be applied to the antenna and the actual RSSI value in address 0xB4 and 0xB5 is measured. The MSB and LSB bits should be ignored and the remaining actual RSSI value bits [8:1] must be stored into the Device Data register in address 0xA6. The RSSI actual value is now aligned so that the reference level produces the value of 0b0000000000.

7.3.4.2 RSSI Accuracy

The automatic gain control (AGC) is setting the gain of the analog front-end with eight 6dB steps. The RSSI measurement can be accurately done only after the gain is settled. For accurate RSSI value, minimum payload length recommendation presented in Table 10 must be used.

Four RSSI registers (one for each RX data buffer page) are accessible by the MCU via SDI.

Table 10. Minimum Payload Recommendations

Data rate (kbps)	Minimum payload length (byte)
250	-

Table 10. Minimum Payload Recommendations

Data rate (kbps)	Minimum payload length (byte)
1000	8
2000	18

7.3.4.3 RSSI during pairing and LBT

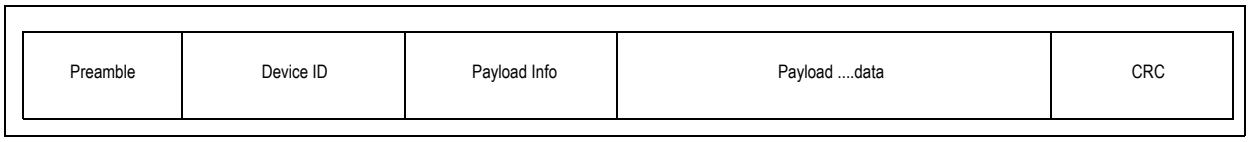
During pairing and LBT, the aligned actual RSSI value is checked against the RSSI threshold set in the LOG_RSSI_THR<9:0> register in address 0xB2 and 0xB3. In order to have a meaningful values for the threshold, the RSSI calibration must have been performed.

During pairing, the aligned actual RSSI value must be above the threshold value. If the RSSI_check is disabled, the RSSI threshold comparison is not performed and the pairing is done with the first received device.

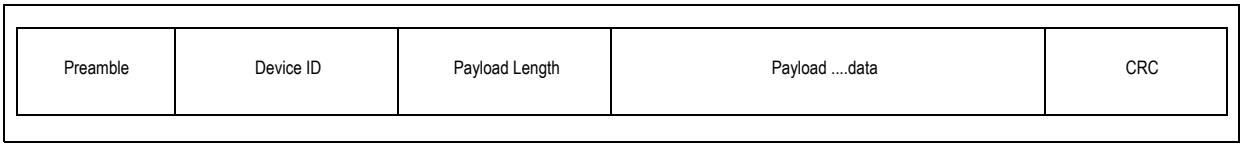
During LBT, the channel is considered free if the aligned actual RSSI value is below the threshold. If the RSSI_check is disabled, the RSSI threshold comparison is not performed and the channel is always considered to be free.

7.3.5 Data Package Structure

The data package consists of preamble, device ID, payload info, payload and CRC.



The MCDT package differs from the normal data package as presented below. It consists of preamble, device ID, payload length (1-byte), payload and CRC.



For detailed description of MCU controlled data transfer mode (MCDT) see 7.3.12

7.3.5.1 Preamble

8-bit long preamble is automatically added and removed by the Link Manager.

7.3.5.2 Device ID

The device ID is a unique 5-byte number, which allows the master to differentiate between own and foreign clients. It is transmitted always directly after preamble and is divided into device type and serial number like presented in Table 11.

Table 11. Device ID

Device Type	Serial Number
2-bytes	3-bytes

Device type: The device type allows the master/client to distinguish between different client types or vice versa in two way communication. There is no restriction for how many same device type clients are paired with the master.

The device type can be different for different client types. A 10-entry device type table must be filled by the MCU.

Serial Number: The individual serial number is used to identify the required client/master.

7.3.5.3 Payload Info

The payload info bits are automatically added by the link manager. The payload info contains information about payload length, re-transmission index (RTI), and package type (PACK) as in Table 12.

Table 12. Payload Info Bits

Payload Info bit	# of bits	Description	
Payload length	5	00000	1 byte
		00001	2 bytes
		00010	3 bytes
		00011	4 bytes
		....	....
		11111	32 bytes
Re-transmission index (RTI)	2	00	0 times re-transmitted package
		01	1 times re-transmitted package
		10	2 times re-transmitted package
		11	3 times re-transmitted package
Package type (PACK)	4	0000	Data
		0001	LMB
		0010	ACK0
		0011	ACK1
		0100	PAIR0
		0101	PAIR1
		0110	WAKEUP
		0111	LIB
		1000	TEMP_LMB
		1001	TEMP_PAIR1
		1010	Reserved
		....	....
		1111	Reserved
Reserved	5		Reserved

The link manager calculates the payload length in 8-bit steps and the value is added automatically to the payload info.

The re-transmission index is incremented by the link manager whenever a new re-transmission is done. The maximum number of re-transmissions is three.

The package type indicates the information content of the package.

7.3.5.4 Payload Data

The following are the two payload data modes:

Normal Mode: When a data package is correctly received (no CRC error), the link manager removes the device ID, payload info and CRC and the payload is stored into a buffer. An interrupt is set and the MCU can then load the data from the RX buffer. When the data package is transmitted, the MCU must have written the payload into a TX buffer, the link manager automatically adds the preamble, device ID, payload info (when applicable), and CRC to the transmitted data.

The maximum length of the payload data is 32 bytes and it is programmable with 1-byte steps.

MCDT Mode: When a package with the correct device type is received, the device type index is stored in 1st byte and the following serial number in 2nd, 3rd and 4th byte of the active RX data buffer. The payload is stored into the buffer, CRC is automatically computed and the result is offered as a flag in the SDI memory map. After the MCDT transmit command, the framer combines the MCDT package. Preamble, device ID, payload length (retrieved from the SDI slave), and the CRC are automatically added to the transmitted data.

The maximum length of the payload data is 28 bytes and it is programmable with 1-byte steps.

7.3.5.5 CRC

The payload data is followed by 2 CRC bytes. The CRC-16-CCITT is used (polynomial: $x^{16}+x^{12}+x^5+1$, the initial value is retrieved from the device).

The CRC check is always performed (CRC ok/not ok flag is set in the appropriate client table) and the received data is stored in to a RX data buffer. In case of the rx_data_done_0/1 and rx_data_failed interrupts are not masked and

- CRC pass, the rx_data_done_0/1 interrupt is set. Buffer selection is switched to the other RX buffer.
- CRC fail, the rx_data_failed interrupt is set. If CRC_interrupt_en = 1 (CRC interrupt enabling bit in the memory map), the rx_data_done_0/1 interrupt is set. Buffer selection is switched to the other RX buffer.
- CRC fail, the rx_data_failed interrupt is set. If CRC_interrupt_en = 0, the rx_data_done_0/1 interrupt is not set. Buffer selection stays on the current RX buffer.

7.3.5.6 Buffer Selection

The frame management is done using four separate 32-byte data buffers; 2 for RX and 2 for TX. The selection mechanism switches between the buffers to ensure maximum data throughput.

RX Data Buffer Mechanism

Data packets are saved into RX buffers in an alternative approach; if one buffer is currently in use, the next data packet will be saved into the other buffer. When a packet is received in one of the buffers, a corresponding interrupt (rx_data_done_0/1) is set.

Selection between RX buffers depends on the CRC result. The status bit (0x0A, buffer_status[2]) indicates the currently selected RX buffer.

TX Data Buffer Mechanism

During one TX cycle (transmission of one data package including possible re-transmissions), the same TX buffer is used. After data transmission, tx_data_done_0/1 interrupt is set. If both TX buffers contain old data, the selected buffer is not changed. If the unselected buffer contains new data, it will be used for the next data transmission.

A failure in data transmission is indicated by tx_data_failed interrupt. The status bit (0x0A, buffer_status[3]) indicates the currently selected TX buffer.

7.3.6 System Timing Error

In order to guarantee that the master always receives the next data package successfully, even in case of maximum timing offset between the master and the client, the receive window must be wide enough. The timing offset is caused by the inaccuracy of the XTAL or the on-chip RC oscillator. The initial total XTAL tolerance can be set in the CLK_CONTROL_0<2:0> register in address 0x01.

Table 13. Supported XTAL Tolerances

Total XTAL tolerance [ppm]
±50
±100
±150
±200
±250
±300

The RX window size is increased after each missed communication burst. The increase in size depends on the maximum XTAL accuracy.

7.3.7 Pairing

Pairing is exchange of device IDs between a master and a client. The device IDs are stored in stored in the client table.

Pairing is a procedure where a new client is introduced to a master and is required prior to any transmission of payload data. The pairing is done on a dedicated frequency channel. Pairing can only be done when the master and the client share the same RF channel and communication mode. Wakeup is still needed prior to communication. The pairing settings (e.g. the pairing/wakeup channel, communication parameters, necessary timings, and if the device is defined as master or client) are stored in the pair/wake table (0x90…0x96).

The MCU must fill the device type table and the pair/wake table prior to pairing.

Pairing can be permanent or temporary.

- Permanent pairing: During permanent pairing, the master and the client exchange the device IDs of each other and store this information permanently. The information is maintained as long as battery voltage is connected or until the stored data is overwritten by the MCU.
- Temporary pairing: During temporary pairing, the master and the client exchange device IDs. They do not store the device IDs permanently, but only for the temporary communication session.

During pairing, the master looks for clients with a certain device type, which is stored in the device type table (0x10…0x23). It is recommended to set non-zero values for all device types in the device type table to avoid triggering to noise and pairing to fail. Since it is not possible to distinguish between the required own clients and foreign clients, pairing in clean RF environment is recommended.The RSSI threshold set by the MCU can be used to select the correct client if interpreting the RSSI results during pairing is enabled. For more information see RSSI 7.3.4

RSSI check enabling bit:

0x9A gen_pur_lm_settings_0<7>=0 RSSI based pairing disabled

0x9A gen_pur_lm_settings_0<7>=1 RSSI based pairing enabled.

7.3.7.1 Permanent Pairing

The pairing sequence is set by MCU command (do_pair: 0C). Client transmits PAIR0 packages and waits a reply from a master as shown in Figure 5. The master is set to receive mode with certain duty cycle (see Table 14) set in the GEN_PUR_LM_SETTINGS_3<4:1> register in address 0x97 and accepts only PAIR0 packages.

If the master receives the PAIR0 package correctly, it concludes that the client is wanted. If interpreting of the RSSI measurement result is enabled and the threshold is exceeded, the master replies with PAIR1 package. Client accepts PAIR1 packages and if the threshold is exceeded, the exchange of the PAIR1 package is acknowledged as shown in Figure 5. If interpreting of the RSSI measurement is disabled, no threshold check is done and correctly received packages are always replied.

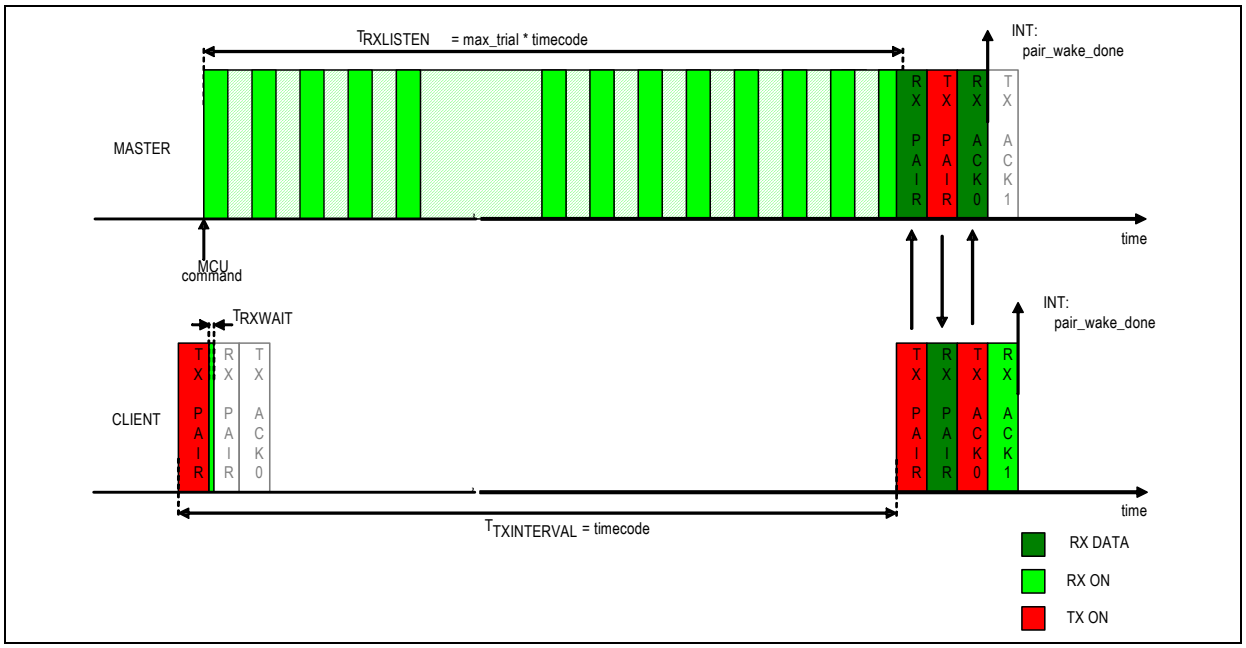
If any of the package is not correctly received, the master informs the client with an acknowledgement packet that the pairing is failed (device ID is written into the client table, but the pairing bit is not set).

After successful pairing, the master and the client are configured for full device ID and pairing bits are set. The MCU at any time can override the pairing bit.

Table 14. Duty Cycle Specification

RX on time (µs)	Duty cycle (%)			
800	10	20	40	100
1000	12.5	25	50	100
1600	10	20	40	100
2000	12.5	25	50	100

Figure 5. Permanent Pairing



7.3.7.2 Temporary Pairing

During temporary pairing, the exchanged device IDs are not stored permanently, but only for the temporary communication session. Two different possibilities are described below.

- Only the client and the temporary master are present: The prerequisite for this case is that the client is not having active communication with a permanent master. Therefore, the temporary master can control the communication.

  The temporary master is set to receive mode by MCU command (do_temp_pair: 0F) with certain duty cycle and is configured to check the received 2-byte device type as in normal pairing (see Figure 5). Accepted package types to which the device is sensitive during temporary pairing are set in the GEN_PUR_LM_SETTINGS_1<7:6> in address 0x99 as presented in Table 15.

Table 15. Accepted packages in temporary pairing

temp_pair_sen[1:0]	Master	Client
00	LIB	TEMP_LMB
01	PAIR0, LIB	PAIR1, TEMP_LMB, LMB
1x	PAIR0	PAIR1, LMB

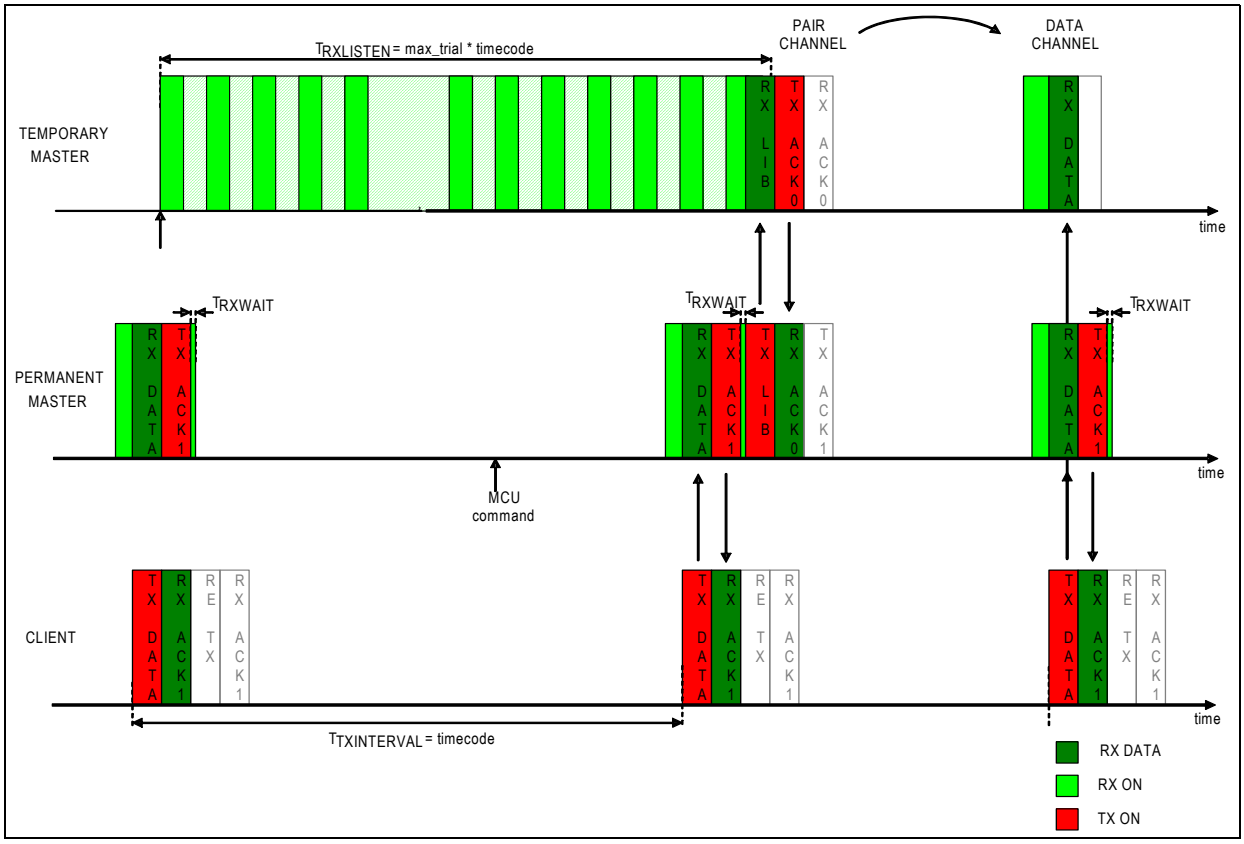
  The temporary pairing sequence of the client is set by MCU command (do_pair: 0C or do_wake_up: 08). The client transmits PAIR0 packages and waits for a reply from master.The client is set to be sensitive to TEMP_LMB packages and the master to PAIR0 packages.

  If the temporary master receives the PAIR0 package and the threshold is exceeded in case of the interpreting of the RSSI measurement result is enabled, it replies with TEMP_LMB package. If the TEMP_LMB package is successfully exchanged (the threshold is exceeded in case of the interpreting of the RSSI measurement result is enabled), the client tables are updated and DATA mode is entered using the TEMP_LMB settings. If interpreting of the RSSI measurement is disabled, no threshold check is done and correctly received packages are always replied.

- The client, the permanent master and the temporary master are present: The prerequisite for this case is that permanent pairing has been done between the client and the permanent master. Also, the client and the permanent master have active data communication, that has priority, at certain communication channel and alternate between sleep and data modes.

  As shown in Figure 6, after MCU command (do_send_lib: 10), the permanent master transmits the corresponding LIB package as set in the client table (GEN_PUR_LM_SETTINGS_0[2:0]). The temporary master is set to receive mode (do_temp_pair: 0F) and it is set to be sensitive only to LIB packages. If the temporary master receives the LIB package successfully and the threshold is exceeded in case of the interpreting of the RSSI measurement result is enabled, the client table is updated and the temporary master is directly set to DATA mode using the LIB settings. The LIB package contains all necessary parameters that the temporary master can listen to the ongoing data communication between the client and the permanent master. As many LIB packages as waked up clients can be send to the temporary master.

Figure 6. Temporary Pairing between Client, Permanent, and Temporary Masters



7.3.8 Wakeup

Wakeup (Synchronization) is exchange of communication parameters and resetting the seed of the PRBS generator for data exchange. If the wakeup fails, the communication parameters are not changed.

The synchronization can only be done when the master and the client share the same RF channel and communication mode. The wakeup settings (e.g. the pairing/wakeup channel, communication parameters, and necessary timings) are stored in the pair/wake table (0x90…0x96).

The prerequisites for synchronization is that pairing has to be done. The master and the clients know each others device IDs. The MCU can clear the pairing bits of those paired devices it does not want to wake up. In that case, it is responsibility of the MCU to return the original values of the pairing bits.

During wakeup, the master transmits the data communication mode parameters to the client. The MCU can configure the used parameters individually for each client via the Client Tables and those are transmitted in the corresponding LMB package. After successful wakeup, data mode is automatically entered with those settings and the waked bit is set.

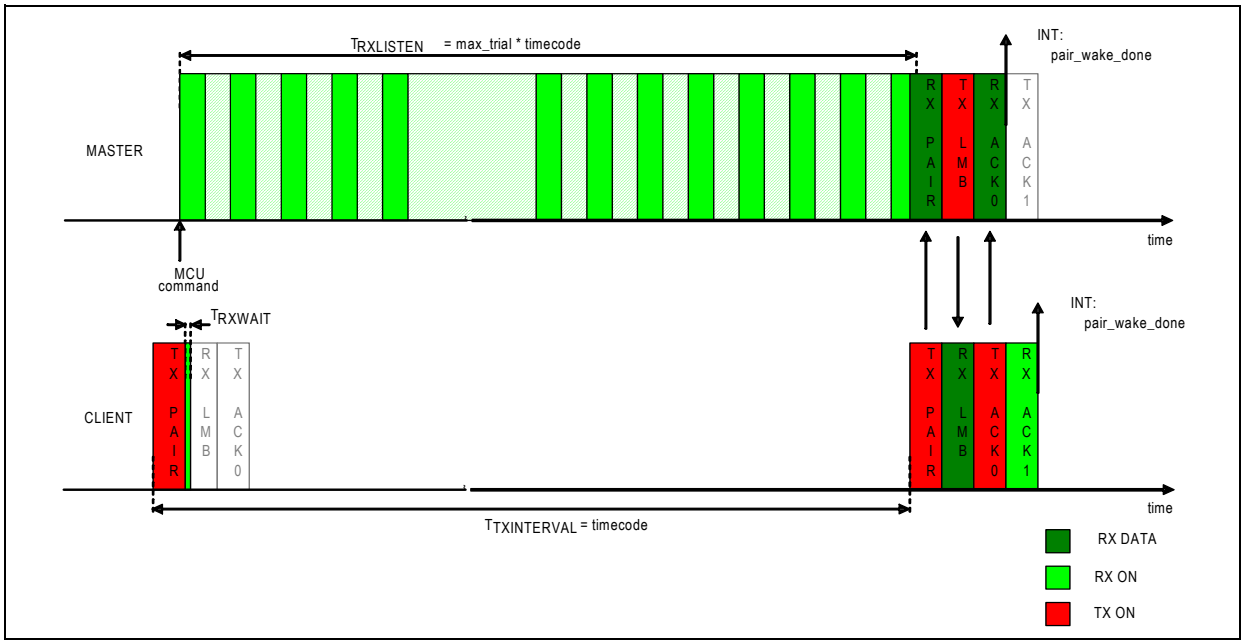
The following are the available wakeup procedures.

7.3.8.1 Standard Wakeup Procedure

The standard wakeup procedure is started by MCU command (do_wakeup: 08) as shown in Figure 7. The client transmits PAIR0 packages and waits for a reply. The master is set to receive mode and it is sensitive to PAIR0 packages.

If the master receives the PAIR0 package correctly, it replies with the LMB package and waits an acknowledgement from the client. The client accepts the LMB package from its master. If the LMB package is correctly received, the exchange of it is acknowledged and data mode is entered with the LMB settings. If the master does not receive an answer, the RX mode is exited and the wakeup is failed.

Figure 7. Standard Wakeup



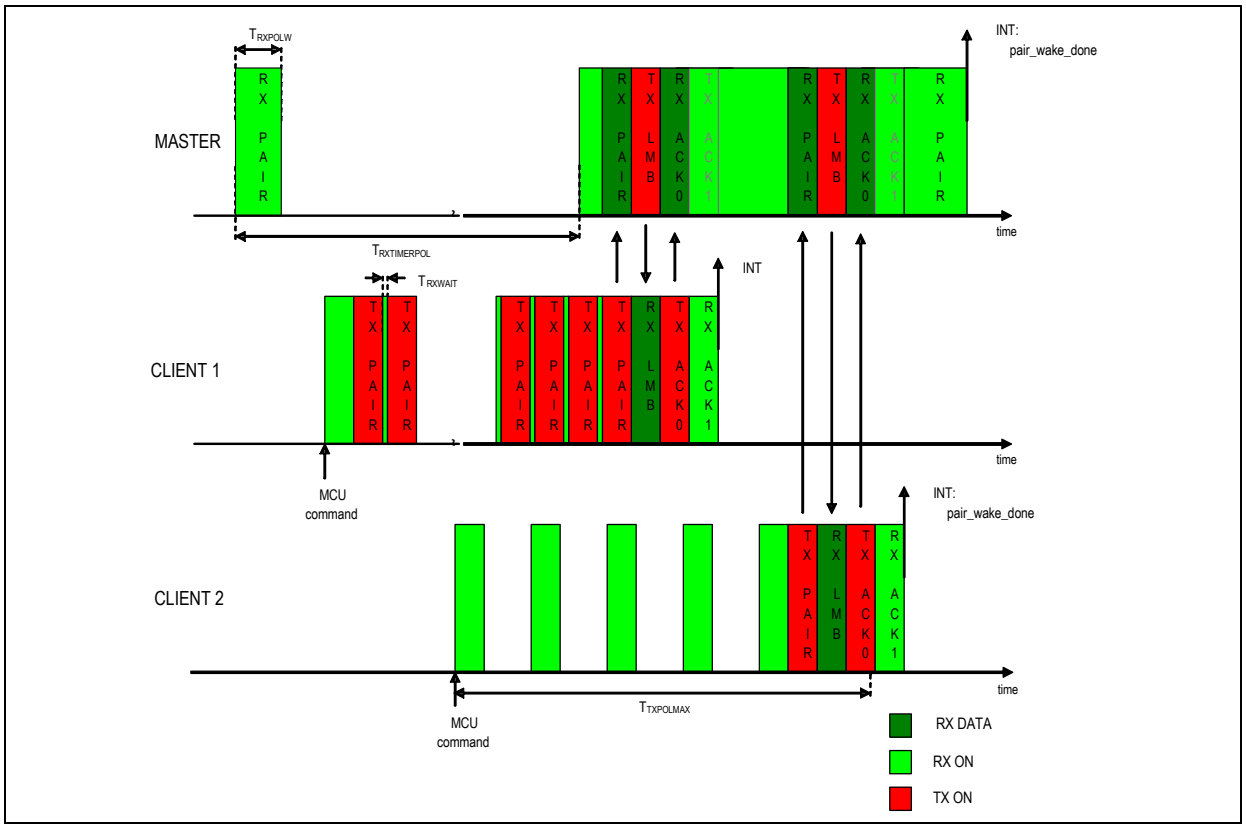
7.3.8.2 Wakeup from Client

This procedure can be interrupted by the other pairing/wakeup procedures. The DATA communication has priority. The master has to maintain the data communication with the active clients during the procedure.

This wakeup procedure is started by MCU command (do_wakeup_from_client: 09). The master is set to receive mode with programmable polling cycle (0x97, GEN_PUR_LM_SETTINGS_3[7:6]) until trial_max (0x96, PAIRWAKE_TABLE_0[7:0]) is reached or all paired clients are woken up. It is sensitive to PAIR0 packages. The client is set to listen-before-talk (LBT) mode to decide whether the channel is occupied or free.

If the channel is free, the client starts transmitting the PAIR0 packages and waits an answer from the master as shown in Figure 8. If the channel is occupied, the receive mode is continued with 50% duty cycle until the maximum polling time (0x97, GEN_PUR_LM_SETTINGS_3[7:6]) or until there are no other transmitting clients. If the master receives the PAIR0 package correctly, it replies with the LMB package. If the client receives the LMB package correctly, the exchange of it is acknowledged and data mode is entered with the LMB settings.

Figure 8. Wakeup from Client



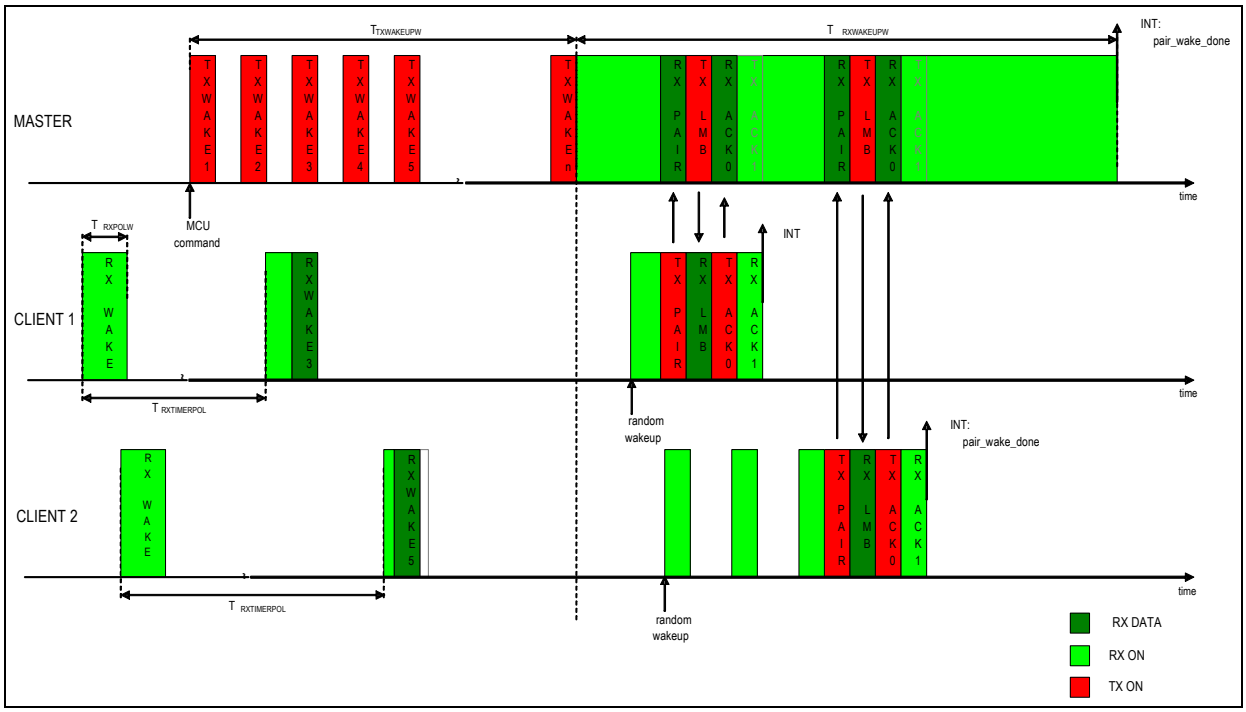
7.3.8.3 Wakeup from Master

This procedure cannot be interrupted by the other pairing/wakeup procedures. Also, the DATA communication has no priority.

This wakeup procedure is started by MCU command (do_wakeup_from_master: 0A). The master starts transmitting the wakeup sequence with programmable number of packages (0x94-0x95, PAIRWAKE_TABLE_2/1) as shown in Figure 9. The client is in polling mode and sensitive to WAKE packages.

After the wakeup sequence, the master is set to receive mode for 2 seconds and is sensitive to PAIR0 packages. If a client receives the WAKE package, it gets a random time within the master receive window and starts the LBT in order to decide whether the channel is occupied or free. If the channel is free, the client starts transmitting the PAIR0 packages and waits an answer from the master. If the master receives the PAIR0 package correctly, it replies with the LMB package. If the client receives the LMB package correctly, the exchange of it is acknowledged and data mode is entered with the LMB settings.

Figure 9. Wakeup from Master



7.3.9 Communication

Communication (Data mode) is transmitting or receiving data. The different communication types set by the master during wakeup are one-way data transmit, auto-acknowledge, and re-transmit (programmable between 0 and 3) of lost data. The latter two can be combined with adaptive channel switching. The data communication has priority.

Before active communication, pairing or initial synchronization must been done. The master synchronizes to the time base of the client. In case the master does not receive the data package during one communication time slot, the next received window of the master is automatically increased by the amount of the programmable timing error (0x01, CLK_CONTROL_0[2:0]). Synchronization is defined as lost if the maximum number of consecutive lost time slots (0x98, GEN_PUR_LM_SETTINGS_2[5:0]) is reached.

7.3.9.1 One-way Data Communication

When the master receives the valid device ID, the link manager synchronizes automatically to the received data package. The data is written to a RX data buffer and CRC check is done. The CRC check result and the data are now available for the MCU.

On the client side, the MCU writes the data into the TX data buffer and the link manager adds the preamble, device ID, payload info, and CRC and the data package is transmitted on the correct time slot.

Note: The adaptive channel switching must be disabled (CLIENT_0_2[7]) for one-way data communication. No ACK1 package is transmitted and therefore the channel would be switched constantly.

7.3.9.2 Auto-Acknowledged Data Communication

When the master receives the valid device ID, the link manager synchronizes automatically to the received data package. The data is written to a RX data buffer and CRC check is done. The CRC check result and the data are now available for the MCU. Immediately after the data package is correctly received, the master transmits the ACK1 package to the client and waits shortly a possible re-transmissions if auto-ACK is enabled (CLIENT_n_1[0]) and the number of re-transmissions (CLIENT_n_0[7:6]) is not reached. If the master does not receive a re-transmitted data package, it assumes that the client has received the ACK1 package. The master is configured for next communication slot (possibly with other client).

On the client side, the MCU writes the data into the TX data buffer and the link manager adds the preamble, device ID, payload info, and CRC and the data package is transmitted on the correct time slot. Immediately after transmitting the data package, the client waits an ACK1 package from the master. If it does not receive the ACK1 package, and re-transmit is enabled and the number of re-transmissions is not reached, the data package is re-transmitted. If the ACK1 package is correctly received, the client is set to sleep until next time slot.

7.3.10 Data Streaming

Data streaming is continuous transmission of payload packages from client to master with a certain duty cycle (CLIENT_n_0[1:0]). The duty cycle value and the corresponding net data rate assume that the full number of selected re-transmissions is needed. The prerequisite for data streaming is that pairing has to been done.

One TX data streaming cycle has the same structure as normal data communication cycle (no ACK, auto-ACK, and re-transmission options RT=0/1/2/3) with same interrupts. Data streaming is defined as lost if the maximum number of consecutive lost time slots (GEN_PUR_LM_SETTINGS_2[5:0]) is reached.

The data streaming is initiated by the master. A streaming_enable bit (CLIENT_n_0[2]) must be set before the wakeup command (do_wakeup: 08, do_wakeup_from_client: 09, do_wakeup_from_master: 0A). During the wakeup procedure, the master replies with the LMB package where the streaming_enable=1 and streaming_duty_cycle is set. After successful exchange of the LMB with the client, data streaming mode is automatically entered. If the wakeup procedure is not finished correctly, the wakeup status bit (CLIENT_n_6[0]) is kept low.

Different data rates calculated depending on data rate, number of re-transmissions, duty cycle, and smart_cal (0x9A, GEN_PUR_LM_SETTINGS_0[5]) settings are presented in Table 16 and Table 17.

Table 16. Net Data Rates for Streaming (smart_cal enabled)

Date Rate	No. re-transmissions	Duty cycle 12.5%	Duty cycle 25%	Duty cycle 50%	Duty cycle 100%
		Net data rate [kbps]			
250kbps	no ACK1	22.3	44.6	89.2	178.4
	0	16.1	32.3	64.5	129.1
	1	8.1	16.2	32.4	64.7
	2	5.4	10.8	21.6	43.2
	3	4.0	8.1	16.2	32.4
1Mbps	no ACK1	74.9	149.9	299.8	599.5
	0	50.1	100.2	200.3	400.6
	1	25.2	50.5	100.9	201.9
	2	16.9	33.7	67.5	134.9
	3	12.7	25.3	50.7	101.3
2Mbps	no ACK1	123.6	247.1	494.2	988.4
	0	77.1	154.2	308.4	616.9
	1	39.0	78.0	156.1	312.2
	2	26.1	52.2	104.5	209.0
	3	19.6	39.3	78.5	157.1

Table 17. Net data rates for streaming (smart_cal disabled)

Date Rate	No. re-transmissions	Duty cycle 12.5%	Duty cycle 25%	Duty cycle 50%	Duty cycle 100%
		Net data rate [kbps]			
250kbps	no ACK1	18.1	36.2	72.4	144.7
	0	13.8	27.6	55.2	110.5
	1	7.5	14.9	29.8	59.7
	2	5.1	10.2	20.4	40.9
	3	3.9	7.8	15.5	31.1

Table 17. Net data rates for streaming (smart_cal disabled)

Date Rate	No. re-transmissions	Duty cycle 12.5%	Duty cycle 25%	Duty cycle 50%	Duty cycle 100%
		Net data rate [kbps]			
1Mbps	no ACK1	42.0	84.1	168.2	336.4
	0	32.9	65.8	131.6	263.1
	1	20.0	40.0	79.9	159.8
	2	14.3	28.7	57.4	114.7
	3	11.2	22.4	44.8	89.5
2Mbps	no ACK1	54.0	107.9	215.9	431.7
	0	42.7	85.4	170.9	341.8
	1	27.7	55.5	110.9	221.8
	2	20.5	41.1	82.1	164.2
	3	16.3	32.6	65.2	130.3

7.3.11 Adaptive Channel Switching

When the Adaptive Channel Switching (ACS) is enabled CLIENT_n_2[7]), every time the communication slot is lost, the link manager will pick up a new frequency channel from the programmable 16-entry ACS channel table (0x80...0x8F) for the next communication slot.

The implemented algorithm is same for a master and clients; the frequency channel is only switched if the communication slot is lost. A new channel is selected until either the communication is again successful or the maximum number of lost communication slots (GEN_PUR_LM_SETTINGS_2[5:0]) is reached.

In order the ACS works properly, wakeup has to be done successfully and the same ACS channel table must be used for the master and for the client.

7.3.12 MCU Controlled Data Transfer (MCDT)

The MCDT is data transmission triggered by the MCU (timing, protocol and operation modes completely managed by the MCU). The link manager is bypassed giving maximum flexibility for the MCU.

The different MCDT commands are:

1. MCDT_wakeup

   Wakes up the 16MHz XTAL and AS3940, the MCU must guarantee that the XTAL is up and running before it starts SCLK.

2. MCDT_sleep

   Only low frequency clock (either 6.25kHz RCO based clock or 32.768kHz XTAL clock) and timers running.

3. MCDT_tx

   The command is only executed after AS3940 is waked.

   After the MCDT transmit command, the framer combines the MCDT package. Preamble and device ID are added, payload length is automatically retrieved from the SDI slave, and the payload data is taken from the TX data buffer. Finally, the CRC is automatically computed. After the transmission is completed, AS3940 is set to standby.

   The sleep mode will only be entered by the command MCDT_sleep.

4. MCDT_rx

   The command is only executed after AS3940 is waked.

   After the MCDT receive command, AS3940 is set in receive mode. Device type (stored in the device type table 0x10…0x23) is used for timing recovery and package filtering. When a package with the correct device type is received, the device type index is stored in 1st byte and the following serial number in 2nd, 3rd and 4th byte of the active RX data buffer. The payload is stored after the serial number, CRC is automatically computed and the result is offered as a flag in the SDI memory map. After the reception is completed, AS3940 is set to standby. If no package with correct device type is received, the MCU can terminate the receive mode on timeout with MCDT_standy command.

   The sleep mode will only be entered by the command MCDT_sleep.

5. MCDT_standby
   The command terminates transmission or reception. 16MHz XTAL and AS3940 waked up.
6. FORCE_STANDBY
   The command terminates both the MCDT or LM controlled transmission or reception.

The used RX/TX parameters (COM mode, PA level and ICF) are retrieved from the pair/wake table (0x90…0x96).

7.3.13 State Diagrams

Figure 10. State Diagram Master

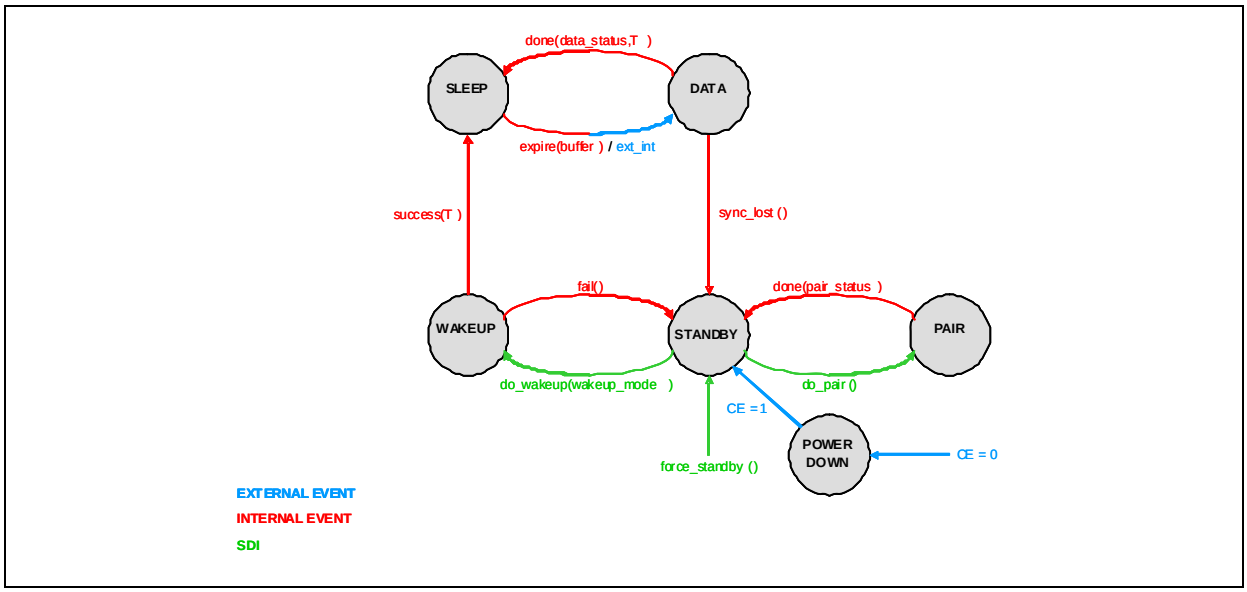
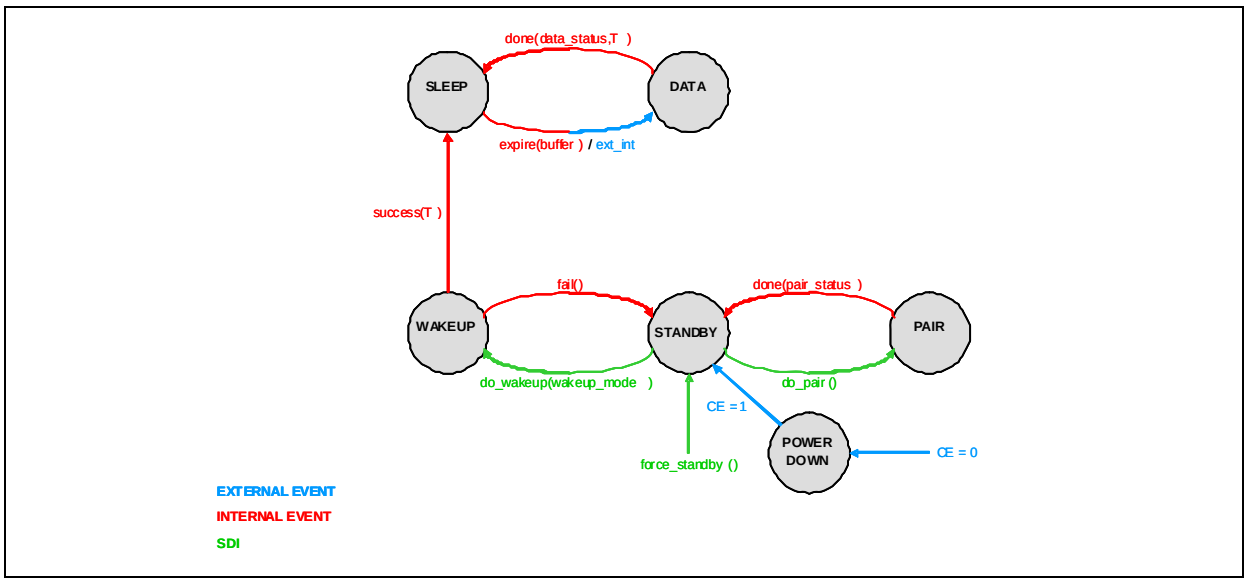


Figure 11. State Diagram Client



8 SDI Description

8.1 SPI Command Information

A 4-wire SPI interface (MCU is SPI master, AS3940 is SPI slave) is defined as following:

- CS chip select, active low
- SCLK bit clock, CPOL=0 (low when idle) is used for the SPI Clock
- MOSI data from MCU to AS3940
- MISO data from AS3940 to MCU

The SPI master always drives the CS and SCLK. The three supported operation cycles are presented below.

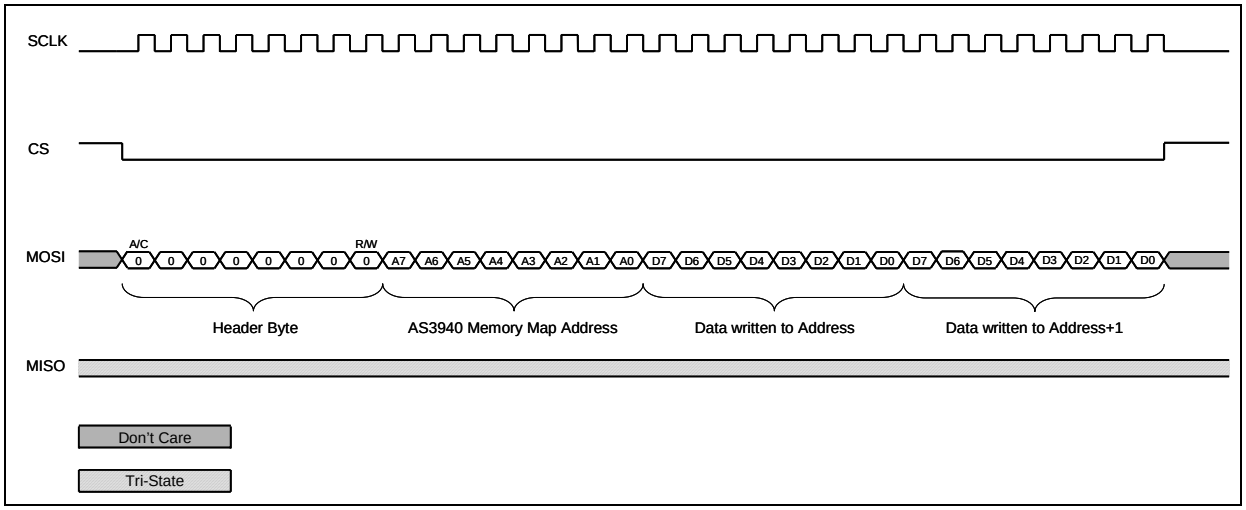
8.1.1 Write Cycle

In write cycle the MCU writes data to AS3940.

The write cycle (see Figure 12) is initiated by activating the CS. The signals on CS and MOSI change with falling edge of SCLK.

After first 8-bits (header byte), next 8 bits are defined as an AS3940 memory map address. The header byte with (A/C=0) and (R/W=0) indicates a write cycle. The next 8 bits contain the data to be written to the specified address. As long as the MCU toggles the SCLK, the AS3940 will interpret the bits on MOSI as data for the next address (auto address increment is supported). The MCU must guarantee the correct number of SCLK edges.

Figure 12. SPI Write Cycle



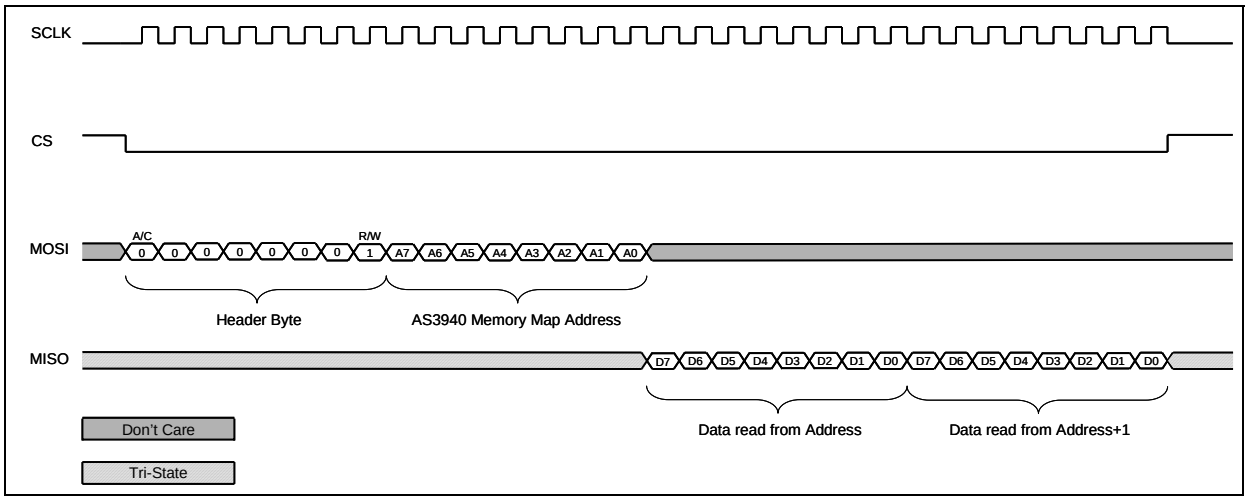
8.1.2 Read Cycle

In read cycle the MCU reads data from AS3940.

The read cycle (see Figure 13) is initiated by activating the CS. The signals on CS, MOSI and MISO change with falling edge of SCLK.

After first 8-bits (header byte), next 8 bits are defined as an AS3940 memory map address. The header byte with (A/C=0) and (R/W=1) indicates a read cycle. The next 8 bits contain the data to be read from the specified address. As long as the MCU toggles the SCLK, the AS3940 will put data on MISO, which is data from the next address (auto address increment is supported). The MCU must guarantee the correct number of SCLK edges.

Figure 13. Read Cycle



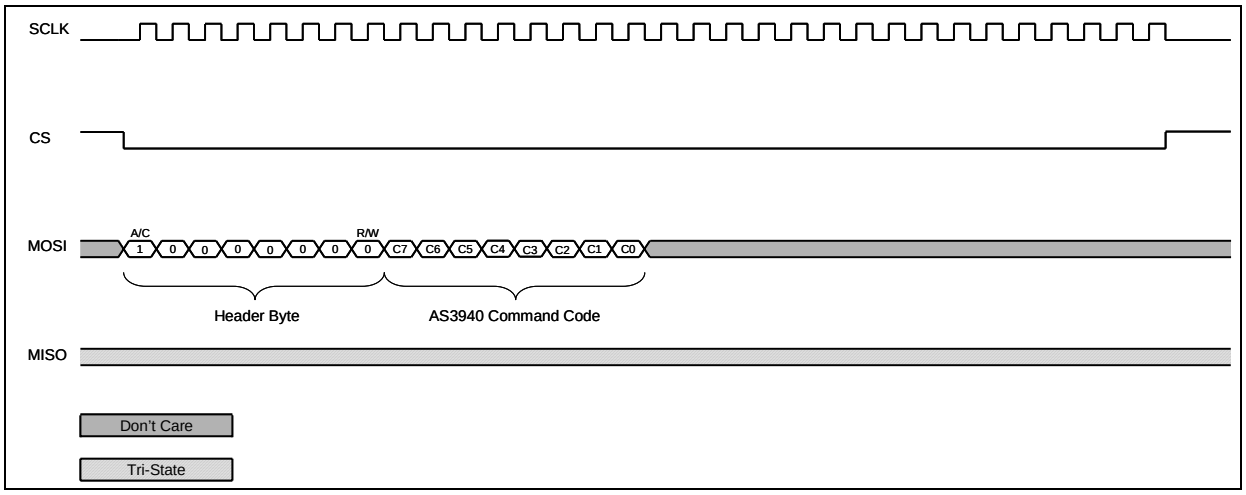
8.1.3 Command Cycle

In command cycle the MCU writes command to AS3940.

The command cycle (see Figure 14) is executed after rising edge of the CS. The signals on CS and MOSI change with falling edge of SCLK.

The header byte with (A/C=1) and (R/W=0) indicate that the next byte is defined as command code for AS3940.

Figure 14. SPI Command Cycle

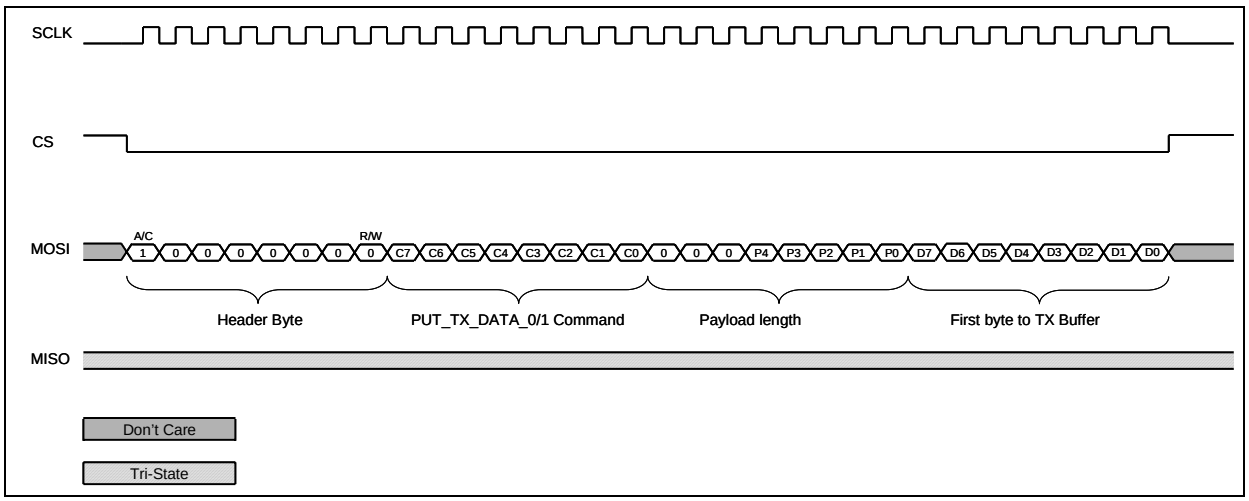


Special commands are defined to exchange data from/to the MCU to/from the AS3940. The different commands are

- PUT_TX_DATA_0 (0010_0000)
- PUT_TX_DATA_1 (0010_0001)
- GET_RX_DATA_0 (0011_0000)
- GET_RX_DATA_1 (0011_0001)

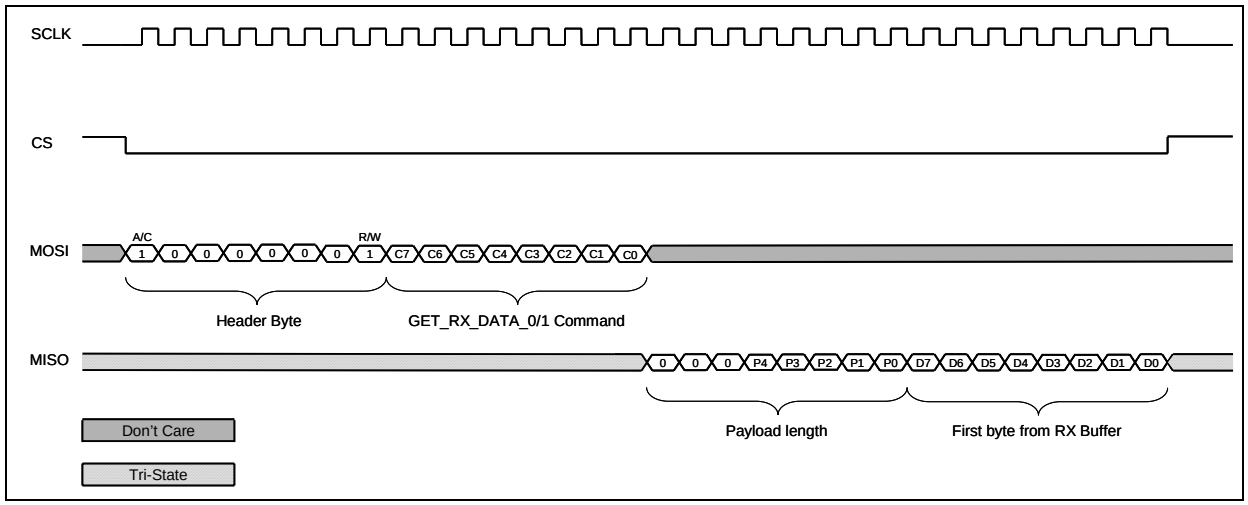
For PUT_TX_DATA_0/1 command (see Figure 15), the next byte defines the payload length followed by the data bytes to be written to the TX buffer. The signals on CS and MOSI change with falling edge of SCLK. The MCU must provide the correct amount edges on SCLK.

Figure 15. PUT_TX_DATA_0/1 Command



For GET_RX_DATA_0/1 command (see Figure 16), the first byte on MISO is the payload length (payload_length=3 equals to 4 data bytes) followed by the data bytes retrieved from the RX buffer. The signals on CS, MOSI, and MISO change with falling edge of SCLK. The MCU must provide the correct amount edges on SCLK

Figure 16. GET_RX_DATA_0/1 Command



After applying a new edge of the CS, the MCU should respect the waiting time of ≥600µs before toggling the SCLK.

8.1.4 SPI Timings

The following figure and table represents SPI timing and timing values.

Figure 17. SPI Timings

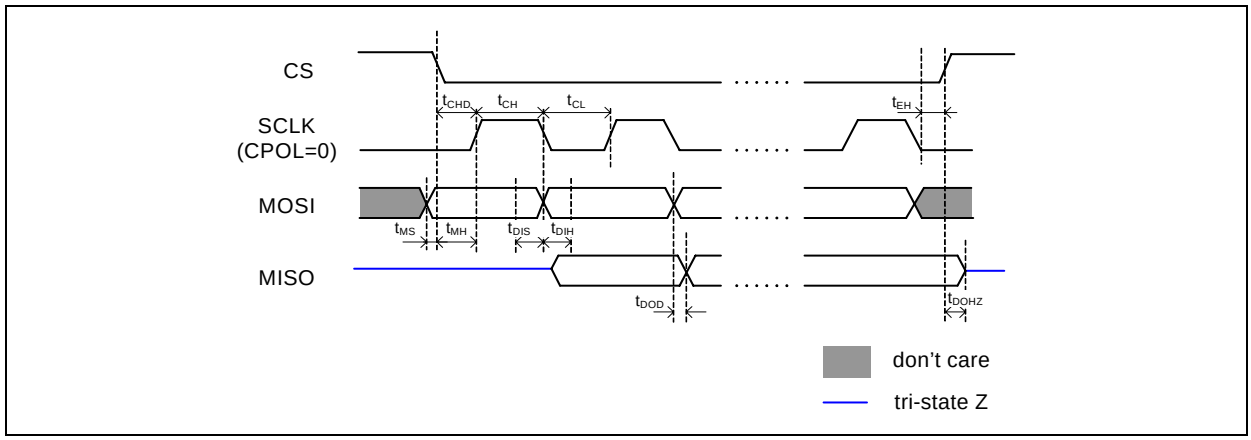


Table 18. General System Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
General						
BR_{SPI}	Bit rate			8		Mbps
t_{CH}	Clock high time			62.5		ns
t_{CL}	Clock low time			62.5		ns
Write timing						
t_{DIS}	Data in setup time		7	10		ns
t_{DIH}	Data in hold time		0	0		ns
t_{EH}	Enable hold time			0		ns
Read timing						
t_{DOD}	Data out delay			3.63		ns
t_{DOHZ}	Data out to high impedance delay			3.3		ns
Timing parameters when leaving the power down mode (for determination of CLK polarity and MCCLK behavior)						
t_{CHD}	Clock hold time (CPOL=0)		10	62.5		ns
t_{MS}	Data in setup time (MCCLK behavior)		0	6		ns
t_{MH}	Data in hold time (MCCLK behavior)		0	10		ns

Note: If AS3940 is in SLEEP mode, CS needs to be pulled low earlier (300µs – 1ms in advance) to accommodate the XTAL start-up.

8.2 SDI Memory Map

8.2.1 Memory Map Overview

The SDI memory map overview is presented in Table 19.

Table 19. SDI Memory Map Overview

Section	Address	Description
General settings, status and IRQ	0x00…0x0A	CLK control, timing settings, interrupt masking and status
RSSI	0x0B…0x0C	RSSI measured by the master and sent back to client in ACK1 package
Reserved	0x0D…0x0E	Reserved
SDI commands	0x0F	Available SDI commands
Device type	0x10…0x2F	Defines the client types with which pairing is possible (must be filled by the MCU)
Client tables	0x30…0x39	Client 0 settings
	0x3A…0x43	Client 1 settings
	0x44…0x4D	Client 2 settings
	0x4E…0x57	Client 3 settings
	0x58…0x61	Client 4 settings
	0x62…0x6B	Client 5 settings
	0x6C…0x75	Client 6 settings
	0x76…0x7F	Client 7 settings
ACS table	0x80…0x8F	Defines the channels used for ACS
SDI settings	0x90…0x99	Defines the pairing settings
Reserved	0x9A…0xA5	Reserved
Device data	0xA6…0xA8	Not used by the LM
	0xA9…0xAD	Serial number
Reserved	0xAE…0xAF	Reserved
RSSI	0xB0…0xB5	Sets the threshold for listen-before-talk, actual RSSI value
Reserved	0xB6…0xE2	Reserved
ENG_BITS	0xE1…0xE3	Set for optimized analog performance of AS3940
Reserved	0xE4…0xFC	Reserved
Chip_ID	0xFD…0xFE	Chip ID of AS3940
Rev_ID	0xFF	Revision number of AS3940

8.2.2 Commands

The different SDI commands are presented in Table 20.

Table 20. SDI Commands

Address	Command	b[7:0]	Description
0x0F	do_wake_up	0000 1000	Exchange of time code (or seed) and communication parameters, master synchronizes to client time base.
	do_wake_up_from_client	0000 1001	Master is set to receive mode for short time with long interval. Client transmits long enough wakeup sequence to catch the receive window of the master.
	do_wake_up_from_master	0000 1010	Client is set to receive mode for short time with long interval. Master transmits long enough wakeup sequence to catch the receive window of the client.
	do_pair	0000 1100	Exchange of device IDs between a master and a client. Pairing is required prior to any transmission of payload data.
	force_stand_by	1000 0000	Forces AS3940 into its standby status. Execution of other commands is immediately stopped.
	do_mcdt_standby	0000_0011	The command terminates transmission or reception. 16MHz XTAL and AS3940 waked up.
	do_mcdt_rx	0000_0100	The command sets AS3940 in receive mode. After the reception is completed, a maskable interrupt (MCDT_RX_READY) is set to inform the MCU and AS3940 is set to standby. If no package with correct device type is received, the MCU can terminate the receive mode on timeout with MCDT_standy command.
	do_mcdt_tx	0000_0101	The command is only executed after AS3940 is waked. The framer combines the MCDT package and after it is transmitted, a maskable interrupt (MCDT_TX_READY) is set to inform the MCU and AS3940 is set to standby.
	do_mcdt_wakeup	0000_0110	The command wakes up the 16MHz XTAL and AS3940, the MCU must guarantee that the XTAL is running before it starts the SCLK.
	do_mcdt_sleep	0000_0111	The command set AS3940 in sleep mode. Only low frequency clock (either 6.25kHz RCO based clock or 32.768kHz XTAL clock) and timers running.
	do_temp_pair	0000_1111	Exchange of device IDs between a master and a client. Pairing is not stored permanently, but only for the temporary communication session.
	do_send_lib	0001_0000	The permanent master transmits the corresponding LIB packages immediately after finishing the communication with the client.
	do_sw_reset	1111_1111	The SPI register map is reset to default values

8.2.3 Memory Map

This section defines the SDI Memory Map of the AS3940 Transceiver IC.

- Addresses are in hex-format
- Per entry, the access type is given (R, W, R/W). In case the access type is R/W, the entry functionality is used to control by W-access; the R-access can be used for read-back (debugging)
- In case a register has W-access or R/W-access, the default value is indicated. Unless specified else, default values are assigned only after applying the supply voltage to AS3940.

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x00	CLK_CONTROL_1	b[7]	R/W[1] 0x66	0	RCO Calibration disabled
				1	RCO Calibration enabled
		b[6]		0	MCCLK disabled
				1	MCCLK enabled
		b[5]		0	RTC disabled
				1	RTC enabled
		b[4:3]		00	active MCCLK set to 1 MHz
				01	active MCCLK set to 2 MHz
				10	active MCCLK set to 4 MHz
				11	active MCCLK set to 8 MHz
		b[2]		0	RTC set to 32.768 kHz
				1	RTC set to 6.25 kHz
		b[1]		0	AS3940 timer clock set to 32.768 kHz
				1	AS3940 timer clock set to 6.25 kHz
		b[0]		0	32.768 kHz oscillator disabled
				1	32.768 kHz oscillator enabled
0x01	CLK_CONTROL_0	b[7:5]	R/W 0x09	not used	
		b[4:3]		00	MCCLK disabled during sleep
				01	MCCLK = 6.25 kHz during sleep
				10	MCCLK stays active during sleep
				11	not used
		b[2:0]		000	RTC tolerance set to ±0 ppm
				001	RTC tolerance set to ±50 ppm
				010	RTC tolerance set to ±100 ppm
				011	RTC tolerance set to ±150 ppm
				100	RTC tolerance set to ±200 ppm
				101	RTC tolerance set to ±250 ppm
				110	RTC tolerance set to ±300 ppm
				111	RTC tolerance set to ±350 ppm

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x02	INT_MASKING_2	b[7]	R/W 0x00	0	tx_data_1 interrupt disabled
				1	tx_data_1 interrupt enabled
		b[6]		0	tx_data_0 interrupt disabled
				1	tx_data_0 interrupt enabled
		b[5]		0	rx_data_1 interrupt disabled
				1	rx_data_1 interrupt enabled
		b[4]		0	rx_data_0 interrupt disabled
				1	rx_data_0 interrupt enabled
		b[3]		0	tx_data_failed interrupt disabled
				1	tx_data_failed interrupt enabled
		b[2]		0	rx_data_failed interrupt disabled
				1	rx_data_failed interrupt enabled
		b[1]		0	pair_wake_done interrupt disabled
				1	pair_wake_done interrupt enabled
		b[0]		0	pair_wake_failed interrupt disabled
				1	pair_wake_failed interrupt enabled
0x03	INT_MASKING_1	b[7]	R/W 0x00	0	lo_bat interrupt disabled
				1	lo_bat interrupt enabled
		b[6]		Reserved	
		b[5]		0	sync_lost interrupt disabled
				1	sync_lost interrupt enabled
		b[4]		0	paired_full interrupt disabled
				1	paired_full interrupt enabled
		b[3]		0	already_paired interrupt disabled
				1	already_paired interrupt enabled
		b[2]		0	tx_ready interrupt disabled
				1	tx_ready interrupt enabled
		b[1]		0	rx_ready interrupt disabled
				1	rx_ready interrupt enabled
		b[0]		0	dev_id_found interrupt disabled
				1	dev_id_found interrupt enabled

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x04	INT_MASKING_0	b[7:0]	R/W 0x00	0	lib_done interrupt disabled
				1	lib_done interrupt enabled
		b[6]		0	lib_failed interrupt disabled
				1	lib_failed interrupt enabled
		b[5]		0	mcdt_rx_ready interrupt disabled
				1	mcdt_rx_ready interrupt enabled
		b[4]		0	mcdt_tx_ready interrupt disabled
				1	mcdt_tx_ready interrupt enabled
		b[3]		0	eoc_request interrupt disabled
				1	eoc_request interrupt enabled
		b[2]		0	unpair_request interrupt disabled
				1	unpair_request interrupt enabled
		b[1:0]		not used	
0x05	INT_STATUS_2	b[7]	R^2	tx_data_1	
		b[6]		tx_data_0	
		b[5]		rx_data_1	
		b[4]		rx_data_0	
		b[3]		tx_data_failed	
		b[2]		rx_data_failed	
		b[1]		pair_wake_done	
		b[0]		pair_wake_failed	
0x06	INT_STATUS_1	b[7]	R	lo_bat	
		b[6]		Reserved	
		b[5]		sync_lost	
		b[4]		paired_full	
		b[3]		already_paired	
		b[2]		tx_ready	
		b[1]		rx_ready	
		b[0]		dev_id_found	
0x07	INT_STATUS_0	b[7]	R	lib_done	
		b[6]		lib_failed	
		b[5]		mcdt_rx_ready	
		b[4]		mcdt_tx_ready	
		b[3]		eoc_request	
		b[2]		unpair_request	
		b[1:0]		not used	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x08	RX_STATUS	b[7:6]	R	not used	
		b[5]		mdct_rx_crc_ok	
		b[4]		rx_data_crc_ok	
		b[3:0]		client_index[3:0]	
0x09	TRX_CHANNEL	b[7]	R	not used	
		b[6:0]		trx_channel	
0x0A	BUFFER_STATUS	b[7:4]	R	not used	
		b[3]		0	TX buffer 0 selected by AS3940
				1	TX buffer 1 selected by AS3940
		b[2]		0	RX buffer 0 selected by AS3940
				1	RX buffer 1 selected by AS3940
		b[1]		0	TX buffer 1 can be refilled by MCU
				1	TX buffer 1 should not be refilled by MCU
		b[0]		0	TX buffer 0 can be refilled by MCU
				1	TX buffer 0 should not be refilled by MCU
0x0B	MASTER_RSSI_1	b[7:2]	R	not used	
		b[1:0]		RSSI[9:8]	
0x0C	MASTER_RSSI_0	b[7:0]	R	RSSI[7:0]	
0x0D		b[7:0]		Reserved	
0x0E		b[7:0]		Reserved	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x0F	COMMAND	b[7:0]	R/W 0x00	0000_0000	Reserved
				1000_0000	force_stand_by
				0000_0011	do_mcdt_standby
				0000_0100	do_mcdt_rx
				0000_0101	do_mcdt_tx
				0000_0110	do_mcdt_wakeup
				0000_0111	do_mcdt_sleep
				0000_1000	do_wake_up
				0000_1001	do_wake_up_from_client
				0000_1010	do_wake_up_from_master
				0000_1100	do_pair
				0000_1111	do_temp_pair
				0001_0000	do_send_lib
				1111_1111	do_sw_reset
0x10	DEV_TYPE_0_1	b[7:0]	R/W 0x00	Device type 0 [15:8]	
0x11	DEV_TYPE_0_0	b[7:0]	R/W 0x00	Device type 0 [7:0]	
0x12	DEV_TYPE_1_1	b[7:0]	R/W 0x00	Device type 1 [15:8]	
0x13	DEV_TYPE_1_0	b[7:0]	R/W 0x00	Device type 1 [7:0]	
0x14	DEV_TYPE_2_1	b[7:0]	R/W 0x00	Device type 2 [15:8]	
0x15	DEV_TYPE_2_0	b[7:0]	R/W 0x00	Device type 2 [7:0]	
0x16	DEV_TYPE_3_1	b[7:0]	R/W 0x00	Device type 3 [15:8]	
0x17	DEV_TYPE_3_0	b[7:0]	R/W 0x00	Device type 3 [7:0]	
0x18	DEV_TYPE_4_1	b[7:0]	R/W 0x00	Device type 4 [15:8]	
0x19	DEV_TYPE_4_0	b[7:0]	R/W 0x00	Device type 4 [7:0]	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x1A	DEV_TYPE_5_1	b[7:0]	R/W 0x00	Device type 5 [15:8]	
0x1B	DEV_TYPE_5_0	b[7:0]	R/W 0x00	Device type 5 [7:0]	
0x1C	DEV_TYPE_6_1	b[7:0]	R/W 0x00	Device type 6 [15:8]	
0x1D	DEV_TYPE_6_0	b[7:0]	R/W 0x00	Device type 6 [7:0]	
0x1E	DEV_TYPE_7_1	b[7:0]	R/W 0x00	Device type 7 [15:8]	
0x1F	DEV_TYPE_7_0	b[7:0]	R/W 0x00	Device type 7 [7:0]	
0x20	DEV_TYPE_8_1	b[7:0]	R/W 0x00	Device type 8 [15:8]	
0x21	DEV_TYPE_8_0	b[7:0]	R/W 0x00	Device type 8 [7:0]	
0x22	DEV_TYPE_9_1	b[7:0]	R/W 0x00	Device type 9 [15:8]	
0x23	DEV_TYPE_9_0	b[7:0]	R/W 0x00	Device type 9 [7:0]	
0x24 - 0x2F				Reserved	
0x30	CLIENT_0_9	b[7:4]	R/W 0x00	Device type index client 0 [3:0]	
		b[3:0]		Serial number client 0 [23:20]	
0x31	CLIENT_0_8	b[7:0]	R/W 0x00	Serial number client 0 [19:12]	
0x32	CLIENT_0_7	b[7:0]	R/W 0x00	Serial number client 0 [11:4]	
0x33	CLIENT_0_6	b[7:4]	R/W 0x02	Serial number client 0 [3:0]	
		b[3]		0	client 0 not paired
				1	client 0 paired
		b[2]		0	client 0 of AS3940 type
				1	Reserved
		b[1]		0	client 0 data CRC not OK
				1	client 0 data CRC OK
		b[0]		0	client 0 not waked up
				1	client 0 waked up
0x34	CLIENT_0_5	b[7]	R	0	client 0 in sync
				1	client 0 sync lost
		b[6:0]		0b0000000	
0x35	CLIENT_0_4	b[7:5]	R	0b000	
		b[4:0]		Client 0 BLTH[4:0]	
0x36	CLIENT_0_3	b[7:0]	R/W 0x00	Client 0 time code [7:0]	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x37	CLIENT_0_2	b[7]	R/W 0x05	0	ACS disabled for client 0
				1	ACS enabled for client 0
		b[6:0]		ICF[6:0] for client 0	
0x38	CLIENT_0_1	b[7:5]	R/W 0x01	COM[2:0] for client 0	
		b[4:1]		PA[3:0] for client 0	
		b[0]		0	auto acknowledge disabled for client 0
				1	auto acknowledge enabled for client 0
0x39	CLIENT_0_0	b[7:6]	R/W 0xC8	RT[1:0] for client	
		b[5]	R	0	client 0 battery voltage above threshold
				1	client 0 battery voltage below threshold
		b[4:3]	R/W 0xC8	timecode scaling client 0	
		b[2]		0	client 0 streaming disabled
				1	client 0 streaming enabled
		b[1:0]		stream_duty_cycle[1:0] for client 0	
0x3A	CLIENT_1_9	b[7:4]	R/W 0x00	Device type index client 1 [3:0]	
		b[3:0]		Serial number client 1 [23:20]	
0x3B	CLIENT_1_8	b[7:0]	R/W 0x00	Serial number client 1 [19:12]	
0x3C	CLIENT_1_7	b[7:0]	R/W 0x00	Serial number client 1 [11:4]	
0x3D	CLIENT_1_6	b[7:4]	R/W 0x02	Serial number client 1 [3:0]	
		b[3]		0	client 1 not paired
				1	client 1 paired
		b[2]		0	client 1 of AS3940 type
				1	Reserved
		b[1]		0	client 1 data CRC not OK
				1	client 1 data CRC OK
		b[0]		0	client 1 not waked up
				1	client 1 waked up
0x3E	CLIENT_1_5	b[7]	R	0	client 1 in sync
				1	client 1 sync lost
		b[6:0]		0b0000000	
0x3F	CLIENT_1_4	b[7:5]	R	0b000	
		b[4:0]		Client 1 BLTH[4:0]	
0x40	CLIENT_1_3	b[7:0]	R/W 0x00	Client 1 time code [7:0]	
0x41	CLIENT_1_2	b[7]	R/W 0x05	0	ACS disabled for client 1
				1	ACS enabled for client 1
		b[6:0]		ICF[6:0] for client 1	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x42	CLIENT_1_1	b[7:5]	R/W 0x01	COM[2:0] for client 1	
		b4:1]		PA[3:0] for client 1	
		b[0]		0	auto acknowledge disabled for client 1
				1	auto acknowledge enabled for client 1
0x43	CLIENT_1_0	b[7:6]	R/W 0xC8	RT[1:0] for client	
		b[5]	R	0	client 1 battery voltage above threshold
				1	client 1 battery voltage below threshold
		b[4:3]	R/W 0xC8	time code scaling client 1	
		b[2]		0	client 1 streaming disabled
		b[2]		1	client 1 streaming enabled
		b[1:0]		stream_duty_cycle[1:0] for client 1	
0x44	CLIENT_2_9	b[7:4]	R/W 0x00	Device type index client 2 [3:0]	
		b[3:0]		Serial number client 2 [23:20]	
0x45	CLIENT_2_8	b[7:0]	R/W 0x00	Serial number client 2 [19:12]	
0x46	CLIENT_2_7	b[7:0]	R/W 0x00	Serial number client 2 [11:4]	
0x47	CLIENT_2_6	b[7:4]	R/W 0x02	Serial number client 2 [3:0]	
		b[3]		0	client 2 not paired
				1	client 2 paired
		b[2]		0	client 2 of AS3940 type
		b[2]		1	Reserved
		b[1]		0	client 2 data CRC not OK
				1	client 2 data CRC OK
		b[0]		0	client 2 not waked up
				1	client 2 waked up
0x48	CLIENT_2_5	b[7]	R	0	client 2 in sync
				1	client 2 sync lost
		b[6:0]		0b0000000	
0x49	CLIENT_2_4	b[7:5]	R	0b000	
		b[4:0]		Client 2 BLTH[4:0]	
0x4A	CLIENT_2_3	b[7:0]	R/W 0x00	Client 2 time code [7:0]	
0x4B	CLIENT_2_2	b[7]	R/W 0x05	0	ACS disabled for client 2
				1	ACS enabled for client 2
		b[6:0]		ICF[6:0] for client 2	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x4C	CLIENT_2_1	b[7:5]	R/W 0x01	COM[2:0] for client 2	
		b[4:1]		PA[3:0] for client 2	
		b[0]		0	auto acknowledge disabled for client 2
				1	auto acknowledge enabled for client 2
0x4D	CLIENT_2_0	b[7:6]	R/W 0xC8	RT[1:0] for client	
		b[5]	R	0	client 2 battery voltage above threshold
				1	client 2 battery voltage below threshold
		b[4:3]	R/W 0xC8	time code scaling client 2	
		b[2]		0	client 2 streaming disabled
		b[2]		1	client 2 streaming enabled
		b[1:0]		stream_duty_cycle[1:0] for client 2	
0x4E	CLIENT_3_9	b[7:4]	R/W 0x00	Device type index client 3 [3:0]	
		b[3:0]		Serial number client 3 [23:20]	
0x4F	CLIENT_3_8	b[7:0]	R/W 0x00	Serial number client 3 [19:12]	
0x50	CLIENT_3_7	b[7:0]	R/W 0x00	Serial number client 3 [11:4]	
0x51	CLIENT_3_6	b[7:4]	R/W 0x02	Serial number client 3 [3:0]	
		b[3]		0	client 3 not paired
				1	client 3 paired
		b[2]		0	client 3 of AS3940 type
		b[2]		1	Reserved
		b[1]		0	client 3 data CRC not OK
				1	client 3 data CRC OK
		b[0]		0	client 3 not waked up
				1	client 3 waked up
0x52	CLIENT_3_5	b[7]	R	0	client 3 in sync
				1	client 3 sync lost
		b[6:0]		0b0000000	
0x53	CLIENT_3_4	b[7:5]	R	0b000	
		b[4:0]		Client 3 BLTH[4:0]	
0x54	CLIENT_3_3	b[7:0]	R/W 0x00	Client 3 time code [7:0]	
0x55	CLIENT_3_2	b[7]	R/W 0x05	0	ACS disabled for client 3
				1	ACS enabled for client 3
		b[6:0]		ICF[6:0] for client 3	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x56	CLIENT_3_1	b[7:5]	R/W 0x01	COM[2:0] for client 3	
		b[4:1]		PA[3:0] for client 3	
		b[0]		0	auto acknowledge disabled for client 3
				1	auto acknowledge enabled for client 3
0x57	CLIENT_3_0	b[7:6]	R/W 0xC8	RT[1:0] for client	
		b[5]	R	0	client 3 battery voltage above threshold
				1	client 3 battery voltage below threshold
		b[4:3]	R/W 0xC8	timecode scaling client 3	
		b[2]		0	client 3 streaming disabled
		b[2]		1	client 3 streaming enabled
		b[1:0]		stream_duty_cycle[1:0] for client 3	
0x58	CLIENT_4_9	b[7:4]	R/W 0x00	Device type index client 4 [3:0]	
		b[3:0]		Serial number client 4 [23:20]	
0x59	CLIENT_4_8	b[7:0]	R/W 0x00	Serial number client 4 [19:12]	
0x5A	CLIENT_4_7	b[7:0]	R/W 0x00	Serial number client 4 [11:4]	
0x5B	CLIENT_4_6	b[7:4]	R	Serial number client 4 [3:0]	
		b[3]	R/W 0x02	0	client 4 not paired
				1	client 4 paired
		b[2]		0	client 4 of AS3940 type
		b[2]		1	Reserved
		b[1]		0	client 4 data CRC not OK
				1	client 4 data CRC OK
		b[0]		0	client 4 not waked up
				1	client 4 waked up
0x5C	CLIENT_4_5	b[7]	R	0	client 4 in sync
				1	client 4 sync lost
		b[6:0]		0b0000000	
0x5D	CLIENT_4_4	b[7:5]	R	0b000	
		b[4:0]		Client 4 BLTH[4:0]	
0x5E	CLIENT_4_3	b[7:0]	R/W 0x00	Client 4 time code [7:0]	
0x5F	CLIENT_4_2	b[7]	R/W 0x05	0	ACS disabled for client 4
				1	ACS enabled for client 4
		b[6:0]		ICF[6:0] for client 4	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x60	CLIENT_4_1	b[7:5]	R/W 0x01	COM[2:0] for client 4	
		b[4:1]		PA[3:0] for client 4	
		b[0]		auto acknowledge disabled for client 4	
				auto acknowledge enabled for client 4	
0x61	CLIENT_4_0	b[7:6]	R/W 0xC8	RT[1:0] for client	
		b[5]	R	0	client 4 battery voltage above threshold
				1	client 4 battery voltage below threshold
		b[4:3]	R/W 0xC8	timecode scaling client 4	
		b[2]		0	client 4 streaming disabled
		b[2]		1	client 4 streaming enabled
		b[1:0]		stream_duty_cycle[1:0] for client 4	
0x62	CLIENT_5_9	b[7:4]	R/W 0x00	Device type index client 5 [3:0]	
		b[3:0]		Serial number client 5 [23:20]	
0x63	CLIENT_5_8	b[7:0]	R/W 0x00	Serial number client 5 [19:12]	
0x64	CLIENT_5_7	b[7:0]	R/W 0x00	Serial number client 5 [11:4]	
0x65	CLIENT_5_6	b[7:4]	R/W 0x02	Serial number client 5 [3:0]	
		b[3]		0	client 5 not paired
				1	client 5 paired
		b[2]		0	client 5 of AS3940 type
		b[2]		1	Reserved
		b[1]		0	client 5 data CRC not OK
				1	client 5 data CRC OK
		b[0]		0	client 5 not waked up
				1	client 5 waked up
0x66	CLIENT_5_5	b[7]	R	0	client 5 in sync
				1	client 5 sync lost
		b[6:0]		0b0000000	
0x67	CLIENT_5_4	b[7:5]	R	0b000	
		b[4:0]		Client 5 BLTH[4:0]	
0x68	CLIENT_5_3	b[7:0]	R/W 0x00	Client 5 time code [7:0]	
0x69	CLIENT_5_2	b[7]	R/W 0x05	0	ACS disabled for client 5
				1	ACS enabled for client 5
		b[6:0]		ICF[6:0] for client 5	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x6A	CLIENT_5_1	b[7:5]	R/W 0x01	COM[2:0] for client 5	
		b[4:1]		PA[3:0] for client 5	
		b[0]		0	auto acknowledge disabled for client 5
				1	auto acknowledge enabled for client 5
0x6B	CLIENT_5_0	b[7:6]	R/W 0xC8	RT[1:0] for client	
		b[5]	R	0	client 5 battery voltage above threshold
				1	client 5 battery voltage below threshold
		b[4:3]	R/W 0xC8	timecode scaling client 5	
		b[2]		0	client 5 streaming disabled
		b[2]		1	client 5 streaming enabled
		b[1:0]		stream_duty_cycle[1:0] for client 5	
0x6C	CLIENT_6_9	b[7:4]	R/W 0x00	Device type index client 6 [3:0]	
		b[3:0]		Serial number client 6 [23:20]	
0x6D	CLIENT_6_8	b[7:0]	R/W 0x00	Serial number client 6 [19:12]	
0x6E	CLIENT_6_7	b[7:0]	R/W 0x00	Serial number client 6 [11:4]	
0x6F	CLIENT_6_6	b[7:4]	R/W 0x02	Serial number client 6 [3:0]	
		b[3]		0	client 6 not paired
				1	client 6 paired
		b[2]		0	client 6 of AS3940 type
		b[2]		1	Reserved
		b[1]		0	client 6 data CRC not OK
				1	client 6 data CRC OK
		b[0]		0	client 6 not waked up
				1	client 6 waked up
0x70	CLIENT_6_5	b[7]	R	0	client 6 in sync
				1	client 6 sync lost
		b[6:0]		0b0000000	
0x71	CLIENT_6_4	b[7:5]	R	0b000	
		b[4:0]		Client 6 BLTH[4:0]	
0x72	CLIENT_6_3	b[7:0]	R/W 0x00	Client 6 time code [7:0]	
0x73	CLIENT_6_2	b[7]	R/W 0x05	0	ACS disabled for client 6
				1	ACS enabled for client 6
		b[6:0]		ICF[6:0] for client 6	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x74	CLIENT_6_1	b[7:5]	R/W 0x01	COM[2:0] for client 6	
		b[4:1]		PA[3:0] for client 6	
		b[0]		0	auto acknowledge disabled for client 6
				1	auto acknowledge enabled for client 6
0x75	CLIENT_6_0	b[7:6]	R/W 0xC8	RT[1:0] for client	
		b[5]	R	0	client 6 battery voltage above threshold
				1	client 6 battery voltage below threshold
		b[4:3]	R/W 0xC8	timecode scaling client 6	
		b[2]		0	client 6 streaming disabled
		b[2]		1	client 6 streaming enabled
		b[1:0]		stream_duty_cycle[1:0] for client 6	
0x76	CLIENT_7_9	b[7:4]	R/W 0x00	Device type index client 7 [3:0]	
		b[3:0]		Serial number client 7 [23:20]	
0x77	CLIENT_7_8	b[7:0]	R/W 0x00	Serial number client 7 [19:12]	
0x78	CLIENT_7_7	b[7:0]	R/W 0x00	Serial number client 7 [11:4]	
0x79	CLIENT_7_6	b[7:4]	R/W 0x02	Serial number client 7 [3:0]	
		b[3]		0	client 7 not paired
				1	client 7 paired
		b[2]		0	client 7 of AS3940 type
		b[2]		1	Reserved
		b[1]		0	client 7 data CRC not OK
				1	client 7 data CRC OK
		b[0]		0	client 7 not waked up
				1	client 7 waked up
0x7A	CLIENT_7_5	b[7]	R	0	client 7 in sync
				1	client 7 sync lost
		b[6:0]		0b0000000	
0x7B	CLIENT_7_4	b[7:5]	R	0b000	
		b[4:0]		Client 7 BLTH[4:0]	
0x7C	CLIENT_7_3	b[7:0]	R/W 0x00	Client 7 time code [7:0]	
0x7D	CLIENT_7_2	b[7]	R/W 0x05	0	ACS disabled for client 7
				1	ACS enabled for client 7
		b[6:0]		ICF[6:0] for client 7	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x7E	CLIENT_7_1	b[7:5]	R/W 0x01	COM[2:0] for client 7	
		b[4:1]		PA[3:0] for client 7	
		b[0]		0	auto acknowledge disabled for client 7
				1	auto acknowledge enabled for client 7
0x7F	CLIENT_7_0	b[7:6]	R/W 0xC8	RT[1:0] for client	
		b[5]	R	0	client 7 battery voltage above threshold
				1	client 7 battery voltage below threshold
		b[4:3]	R/W 0xC8	timecode scaling client 7	
		b[2]		0	client 7 streaming disabled
		b[2]		1	client 7 streaming enabled
		b[1:0]		stream_duty_cycle[1:0] for client 7	
0x80	ACS_CHANNEL_0	b[7]	R/W 0x05	not used	
		b[6:0]		channel nr of ACS channel 0	
0x81	ACS_CHANNEL_1	b[7]	R/W 0x08	not used	
		b[6:0]		channel nr of ACS channel 1	
0x82	ACS_CHANNEL_2	b[7]	R/W 0x0B	not used	
		b[6:0]		channel nr of ACS channel 2	
0x83	ACS_CHANNEL_3	b[7]	R/W 0x0E	not used	
		b[6:0]		channel nr of ACS channel 3	
0x84	ACS_CHANNEL_4	b[7]	R/W 0x11	not used	
		b[6:0]		channel nr of ACS channel 4	
0x85	ACS_CHANNEL_5	b[7]	R/W 0x14	not used	
		b[6:0]		channel nr of ACS channel 5	
0x86	ACS_CHANNEL_6	b[7]	R/W 0x17	not used	
		b[6:0]		channel nr of ACS channel 6	
0x87	ACS_CHANNEL_7	b[7]	R/W 0x1A	not used	
		b[6:0]		channel nr of ACS channel 7	
0x88	ACS_CHANNEL_8	b[7]	R/W 0x1D	not used	
		b[6:0]		channel nr of ACS channel 8	
0x89	ACS_CHANNEL_9	b[7]	R/W 0x20	not used	
		b[6:0]		channel nr of ACS channel 9	
0x8A	ACS_CHANNEL_A	b[7]	R/W 0x23	not used	
		b[6:0]		channel nr of ACS channel 10	
0x8B	ACS_CHANNEL_B	b[7]	R/W 0x26	not used	
		b[6:0]		channel nr of ACS channel 11	
0x8C	ACS_CHANNEL_C	b[7]	R/W 0x29	not used	
		b[6:0]		channel nr of ACS channel 12	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description	
0x8D	ACS_CHANNEL_D	b[7]	R/W 0x2C	not used	
		b[6:0]		channel nr of ACS channel13	
0x8E	ACS_CHANNEL_E	b[7]	R/W 0x2F	not used	
		b[6:0]		channel nr of ACS channel 14	
0x8F	ACS_CHANNEL_F	b[7]	R/W 0x32	not used	
		b[6:0]		channel nr of ACS channel 15	
0x90	PAIRWAKE_TABLE_6	b[7]	R/W 0x05	not used	
		b[6:0]		ICF[6:0]	
0x91	PAIRWAKE_TABLE_5	b[7:3]	R/W 0x00	not used	
		b[2:0]		COM[2:0]	
0x92	PAIRWAKE_TABLE_4	b[7:6]	R/W 0x10	not used	
		b[5:4]		time code scaling[1:0]	
		b[3:0]		PA[3:0]	
0x93	PAIRWAKE_TABLE_3	b[7:0]	R/W 0x00	Time code [7:0]	
0x94	PAIRWAKE_TABLE_2	b[7]	R/W 0x00	not used	
		b[6:0]		TNOWUP [14:8]	
0x95	PAIRWAKE_TABLE_1	b[7:0]	R/W 0x0A	TNOWUP [7:0]	
0x96	PAIRWAKE_TABLE_0	b[7:0]	R/W 0x0F	Trial_max [7:0]	
0x97	GEN_PUR_LM_SETTINGS_3	b[7:6]	R/W 0x1E	00	Tpolmax = 0.25 s
				01	Tpolmax = 0.50 s
				10	Tpolmax = 1.00 s
				11	Tpolmax = 2.00 s
		b[5]		0	CRC reverse disabled
				1	CRC reverse enabled
		b[4:3]			rx_on_time[1:0]
		b[2:1]			duty_cycle[1:0]
		b[0]		0	device defined as client
		b[0]		1	device defined as master
0x98	GEN_PUR_LM_SETTINGS_2	b[7]	R/W 0x8F	0	16 MHz XTAL startup < 1 ms
				1	16 MHz XTAL startup < 2 ms
		b[6]		Reserved	
		b[5:0]		sync_lost_max[5:0]	

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description
0x99	GEN_PUR_LM_SETTINGS_1	b[7:6]	R/W 0x80	temp_pair_sen[1:0]
		b[5]	R	0 own battery voltage above threshold 1 own battery voltage below threshold
		b[4:0]	R/W 0x80	BLTH[4:0]
0x9A	GEN_PUR_LM_SETTINGS_0	b[7]	R/W 0x00	rssi_check_en
		b[6]		crc_interpret_disable
		b[5]		smart_cal_en
		b[4]		EOC_request
		b[3]		unpair_request
		b[2:0]		client_index[2:0]
0x9B - 0xA5				Reserved
0xA6	DEVICE_DATA_7	b[7:0]	R/W 0xFF	rssi_align [9:2] **Note:** rssi_align[1:0] = 2'b01(hardcoded)
0xA7	DEVICE_DATA_6	b[7:0]	R/W 0xFF	crc_initial [15:8]
0xA8	DEVICE_DATA_5	b[7:0]	R/W 0xFF	crc_initial [7:0]
0xA9	DEVICE_DATA_4	b[7:0]	R/W 0xFF	device_type [15:8]
0xAA	DEVICE_DATA_3	b[7:0]	R/W 0xFF	device_type [7:0]
0xAB	DEVICE_DATA_2	b[7:0]	R/W 0xFF	serial_number [23:16]
0xAC	DEVICE_DATA_1	b[7:0]	R/W 0xFF	serial_number [15:8]
0xAD	DEVICE_DATA_0	b[7:0]	R/W 0xFF	serial_number[7:0]
0xAE				Reserved
0xAF				Reserved
0xB0	CORRELATION_THR_1	b[7:4]	R/W 0x00	not used
		b[3:0]		Correlation threshold bit [11:8]
0xB1	CORRELATION_THR_0	b[7:0]	R/W 0x00 (0x0A)	Correlation threshold bit [7:0]
0xB2	LOG_RSSI_THR_1	b[7:2]	R/W 0x00	not used
		b[1:0]		Threshold RSSI bit [9:8]
0xB3	LOG_RSSI_THR_0	b[7:0]	R/W 0x00	Threshold RSSI bit [7:0]
0xB4	LOG_RSSI_ACT_VALUE_1	b[7:2]	R	not used
		b[1:0]		Actual LOG RSSI value bit [9:8]
0xB5	LOG_RSSI_ACT_VALUE_0	b[7:0]	R	Actual LOG RSSI value bit [7:0]

Table 21. Description of Registers

Address	Register Name	Bit	Type	Description
0xB6 - 0xDF				Reserved
0xE0				Reserved
0xE1	ENG_BITS_3	b[7:0]	R/W 0x80 (0x69)	Engineering bits
0xE2	ENG_BITS_2	b[7:0]	R/W 0x20 (0x24)	Engineering bits
0xE3	ENG_BITS_1	b[7:0]	R/W 0x19 (0x58)	Engineering bits
0xE4	ENG_BITS_0	b[7:0]	R/W 0x51	Engineering bits
0xE5 - 0xFC				Reserved
0xFD	CHIP_ID_1	b[7:0]	R 0x45	chip ID [15:8]
0xFE	CHIP_ID_0	b[7:0]	R 0x6D	chip ID [7:0]
0xFF	REV_ID	b[7:0]	R 0x01	Rev ID [7:0]

1. The default value of this register is set after applying the supply to AS3940 and after '1' at the CE input (pin 25).
2. Reading the status registers 0x05 and 0x06 will automatically reset the data to 0x00.

8.2.4 Register Description

This section gives more information on the functionality of the SDI registers. Unless indicated differently, the register is R/W.

Some reserved registers are used to control the internal modem operation and it is HIGHLY RECOMMENDED not to change the value of those registers. On the other hand, it is HIGHLY RECOMMENDED to change the default values of the registers 0x10..0x23 (See Address 0x10 - 0x23: DEVICE TYPE TABLE on page 61) for optimized behavior of AS3940.

8.2.4.1 Address 0x00: CLK_CONTROL_1

- b[7]: to activate the RCO Calibration. A calibration takes about 20 ms; during this time it has to be assured that the 16 MHz XTAL stays on.
  - b[7] = 0 RCO Calibration disabled.
  - b[7] = 1 RCO Calibration enabled.
- b[6]: to activate the signal on the MCCLK output (pin 15) during active modes of the AS3940. A mode is defined as active in case the 16 MHz XTAL of the AS3940 is enabled.
  - b[6] = 0 MCCLK at pin 15 is fixed '0'.
  - b[6] = 1 MCCLK at pin 15 outputs a clock signal. Frequency is set by b[4:3] of this same control byte.
- b[5]: to activate the signal on the RTC output (pin 23).
  - b[5] = 0 RTC at pin 23 is fixed '0'.
  - b[5] = 1 RTC at pin 23 outputs a clock signal. Frequency is set by b[2] of this same control byte.
- b[4:3]: sets the frequency of the signal on the MCCLK output (pin 15) during active modes.
  - b[4:3] = 00 MCCLK at pin 15 set to 1 MHz.
  - b[4:3] = 00 MCCLK at pin 15 set to 2 MHz.
  - b[4:3] = 00 MCCLK at pin 15 set to 4 MHz.
  - b[4:3] = 00 MCCLK at pin 15 set to 8 MHz.

- b[2]: sets the frequency of the signal on the RTC output (pin 23).
  - b[2] = 0 RTC at pin 23 set to 32768 Hz. This setting is supported when a 32768 Hz XTAL is applied to pins 21 and 22 of the AS3940.
  - b[2] = 1 RTC at pin 23 set to 6.25 kHz, derived from the on-chip RC Oscillator.
- b[1]: sets the frequency of the signal used by the internal timers of the AS3940.
  - b[1] = 0 internal timer clock set to 32768 Hz. This setting is supported when a 32768 Hz XTAL is applied to pins 21 and 22 of the AS3940.
  - b[1] = 1 internal timer set to 6.25 kHz, derived from the on-chip RC Oscillator.
- b[0]: enables the 32768 XTAL oscillator. This bit must be set in case the internal timer application or the external MCU want to make use of this clock
  - b[0] = 0 32768 XTAL oscillator disabled.
  - b[0] = 1 32768 XTAL oscillator enabled.

8.2.4.2 Address 0x01: CLK_CONTROL_0

- b[7:5] Reserved
- b[4:3]: sets the frequency of the signal on the MCCLK output (pin 15) during sleep mode.
  - b[4:3] = 00 MCCLK disabled during sleep.
  - b[4:3] = 00 MCCLK is set to 6.25 kHz during sleep.
  - b[4:3] = 00 MCCLK is set to the frequency as in active mode. Frequency is determined by the clk_contol_1 b[4:3].
  - b[4:3] = 00 Reserved.
- b[2:0]: sets the frequency tolerance of the clock used by the internal timers. The AS3940 Link Manager takes the tolerance into account while calculating receiving windows.
  - b[2:0] = 001 timer tolerance set to ±50 ppm.
  - b[2:0] = 010 timer tolerance set to ±100 ppm.
  - b[2:0] = 011 timer tolerance set to ±150 ppm.
  - b[2:0] = 100 timer tolerance set to ±200 ppm.
  - b[2:0] = 101 timer tolerance set to ±250 ppm.
  - b[2:0] = 110 timer tolerance set to ±300 ppm.
  - b[2:0] = 111 timer tolerance set to ±350 ppm.

8.2.4.3 Address 0x02: INT_MASKING_2

Masking of the interrupts sets which internal interrupt events are routed to the INT pin (pin 24). The masking does not disable the interrupt status registers, the register values are always updated even the interrupt itself would not be passed on to the INT pin. For information on the interrupt functionality, (see Address 0x05: INT_STATUS_2 (Read only) on page 59).

- b[7] Masking of the tx_data_1 interrupt.
  - b[7] = 0 tx_data_1 interrupt disabled.
  - b[7] = 1 tx_data_1 interrupt enabled.
- b[6] Masking of the tx_data_0 interrupt.
  - b[6] = 0 tx_data_0 interrupt disabled.
  - b[6] = 1 tx_data_0 interrupt enabled.
- b[5] Masking of the rx_data_1 interrupt.
  - b[5] = 0 rx_data_1 interrupt disabled.
  - b[5] = 1 rx_data_1 interrupt enabled.
- b[4] Masking of the rx_data_0 interrupt.
  - b[4] = 0 rx_data_0 interrupt disabled.
  - b[4] = 1 rx_data_0 interrupt enabled.
- b[3] Masking of the tx_data_failed interrupt.
  - b[3] = 0 tx_data_failed interrupt disabled.
  - b[3] = 1 tx_data_failed interrupt enabled.
- b[2] Masking of the rx_data_failed interrupt.
  - b[2] = 0 rx_data_failed interrupt disabled.
  - b[2] = 1 rx_data_failed interrupt enabled.

- b[1] Masking of the pair_wake_done interrupt.
  - b[1] = 0 pair_wake_done interrupt disabled.
  - b[1] = 1 pair_wake_done interrupt enabled.
- b[0] Masking of the pair_wake_failed interrupt.
  - b[0] = 0 pair_wake_failed interrupt disabled.
  - b[0] = 1 pair_wake_failed interrupt enabled.

8.2.4.4 Address 0x03: INT_MASKING_1

Masking of the interrupts sets which internal interrupt events are routed to the INT pin (pin 24). The masking does not disable the interrupt status registers, the register values are always updated even the interrupt itself would not be passed on to the INT pin. For information on the interrupt functionality, (see Address 0x06: INT_STATUS_1 (Read only) on page 59).

- b[7] Masking of the lo_bat interrupt.
  - b[7] = 0 lo_bat interrupt disabled.
  - b[7] = 1 lo_bat interrupt enabled.
- b[6] Masking of the otp_ready interrupt.
  - reserved
- b[5] Masking of the sync_lost interrupt.
  - b[5] = 0 sync_lost interrupt disabled.
  - b[5] = 1 sync_lost interrupt enabled.
- b[4] Masking of the paired_full interrupt.
  - b[4] = 0 paired_full interrupt disabled.
  - b[4] = 1 paired_full interrupt enabled.
- b[3] Masking of the already_paired interrupt.
  - b[3] = 0 already_paired interrupt disabled.
  - b[3] = 1 already_paired interrupt enabled.
- b[2] Masking of the tx_ready interrupt.
  - b[2] = 0 tx_ready interrupt disabled.
  - b[2] = 1 tx_ready interrupt enabled.
- b[1] Masking of the rx_ready interrupt.
  - b[1] = 0 rx_ready interrupt disabled.
  - b[1] = 1 rx_ready interrupt enabled.
- b[0] Masking of the dev_id_found interrupt.
  - b[1] = 0 dev_id_found interrupt disabled.
  - b[1] = 1 dev_id_found interrupt enabled.

8.2.4.5 Address 0x04: INT_MASKING_0

Masking of the interrupts sets which internal interrupt events are routed to the INT pin (pin 24). The masking does not disable the interrupt status registers, the register values are always updated even the interrupt itself would not be passed on to the INT pin. For information on the interrupt functionality, (see Address 0x07: INT_STATUS_0 (Read only) on page 60).

- b[7] Masking of the lib_done interrupt.
  - ob[7] = 0 lib_done interrupt disabled.
  - ob[7] = 1 lib_done interrupt enabled.
- b[6] Masking of the lib_failed interrupt.
  - ob[6] = 0 lib_failed interrupt disabled.
  - ob[6] = 1 lib_failed interrupt enabled.
- b[5] Masking of the mcdt_rx_ready interrupt.
  - ob[5] = 0 mcdt_rx_ready interrupt disabled.
  - ob[5] = 1 mcdt_rx_ready interrupt enabled.
- b[4] Masking of the mcdt_tx_ready interrupt.
  - ob[4] = 0 mcdt_tx_ready interrupt disabled.
  - ob[4] = 1 mcdt_tx_ready interrupt enabled.

- b[3] Masking of the eoc_request interrupt.
  - ob[4] = 0 eoc_request interrupt disabled.
  - ob[4] = 1 eoc_request interrupt enabled.
- b[2] Masking of the unpair_request interrupt.
  - ob[2] = 0 unpair_request interrupt disabled.
  - ob[2] = 1 unpair_request interrupt enabled.
- b[1:0] not used.

8.2.4.6 Address 0x05: INT_STATUS_2 (Read only)

After the interrupt signal becomes available to the MCU (pin 24), additional information on the source of the interrupt can be retrieved via registers int_status_2, int_status_1 and int_status_0. After reading one of the int_status registers, the content of that specific register is cleared.

- b[7] tx_data_1 interrupt active.
  This interrupt is set when a DATA packet from TX buffer 1 is transmitted.
- b[6] tx_data_0 interrupt active.
  This interrupt is set when a DATA packet from TX buffer 0 is transmitted.
- b[5] rx_data_1 interrupt active.
  This interrupt becomes active when a DATA packet is received and stored in RX Buffer 1. The interrupt is set independent form the CRC status of reception.
- b[4] rx_data_0 interrupt active.
  This interrupt becomes active when a DATA packet is received and stored in RX Buffer 0. The interrupt is set independent form the CRC status of reception.
- b[3] tx_data_failed interrupt active.
  This interrupt is only valid in case the AS3940 is set up as client. The interrupt is set in case a client did not receive an error free acknowledge within the allowed amount of re-transmissions.
- b[2] rx_data_failed interrupt is active.
  This interrupt is only valid in case the AS3940 is set up as master. The interrupt is set in case a master has not received an error free data packet within the allowed amount of re-transmissions.
- b[1] pair_wake_done interrupt is active.
  This interrupt becomes active when the pairing or wakeup procedure is successfully finished.
- b[0] pair_wake_failed interrupt is active.
  This interrupt becomes active when the pairing or wakeup procedure is failed.

8.2.4.7 Address 0x06: INT_STATUS_1 (Read only)

- b[7] lo_bat interrupt active.
  This interrupt is set when the battery voltage is over the threshold.
- b[6] reserved
- b[5] sync_lost interrupt active.
  In case the AS3940 is set up as master, it indicates that time synchronization is lost with one of the paired clients. In case the AS3940 is set up as client, it indicates that time synchronization is lost with the paired master.
- b[4] paired_full interrupt active.
  In case the AS3940 is set up as master, it indicates that already 8 clients are paired. In case the AS3940 is set up as client, it indicates that it is already paired to a master.
- b[3] already_paired interrupt is active.
  This interrupt is set when a pairing is done with an already paired device.
- b[2] tx_ready interrupt is active.
  This interrupt is set when the TX Controller is ready.
- b[1] rx_ready interrupt is active.
  This interrupt is set when the RX Controller is ready.
- b[0] dev_id_found interrupt is active.
  This interrupt is set when an ID of a paired device is received.

8.2.4.8 Address 0x07: INT_STATUS_0 (Read only)

- b[7] lib_done interrupt is active.
  This interrupt is set when the temporary paired (LIB packet) is successful.
- b[6] lib_failed interrupt is active.
  This interrupt is set when the temporary paired (LIB packet) has failed.
- b[5] mcdt_rx_ready interrupt is active.
  This interrupt is set when a packet in MCDT mode is received.
- b[4] mcdt_tx_ready interrupt is active.
  This interrupt is set when a packet in MCDT mode is transmitted.
- b[3] eoc_request interrupt is active.
  This interrupt is set when a request for End Of Communication is received.
- b[2] unpair_request interrupt is active.
  This interrupt is set when a request to unpair is received.
- b[1:0] not used

8.2.4.9 Address 0x08: RX_STATUS (Read only)

After reception of a data packet, additional information can be retrieved via this register.

- b[7:6] not used
- b[5] mcdt_rx_crc_ok
  - b[5] = 0 CRC error in the last received MCDT DATA packet.
  - b[5] = 1 no CRC error in the last received MCDT DATA packet.
- b[4] rx_data_crc_ok
  - b[4] = 0 CRC error in the last received DATA packet.
  - b[4] = 1 no CRC error in the last received DATA packet.
- b[3:0] client_index[3:0]. In case the AS3940 is configured as master, the client index indicates from which client data is received. Client_index[3] is always ‘0’.

8.2.4.10 Address 0x09: TRX_CHANNEL (Read only)

After a communication session (RX or TX), the used RF channel is readable. This register can be used e.g. to monitor the frequency channel switching.

- b[7] not used
- b[6:0] trx_channel

The RF frequency used is (2400 + trx_channel) MHz. trx_channel settings from 0 to 4 are not supported.

8.2.4.11 Address 0x0A: BUFFER_STATUS (Read only)

In the AS3940, two RX buffers and two TX buffer are integrated. All buffers have the size of 32 bytes (256 bits). Via the bits in this register, the buffer usage by the AS3940 can be checked.

- b[7:4] not used
- b[3] tx_buffer usage
  - b[3] = 0 TX Buffer 0 is used by AS3940. At transmission of a DATA packet, payload will be transmitted from TX Buffer 0.
  - b[3] = 1 TX Buffer 1 is used by AS3940. At transmission of a DATA packet, payload will be transmitted from TX Buffer 1.
- b[2] rx_buffer usage
  - b[2] = 0 RX Buffer 0 is used by AS3940. At reception of a DATA packet, payload will be stored in RX Buffer 0.
  - b[2] = 1 RX Buffer 1 is used by AS3940. At reception of a DATA packet, payload will be stored in RX Buffer 1.
- b[1] TX_buffer 1 usage
  - b[1] = 0 TX Buffer 1 can be used by the MCU for store new payload for a DATA packet to be transmitted.
  - b[1] = 1 TX Buffer 1 is used by AS3940. No access control is provided to TX Buffer 1 and it is highly recommended not to access TX Buffer 1 by the MCU.
- b[0] TX_buffer 0 usage
  - b[0] = 0 TX Buffer 0 can be used by the MCU for store new payload for a DATA packet to be transmitted.
  - b[0] = 1 TX Buffer 0 is used by AS3940. No access control is provided to TX Buffer 0 and it is highly recommended not to access TX Buffer 1 by the MCU.

8.2.4.12 Address 0x0B - 0x0C: MASTER_RSSI (Read only)

During reception of a DATA packet, a master is measuring the RSSI. The master reports the measured RSSI via an ACK packet. During reception of the ACK packet by the client, the RSSI info is readable.

- address 0x0B b[1:0] = master_rssi[9:8]
- address 0x0C b[7:0] = master_rssi[7:0]

Master RSSI is reported as logarithmic value

$$MASTER\_RSSI = 64 \cdot^{2} \log(\frac{\overline{RSSI}}{8})$$

8.2.4.13 Address 0x0F: COMMAND

A set of high level commands are defined for the AS3940. A write action to this register defines and executes the command.

- do_mcdt_standby = 0000_0011: This command terminates transmission or reception. 16MHz XTAL and AS3940 waked up.
- do_mcdt_rx = 0000_0100: This command sets AS3940 in receive mode. After the reception is completed, a maskable interrupt (MCDT_RX_READY) is set to inform the MCU and AS3940 is set to standby. If no package with correct device type is received, the MCU can terminate the receive mode on timeout with MCDT_standy command.
- do_mcdt_tx = 0000_0101: This command is executed only after AS3940 is waked. The framer combines the MCDT package and after it is transmitted, a maskable interrupt (MCDT_TX_READY) is set to inform the MCU and AS3940 is set to standby.
- do_mcdt_wakeup = 0000_0110: This command wakes up the 16MHz XTAL and AS3940, the MCU must guarantee that the XTAL is running before it starts the SCLK.
- do_mcdt_sleep = 0000_0111: This command sets AS3940 in sleep mode. Only low frequency clock (either 6.25kHz RCO based clock or 32.768kHz XTAL clock) and timers are running.
- do_temp_pair = 0000_1111: This command exchanges device IDs between a master and a client. Pairing is not stored permanently, but only for the temporary communication session.
- do_send_lib = 0001_0000: This command sets permanent master to transmit the corresponding LIB packages immediately after finishing the communication with the client.
- do_sw_reset = 1111_1111: This command resets the SPI register map to default values.
- do_prog_device_data = reserved
- force_stand_by = 1000_0000: This command forces the AS3940 in to its standby status. Execution of other commands is immediately stopped.
- do_wake_up = 0000_1000: This command exchanges the time code (or seed) and communication parameters, master synchronizes to client time base.
- do_wake_up_from_client = 0000_1001: This command sets the master to receive mode for short time with long interval. Client transmits long enough wakeup sequence to catch the receive window of the master.
- do_wake_up_from_master = 0000_1010: This command sets the client to receive mode for short time with long interval. Master transmits long enough wakeup sequence to catch the receive window of the client.
- do_pair = 0000_1100: This command exchanges the device IDs between a master and a client. Pairing is required prior to any transmission of payload data.

8.2.4.14 Address 0x10 - 0x23: DEVICE TYPE TABLE

During reception, the RX data path of the AS3940 is only sensitive for information of supported device types. A device type is a 2-byte field.

- address 0x10 = device type 0 [15:8]
- address 0x11 = device type 0 [7:0]

In total a table of 10 supported device types is available. The mapping of the other 9 device types can be seen in the SDI Memory Map.

8.2.4.15 Address 0x30 - 0x7F: CLIENT TABLE

For all of the 8 clients, control and status information is accessible via the client table. For each client, the table structure is identical; detailed information is only given client 0.

- client_0_9 b[7:4] = device type index [3:0] of client 0.
  After pairing, the read-only bit group shows to which kind of a device type the AS3940 is paired. It refers to an index in the device type table (see Address 0x10 - 0x23: DEVICE TYPE TABLE on page 61). This bit group is read only.

- client_0_9 b[3:0] / client_0_8[7:0] / client_0_7[7:0] / client_0_6[7:4] =
  serial number [23:0] of client 0. This bit group is read only.
  During pairing, serial numbers are exchanged between clients and master and the other way around. The client serial numbers exchanged to the master can be read back via this read-only bit-group. In case the device is configured as client, the master serial number is stored in the client 0 table.
- client_0_6 b[3] = client 0 pairing status.
  Via this bit, the MCU of the master can monitor the pairing status of each client.
  - b[3] = 0 client 0 not paired.
  - b[3] = 1 client 0 paired.
- client_0_6 b[2] = Reserved.
- client_0_6 b[1] = CRC status of last received data packet.
  In case a data packet is received from client 0, the CRC status of that packet is reported. This bit is read only.
  - b[1] = 0 client 0 data packet CRC not OK.
  - b[1] = 1 client 0 data packet CRC OK.
- client_0_6 b[0] = wake up status.
  This bit indicates whether a client is waked up. The master determines this based upon the clients response to a wake up sequence. This bit is read only.
  - b[0] = 0 client 0 not waked up.
  - b[0] = 1 client 0 waked up.
- client_0_5 b[7] = synchronization status.
  This bit indicates whether the master is still synchronized with the master. Synchronization is considered lost when then number of consecutive time slots with unsuccessful data exchange exceeds the max_sync_lost value (see Address 0x97 - 0x9A: GEN_PUR_LM_SETTING3/2/1/0 on page 65). This bit is read only.
  - b[7] = 0 client 0 in sync.
  - b[7] = 1 client 0 synchronization lost.
- client_0_4 b[4:0] = client 0 battery level threshold.
  Before transmission of an ACK0/ACK1 packet, the battery voltage is compared with a threshold value. The results of the compare plus the threshold are transmitted in the ACK0/ACK1 packet. After receiving this info, the BLTH content is readable. This bit group is read only.
  In case the AS3940 is configures as master, battery information per client is available. In case the AS3940 is configured as client, the client 0 table is used to store the information.
- client_0_3 b[7:0] = client 0 timecode.
  Timecode used by client 0. The periodicity of client 0 equals (895 + timecode)/2048 s. In case the timecode is set 0xFF, client 0 operates with random timecode.
- client_0_2 b[7] = ACS enabling.
  For interference robustness during DATA mode, a ACS algorithm can be enabled. The RF frequencies used for ACS are derived from the ACS table.
  - b[7] = 0 ACS for client 0 disabled during DATA mode.
  - b[7] = 1 ACS for client 0 enabled during DATA mode.
- client_0_2 b[6:0] = ICF
  In case the ACS is disabled, the RF frequency set via ICF is used in DATA mode by client 0. The RF frequency used is (2400 + ICF) MHz. ICF settings from 0 up to 4 are not supported.

  In case the ACS is enabled, b[3:0] of ICF is used as point to the ACS table to indicate the initial frequency used during ACS
- client_0_1 b[7:5] = COM[2:0]
  Communication setting used by client 0 in the DATA mode.
  - COM[2:0] = 000 250 kbit/s, 160 kHz peak deviation.
  - COM[2:0] = 001 1 Mbit/s, 160 kHz peak deviation.
  - COM[2:0] = 010 1 Mbit/s, 400 kHz peak deviation.
  - COM[2:0] = 011 2 Mbit/s, 320 kHz peak deviation.
  - COM[2:0] = 100 2 Mbit/s, 800 kHz peak deviation.
  - COM[2:0] = 101 reserved.
  - COM[2:0] = 110 reserved.
  - COM[2:0] = 111 reserved.

- client_0_1 b[4:1] = PA[3:0]
  Output power used by client 0 during transmission.
  - PA[3:0] = 0000 0 dBm.
  - PA[3:0] = 0001 -3 dBm.
  - PA[3:0] = 0010 -6 dBm.
  - PA[3:0] = 0011 -9 dBm.
  - PA[3:0] = 0100 -12 dBm.
  - PA[3:0] = 0101 -15 dBm.
  - PA[3:0] = 0110 -18 dBm.
  - PA[3:0] = 0111 -21 dBm.
  - PA[3:0] = 1xxx -24 dBm.
- client_0_1 b[0] = enabling of auto-acknowledge.
  After client 0 has sent a DATA packet, an ACK packet may be send by the master.
  - b[0] = 0 auto acknowledgement disabled in DATA mode.
  - b[0] = 0 auto acknowledgement disabled in DATA mode.
- client_0_0 b[7:6] = RT[1:0].
  In DATA mode, a client may retransmit the DATA packet in case the master did not acknowledge. The maximum number of retransmissions can be set,
  - RT[1:0] = 00 no retransmission.
  - RT[1:0] = 01 maximal 1 retransmission.
  - RT[1:0] = 10 maximal 2 retransmissions.
  - RT[1:0] = 11 maximal 3 retransmissions.
- client_0_0 b[5] = battery level
  This bit is transmitted in any ACK0/ACK1 packet. Together with the battery level threshold it gives information of the battery voltage of the device transmitting the ACK packet.
  - b[0] = 0 battery voltage above threshold.
  - b[0] = 1 battery voltage below threshold.
- client_0_0 b[4:3] = time code scaling[1:0]

  The time codes used in the client table (client_0_3 b[7:0]) can be scaled.
  - time code scaling[1:0] = 00 scale by 0.5
  - time code scaling[1:0] = 01 scaled by 1
  - time code scaling[1:0] = 10 scaled by 2
  - time code scaling[1:0] = 11 scaled by 4
- client_0_0 b[2] = stream_enable.
  This bit is defines whether data exchange between client and master is done in streaming mode.
  - b[2] = 0 streaming disabled.
  - b[2] = 1 streaming enabled.
- client_0_0 b[1:0] = stream_duty_cycle[1:0].
  In case streaming is enabled, the stream duty cycle is used during data exchange.
  - stream_duty_cycle[1:0] = 00 --12.5%.
  - stream_duty_cycle [1:0] = 01 --25%.
  - stream_duty_cycle [1:0] = 10 --50%.
  - stream_duty_cycle [1:0] = 11 --100%.

8.2.4.16 Address 0x80 - 0x8F: ACS TABLE

In case ACS is enabled, the ACS algorithm selects an entry of the ACS table. The MCU needs to fill in the RF frequencies actually used. For all the entries, the following is defined:

- b[7] = reserved.
- b[6:0] = RF channel.
  The RF frequency used is (2400 + RF channel) MHz. RF channel settings from 0 up to 4 are not supported.

8.2.4.17 Address 0x90: PAIRWAKE_TABLE_6

Sets the RF frequency used by the AS3940. The RF frequency is (2400 + ICF) MHz. ICF settings from 0 up to 4 are not supported.

- pairwake_table_6[7] = Reserved.
- pairwake_table_6[6:0] = ICF[6:0].

8.2.4.18 Address 0x91: PAIRWAKE_TABLE_5

- pairwake_table_5[7:3] = Reserved.
- pairwake_table_5[2:0] = COM[2:0].

Sets the communication mode used by the AS3940.

- COM[2:0] = 000 250 kbit/s, 160 kHz peak deviation.
- COM[2:0] = 001 1 Mbit/s, 160 kHz peak deviation.
- COM[2:0] = 010 1 Mbit/s, 400 kHz peak deviation.
- COM[2:0] = 011 2 Mbit/s, 320 kHz peak deviation.
- COM[2:0] = 100 2 Mbit/s, 800 kHz peak deviation.
- COM[2:0] = 101 reserved.
- COM[2:0] = 110 reserved.
- COM[2:0] = 111 reserved.

8.2.4.19 Address 0x92: PAIRWAKE_TABLE_4

Set the transmission power used by the AS3940.

- pairwake_table_4[7:6] = Reserved.
- pairwake_table_4[5:4] = time_code_scaling[1:0].
- pairwake_table_4[3:0] = PA[3:0].

The time codes used in paring and wakeup (pairwake_table_3) can be scaled.

time_code_scaling[1:0] = 00 scale by 0.5

time_code_scaling[1:0] = 01 scaled by 1

time_code_scaling[1:0] = 10 scaled by 2

time_code_scaling[1:0] = 11 scaled by 4

Output power used during pairing and wakeup.

- PA[3:0] = 0000 TX Power set to 0 dBm.
- PA[3:0] = 0001 TX Power set to -3 dBm.
- PA[3:0] = 0010 TX Power set to -6 dBm.
- PA[3:0] = 0011 TX Power set to -9 dBm.
- PA[3:0] = 0100 TX Power set to -12 dBm.
- PA[3:0] = 0101 TX Power set to -15 dBm.
- PA[3:0] = 0110 TX Power set to -18 dBm.
- PA[3:0] = 0111 TX Power set to -21 dBm.
- PA[3:0] = 1xxx TX Power set to -24 dBm.

8.2.4.20 Address 0x93: PAIRWAKE_TABLE_3

- pairwake_table_3[7:0] = timecode[7:0].

Time code used by the AS3940 during paring and wake up. The periodicity equals time_code_scaling*(895 + timecode)/2048 s. Random time code is not supported during wake up and pairing.

8.2.4.21 Address 0x94 - 0x95: PAIRWAKE_TABLE_2/1

- pairwake_table_2[7] = Reserved.
- pairwake_table_2[6:0] = tnowup[14:8].
- pairwake_table_1[7:0] = tnowup[7:0].

During a wake-up by master procedure, the total number of wake-up packages transmitted by the master can be set.

8.2.4.22 Address 0x96: PAIRWAKE_TABLE_0

During pairing and some of the supported wake-up procedures, the master carries out a number of trials to communicate with a client. The maximum number trials the master uses can be set via this register.

- pairwake_table_0[7:0] = trial_max[7:0]

8.2.4.23 Address 0x97 - 0x9A: GEN_PUR_LM_SETTING3/2/1/0

A number of general purpose settings are defined for the Link Manager. They are controlled via registers 0x97 and 0x9A

- gen_pur_lm_settings_3[7:6] = T_polmax[1:0].
  - T_polmax[1:0] = 00 0.25 s.
  - T_polmax[1:0] = 01 0.5 s.
  - T_polmax[1:0] = 10 1.0 s.
  - T_polmax[1:0] = 11 2.0 s.
- gen_pur_lm_settings_3[5]= CRC reversing.
- gen_pur_lm_settings_3[4:3] = RX duty cycle on time [1:0].
  - RX on time[1:0] = 00 RX on time = 793 µs.
  - RX on time[1:0] = 01 RX on time = 1007 µs.
  - RX on time[1:0] = 10 RX on time = 1587 µs.
  - RX on time[1:0] = 11 RX on time = 2014 µs.

  Used in pairing and standard wake-up.
- gen_pur_lm_settings_3[2:1] = duty cycle[1:0].
  - duty cycle[1:0] = 00 duty cycle = 10.2% in case RX on time [0] = 0.
    duty cycle = 12.9% in case RX on time [0] = 1.
  - duty cycle[1:0] = 01 duty cycle = 20.3% in case RX on time [0] = 0.
    duty cycle = 25.8% in case RX on time [0] = 1.
  - duty cycle[1:0] = 10 duty cycle = 40.6% in case RX on time [0] = 0.
    duty cycle = 51.6% in case RX on time [0] = 1.
  - duty cycle[1:0] = 11 duty cycle = 100%.
- gen_pur_lm_settings_3[0] = 0 device defined as client.
  gen_pur_lm_settings_3[0] = 1 device defined as master.
- gen_pur_lm_settings_2[7] = xtal_start.
  - xtal_start = 0 → 16 MHz XTAL startup time < 1 ms.
  - xtal_start = 1 → 16 MHz XTAL startup time < 2 ms.
- gen_pur_lm_settings_2[6] = Reserved
- gen_pur_lm_settings_2[5:0] = sync_lost_max[5:0].
  Set the number of consecutive failing data exchanges between client and master before synchronization is considered lost.
- gen_pur_lm_settings_1[7:6] = temp_pair_sen[1:0].
  Indicates to which packet-types the AS3940 is sensitive during temporary pairing.
  - temp_pair_sen[1:0] = 00
    master only sensitive to LIB
    client only sensitive to TEMP_LMB
  - temp_pair_sen[1:0] = 01
    master only sensitive to 2PAIR0 and LIB
    client only sensitive to TEMP_LMB, LMB and 2PAIR1
  - temp_pair_sen[1:0] = 1*
    master only sensitive to 2PAIR0
    client only sensitive to LMB and 2PAIR1
- gen_pur_lm_settings_1[5] = battery voltage status.
  - 0 battery voltage above threshold.
  - 1 battery voltage below threshold.

During transmission of ACK/3ACK or DATA/DP0 packets, the battery measurement procedure is enabled. The result of the measurement is reported. The threshold level used is set in gen_pur_lm_settings_1, b[4:0].

- gen_pur_lm_settings_1[4:0] = blth[4:0]
  Interpreted as unsigned integer. Threshold = 1.95 V + blth * 50 mV
- gen_pur_lm_settings_0[7:6] = rssi_check_en.
  Indicates whether RSSI level is used during pairing and temporary pairing.
- gen_pur_lm_settings_0[6] = crc_interpret_en.
  Indicates whether an interrupt is given in case the CRC of a received data packet has failed.
- gen_pur_lm_settings_0[5] = smart_cal_en.
  Enables smart VCO calibration.
- gen_pur_lm_settings_0[4] = EOC_request.
  Bit setting used in ACK1 package. A master is able to send a request to a client to end the communication.
- gen_pur_lm_settings_0[3] = unpair_request. A master is able to send a request to unpair a client.
  Bit setting used in ACK1 package
- gen_pur_lm_settings_0[2:0] = client_index[2:0].
  Indicated to which client the LIB package is sent and indicates to for which client the ACK1 EOC/unpair request bit is set.

8.2.4.24 Address 0xA6 - 0xAD: DEVICE_DATA

- address 0xa6 b[7:0] = rssi_align [9:2]
  - rssi_align[1:0] = 2'b01 (hardcoded)
- address 0xA7 b[7:0] = crc_initial [15:8]
- address 0xA8 b[7:0] = crc_initial [7:0]
- address 0xA9 b[7:0] = device_type [15:8]
- address 0xAA b[7:0] = device_type [7:0]
- address 0xAB b[7:0] = serial_number [23:16]
- address 0xAC b[7:0] = serial_number [15:8]
- address 0xAD b[7:0] = serial_number[7:0]

8.2.4.25 Address 0xB0 - 0xB1: CORRELATION_THR

Via this register, the correlation threshold can be set. This is used to avoid false triggering on noise. The threshold is interpreted as a two's complement number, however only positive numbers (0x000...0x7FF) should be used.

- address 0xB0
  - b[7:4] = Reserved
  - b[3:0] = correlation_thr [11:8]
- address 0xB1
  - b[7:0] = correlation_thr [7:0]

8.2.4.26 Address 0xB2 - 0xB3: LOG_RSSI_THR

Via this register, the RSSI threshold can be set. If during LBT the aligned RSSI level is above this threshold, is channel is defined as busy. If during pairing the aligned RSSI level is below the threshold, pairing is not accepted.

- address 0xB2
  - b[7:2] = not used.
  - b[1:0] = log_rssi_thr[9:8]
- address 0xB3
  - b[7:0] = log_rssi_thr [7:0]

8.2.4.27 Address 0xB4 - 0xB5: LOG_RSSI_ACT_VALUE (Read only)

To align the RSSI value, a measurement must be carried out by applying an RF signal with a known level to the AS3940. By putting the AS3940 in transparent RX mode (via ENG_BITS 0xE4 b[7]), the content of those registers gives the average measured level. This level can be used as alignment value.

- address 0xB4
  - b[7:2] = not used.
  - b[1:0] = log_rssi_act_value[9:8]
- address 0xB4
  - b[7:0] = log_rssi_act_value[7:0]

8.2.4.28 Address 0xE1 - 0xE4: ENG_BITS

Via this register, the analog performance of the transceiver is optimized.

- Address 0xE1

The recommended value of this register is 0x69 (default value 0x80). The front-end gain is set at maximum (0x110) to get the highest sensitivity figures. The Synthesizer setting (0x1001) is used to get the optimum operation.

- b[7] = Reserved
- b[6:4] = Front-end gain tuning
- b[3:0] = Synthesizer tuning

- Address 0xE2

The recommended value of this register is 0x24 (default value 0x20). The PA mode is set at minimum (0b00) to get 0dBm output power in TX mode using the reference application board. Higher values (0b01 and 0b10) give more output power, but also more harmonics/spurs. Power could be increased in a more linear way by lowering the external bias resistor Rext (Only R1 = 560 recommended). The IF filter gain is set at maximum (0b1) to get the highest receiver gain and best sensitivity figures.

- b[7:6] = PA mode tuning
- b[5] = PA reference tuning
- b[4:3] = Reserved
- b[2] = IF filter gain tuning
- b[1:0] = Reserved

- Address 0xE3

The recommended value of this register is 0x58 (default value 0x19). The DEVICE_DATA (0xA6-0xAD) registers are enabled (0b1). PA amplitude loop has to be set at 3 (0b011) to get 0dBm output power in TX mode using the reference application board. Higher values give a little more power, but also more harmonics/spurs. Power could be increased in a more linear way by lowering the external bias resistor Rext (Only R1 = 560 recommended).

- b[7] = Reserved
- b[6] = Enabling of the DEVICE_DATA (0xA6-0xAD) Registers
- b[5:3] = PA amplitude loop tuning
- b[2:0] = Reserved

- Address 0xE4

The default value of this register is 0x51. The RSSI readout adjustment can be enabled by setting the RSSI alignment mode bit high (0b1). The TX DAC (0b1), bandgap (0b100), and ADC bias (0b01) tuning bits are set for optimum operation.

- b[7] = RSSI alignment mode
- b[6] = TX DAC tuning
- b[5] = Reserved
- b[4:2] = Bandgap tuning
- b[1:0] = ADC bias tuning

8.2.4.29 Address 0xFD-FE: CHIP_ID (Read only)

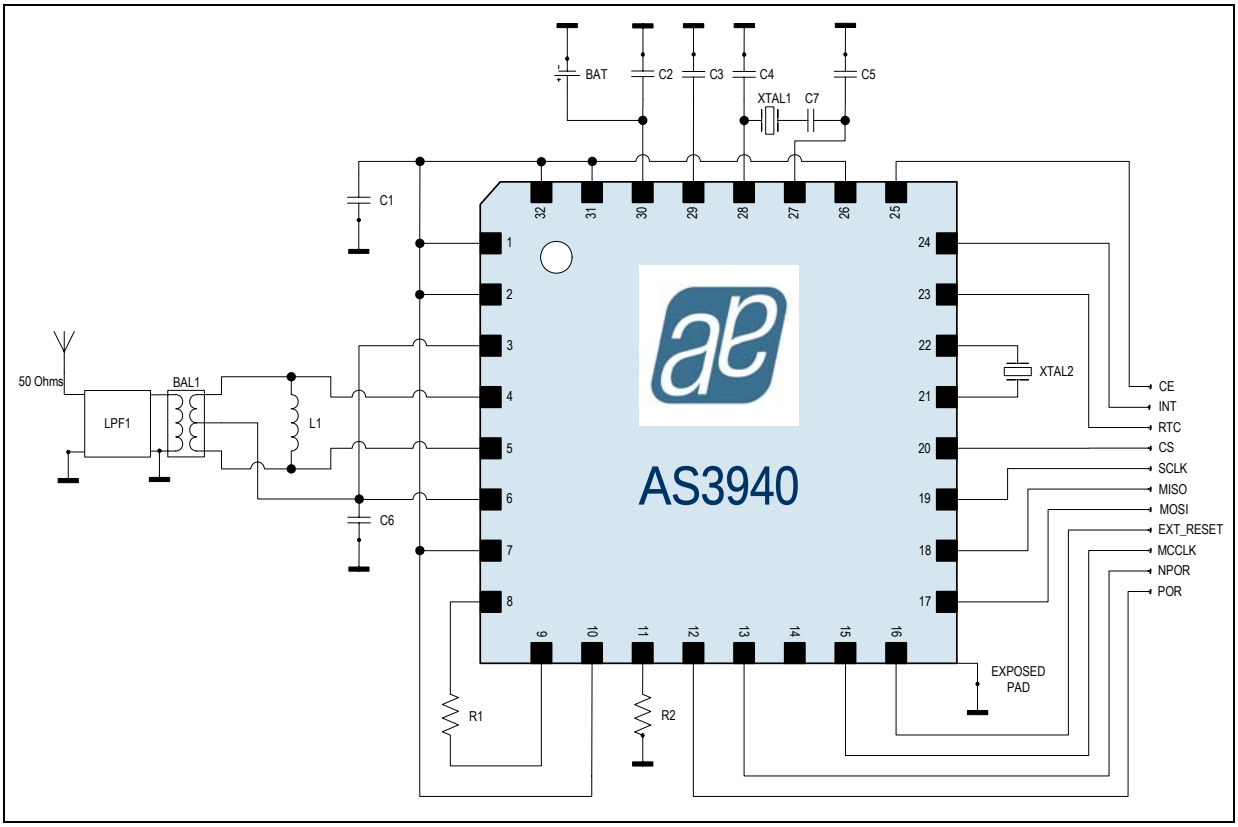
This register group reads back with content 0x456D, which is the hex format of 17773. This last number is the unique identification number for the AS3940 at austriamicrosystems.

8.2.4.30 Address 0xFF: REV_ID (Read only)

This register is used to read back the hardware revision of the chip. ES2 is identified as 0x10.

9 Application Information

Figure 18. AS3940 Application diagram



AS3940 requires the following external components.

Table 22. External Components

Num	Component	Value	Description	Note
1	C1	1 µF	Analog Voltage regulator de-coupling capacitor	Ceramic capacitor
2	C2	100pF	Supply de-coupling	5%
3	XTAL1	16 MHz	example of Crystal parameters: RS=40Ω, C0=1.2pF, C1=2.36fF	16 MHz fundamental mode crystal, 18pF load capacitance, ±20ppm initial tolerance, ±20ppm variation over the temperature range, preferably with a low pullability (low C1)
4	C4	33 pF	Crystal load capacitor	5%
5	C5	27 pF	Crystal load capacitor	5%
6	C3	100 pF	Digital Voltage regulator de-coupling capacitor	5%
7	C6	100 pF	Decoupling CM pin	0402, 5%
8	C7	22pF	Crystal capacitor	5%
9	L1	2.4 nH	RF matching network inductor	±0.2nH LQW15AN 2N4COOB Murata 0402
10	LP1		Murata: LFL152G45TC1A219	LP filter
11	BAL1		Murata: LDB212G4020C-001	Balun

Table 22. External Components

Num	Component	Value	Description	Note
12	R1	560	Accurate external resistor to define the PA gain	1%
13	XTAL2	32768 Hz	Standard Watch Crystal for 12.5 pF load capacitance	Optional in application

10 Package Drawings and Markings

The product is available in a QFN 32 pin (5mm x 5mm) package

Figure 19. Package Drawings

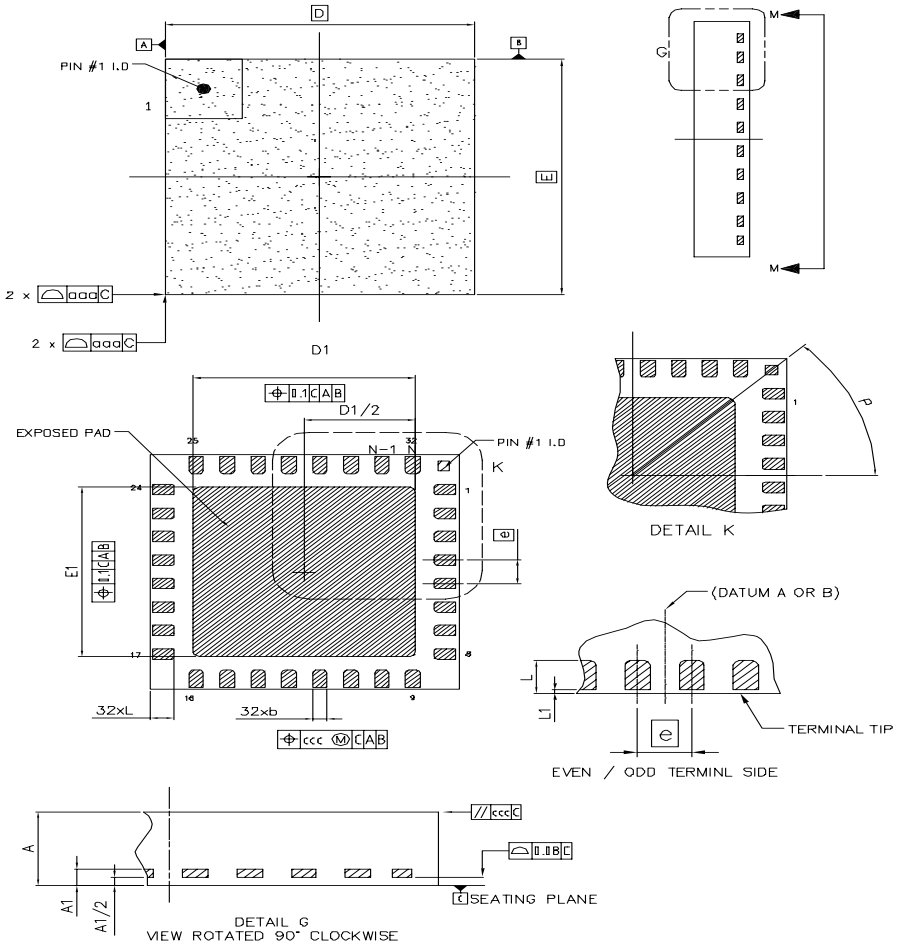


Table 23. Dimensions

Symbol	Min	Typ	Max	Symbol	Min	Typ	Max
A	0.80		1.00	e	0.50 BSC		
A1	0.203 REF			L	0.30	0.40	0.50
b	0.18	0.23	0.30	L1			0.10
D	5.00 BSC			P	45° BSC		
E	5.00 BSC			aaa	0.15		
D1	3.50	3.60	3.70	ccc	0.10		
E1	3.50	3.60	3.70				

Note: All dimensions are in Millimeters and angles in Degrees

Dimensioning and Tolerances confirm to ASME Y14.5M-1994

Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge to 0.1mm is acceptable.

11 Ordering Information

The devices are available as the standard products shown in Table 24.

Table 24. Ordering Information

Model	Description	Delivery Form[1]	Package
AS3940-BQFT	Tape & Reel 1000 pcs (AS3940 QFN)	Tape & Reel	QFN 32 pin (5mm x 5mm)

1. Dry Pack sensitivity Level =3 according to IPC/JEDEC J-STD-033A for full reels.

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

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