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Application Manual

Real Time Clock Module

RX8900SA CE

Product name	Product number
RX8900SA UA (+/-3.4 x 10^{-6} / -40°C to +85°C)	X1B000292000100
RX8900SA UB (+/-5.0 x 10^{-6} / -40°C to +85°C)	X1B000292000200
RX8900SA UC (+/-5.0 x 10^{-6} / -30°C to +70°C)	X1B000292000300
RX8900CE UA (+/-3.4 x 10^{-6} / -40°C to +85°C)	X1B000301000100
RX8900CE UB (+/-5.0 x 10^{-6} / -40°C to +85°C)	X1B000301000200
RX8900CE UC (+/-5.0 x 10^{-6} / -30°C to +70°C)	X1B000301000300

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ETM45E Revision History

Rev No.	Date	Page	Description
ETM45E-01	26.Jan.2015		Release
ETM45E-04	20.Sep.2016	5	I2C-bus active current
		39	Recommended soldering pattern Optimization of the text
ETM45E-05	14.Oct.2016	24	Add circuit diagram Ex.4 Optimization of the text
		25	8.8.3 Optimization of the text
		26	Optimization of the text
ETM45E -06	12.Jun.2018	13 15 21	8.2.7. Control register Default value was corrected. 5) RESET bit RESET function explanation was updated. 8.5.2. Related registers Address of table was corrected.
ETM45E -07	12.Feb.2019	32 -11 21 25 27 31 ~ 36 47 48	Reference characteristics of Pch-SW and Diode Block diagram of FOUT, Block diagram of Timer interruption Block diagram of Time Update interruption Block diagram of Alarm interruption All renewal of 8.8. Battery backup switchover function Updated Figure of 8.13 Connection example. Note for SA-Package.
ETM45E -08	10.Apr.2019	6 33.34 36	Updated access time 1 sec (Max.) from 0.95sec. Updated VDD drop detection. Inserted 8.8.8 Note: Diode characteristics.

Contents

I²C-Bus Interface Real-time Clock Module

RX8900 SA / CE

- Features built-in 32.768 kHz DTCXO, High Stability.
- Supports I²C-Bus's high-speed mode (Up to 400 kHz)
- Alarm interrupt function for day, date, hour, and minute settings
- Wakeup timer interruption
- Time update interrupt function (Seconds, minutes)
- Temperature compensated 32.768 kHz output with OE function (FOE and FOUT pins)
- Auto correction of leap years (from 2000 to 2099)
- Wide interface voltage range: 2.5 V to 5.5 V
- Wide time-keeping voltage range:1.6 V to 5.5 V
- Low current consumption: 0.70μA / 3 V (Typ.)
- Built-in Backup switchover circuit (trickle charge)

1. Overview

This module is an I²C bus interface-compliant real-time clock which includes a 32.768 kHz DTCXO.
In addition to providing a calendar (year, month, date, day, hour, minute, second) function and a clock counter function, this module provides an abundance of other functions including an alarm function, Wakeup timer function, time update interrupt function, and 32.768 kHz output function. By the battery backup switchover function and the interface power supply input pin, RX8900 can support various power supply circuitries.
The devices in this module are fabricated via a C-MOS process for low current consumption, which enables long-term battery back-up.

2. Block Diagram

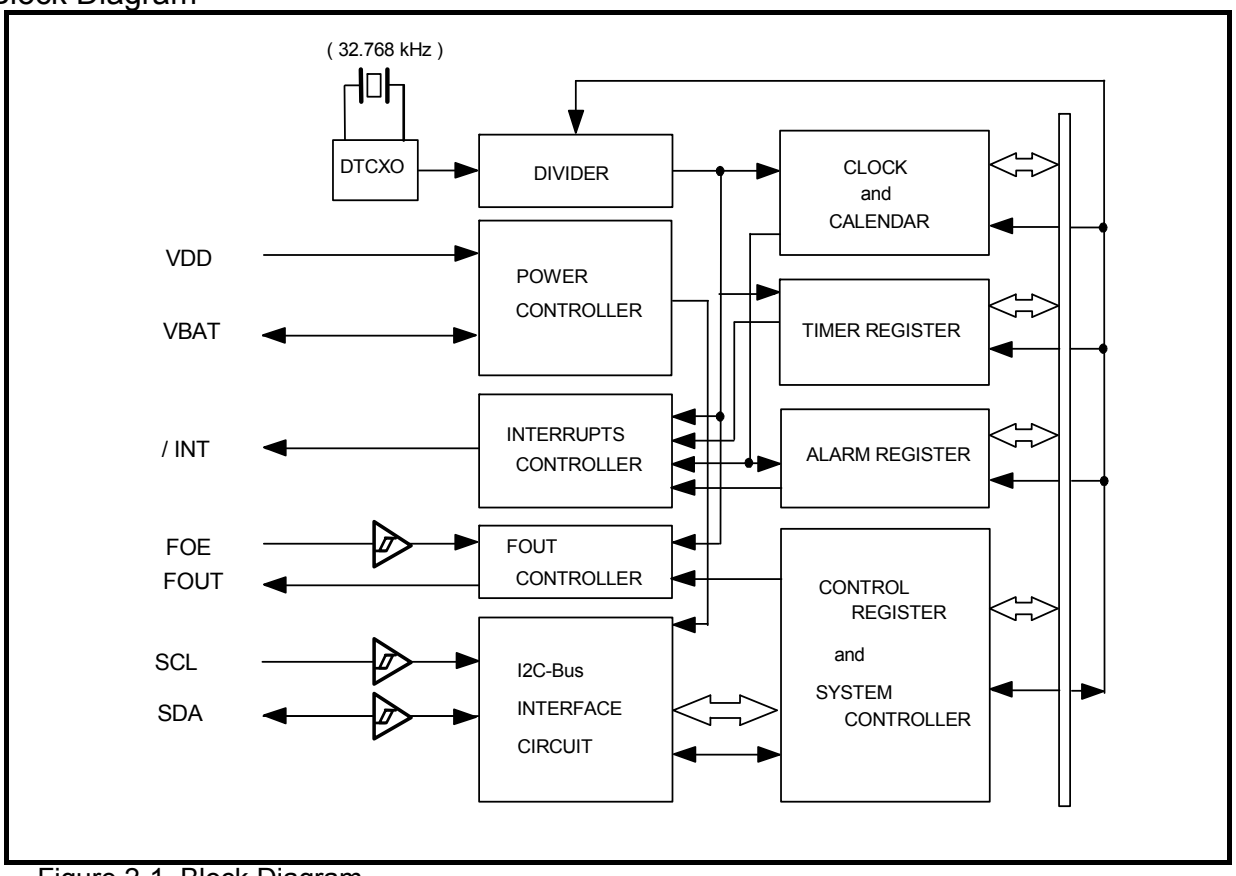


Figure 2-1. Block Diagram

3. Terminal description

3.1. Terminal connections

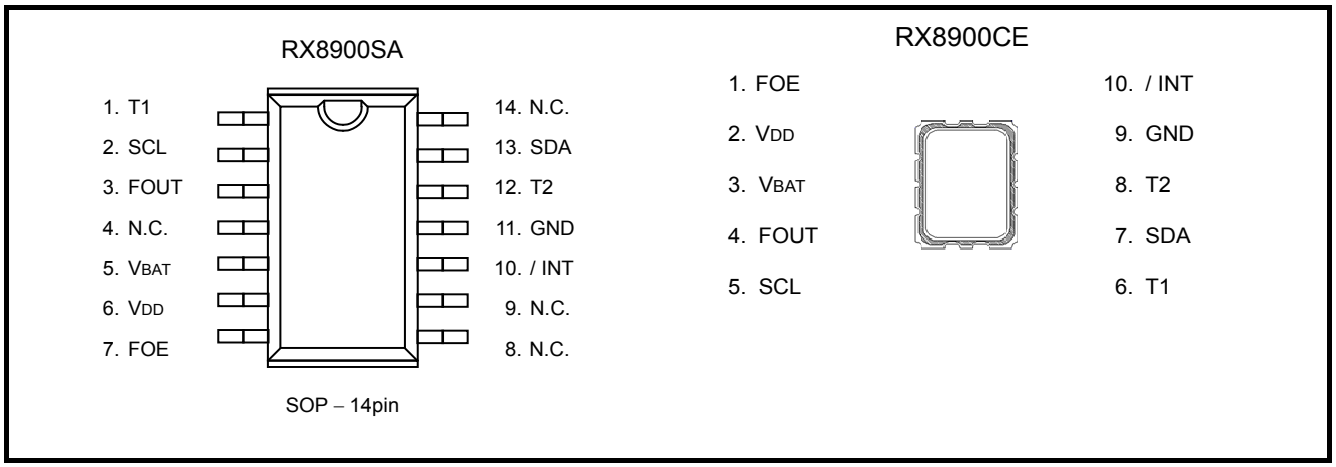


Figure 3-1. Package

3.2. Pin Functions

Table 3-1. Pin Description

Signal name	I/O	Function
SDA	I/O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I^2C communications. Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull-up resistance relative to the signal line capacity.
SCL	Input	This is the serial clock input pin for I^2C Bus communications.
FOUT	Output	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. (depend on FSEL bit) When output is stopped, the FOUT pin = "Hi-Z" (high impedance).
FOE	Input	This is an input pin used to control the output mode of the FOUT pin. When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped.
/ INT	Output	This pin is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin.
VBAT	–	This is the power supply pin for backup battery. Connect this pin to a large-capacity capacitor, a secondary battery or similar. When the battery switchover function is not needed, VBAT must be connected to VDD.
VDD	–	This pin is connected to a positive power supply.
GND	–	This pin is connected to a ground.
TEST	Input	Used by the manufacturer for testing. (Do not connect externally.)
T1	Input	Used by the manufacturer for testing. (Do not connect externally.)
T2	–	Used by the manufacturer for testing. (Do not connect externally.)
N.C.	–	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND or VDD.

Note: Be sure to connect a bypass capacitor rated at least 0.1 µF between VDD and GND, VBAT and GND.

4. Absolute Maximum ratings

Table 4-1. Absolute Maximum Rating GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage (1)	V_{DD}	Between V_{DD} and GND	−0.3 to +6.5	V
Supply voltage (2)	V_{BAT}	Between V_{BAT} and GND	−0.3 to +6.5	V
Input voltage (2)	V_{IN}	FOE,SCL, SDA pins	GND−0.3 to +6.5	V
Output voltage (1)	V_{OUT1}	FOUT pin	GND−0.3 to V_{DD}+0.3	V
Output voltage (2)	V_{OUT2}	SDA and /INT pins	GND−0.3 to +6.5	V
Storage temperature	T_{STG}	When stored separately, without packaging	−55 to +125	°C

5. Recommended Operating Conditions

Table 5-1. Recommended Operating Conditions GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage Normal mode (2)	V_{ACCSW}	Between V_{DD} and GND	2.5	3.0	5.5	V
Operating supply voltage In case of single supply (VDD = VBAT) (1)	V_{ACC}	Between V_{DD} and GND (V_{DD} = V_{BAT})	1.6	3.0	5.5	V
Backup power supply voltage	V_{BAT}	Between V_{BAT} and GND	1.6	3.0	5.5	V
Temp. compensation voltage	V_{TEM}	Temperature compensation voltage	2.0	3.0	5.5	V
Clock supply voltage	V_{CLK}	–	1.6	3.0	5.5	V
Operating temperature	T_{OPR}	No condensation	−40	+25	+85	°C

*To apply Min. value of VACC and VCLK, the VDD and VBAT needs to be supplied with more than 2.5V at least for the oscillation to stabilize (oscillation start time tSTA).
* VACCSW is the normal mode operation voltage, at which the Battery backup switchover function is enabled.
*The Min. value of VCLK is the Min. voltage required to retain the time counting function; it is however necessary to maintain VTEM till the oscillation of the oscillator has stabilized (oscillation start time tSTA).
* The temperature compensation stops working below Min. value of VTEM.

5.1. I2C-bus active current

Reference characteristic data (Typical)

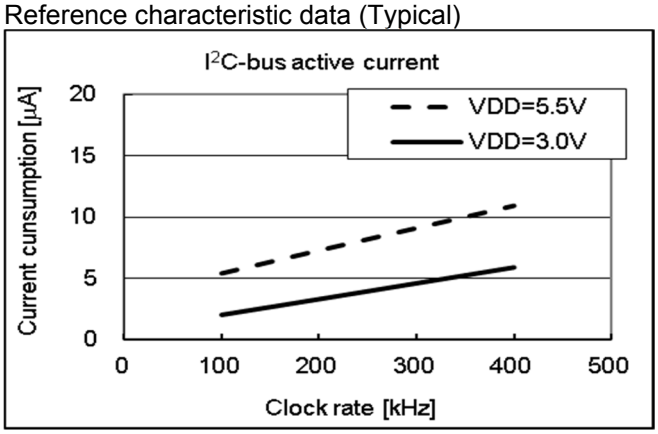


Figure 7-3. I2C bus current consumption

6. Frequency Characteristics

Table 6-1. Frequency Characteristics GND = 0 V

Item	Symbol	Condition		Rating	Unit
Frequency stability	Δ f / f	U A	Ta= 0 to +50 °C, V_{DD}=3.0 V Ta=–40 to +85 °C, V_{DD}=3.0 V	± 1.9 (*1) ± 3.4 (*2)	× 10^{-6}
		U B	Ta= 0 to +50 °C, V_{DD}=3.0 V Ta=–40 to +85 °C, V_{DD}=3.0 V	± 3.8 (*3) ± 5.0 (*4)	
		U C	Ta= 0 to +50 °C, V_{DD}=3.0 V Ta=–30 to +70 °C, V_{DD}=3.0 V	± 3.8 (*3) ± 5.0 (*4)	
Frequency/voltage characteristics	f / V	Ta= +25 °C, V_{DD}=2.0 V to 5.5 V		± 1.0 Max.	× 10^{-6} / V
Oscillation start time	t_{STA}	Ta= +25 °C, V_{DD}=1.6 V ~ 5.5 V Ta=–40 to +85 °C, V_{DD}=1.6 V to 5.5 V		1.0 Max. 3.0 Max.	s
Aging	fa	Ta= +25 °C, V_{DD}=3.0 V, first year		± 3 Max.	× 10^{-6} / year
Temperature Sensor Accuracy	Temp	VDD=3.0 V		± 5.0 Max.	°C

*1) Equivalent to ±5 seconds of month deviation. *2) Equivalent to ±9 seconds of month deviation.
*3) Equivalent to ±10 seconds of month deviation. *4) Equivalent to ±13 seconds of month deviation.

7. Electrical Characteristics

7.1 DC characteristics

Table 7-1 DC characteristics *Unless otherwise specified, GND = 0 V, V_{DD} =V_{BAT} = 2.5 V to 5.5 V, Ta = –40 °C to +85 °C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Average Current consumption(1)	I_{DD1}	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND, V_{DD} = V_{BAT} FOUT : output OFF (High Z) Compensation interval 2.0 s VDET3 voltage detection time 2ms	V_{DD} = 5 V		0.72	1.50	µA
Average Current consumption(2)	I_{DD2}		V_{DD} = 3 V		0.70	1.40	
Current consumption(3)	I_{DD3}	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = V_{DD}, V_{DD} = V_{BAT} FOUT :32.768 kHz, CL =0pF Compensation interval 2.0 s VDET3 voltage detection time 2ms	V_{DD} = 5 V		1.60	2.50	µA
Current consumption(4)	I_{DD4}		V_{DD} = 3 V		1.15	2.40	
Current consumption (5)	I_{DD5}	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = V_{DD}, V_{DD} = V_{BAT} FOUT :32.768 kHz, CL =30pF Compensation interval 2.0 s VDET3 voltage detection time 2ms	V_{DD} = 5 V		6.70	8.00	µA
Current consumption (6)	I_{DD6}		V_{DD} = 3 V		4.30	5.50	
Current consumption (7)	I_{DD7}	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND, V_{DD} = V_{BAT} FOUT : output OFF (High Z) Compensation OFF VDET3 voltage detection time 2ms	V_{DD} = 5 V		0.70	1.45	µA
Current consumption (8)	I_{DD8}		V_{DD} = 3 V		0.68	1.35	
Peak Current consumption(9)	I_{DD9}	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND, V_{DD} = V_{BAT} FOUT : output OFF (High Z) Compensation ON (peak)	V_{DD} = 5 V		55	100	µA
Peak Current consumption (10)	I_{DD10}		V_{DD} = 3 V		50	95	
High-level input voltage	V_{IH}	SCL, SDA, FOE pins		0.8 × V_{DD}		5.5	V
Low-level input voltage	V_{IL}	SCL, SDA, FOE pins		GND – 0.3		0.2 × V_{DD}	V
High-level output voltage	V_{OH1}	FOUT pin	V_{DD}=5 V, I_{OH}=–1 mA	4.5		5.0	V
	V_{OH2}		V_{DD}=3 V, I_{OH}=–1 mA	2.2		3.0	
	V_{OH3}		V_{DD}=3 V, I_{OH}=–100 µA	2.9		3.0	
Low-level output voltage	V_{OL1}	FOUT pin	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.5	V
	V_{OL2}		V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.8	
	V_{OL3}		V_{DD}=3 V, I_{OL}=100 µA	GND		GND+0.1	
	V_{OL4}	/ INT pin	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.25	V
	V_{OL5}		V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.4	
	V_{OL6}	SDA pin	V_{DD} ≥2 V, I_{OL}=3 mA	GND		GND+0.4	V
Input leakage current	I_{LK}	FOE, SCL, SDA pins, V_{IN} = V_{DD} or GND		–0.5		0.5	µA
Output leakage current	I_{OZ}	/ INT, SDA, FOUT pins, V_{OUT} = V_{DD} or GND		–0.5		0.5	µA

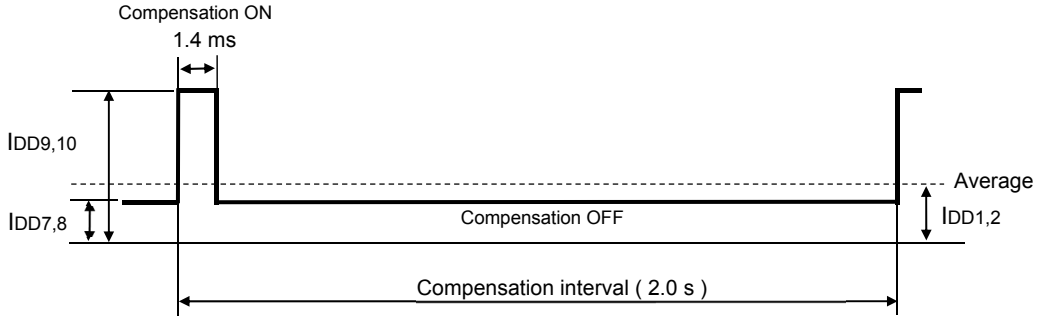


Figure 7-1. Temperature compensation current consumption

7.2. AC Characteristics

Table 7-2. AC Characteristics

* Unless otherwise specified,
GND = 0 V , V_{DD} = 2.5 V to 5.5 V , Ta = −40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}				400	kHz
Start condition setup time	$t_{SU;STA}$		0.6			µs
Start condition hold time	$t_{HD;STA}$		0.6			µs
Data setup time	$t_{SU;DAT}$		100			ns
Data hold time	$t_{HD;DAT}$		0			ns
Stop condition setup time	$t_{SU;STO}$		0.6			µs
Bus idle time between start condition and stop condition	t_{BUF}		1.3			µs
Time when SCL = "L"	t_{LOW}		1.3			µs
Time when SCL = "H"	t_{HIGH}		0.6			µs
Rise time for SCL and SDA	t_r				0.3	µs
Fall time for SCL and SDA	t_f				0.3	µs
Allowable spike time on bus	t_{SP}				50	ns
FOUT duty	t_W /t	50% of V_{DD} level	40	50	60	%

Note: These timing specifications are applied in access by 400kHz.

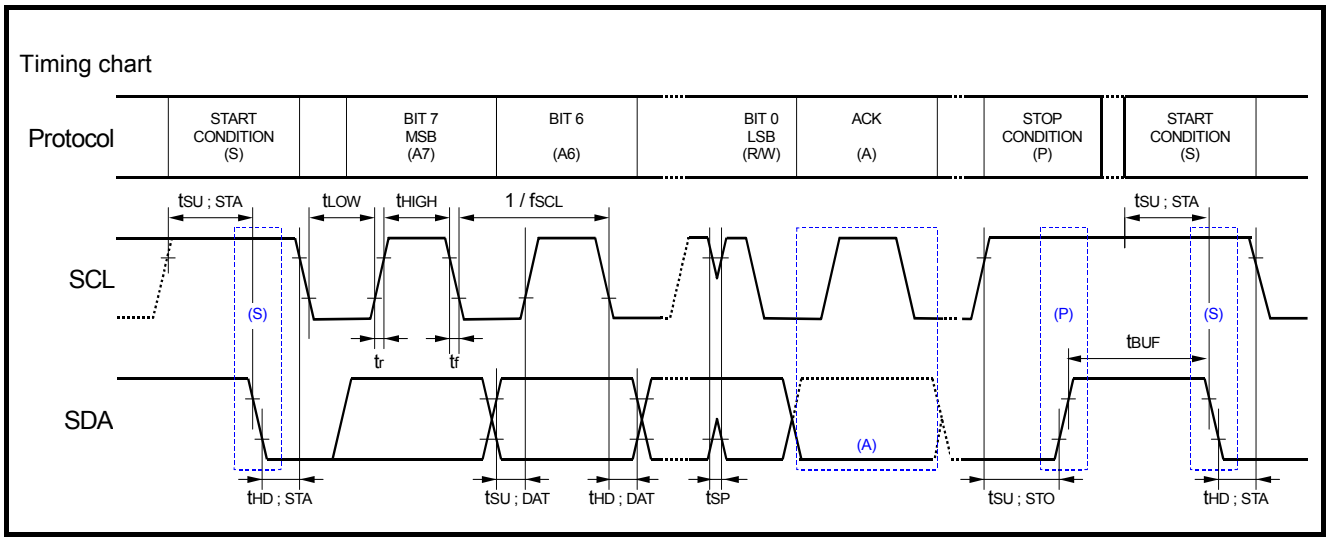


Figure 7-2 I2C Bus Timing Chart

Warning: When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access **should be completed within 1 seconds**.
If such communication requires 1 **seconds** or longer, the I^2C bus interface is reset by the internal bus timeout function.
When bus-time-out occur, SDA turns to Hi-Z input mode.

Note: During access to the time registers, the time counting is on hold! This means that up to 1 second can be “lost” in case of unsuccessful communication as mentioned above!
Please make sure to send I2C start condition before actual transmission of the RTCs slave address as otherwise the slave address appears to be shifted by 1 bit!

8. Use Methods

8.1. Description of Registers

8.1.1. Write / Read and Bank Select

Address 00h to 0Fh : Basic time and calendar register … Compatible with RX-8803.
Time and date registers have two addresses from 00h to 06h and 10h to 16h (either can be used with equal results).
Addresses 17h to 18h are Temperature Data, Backup power supply control register

8.1.2. Register table (Basic time and calendar registers)

Table 8-1. Basic Time and Calendar Registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
00 or 10	SEC	○	40	20	10	8	4	2	1	P	P
01 or 11	MIN	○	40	20	10	8	4	2	1	P	P
02 or 12	HOUR	○	○	20	10	8	4	2	1	P	P
03 or 13	WEEK	○	6	5	4	3	2	1	0	P	P
04 or 14	DAY	○	○	20	10	8	4	2	1	P	P
05 or 15	MONTH	○	○	○	10	8	4	2	1	P	P
06 or 16	YEAR	80	40	20	10	8	4	2	1	P	P
07	RAM	•	•	•	•	•	•	•	•	P	P
08	MIN Alarm	AE	40	20	10	8	4	2	1	P	P
09	HOUR Alarm	AE	•	20	10	8	4	2	1	P	P
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	P	P
	DAY Alarm		•	20	10	8	4	2	1		
0B or 1B	Timer Counter 0	128	64	32	16	8	4	2	1	P	P
0C or 1C	Timer Counter 1	•	•	•	•	2048	1024	512	256	P	P
0D or 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	P	P
0E or 1E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	P	P
0F or 1F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	P	P

P : Possible , I : Invalid

Note After the initial power-up (from 0 V) or in case the VLF bit returns "1" , make sure to initialize all registers, before using the RTC.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

- During the initial power-up, the following are the default settings for the register values
  Initial value_0 : TEST,WADA,USEL,TE,FSEL1,FSEL0,TSEL0,UF,TF,AF,CSEL1,UIE,TIE,AIE,RESET
  VDETOFF,SWOFF,BKSMP1,BKSMP0
  Initial value_1 : TSEL1,VLF,VDET,CSEL0
  ∗ At this point, all other register values are undefined, so be sure to perform a reset before using the module.

- Only a "0" can be written to the UF, TF, AF, VLF, or VDET bit.

- Any bit marked with "○" should be used with a value of "0" after initialization.

- Any bit marked with "●" is a RAM bit that can be used to read or write any data.

- The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.

- If an alarm function is not used, registers 08h-0Ah can be used as RAM. (AIE : "0")

- Reading register value of address 0Bh-0Ch is pre-set data.
  If a timer function is not used, register of 0Bh-0Ch can be used as RAM. (TE,TIE : "0")

8.1.3. Register table (Temperature Data, Backup power supply control register)

Table 8-2. Register table (Temperature Data, Backup power supply control register)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
17	TEMP	128	64	32	16	8	4	2	1	P	I
18	Backup Function	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0	P	P
19	Not use	○	○	○	○	○	○	○	○	P	I
1A	Not use	○	○	○	○	○	○	○	○	P	I

P : Possible , I : Invalid

8.1.4. Quick Reference

Table 8-3 Register Quick Reference

Update interrupt timing		Default
USEL = 0	Once per seconds.	√
USEL = 1	Once per minutes.	
Output Frequency selection		
FSEL1, FSEL0 = 00	32.768Khz	√
FSEL1, FSEL0 = 01	1024Hz	
FSEL1, FSEL0 = 10	1Hz	
FSEL1, FSEL0 = 11	32.768kHz	
Timer source clock selection.		
TSEL1, TSEL0 = 00	64Hz	
TSEL1, TSEL0 = 01	every Seconds update	
TSEL1, TSEL0 = 10	every Minutes update.	√
TSEL1, TSEL0 = 11	4096Hz	
Temperature compensation selection		
CSEL1, CSEL0 = 00	0.5 sec	
CSEL1, CSEL0 = 01	2.0 sec	√
CSEL1, CSEL0 = 10	10 sec	
CSEL1, CSEL0 = 11	30 sec	

8.2. Details of Registers

8.2.1. Clock counter (SEC - HOUR)

Table 8-4. Clock Counter Registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00, 10	SEC	○	40	20	10	8	4	2	1
01, 11	MIN	○	40	20	10	8	4	2	1
02, 12	HOUR	○	○	20	10	8	4	2	1

∗) "o" indicates write-protected bits. A zero is always read from these bits.

- The clock counter counts seconds, minutes, and hours.
- The data format is BCD format. For example, when the "seconds" register value is "0101 1001" it indicates 59 seconds.

∗ Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

1) Second counter

Table 8-5 Second Counter Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00, 10	SEC	○	40	20	10	8	4	2	1

- This second counter counts from "00" to "01," "02," and up to 59 seconds, after which it starts again from 00 seconds.

2) Minute counter

Table 8-6. Minute Counter Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01, 11	MIN	○	40	20	10	8	4	2	1

- This minute counter counts from "00" to "01," "02," and up to 59 minutes, after which it starts again from 00 minutes.

3) Hour counter

Table 8-7 Hour Counter Register

Address		Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
02, 12		HOUR	○	○	20	10	8	4	2	1

- This hour counter counts from "00" hours to "01," "02," and up to 23 hours, after which it starts again from 00 hours.

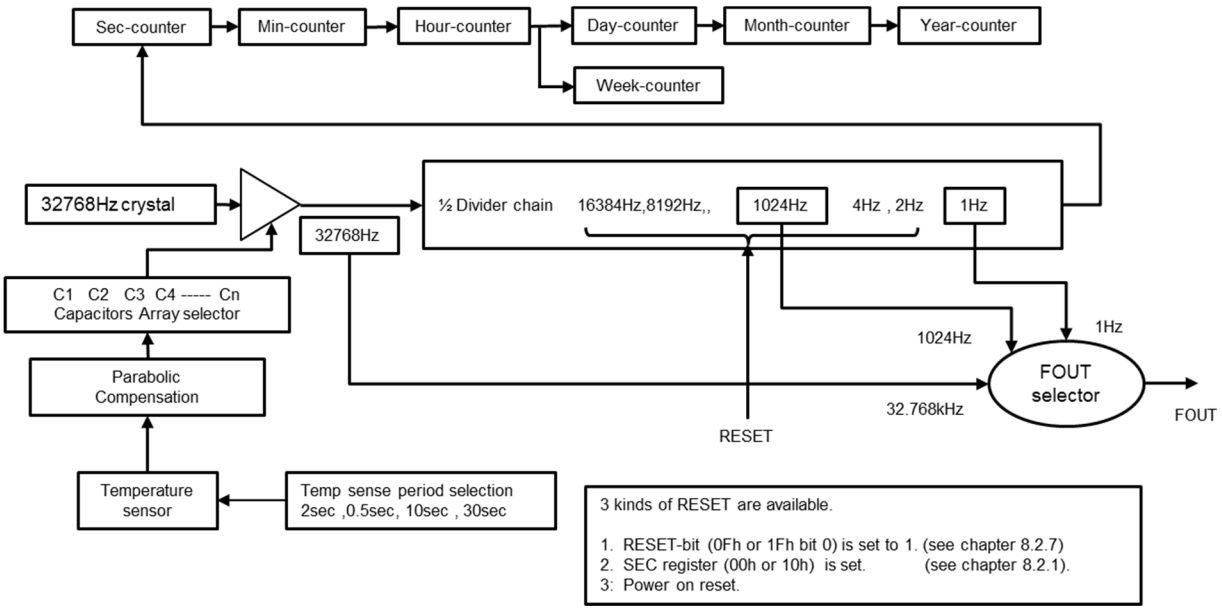


Figure 8-1 32768Hz Divider, Counter, FOUT

8.2.2. Calendar counter (WEEK - YEAR)

Table 8-8. Calendar counter Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
03, 13	WEEK	○	6	5	4	3	2	1	0

∗) "o" indicates write-protected bits. A zero is always read from these bits.

1) Day of the WEEK counter

- The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
  The day data values are counted as follows: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
- The correspondence between days and count values is shown below.

Table 8-9. Week Counter Register

WEEK	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day	Data [h]
Write/Read	0	0	0	0	0	0	0	**1**	Sunday	01 h
	0	0	0	0	0	0	**1**	0	Monday	02 h
	0	0	0	0	0	**1**	0	0	Tuesday	04 h
	0	0	0	0	**1**	0	0	0	Wednesday	08 h
	0	0	0	**1**	0	0	0	0	Thursday	10 h
	0	0	**1**	0	0	0	0	0	Friday	20 h
	0	**1**	0	0	0	0	0	0	Saturday	40 h
Write prohibit	∗ Do not set "1" to more than one day at the same time. Also, note with caution that any setting other than the seven shown above should not be made as it may interfere with normal operation.								–	–

Table 8-10. Date Counter Registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
04, 14	DAY	○	○	20	10	8	4	2	1
05, 15	MONTH	○	○	○	10	8	4	2	1
06, 16	YEAR	80	40	20	10	8	4	2	1

∗) "o" indicates write-protected bits. A zero is always read from these bits.

- The auto calendar function updates all dates, months, and years from January 1, 2001 to December 31, 2099.
- The data format is BCD format. For example, a date register value of "0011 0001" indicates the 31st.

∗ Note with caution that writing non-existent date data may interfere with normal operation of the calendar counter.

2) Da~~te~~ counter

Table 8-11. Day Counter Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
04, 14	DAY	○	○	20	10	8	4	2	1

- The updating of dates by the date counter varies according to the month setting.

∗ A leap year is set whenever the year value is a multiple of four (such as 04, 08, 12, 88, 92, or 96). In February of a leap year, the counter counts dates from "01," "02," "03," to "28," "29," "01," etc.

Table 8-12. Date update pattern

DAY	Month	Date update pattern
Write/Read	1, 3, 5, 7, 8, 10, or 12	01, 02, 03 ~ 30, 31, 01 ~
	4, 6, 9, or 11	01, 02, 03 ~ 30, 01, 02 ~
	February in normal year	01, 02, 03 ~ 28, 01, 02 ~
	February in leap year	01, 02, 03 ~ 28, 29, 01 ~

3) Month counter

Table 8-13. Month counter Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
05, 15	MONTH	○	○	○	10	8	4	2	1

- The month counter counts from 01 (January), 02 (February), and up to 12 (December), then starts again at 01 (January).

4) Year counter

Table 8-14. Year Counter Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
06, 16	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

- The year counter counts from 00, 01, 02 and up to 99, then starts again at 00.
- Any year that is a multiple of four (04, 08, 12, 88, 92, 96, etc.) is handled as a leap year.

8.2.3. Alarm registers

Table 8-15. Alarm Registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	•	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1

- The alarm interrupt function is used, along with the **AEI, AF, and WADA bits**, to set alarms for specified date, day, hour, and minute values.
- When the settings in the above alarm registers and the WADA bit match the current time, the /INT pin goes to low level and "1" is set to the AF bit to report that an alarm interrupt event has occurred.

8.2.4. Fixed-cycle timer control registers

Table 8-16. Fixed-cycle timer control registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0B, 1B	Timer Counter 0	128	64	32	16	8	4	2	1
0C, 1C	Timer Counter 1	•	•	•	•	2048	1024	512	256

- These registers are used to set the preset countdown value for the fixed-cycle timer interrupt function. The **TE, TF, TIE, and TSEL0/1 bits** are also used to set the fixed-cycle timer interrupt function.
- When the value in the above fixed-cycle timer control register changes from 001h to 000h, the /INT pin goes to low level and "1" is set to the TF bit to report that a fixed-cycle timer interrupt event has occurred.

8.2.5. Extension register

Table 8-17. Extension Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D, 1D	Extension Register (Default)	TEST (0) mandatory	WADA (–)	USEL (–)	TE (–)	FSEL1 (0)	FSEL0 (0)	TSEL1 (–)	TSEL0 (–)

∗1) "The default value is the value that is read (or is set internally) after powering up from 0 V

∗2) "0 mandatory" 0" Make sure to always write 0 into this bit.

∗3) "–" indicates a default value is undefined.

- This register is used to specify the target for the alarm function or time update interrupt function and to select or set operations such as fixed-cycle timer operations.

1) TEST bit
This is the manufacturer's test bit. Its value should always be "0".
Be careful to avoid writing a "1" to this bit when writing to other bits.

Table 8-18. TEST bit

TEST	Data	Description
Write/Read	0	Normal operation mode ∗ Default
	1	Setting prohibited (manufacturer's test bit)

2) WADA (Week Alarm/Day Alarm) bit
This bit is used to specify either WEEK or DAY as the target of the alarm interrupt function.
Writing a "1" to this bit specifies a DAY alarm, meaning the alarm interrupt is initiated independent of the actual day when the set time is reached.
Writing a "0" to this bit specifies a WEEK alarm, so an alarm interrupt is only generated when the set time is reached on a dedicated day of a week.

3) USEL (Update Interrupt Select) bit
This bit is used to define if the RTC should output a "second update" or "minute update" interrupt, allowing to synchronize external clocks with the time registers of the RTC.

Table 8-19. USEL bit

USEL	Data	update interrupts	Auto reset time tRTN
Write/Read	0	second update ∗ Default	500 ms
	1	minute update	Min. 7.813 ms

4) TE (Timer Enable) bit
This bit controls the start/stop setting for the fixed-cycle timer interrupt function.
Writing a "1" to this bit specifies starting of the fixed-cycle timer interrupt function (a countdown starts from a preset value).
Writing a "0" to this bit specifies stopping of the fixed-cycle timer interrupt function.

5) FSEL0,1 (FOUT frequency Select 0, 1) bits
The combination of these two bits is used to set the FOUT frequency.
Note: All frequencies are temperature compensated!

Table 8-20. FSEL bits

FSEL0,1	FSEL1 (bit 3)	FSEL0 (bit 2)	FOUT frequency
Write/Read	0	0	32768 Hz Output ∗ Default
	0	1	1024 Hz Output
	1	0	1 Hz Output
	1	1	32768 Hz Output

6) TSEL0,1 (Timer Select 0, 1) bits
The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

Table 8-21. TSEL bits

TSEL0,1	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock
Write/Read	0	0	4096 Hz / Once per 244.14 μs
	0	1	64 Hz / Once per 15.625 ms
	1	0	"Second" update / Once per second
	1	1	"Minute" update / Once per minute

8.2.6. Flag register

Table 8-22. Flag Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0E, 1E	Flag register (Default)	○ (0)	○ (0)	UF (–)	TF (–)	AF (–)	○ (0)	VLF (1)	VDET (1)

Default is values loaded automatically after power ON from 0V.
"o" indicates write-protected bits. A zero is always read from these bits.
"–" indicates a default value is undefined.

1) VLF (Voltage Low Flag) bit

VLF indicates the retained reliability of clock functions and internal data.
When VLF was set to "1", it indicates possibility that was lost of both memorized data and clock calendar data.
The factor of VLF are 2kinds.
1 Supply voltage drop less than 1.6V(VCLK) was detected.
VLF-voltage-detector is active in anytime. Detection velocity is about 1ms to 10ms.
2 The internal crystal oscillation was stopped. This detector is active in anytime.
Detection velocity is about 100ms.
Once VLF value was set to "1", its "1" is retained until a "0" is written to it.
After initial power ON from 0 V, make sure VLF was set to "1".

Table 8-23. VLF bit

VLF	Data	Description
Write	0	The VLF bit is cleared to zero to prepare for the next status detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	No supply voltage drop occurred, so data are not compromised.
	1	Low voltage has been detected, so data loss might have occurred, and time information might be compromised. All registers must be initialized. (This setting is retained until a "zero" is written to this bit.)

2) VDET (Voltage Detection Flag) bit

VDET indicates the retained reliability of temperature compensation.
When VET was set to "1", it indicates possibility that was lost of clock stability history.
The factor of VDET.
Supply voltage drop less than 1.95V(VDET) was detected.
VDET is detected in every temperature compensation timing. Detection velocity is about 1ms to 10ms.
Once VDET value is "1", VDET is retained until a "0" is written to it.
After powering up from 0 V, make sure to set this bit's value to "1".

Table 8-24. VDET bit

VDET	Data	Description
Write	0	The VDET bit is cleared to zero to prepare for the next low voltage detection.
	1	Invalid (writing a 1 will be ignored)!
Read	0	Temperature compensation is normal.
	1	Temperature compensation has been stopped.

3) UF (Update Flag) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a time update interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
* For details, see "8.4. Time Update Interrupt Function".

4) TF (Timer Flag) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
* For details, see "8.3. Fixed-cycle Timer Interrupt Function".

5) AF (Alarm Flag) bit
If set to "0" beforehand, this flag bit's value changes from "0" to 1" when an alarm interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.
* For details, see "8.5. Alarm Interrupt Function".

8.2.7. Control register

Table 8-25. Control Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0F, 1F	Control Register (Default)	CSEL1 (0)	CSEL0 (1)	UIE (0)	TIE (0)	AIE (0)	○ (0)	○ (0)	RESET (0)

*1) The default value is the value that is read (or is set internally) after powering up from 0 V.
*2) "o" indicates write-protected bits. A zero is always read from these bits.
*3) "–" indicates no default value has been defined.

- This register is used to control interrupt event output from the /INT pin and the stop/start status of clock and calendar operations.

1) CSEL0,1 (Compensation interval Select 0, 1) bits
The combination of these two bits is used to set the temperature compensation interval.

Table 8-26. CSEL bits

CSEL0,1	CSEL1 (bit 7)	CSEL0 (bit 6)	Compensation interval
Write/Read	0	0	0.5 s
	0	1	2.0 s * Default
	1	0	10 s
	1	1	30 s

2) UIE (Update Interrupt Enable) bit
When a time update interrupt event is generated (when the UF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).
When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.
When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

Table 8-27. UIE bit

UIE	Data	Function
Write/Read	0	When a time update interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared (/INT status changes from low to Hi-Z) earliest 7.813 ms after the interrupt occurs.

3) TIE (Timer Interrupt Enable) bit
When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status

remains Hi-Z). When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.
When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

Table 8-28. TIE bit

TIE	Data	Function
Write/Read	0	When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

4) AIE (Alarm Interrupt Enable) bit
When an alarm timer interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies if an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).
When a "1" is written to this bit, an interrupt signal is generated (/INT status changes from Hi-Z to low) when an interrupt event is generated.
When a "0" is written to this bit, no interrupt signal is generated when an interrupt event occurs.

Table 8-29. AIE bit

AIE	Data	Function
Write/Read	0	When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status changes from low to Hi-Z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When an alarm interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's AIE bit is "1". This setting is retained until the AF bit value is cleared to zero. (No automatic cancellation)

* For details, see "8.5. Alarm Interrupt Function".

[Caution]
(1) The /INT pin is a shared interrupt output pin for three types of interrupts. It outputs the OR'ed result of these interrupt outputs. When an interrupt has occurred (when the /INT pin is at low level), the UF, TF, read AF flags to determine which flag has a value of "1"
(this indicates which type of interrupt event has occurred).
(2) The status of update interrupt, timer interrupt and alarm interrupt can be checked by software polling without using the /INT pin. In this case, write "0" into UIE, TIE, and AIE bits to avoid physical interrupt generation and thus reduce power consumption.

5) RESET bit

RESET bit was prepared for the synchronized starting of time or timer.
The detailed function of reset.

For example.
S is start condition. P is stop condition. RS is re-start condition.

S---Slave address(w)---ACK1---0Fh---ACK2---01h---ACK3---RS---R/W access----P.

RESET-bit is set at ACK3, but RESET doesn't execute.
after set of RESET, RESET-function executes momentarily at next P, and RESET-bit clears automatically.
RESET area of circuit is the count-down-chain of 2Hz from 16kHz, are cleared.
Therefore, RESET do not affect 32kHz output.
Next update timing of a Seconds counter from RESET.
That range is 1000ms-30.5μs from just 1000ms.
RESET affects to time update interruption, alarm, and timer.

Note:
RESET is not released by the reception of a RE-START condition before receiving a STOP condition.
Unnecessary use of RESET will be the cause of delay error of Calendar and Clock.

8.2.8. Temperature Data register

Table 8-30. Temperature Data Register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
17	TEMP	128	64	32	16	8	4	2	1

1) Temperature Data register

This register can be used to read digital temperature data.
The temperature data are updated during operation of the temperature compensation circuit.
You can make a conversion to a centigrade by temperature data by calculating in the following expression.

Temperature[℃] = (TEMP[7:0] * 2 – 187.19) / 3.218

8.2.9. Backup power supply control register

Table 8-31. Backup power supply control register

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
18	Backup Function	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0

This register controls the functionality of the power switchover and backup function.

1) VDETOFF bit (Voltage Detector OFF)
This bit controls the voltage detection circuit of the main power supply VDD.
＊ For details, see “8.8.5. Related registers of the backup power supply switchover function”

2) SWOFF bit (Switch OFF)
This bit controls the internal P-MOS switch for preventing back flow.
＊ For details, see “8.8.5. Related registers of the backup power supply switchover function”.

3) BKSMP1, BKSMP0 bit (Backup mode Sampling time)
These bits control the operation time when to be intermittently driven the VDD voltage detection.
＊ For details, see “8.8.5. Related registers of the backup power supply switchover function”

8.3. Fixed Cycle Timer Interrupt Function

This interruption is released automatically, that is most suitable for a wakeup timer or an interval operation system. The fixed-cycle timer interrupt generation function generates an interrupt event periodically at any fixed cycle set between 244.14 μs and 4095 minutes.
When an interrupt event is generated, the /INT pin goes to low level and "1" is set to the TF bit to report that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low-level to Hi-Z).

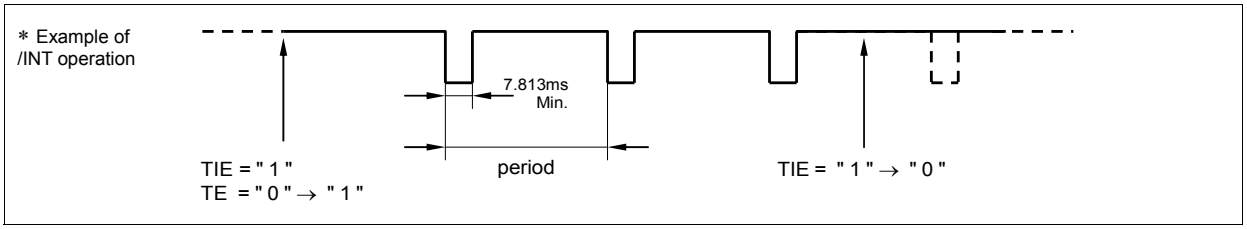


Figure 8-2 Wakeup Timer Interrupt.

8.3.1. Diagram of fixed-cycle timer interrupt function

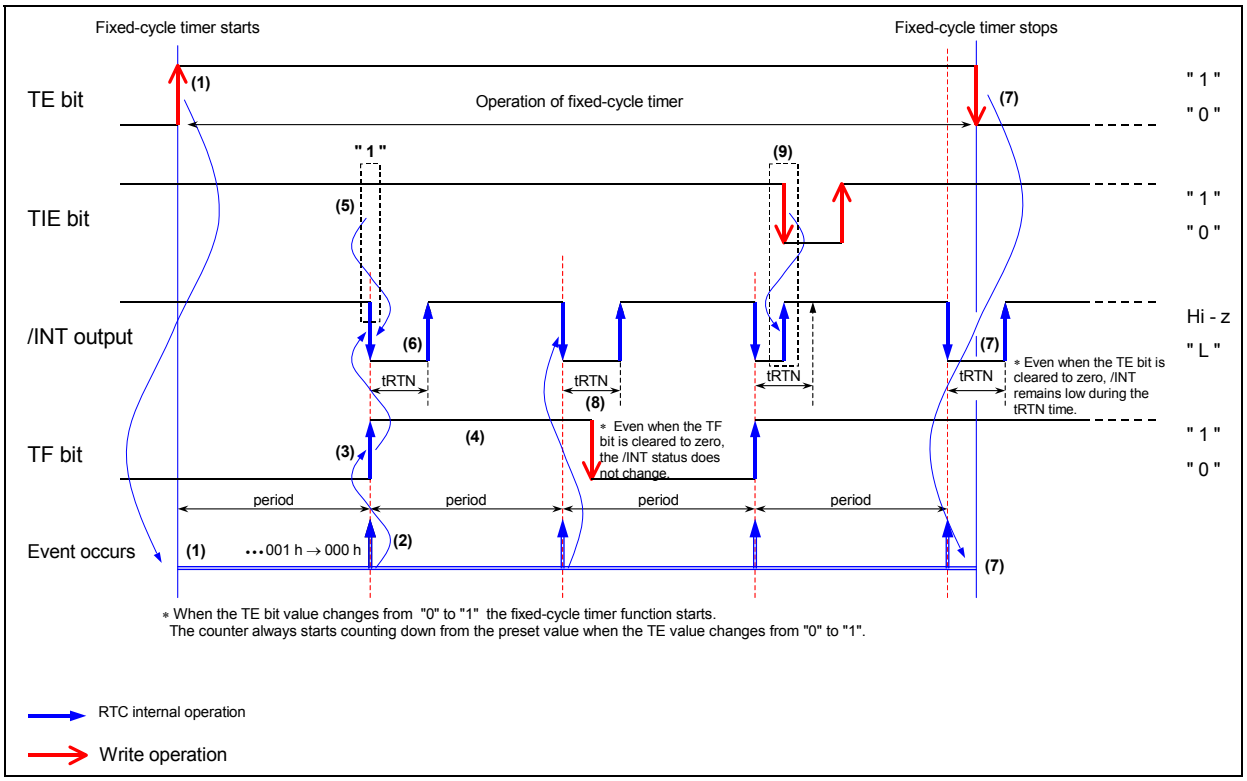


Figure 8-3 Fixed-cycle Timer Interrupt Timing Chart.

(1) When a "1" is written to the TE bit, the fixed-cycle timer countdown starts from the preset value.

(2) A fixed-cycle timer interrupt event starts a countdown based on the countdown period (source clock). When the count value changes from 001h to 000h, an interrupt event occurs.
∗ After the interrupt event occurs, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

(3) When a fixed-cycle timer interrupt event occurs, "1" is written to the TF bit.

(4) When the TF bit = "1" its value is retained until it is cleared to zero.

(5) If the TIE bit = "1" when a fixed-cycle timer interrupt occurs, /INT pin output goes low.
∗ If the TIE bit = "0" when a fixed-cycle timer interrupt occurs, /INT pin output remains Hi-Z.

(6) Output from the /INT pin remains low during the tRTN period following each event, after which it is automatically cleared to Hi-Z status.
∗ /INT is again set low when the next interrupt event occurs.

(7) When a "0" is written to the TE bit, the fixed-cycle timer function is stopped, and the /INT pin is set to Hi-Z status.
∗ When /INT = low, the fixed-cycle timer function is stopped. The tRTN period is the maximum amount of time before the /INT pin status changes from low to Hi-Z.

(8) As long as /INT = low, the /INT pin status does not change when the TF bit value changes from "1" to "0".

(9) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the TIE bit value changes from "1" to "0".

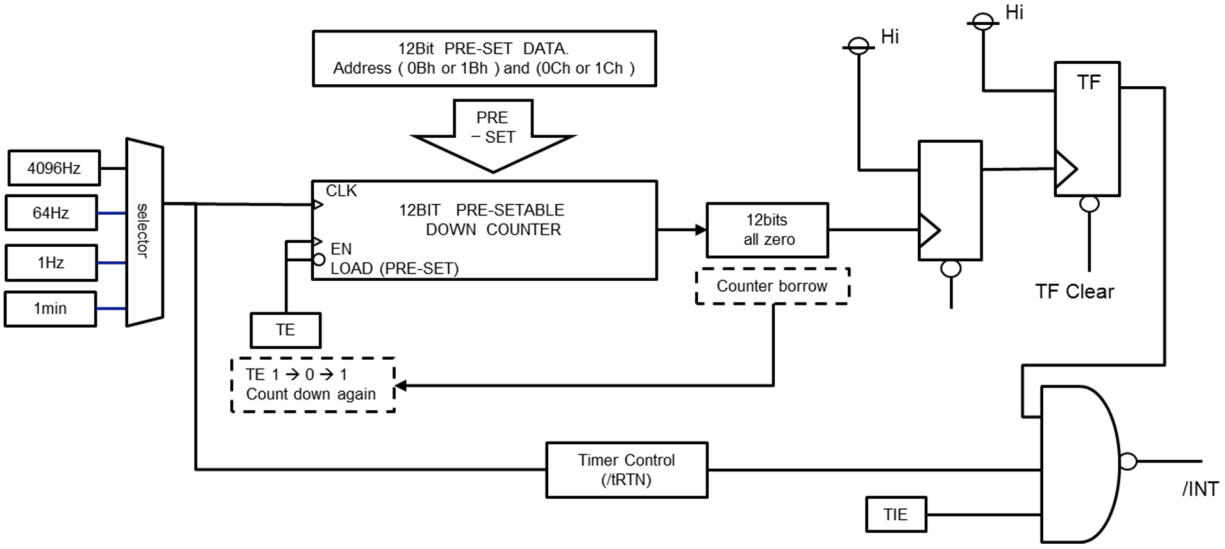


Figure 8-4. Fixed-cycle Timer Interrupt Block Diagram

8.3.2. Related registers for function of time update interrupts.

Table 8-32. Related registers for function of time update interrupts.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0B, 1B	Timer Counter 0	**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
0C, 1C	Timer Counter 1	•	•	•	•	**2048**	**1024**	**512**	**256**
0D, 1D	Extension Register	TEST	WADA	USEL	**TE**	FSEL1	FSEL0	**TSEL1**	**TSEL0**
0E, 1E	Flag Register	○	○	UF	**TF**	AF	EVF	VLF	VDET
0F, 1F	Control Register	CSEL1	CSEL0	UIE	**TIE**	AIE	EIE	○	RESET

∗1) "o" indicates write-protected bits. A zero is always read from these bits.

∗2) Bits marked with "•" are RAM bits that can contain any value and are read/write-accessible.

∗ Before entering settings for operations, we recommend writing a "0" to the TE and TIE bits to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the RESET bit value is "1" the time update interrupt function does not operate.

∗ When the fixed-cycle timer interrupt function is not being used, the fixed-cycle timer control register (0Bh to 0Ch) can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

1) TSEL0,1 bits (Timer Select 0, 1)
The combination of these two bits is used to set the countdown period (source clock) for the fixed-cycle timer interrupt function (four settings can be made).

Table 8-33. TSEL bits

TSEL0,1	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock	Auto reset time tRTN (Min.)	Effects of RESET bits
Write/Read	0	0	4096 Hz /Once per 244.14 μs	122 μs	–
	0	1	64 Hz / Once per 15.625 ms	7.813 ms	∗ Does not operate when the RESET bit value is "1".
	1	0	"Second" update /Once per second	7.813 ms	
	1	1	"Minute" update /Once per minute	7.813 ms	

∗1) The /INT pin's auto reset time (tRTN) varies as shown above according to the source clock setting.

∗2) When the source clock has been set to "second update" or "minute update", the timing of both countdown and interrupts is coordinated with the clock update timing.

2) Fixed-cycle Timer Control register (Reg - 0Bh to 0Ch)

This register is used to set the default (preset) value for the counter. Any count value from 1 (001 h) to 4095 (FFFh) can be set. The counter counts down based on the source clock's period, and when the count value changes from 001h to 000h, the TF bit value becomes "1".

The countdown that starts when the TE bit value changes from "0" to "1" always begins from the set value.

Be sure to write "0" to the TE bit before writing a value into the timer counter register. If a value is written while TE = "1" the first subsequent event will not be generated correctly.

Table 8-34. Timer Counter Registers

Address 0C,1C Timer Counter 1								Address 0B,1B Timer Counter 0							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
•	•	•	•	2048	1024	512	256	128	64	32	16	8	4	2	1

3) TE (Timer Enable) bit

This bit controls the start/stop setting for the fixed-cycle timer interrupt function.

Table 8-35. TE bit

TE	Data	Description
Write/Read	0	Stops fixed-cycle timer interrupt function.
	1	Starts fixed-cycle timer interrupt function. * The countdown that starts when the TE bit value changes from "0" to "1" always begins from the preset value.

4) TF (Timer Flag) bit

If set to "0" beforehand, this flag bit's value changes from "0" to 1" when a fixed-cycle timer interrupt event has occurred. Once this flag bit's value is "1", its value is retained until a "0" is written to it.

Table 8-36. TF bit

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z).
	1	Invalid (writing a 1 will be ignored)!
Read	0	Fixed-cycle timer interrupt events are not detected.
	1	Fixed-cycle timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

5) TIE (Timer Interrupt Enable) bit

When a fixed-cycle timer interrupt event occurs (when the TF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

Table 8-37. TIE bit

TIE	Data	Description
Write/Read	0	1) When a fixed-cycle timer interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When a fixed-cycle timer interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z). * Even when the TIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L").
	1	When a fixed-cycle timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a fixed-cycle timer interrupt event has been generated low-level output from the /INT pin occurs only when the value of the control register's TIE bit is "1". Earliest 7.813 ms the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

8.3.3. Fixed-cycle timer interrupt interval (example)

Table 8-38. Fixed-cycle timer interrupt interval

Timer Counter setting	Source clock			
	4096 Hz TSEL1,0 = 0,0	64 Hz TSEL1,0 = 0,1	"Second" update TSEL1,0 = 1,0	"Minute" update TSEL1,0 = 1,1
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
2	488.28 μs	31.25 ms	2 s	2 min
⋮	⋮	⋮	⋮	⋮
41	10.010 ms	640.63 ms	41 s	41 min
205	50.049 ms	3.203 s	205 s	205 min
410	100.10 ms	6.406 s	410 s	410 min
2048	500.00 ms	32.000 s	2048 s	2048 min
⋮	⋮	⋮	⋮	⋮
4095	0.9998 s	63.984 s	4095 s	4095 min

- Time error in fixed-cycle timer
  A time error in the fixed-cycle timer will produce a positive or negative time period error in the selected source clock.

8.3.4. Fixed-cycle timer start timing

Counting down of the fixed-cycle timer value starts at the rising edge of the SCL signal that occurs when the TE value is changed from "0" to "1" (after bit 0 is transferred).

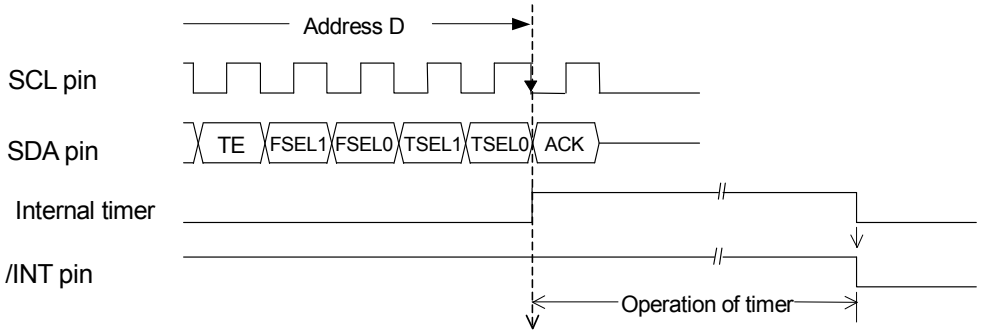


Figure 8-5. Fixed-cycle Timer start-timing.

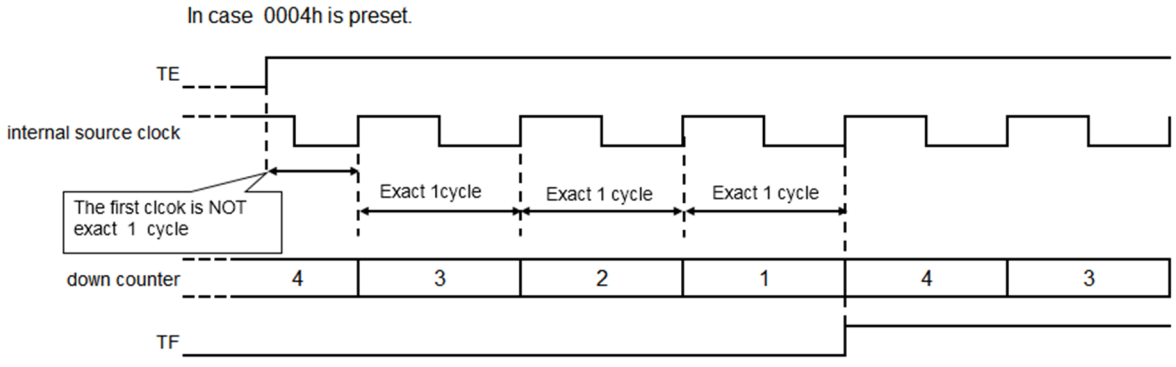


Figure 8-6. Source clock and fixed-cycle timer

8.4. Time Update Interrupt Function

The time update interrupt function generates interrupt events at one-second or one-minute intervals, according to the timing of the internal clock.
When an interrupt event occurs, the UF bit value becomes "1" and the /INT pin goes to low level to indicate that an event has occurred. (However, when a fixed-cycle timer interrupt event has been generated, low-level output from the /INT pin occurs only when the value of the control register's UIE bit is "1". This /INT status is automatically cleared (/INT status changes from low level to Hi-Z) earliest 7.813 ms (fixed value) after the interrupt occurs.

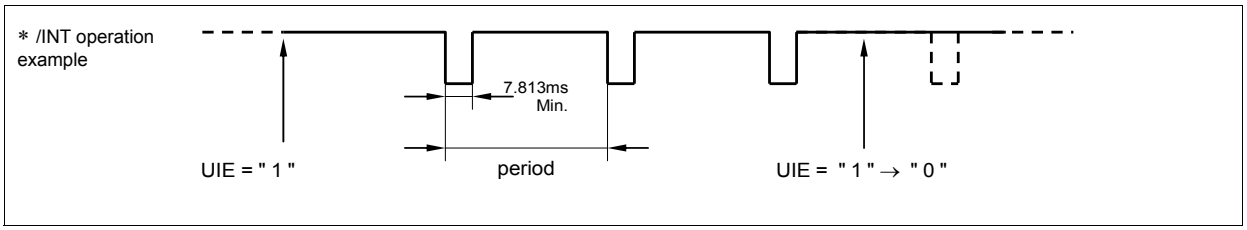


Figure 8-7. Time Update Interrupt

8.4.1. Time update interrupt function diagram

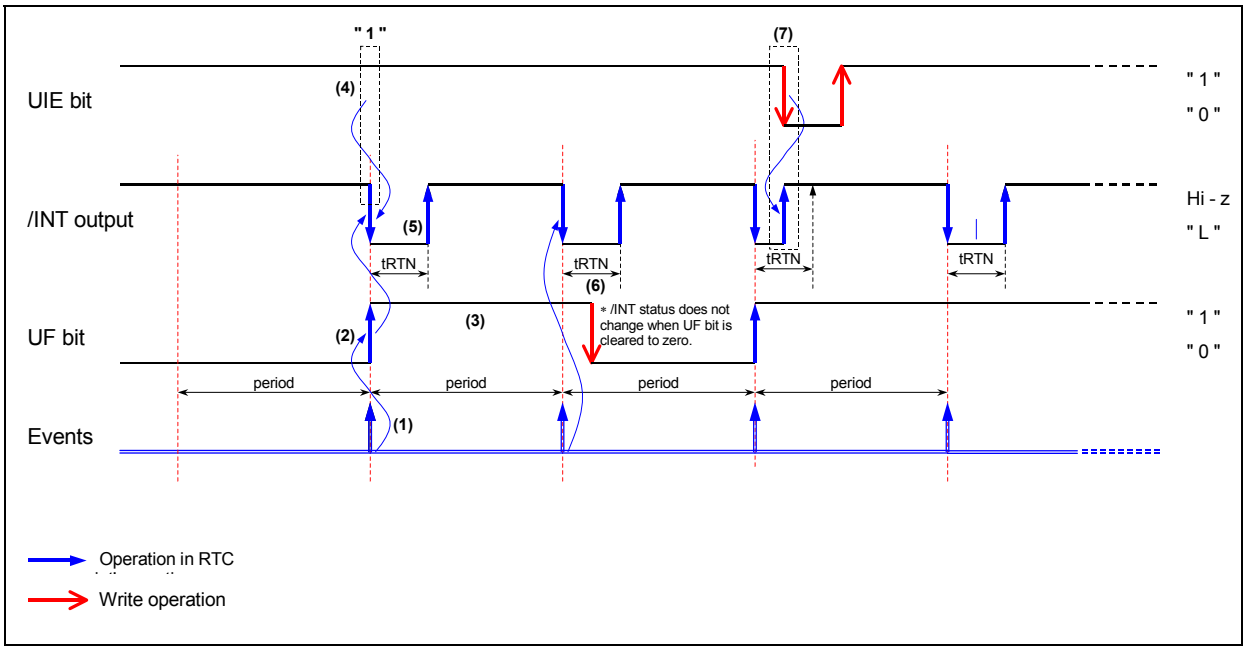


Figure 8-8. Time Update Interrupt Timing Chart.

(1) A time update interrupt event occurs when the internal clock's value matches either the second update time or the minute update time. The USEL bit's specification determines whether it is the second update time or the minute update time that must be matched.

(2) When a time update interrupt event occurs, the UF bit value becomes "1".

(3) When the UF bit value is "1" its value is retained until it is cleared to zero.

(4) When a time update interrupt occurs, /INT pin output is low if UIE = "1".
∗ If UIE = "0" when a timer update interrupt occurs, the /INT pin status remains Hi-Z.

(5) Each time an event occurs, /INT pin output is low only up to the tRTN time (which is fixed as 7.813 ms for time update interrupts) after which it is automatically cleared to Hi-Z.
∗ /INT pin output goes low again when the next interrupt event occurs.

(6) As long as /INT = low, the /INT pin status does not change, even if the UF bit value changes from "1" to "0".

(7) When /INT = low, the /INT pin status changes from low to Hi-Z as soon as the UIE bit value changes from "1" to "0".

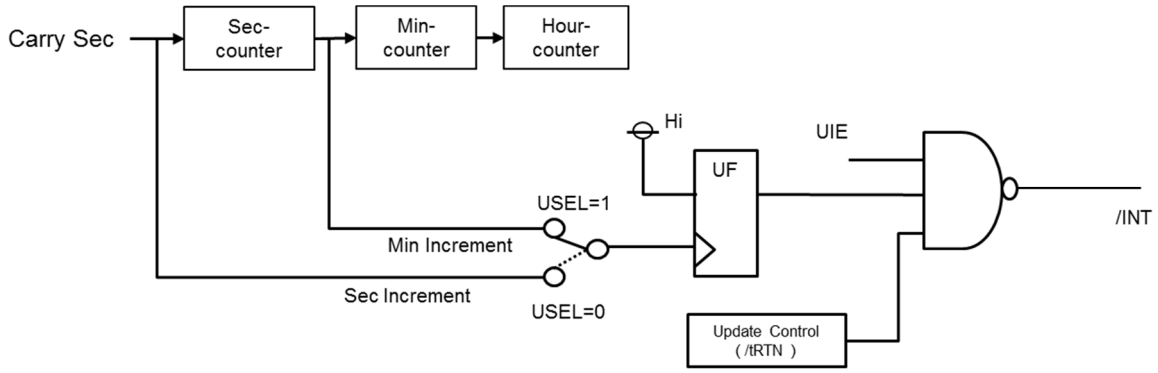


Figure 8-9. Time Update Interrupt Block Diagram

8.4.2. Related registers for time update interrupt functions.

Table 8-39. Related registers for time update interrupt functions.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0D, 1D	Extension Register	TEST	WADA	**USEL**	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E, 1E	Flag Register	○	○	**UF**	TF	AF	○	VLF	VDET
0F, 1F	Control Register	CSEL1	CSEL0	**UIE**	TIE	AIE	○	○	RESET

*) "o" indicates write-protected bits. A zero is always read from these bits.

* Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

* When the RESET bit value is "1" time update interrupt events do not occur.

* Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /INT pin status to low.

1) USEL (Update Interrupt Select) bit
This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

Table 8-40 USEL bit.

USEL	Data	Description
Write/Read	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF (Update Flag) bit
Once it has been set to "0", this flag bit value changes from "0" to "1" when a time update interrupt event occurs. When this flag bit = "1" its value is retained until a "0" is written to it.

Table 8-41. UF bit

UF	Data	Description
Write	0	The UF bit is cleared to zero to prepare for the next status detection * Clearing this bit to zero does not enable the /INT low output status to be cleared (to Hi-Z).
	1	Invalid (writing a 1 will be ignored)!
Read	0	Time update interrupt events are not detected.
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

3) UIE (Update Interrupt Enable) bit
When a time update interrupt event occurs (UF bit value changes from "0" to "1"), this bit selects whether to generate an interrupt signal (/INT status changes from Hi-Z to low) or to not generate it (/INT status remains Hi-Z)

Table 8-42. UIE bit

UIE	Data	Description
Write/Read	0	1) Does not generate an interrupt signal when a time update interrupt event occurs (/INT remains Hi-Z) 2) Cancels interrupt signal triggered by time update interrupt event (/INT changes from low to Hi-Z). * Even when the UIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L").
	1	When a time update interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). * When a time update interrupt event occurs, low-level output from the /INT pin occurs only when the UIE bit value is "1". Earliest 7.813 ms after the interrupt occurs, the /INT status is automatically cleared (/INT status changes from low to Hi-Z).

8.5. Alarm Interrupt Function

The alarm interrupt generation function generates interrupt events for alarm settings such as date, day, hour, and minute settings.
When an interrupt event occurs, the AF bit value is set to "1" and the /INT pin goes to low level to indicate that an event has occurred.

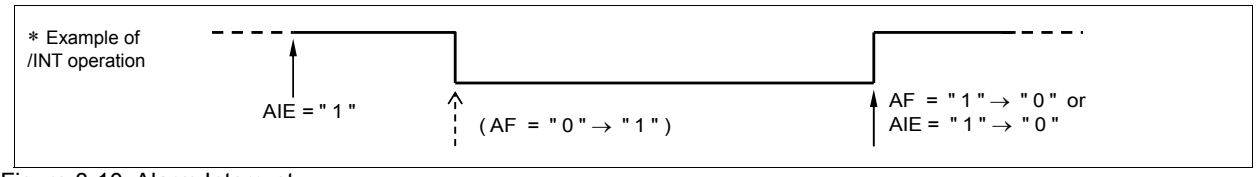


Figure 8-10. Alarm Interrupt

8.5.1. Diagram of alarm interrupt function

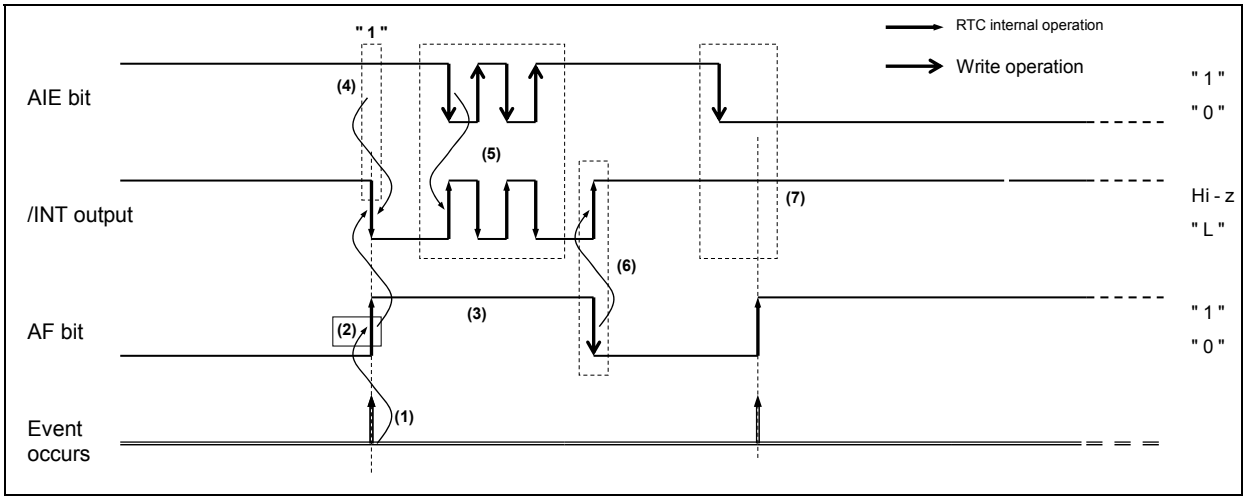


Figure 8-11. Alarm Interrupt Timing Chart.

(1) The minute, hour, day and date, when an alarm interrupt event is supposed to occur has to be set in advance, along with the WADA bit (Note) Even if the current date/time is used as the setting, the alarm will not occur until the counter counts up to the current date/time (i.e., an alarm will occur next time, not immediately).

(2) When a time update interrupt event occurs, the AF bit values becomes "1".

(3) When the AF bit = "1", its value is retained until it is cleared to zero.

(4) If AIE = "1" when an alarm interrupt occurs, the /INT pin output goes low.
* When an alarm interrupt event occurs, /INT pin output goes low, and this status is then held until it is cleared via the AF bit or AIE bit.

(5) If the AIE value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to Hi-Z. After the alarm interrupt occurs and before the AF bit value is cleared to zero, the /INT status can be controlled via the AIE bit.

(6) If the AF bit value is changed from "1" to "0" while /INT is low, the /INT status immediately changes from low to

Hi-Z.

(7) If the AIE bit value is "0" when an alarm interrupt occurs, the /INT pin status remains Hi-Z.

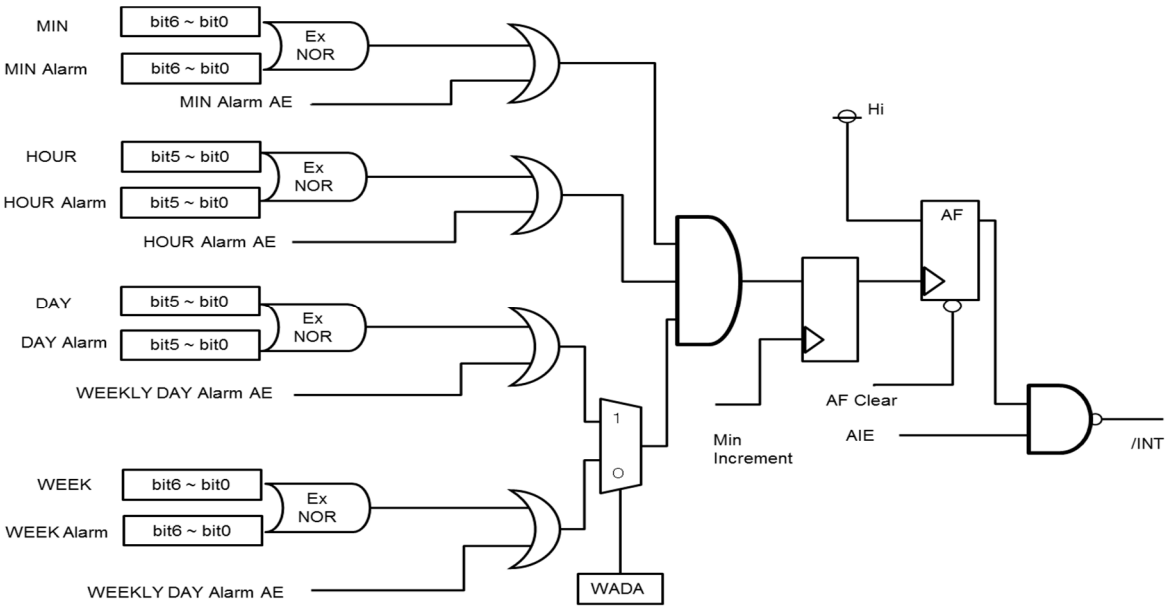


Figure 8-12. Alarm Interrupt Block Diagram

8.5.2. Related registers

Table8-43. Alarm Related Registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01, 11	MIN	○	40	20	10	8	4	2	1
02, 12	HOUR	○	○	20	10	8	4	2	1
03, 13	WEEK	○	6	5	4	3	2	1	0
04, 14	DAY	○	○	20	10	8	4	2	1
08	MIN Alarm	**AE**	40	20	10	8	4	2	1
09	HOUR Alarm	**AE**	•	20	10	8	4	2	1
0A	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
0D, 1D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0
0E, 1E	Flag Register	○	○	UF	TF	**AF**	○	VLF	VDET
0F, 1F	Control Register	CSEL1	CSEL0	UIE	TIE	**AIE**	○	○	RESET

∗1) "o" indicates write-protected bits. A zero is always read from these bits.

∗2) Bits marked with "•" are RAM bits that can contain any value and are read/write-accessible.

∗ Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

∗ When the alarm interrupt function is not being used, the Alarm registers (Reg – 08h to 0Ah) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

∗ When the AIE bit value is "1" and the Alarm registers (Reg – 08h to 0Ah) is being used as a RAM register, /INT may be assert to low level unintentionally.

1) WADA (Week Alarm /Day Alarm) bit
The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

Table 8-44. WADA bit

WADA	Data	Description
Write/Read	0	Sets WEEK as target of alarm function (DAY setting is ignored)
	1	Sets DAY as target of alarm function (WEEK setting is ignored)

2) Alarm registers

Table 8-45. Alarm Registers

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
08	MIN Alarm	AE	40	20	10	8	4	2	1
09	HOUR Alarm	AE	•	20	10	8	4	2	1
0A	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1

The minute, hour, day and date when an alarm interrupt event will occur is set using this register and the WADA bit.

In the WEEK alarm /Day alarm register (Reg - 0Ah), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

When the settings made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /INT pin goes low.
Note: AE-bit is low active, so in order to enable 1 interrupt every hour once the actual minutes match the alarm setting, it is necessary to set the AE of register 08h to 0 and the AE of 09h and 0Ah to 1.
In order to generate an alarm interrupt only once a week, all 3 AE-bits have to be set “0

∗1) The alarm function is not a HW feature but software function inside the RTC!
*2) In case “AE” bit of register 0Ah is set to "1", the day will be ignored and an interrupt occurs ones the actual time matches the minutes and/or hour setting of the alarm register.
(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - 0Ah):
Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only the hour and minute values match the alarm data.

∗3) If all three AE bit values are "1" the week/date and time settings are ignored, and an alarm interrupt event will occur once per minute.

3) AF (Alarm Flag) bit
When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

Table 8-46. AF bit

AF	Data	Description
Write	0	The AF bit is cleared to zero to prepare for the next status detection ∗ Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-Z) when an alarm interrupt event has occurred.
	1	Invalid (writing a 1 will be ignored)!
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE (Alarm Interrupt Enable) bit
When an alarm interrupt event occurs (when the AF bit value changes from "0" to "1"), this bit's value specifies whether an interrupt signal is generated (/INT status changes from Hi-Z to low) or is not generated (/INT status remains Hi-Z).

Table 8-47. AIE bit

AIE	Data	Description
Write/Read	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/INT status remains Hi-Z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/INT status changes from low to Hi-Z). ∗ Even when the AIE bit value is "0" another interrupt event may change the /INT status to low (or may hold /INT = "L").
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-Z to low). ∗ When an alarm interrupt event occurs, low-level output from the /INT pin occurs only when the AIE bit value is "1". This value is retained (not automatically cleared) until the AF bit is cleared to zero.

8.5.3. Examples of alarm settings

1) Example of alarm settings when "Day" has been specified (and WADA bit = "0")

Table 8-48. Examples of alarm setting 1

Day is specified WADA bit = "0"	Reg – A bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S	Reg - 9 HOUR Alarm	Reg - 8 MIN Alarm
Monday through Friday, at 7:00 AM ∗ Minute value is ignored	0	0	1	1	1	1	1	0	07 h	AE = 1
Every Saturday and Sunday, for 30 minutes each hour ∗ Hour value is ignored	0	1	0	0	0	0	0	1	AE = 1	30 h
Every day, at 6:59 AM	0	1	1	1	1	1	1	1	18 h	59 h
	1	X	X	X	X	X	X	X		

X: Don't care

2) Example of alarm settings when "Day" has been specified (and WADA bit = "1")

Table8-49. Examples of alarm setting 2

Day is specified WADA bit = "1"	Reg - A bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01	Reg - 9 HOUR Alarm	Reg - 8 MIN Alarm
First of each month, at 7:00 AM ∗ Minute value is ignored	0	0	0	0	0	0	0	1	07 h	AE = 1
15th of each month, for 30 minutes each hour ∗ Hour value is ignored	0	0	0	1	0	1	0	1	AE = 1	30 h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18 h	59 h

X: Don't care

8.6. The interrupt functions via /INT-pin or polling.

1) How to identify events, when the interruption was occurred.

/INT output pin is common output terminal of interrupt events of three types (Fixed-cycle timer interrupt , Alarm interrupt, Time update interrupt).
When INT asserted to Low, the system can determine in which interruption was occurred, by confirming status of (TF,AF, UF).

2) The method of detection of interruption with not using an INT output.

1. be left open INT.
2. be clears to 0 in TIE, AIE, and UIE bits.
3. monitor the TF, AF, UF. (Polling).

8.7. Temperature compensation function.

8.7.1. over view

During the production process of the RTC, we are programming the individual characteristics of the built-in crystal into the non-volatile memory of the RTC. The build-in temperature sensor measures the actual temperature of the module and compensates the oscillation frequency of the crystal oscillator using the stored compensation data. This way not only the time information is temperature compensated, but as well the FOUT signal, even when outputting 32.768kHzThis function works in the supply voltage range VTEM.

8.7.2. Related registers for temperature compensation function

Table 8-50. Temperature compensation Register

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0F,1F	Control Register	**CSEL1**	**CSEL0**	UIE	TIE	AIE	○	○	RESET

1) CSEL1, CSEL0 bit (Compensation Interval Select 1,0)
This bit sets an interval of a temperature compensation operation.
Current consumption decreases when increasing the Compensation Interval by means CSEL1,0.CSEL1,0 is set at the time of initial power-up to ("0","1") .

Table 8-51. CSEL bits

CSEL1	CSEL0	Compensation Interval
0	0	0.5 s
0	1	2.0 s
1	0	10 s
1	1	30 s

Even if the power supply voltage falls below VTEM and a VDET bit is set to "1", the temperature compensation operation is performed again if the supply voltage raises above VTEM.

8.8. Battery backup switchover function

8.8.1. Description of Battery backup switchover function

This function consists of a supply voltage detector "Voltage Detector", which detects if the main supply voltage "VDD" drops below a threshold (VDET3). During the voltage detection period, the built-in Pch-switch located between the main supply voltage pin "VDD" and the backup power supply pin "VBAT".(see Figure 8-13.) is opened,

in case of VDET3 < VDD, the RTC moves back into Normal Mode, else (VDD ≦VDET3) it switches into Backup Mode.

To be able to measure the supply voltage applied to VDD-pin, the Pch-switch opens once every second and the diode stops current flows from VBAT over the RTC into VDD.

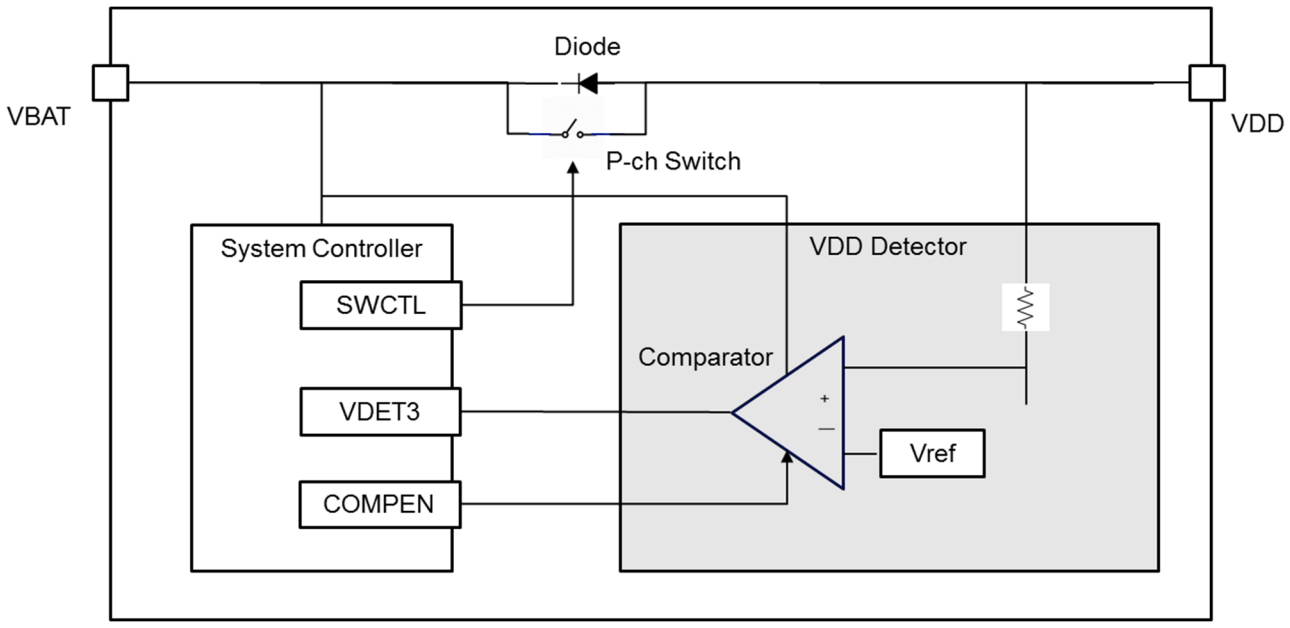


Figure 8-13. Battery Backup Switchover Block Diagram

8.8.2. The power switchover control.

To enable the battery backup switchover function, the voltage comparator (VDD Detector) should be activated by means of the VDETOFF bit. If VDETOFF=0, the power switchover function is activated and in case VDETOFF=1 this function is OFF.

In case the power switchover function is activated, the internal COMPEN signal is generated 62.5msec after the second counter incremented and thus the voltage comparator becomes active.

The comparator active period (VDD measurement period) is controlled through BKSMP0, BKSMP1 bits. There are two modes, VDET3 < VDD (Normal Mode), VDD ≦ VDET3 (Backup Mode).

< Normal Mode > VDD voltage is detected every one second.
Comparator function intermittently ON, Pch-Switch intermittently OFF
In case of VDD ≦ VDET3, it moves to Backup Mode.

< Backup Mode > VDD voltage is detected every one second.
Comparator function intermittently ON, Pch-Switch OFF in Backup Mode
In case of VDET3 < VDD, it moves to Normal Mode.

8.8.3. Battery Backup switchover related register.

Table 8-52. Battery Backup switchover related register.

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
18	Backup Function	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0

This register controls comparator, Pch-Switch, status and detection period.

8.8.4. Battery Backup switchover related register setting.

After power on reset, VDETOFF=0, SWOFF= 0, BKSMP0=0, BKSMP1=0 are set as default value.

So 1sec after power on reset, VDD voltage is detected and goes to Normal Mode (VDET3 < VDD) or Backup Mode (VDD ≦ VDET3).

The duration of VDD voltage detection is controlled by means of BKSMP0-bit, BKSMP1-bit and can be set to be 2msec, 16msec, 128sec or 256msec. VDD voltage is detected at the end of this time, so at the falling edge of the comparator ON signal.

Table 8-53. Battery Backup switchover related register setting

VDD detector	VDETOFF	SWOFF	BKSMP1	BKSMP0	VDET3 Sampling operation period	Pch-Switch ON/OFF	Remarks
ON	0	X	0	0	2ms	2ms OFF	VDETOFF:0,BKSMP1:0 ,BKSMP0:0 default
			0	1	16ms	16ms OFF	
			1	0	128ms	128ms OFF	
			1	1	256ms	256ms OFF	
OFF	1	0	X	X	OFF	ON	VDD and VBAT short circuit via Pch-switch
		1	X	X	OFF	OFF	VDD connected via diode to VBAT

X = Don't care.

Table 8-54. Diode (between VDD and VBAT) reference characteristic's

term	Characteristics	Condition
On-Resistance of Pch-Switch.	100 ohm (typ)	VDD = 3.0 V 25 degree C
Vf	0.60 V / 1 mA (typ) 0.85V / 10mA (typ)	VDD = 3.0 V 25 degree C
IR	Less than 4 nA	VDD = 5.5 V -40 to 85 degree C

8.8.5. Mode flow of the battery backup switchover function.

VDD drop below VDET3 can only be detected while the Pch-Switch is OFF (Comparator is enabled.).
In case a VDD drop below VDET3 is detected, the Pch-Switch stays OFF (open), and RTC enters Backup-mode.
When VDD is detected to be higher than VDET3, the Pch-Switch switches back to ON (closed), and RTC remains or enters Normal-mode.

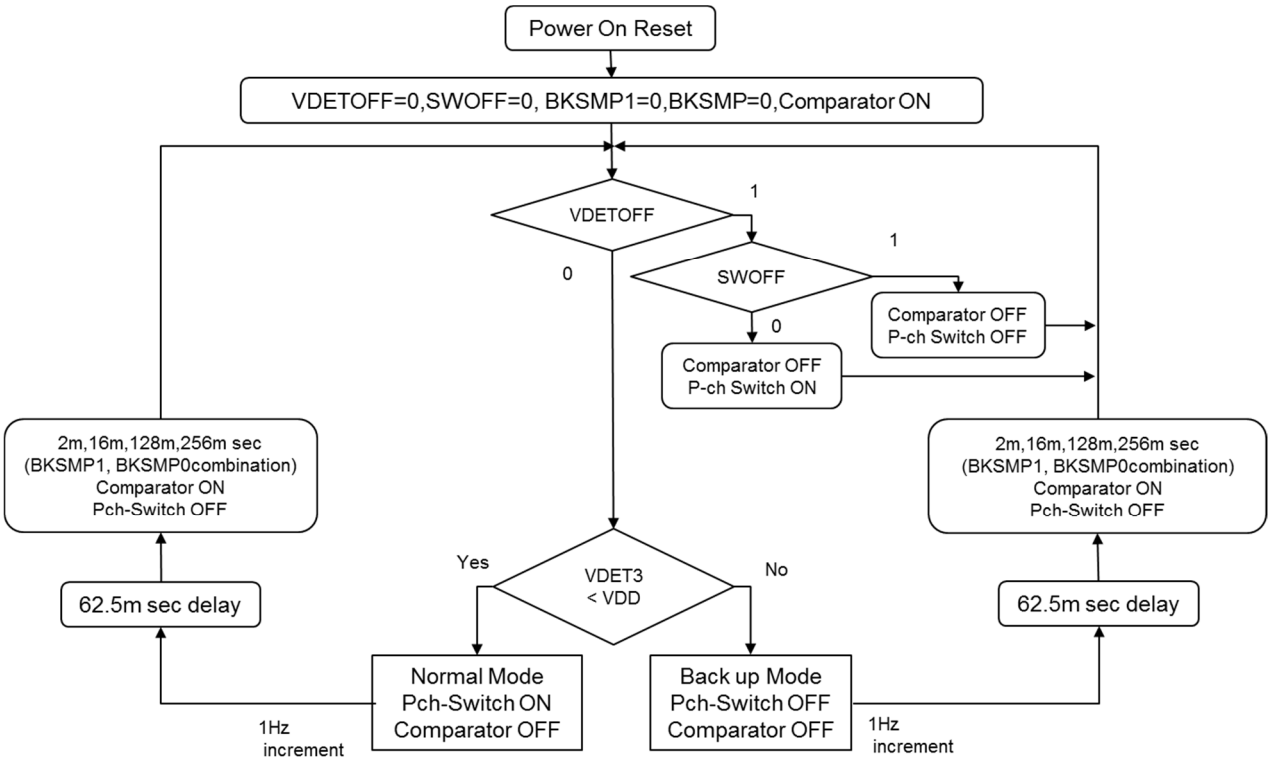


Figure 8-14. Mode flow of the backup power supply switchover function.

8.8.6. The pros and cons of detection period (2msec, 16msec,128msec and 256msec)

Since a VDD drop below VDET3 is only detected while the Pch-switch is open, user should carefully set the VDD detection period (by means of BKSMP0 and BKSMP1) to make sure the VDD voltage applied to the RTC VDD-pin falls below the VDET3 threshold during this time.

Table 8-55. The pros and cons of detection period setting.

Term	VDD voltage detection period		Remarks
	[2 ms] ~ [256 ms]		
Current consumption (Normal Mode)	small large		Longer detecting period increases VDD Detector current consumption.
Backup battery Charging effectiveness (Normal Mode)	Smaller detection period makes better charging effectiveness.		During detection period、Backup battery is charged through Diode.
Actual VDD voltage detecting period (Normal Mode)	Smaller detection period is better for slower VDD falling.	Longer detection period is better for prompt VDD falling.	Voltage detection is possible during detection period. (See Figure 8-16, Figure 8-17)

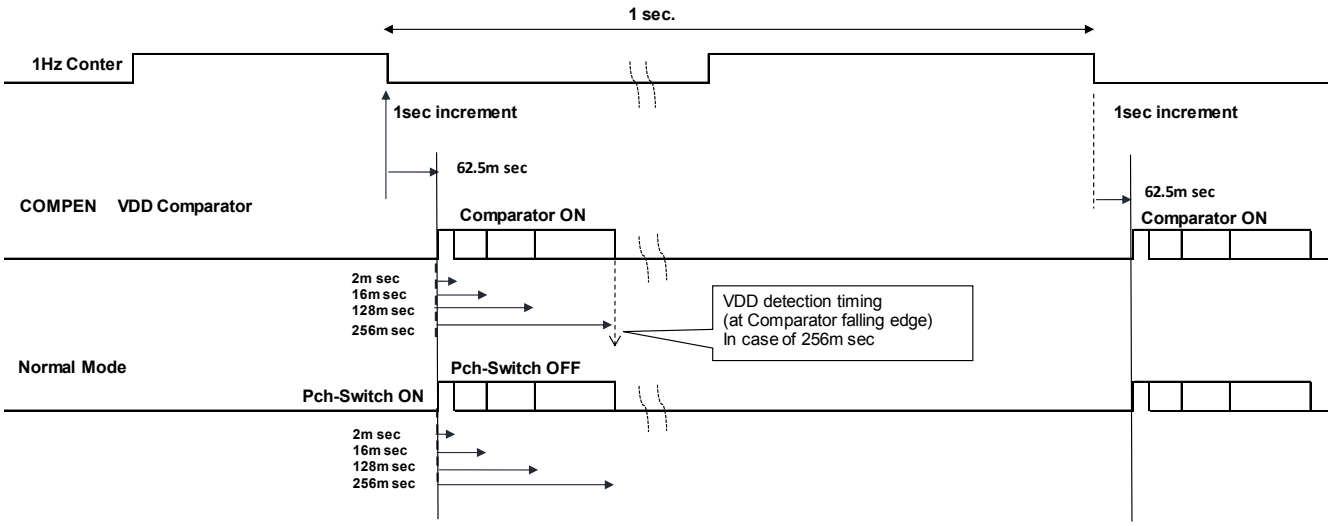


Figure 8-15. Timing chart of the battery backup power switchover function

If the voltage detection period is not set long enough by means of BKSMP0 and BKSMP1, a steep VDD voltage drop might not be detected and thus the backup power supply is discharged into VDD.
Between the voltage detection periods once per second, the Pch-switch is closed and thus the backup power supply discharges into VDD as well. To avoid this backup battery discharge, a diode might be set between VDD pin to power line. (See 8-8-7 Ex.4)

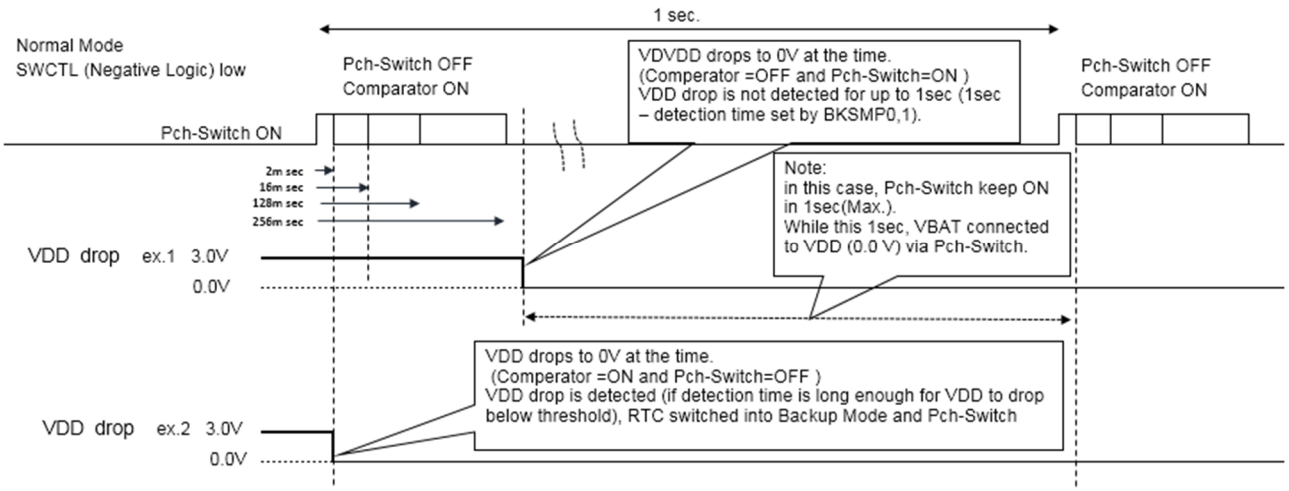


Figure 8-16. VDD drop detection 1

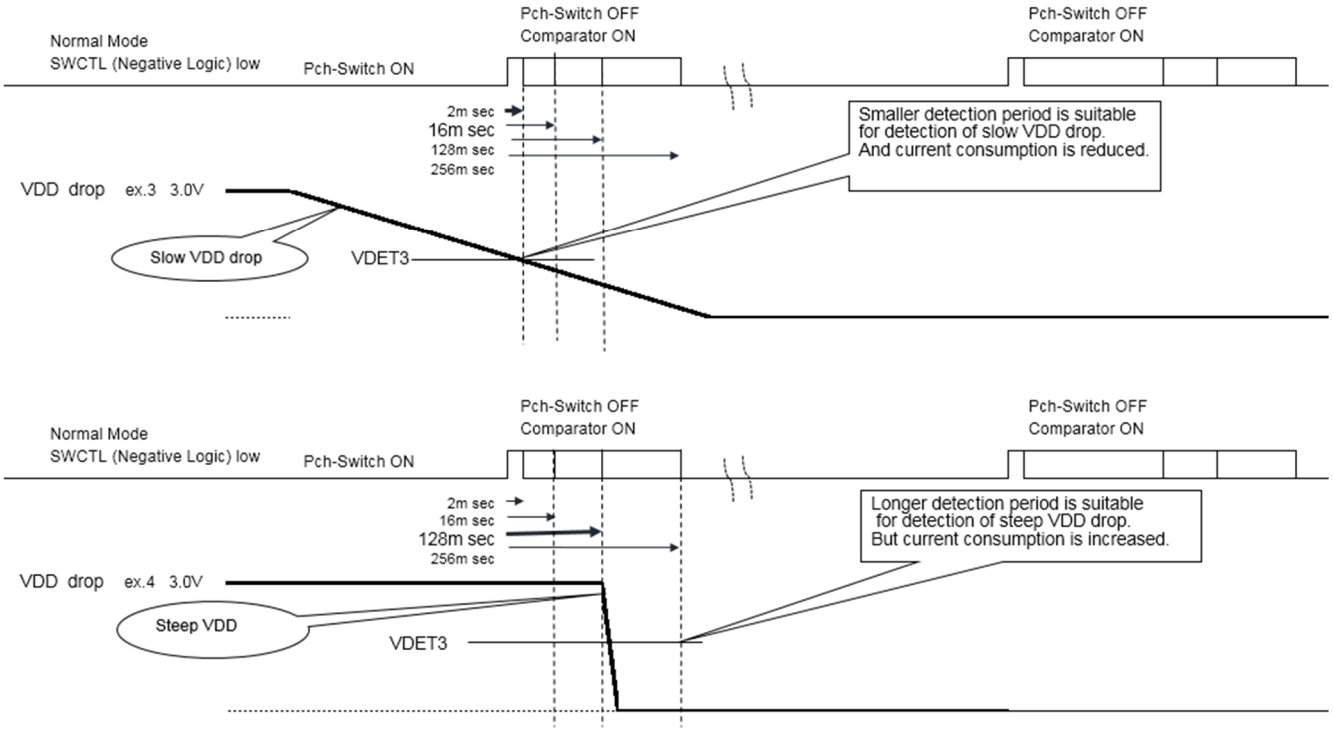


Figure 8-17. VDD drop detection 2

8.8.7 Connection examples

[Ex-1] Single power supply.

External supply should be connected to both VDD and VBAT.
In this case, interface (I2C, FOUT) are active in a supply voltage range from 1.6V to 5.5V anytime.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18h	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0
Data	0	0	0	0	1	X	X	X
Parts	X = Don't care. C = 0.1uF							

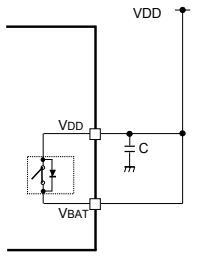


Figure 8-18. EX.1

Ex-2] Non- rechargeable battery. ex. CR2032, AAA-battery

When VDD shut to OFF,
Battery current is leak to VDD(0.0V) while 1sec(Max.).
Refer Figure 8-16.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18h	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0
Data	0	0	0	0	0	0	X	X
Parts	C = 0.1uF. R = 100ohm(Min.) D = Schottky Barrier type							

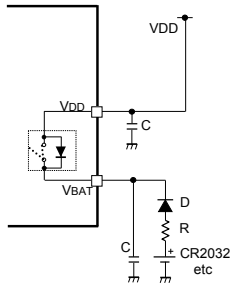


Figure 8-19. EX.2

[Ex-3] Rechargeable battery. ex. EDLC, ML-series

In this case the current limiting resistor on VBAT should be set to 100 Ohm.
Smaller resistor value brings over current to the RTC.
Bigger resistor value might make the supply voltage of the RTC to drop below VLOW or VDET at the time of power-switchover.
When a bigger higher resistor value is required to control the charging current to EDLC, or while 1sec(Max.), current leak into VDD(0.0V) from VBAT is so serious in system, it is recommended to use connection example Ex.4.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18h	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0
Data	0	0	0	0	0	0	X	X
Parts	C = 0.1uF. R = 100ohm(Min.) X = Don't care.							

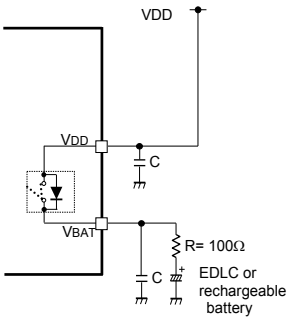


Figure 8-20. EX.3

[Ex-4] For using high value protection resistor.

This circuit is recommended in case a current flow for up to 1 sec from VBAT into VDD, before entering backup-mode is not acceptable or in case the current of the EDLC or rechargeable battery has to be limited to values which can't be assured with a R = 100 Ohm as recommended in Ex.3.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18h	○	○	○	○	VDET OFF	SWOFF	BKSMP1	BKSMP0
Data	0	0	0	0	1	0	X	X
Parts	C = 0.1uF. (Max.) R = 100ohm(Min.) to Free. D = Schottky Barrier type. X = Don't care							

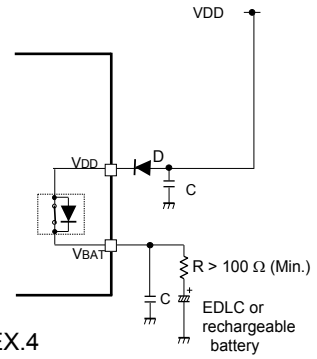


Figure 8-21. EX.4

8.8.8 Note: Diode characteristics.

For example.
In connection Example 2, VDD is 3.3V and CR2032 is 3.0V.
when VF of RTC's Diode is 0.6V, out of RTC's Diode is 2.7V.
and VF of outside Diode is 0.2V, VBAT voltage is 2.8V.
In this case, even if VDD is active, RTC use 2.8V from CR2032 anytime.
as a results, CR2032 life very shorten than an assumption.
In a choice of a diode, consider balance of the voltage carefully.

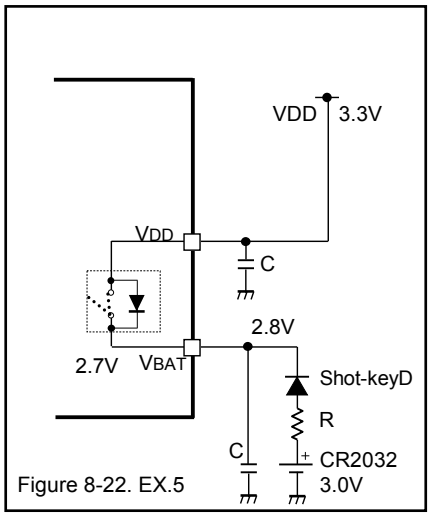


Figure 8-22. EX.5

Example of solution for above.
A Schottky diode(D2) is installed in a VDD side.
and RTC's diode is bypassed.
Therefore, voltage drop of VDD depends on only V/F of D2.
As a result, examination of simple circuitry is possible.

Example

it just Diode-OR-circuit
Confirm each of V/F characteristics carefully.

Address 18h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	○	○	○	○	VDET OFF	SWOFF	BKSMP 1	BKSMP0
Data	0	0	0	0	1	0	X	X

Parts

X Bit = Don't care.
C = 0.1uF.
R = 100Ω(Min.)
D1 & D2 = Schottky Barrier type.

To avoid a wasted leakage current.
When VDD is OFF, I/R characteristics of Diode(D2) is important.
Confirm IR characteristics of Diode with Temp characteristics.

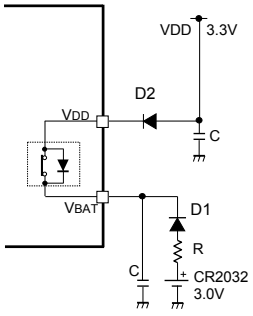


Figure 8-23. EX.6

8.9. Reading/Writing Data via the I2C Bus Interface

8.9.1. Overview of I2C-BUS

The I2C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at high level whenever communications are not being performed.
The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is output while the SCL line is at high level.
The I2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse.

8.9.2. System configuration

All ports connected to the I2C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.
SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).

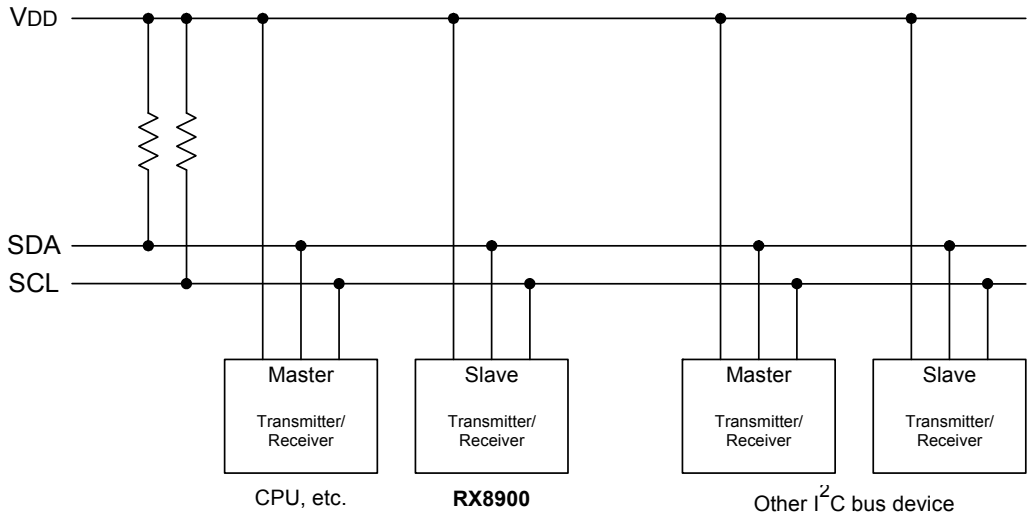


Figure 8-24. I2C bus connection.

Any device that controls the data transmission and data reception is defined as a "Master".
and any device that is controlled by a master device is defined as a “Slave”.
The device transmitting data is defined as a “Transmitter” and the device receiving data is defined as a receiver”

In the case of this RTC module, controllers such as a CPU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on these conditions.

8.9.3. Starting and stopping I²C bus communications

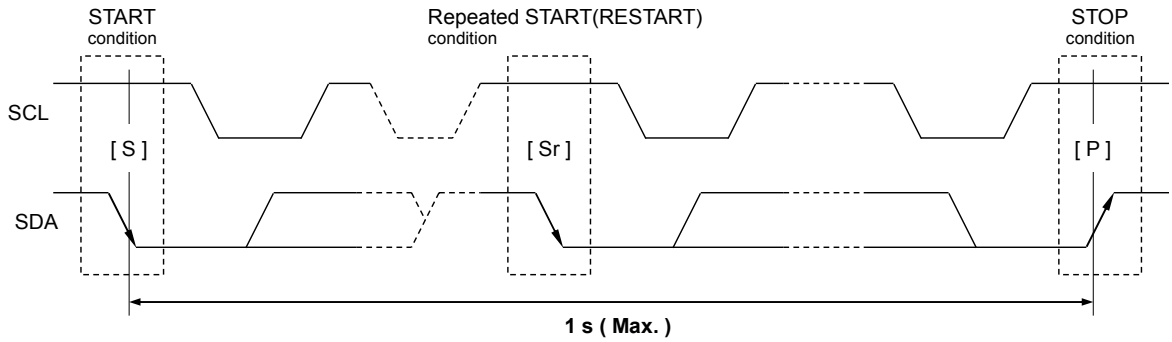


Figure 8-25. I2C bus START, RESRART timing.

1) START condition, repeated START condition, and STOP condition

(1) START condition
- The SDA level changes from high to low while SCL is at high level.

(2) STOP condition
- This condition regulates how communications on the I²C-BUS are terminated. The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)
- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Caution points

∗1) The master device always controls the START, RESTART, and STOP conditions for communications.

∗2) The master device does not impose any restrictions on the timing by which STOP conditions affect transmissions, so communications can be forcibly stopped at any time while in progress. (However, this is only when this RTC module is in receiver mode (data reception mode = SDA released).

∗3) When communicating with this RTC module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur **within 0.95 seconds**. (A RESTART condition may be sent between a START condition and STOP condition, but even in such cases the series of operations from transmitting the START condition to transmitting the STOP condition should still occur **within 0.95 seconds**.)

If this series of operations requires **0.95 seconds or longer,** the I²C bus interface will be automatically cleared and set to standby mode by this RTC module's bus timeout function. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. (When the read operation is invalid, all data that is read has a value of "1"). Restarting of communications begins with transfer of the START condition again

∗4) When communicating with this RTC module, wait **at least 1.3 µs (see the tBUF rule)** between transferring a STOP condition (to stop communications) and transferring the next START condition (to start the next round of communications).

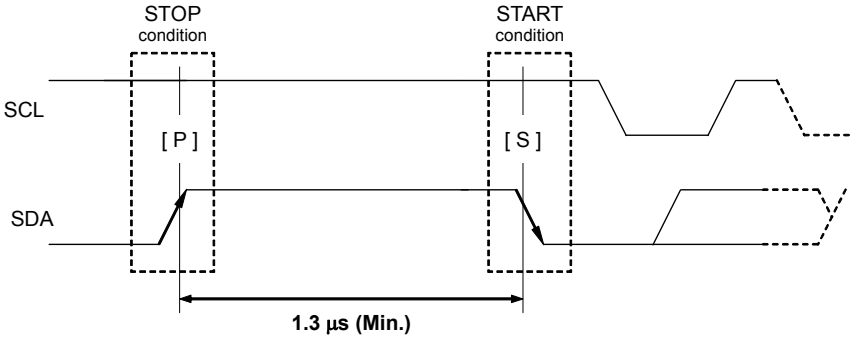


Figure 8-26. I2C bus START STOP condition

8.9.4. Data transfers and acknowledge responses during I²C-BUS communications

1) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition. (**However, the transfer time must be no longer than 0.95 seconds**.)

The address auto increment function operates during both write and read operations.
After address Fh, incrementation goes to address 0h.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) receives data while the SCL line is at high level.

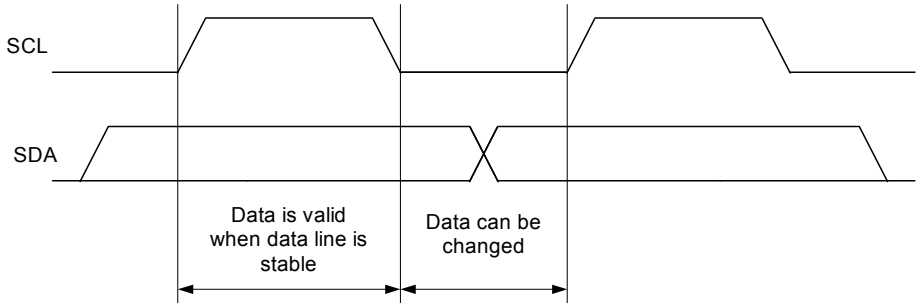


Figure 8-27. I2C bus data transfer

∗ Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

2) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.

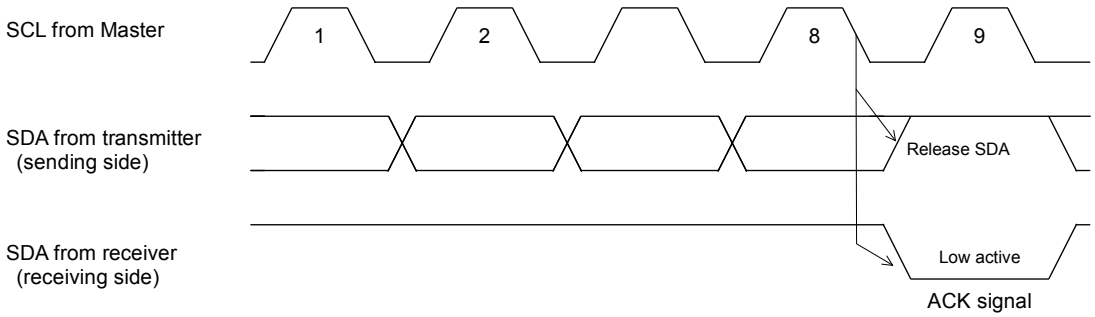


Figure 8-28. I2C bus data acknowledge response

After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

8.9.5. Slave address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. This RTC's slave address is **[0110 010∗]**.
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

Table 8-56. I2C Bus Slave address

	Transfer data	Slave address							R/W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	**65 h**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	1 (= Read)
Write	**64 h**								0 (= Write)

8.9.6 I2C bus protocol

In the following sequence descriptions, it is assumed that the CPU is the master and the RX8900 is the slave.

a. Address specification write sequence

Since the RX8900 includes an address auto increment function, once the initial address has been specified, the RX8900 increments (by one byte) the receive address each time data is transferred.

(1) CPU transfers start condition [S].
(2) CPU transmits the RX8900's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX8900.
(4) CPU transmits write address to RX8900.
(5) Check for ACK signal from RX8900.
(6) CPU transfers write data to the address specified at (4) above.
(7) Check for ACK signal from RX8900.
(8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
(9) CPU transfers stop condition [P].

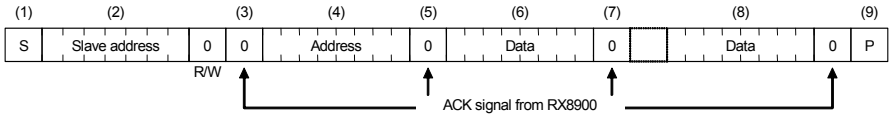


Figure 8-29. Address specification write sequence

b. Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

(1) CPU transfers start condition [S].
(2) CPU transmits the RX8900's slave address with the R/W bit set to write mode.
(3) Check for ACK signal from RX8900.
(4) CPU transfers address for reading from RX8900.
(5) Check for ACK signal from RX8900.
(6) CPU transfers RESTART condition [Sr] (in which case, CPU does not transfer a STOP condition [P]).
(7) CPU transfers RX8900's slave address with the R/W bit set to read mode.
(8) Check for ACK signal from RX8900
(from this point on, the CPU is the receiver and the RX8900 is the transmitter).
(9) Data from address specified at (4) above is output by the RX8900.
(10) CPU transfers ACK signal to RX8900.
(11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
(12) CPU transfers ACK signal for "1".
(13) CPU transfers stop condition [P].

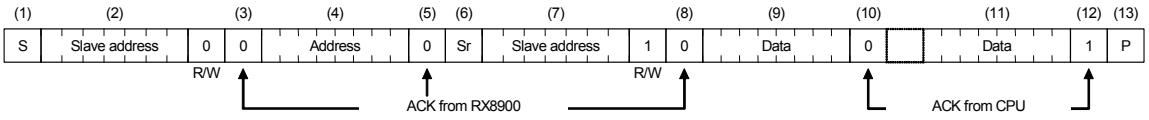


Figure 8-30. Address specification read sequence

c. Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

(1) CPU transfers start condition [S].
(2) CPU transmits the RX8900's slave address with the R/W bit set to read mode.
(3) Check for ACK signal from RX8900
(from this point on, the CPU is the receiver and the RX8900 is the transmitter).
(4) Data is output from the RX8900 to the address following the end of the previously accessed address.
(5) CPU transfers ACK signal to RX8900.
(6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the RX8900.
(7) CPU transfers ACK signal for "1".
(8) CPU transfers stop condition [P].

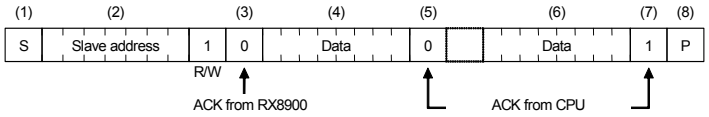


Figure 8-31. Read sequence when address is not specified

d. The address auto increment in Read/Write.
(1) In Basic time and calendar resister.
Address - - - - - - - 08 - 09 - 0A - 0B - 0C - 0D - 0E - 0F - 00 - 01 - 02 - -
(2) In Extension resister
Address - - - - - - - 18 - 19 - 1A - 1B - 1C - 1D - 1E - 1F - 10 - 11 - 12 - -

8.10. Backup and Recovery

*This circuit is sensitive to power supply noise and supply voltage should be stabilized to avoid negative impact on the accuracy.
* tR1 is needed for a proper power-on reset. If this power-on condition cannot be kept, it is necessary to send an initialization routine to the RTC by software.
*In case of repeated ON/OFF of the power supply within short term, it is possible that the power-on reset becomes unstable.
After power-OFF, keep VDD=VBAT=GND for more than 10 seconds for a proper power-on reset.
When Power-on-reset is uncertainty, system can initialize the RTC by the software.
* When a controller goes to shutdown, a CPU sent STOP condition to RTC, then that I2C communication is complete status is recommended.

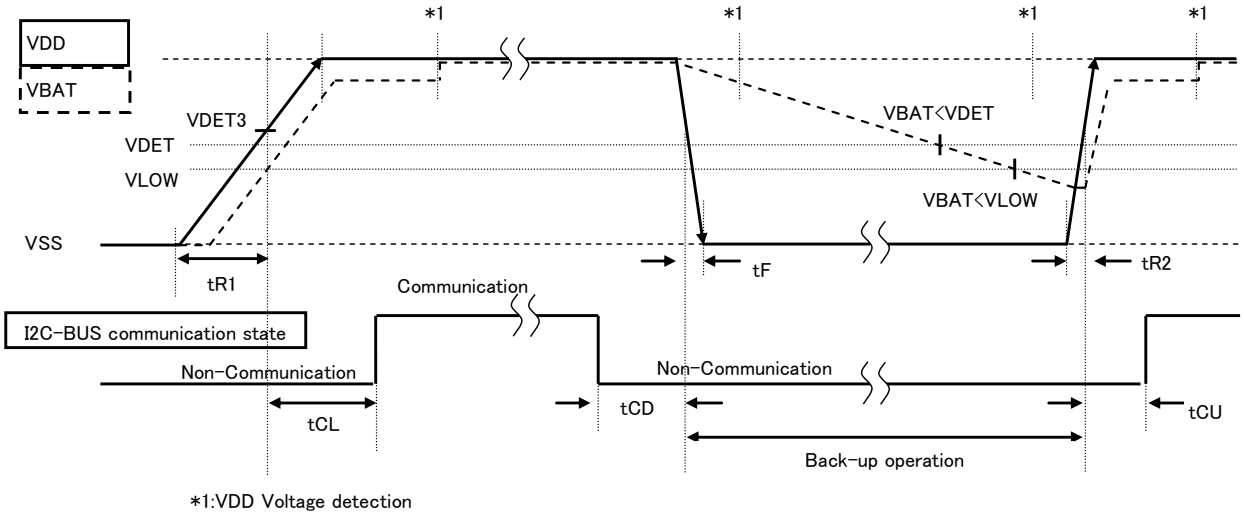


Figure 8-32. VDD power supply sequence

Table 8-57. Power supply, detection voltage

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.
Detection voltage (1) VDET-bit threshold	VDET	-	1.9	1.95	2.0	V
Detection voltage (2) VLF-bit threshold	VLOW	-	1.16	-	1.6	V
Detection voltage (3) Backup-switchover voltage	VDET3	-	2.3	2.4	2.5	V
Power supply rise time1	tR1	VDD=VSS to 2.5V	1	-	10	ms / V
Access wait time (After initial power on)	tCL	After VDD=2.5V	30	-	-	ms
Access disable hold time	tCD	After stop condition	0	-	-	μs / V
Power supply fall time	tF	VDD=2.5V to VSS	2	-	-	μs / V
Power supply rise time2	tR2	VDD=VSS to 2.5V	15	-	-	μs / V
Access wait time (Normal power on)	tCU	After VDD=2.5V	0	-	-	μs

* : tR2 is specifications for an oscillation not to stop. Some clocks are not output by an FOUT terminal.

8.11. The note of access to RTC at the time of backup return and initial power supply

Because most of RTC registers are synchronized with the oscillation clock of the built-in crystal oscillator, the RTC does not work normally without the integrated oscillator having stabilized.
1) The first, System should confirm status of VLF-bit.
2) When VLF is "1", system must initialize all of registers.
3) When initial-power-ON was given to RTC, wait for tSTA(3seconds) for setup of time and Calendar.
But readout access is permitted after 30ms from VDD=VCLK.

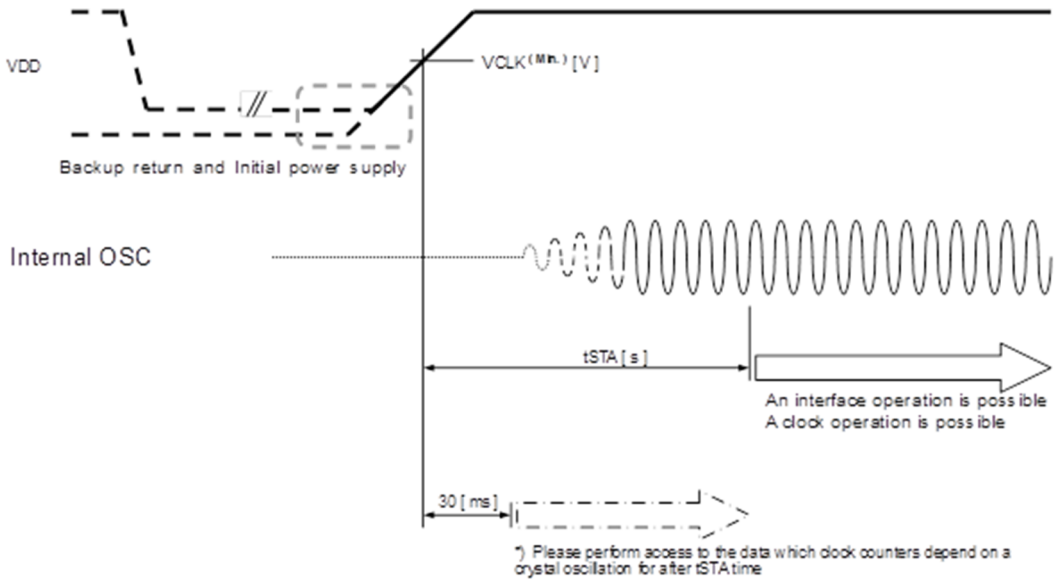


Figure 8-33 Oscillation starting sequence.

8.12. Flow chart

The following flow-chart is one example, but it is not necessarily applicable for every use-case and not necessarily the most effective process for individual applications.

1) An example of the initialization

Ex.1 Initialize

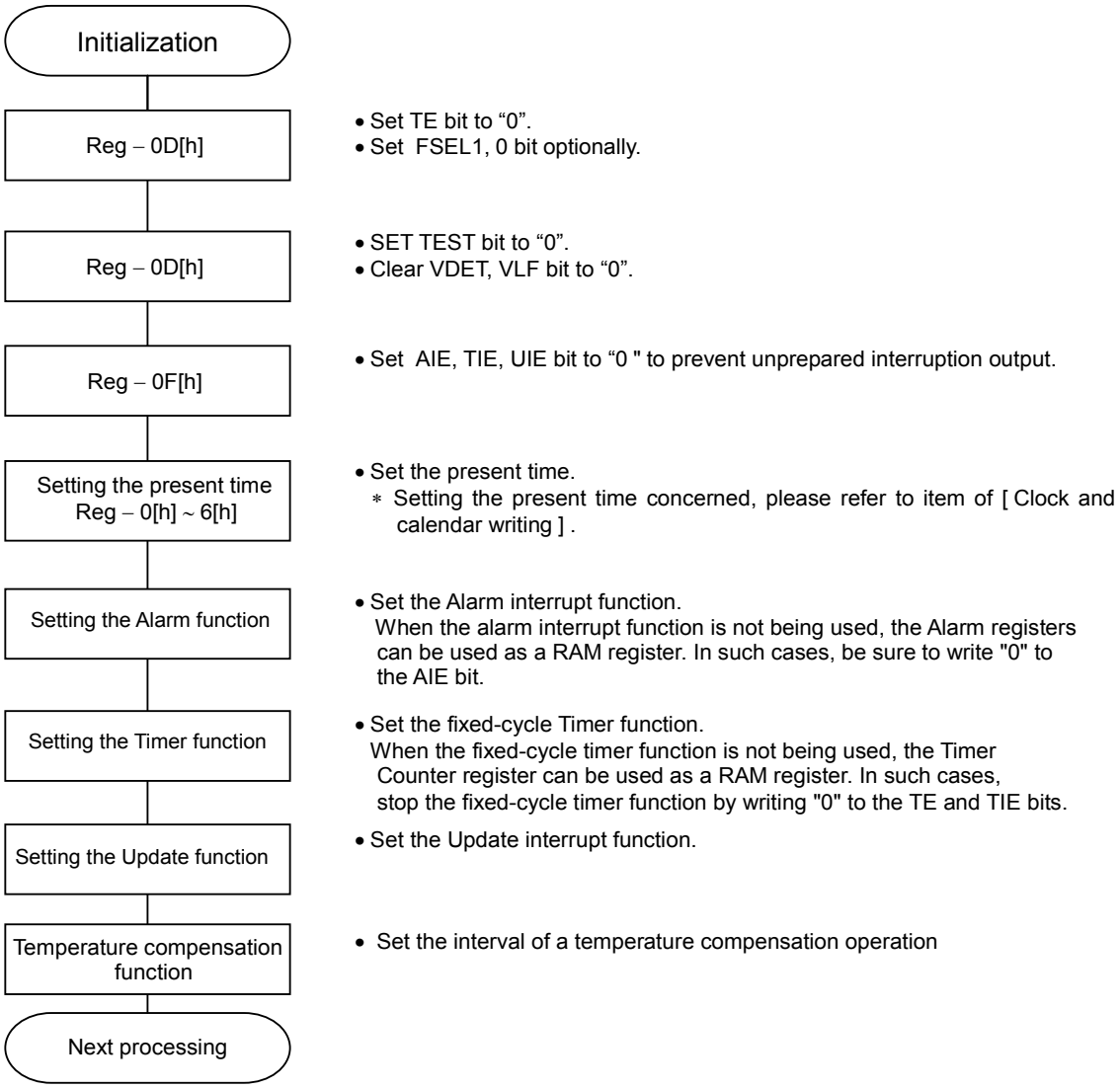


Figure 8-34. An example of the initialization

2) Method of initialization after starting of internal oscillation (VLF stays “0”)

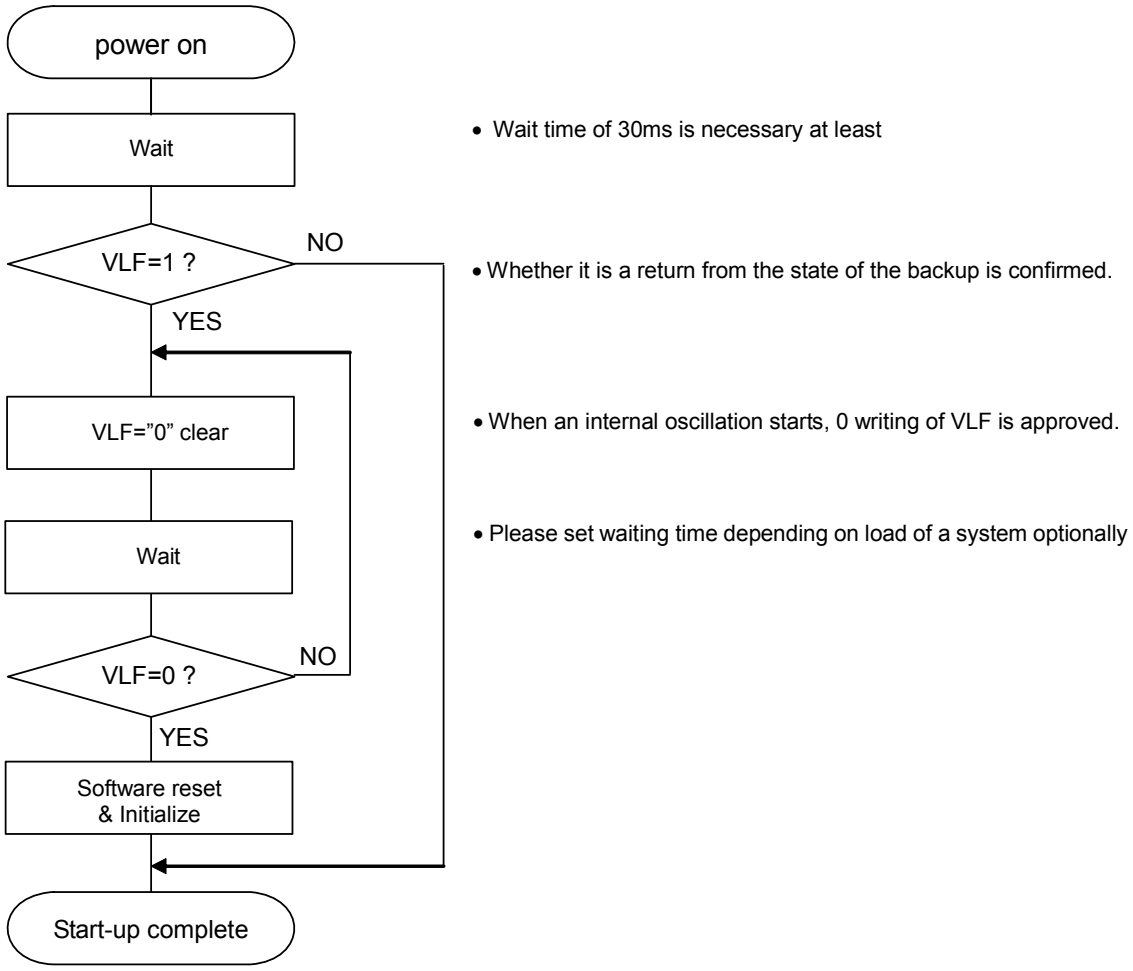
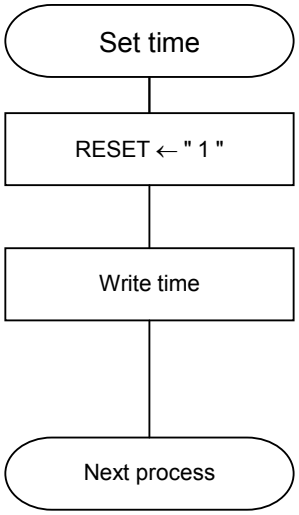


Figure 8-35. Method of initialization after starting of internal oscillation (VLF stays “0”)

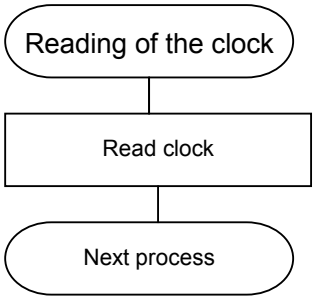
3) The setting of the clock and calendar



- Set RESET bit to “1” to prevent timer update in time setting.
- Write information of [year / month /date [day of the week] hour: minute: second] which is necessary to set (or reset). In case of initialization, please initialize all data.
- Please complete access within 0.95 seconds

Figure 8-36. The setting of the clock and calendar

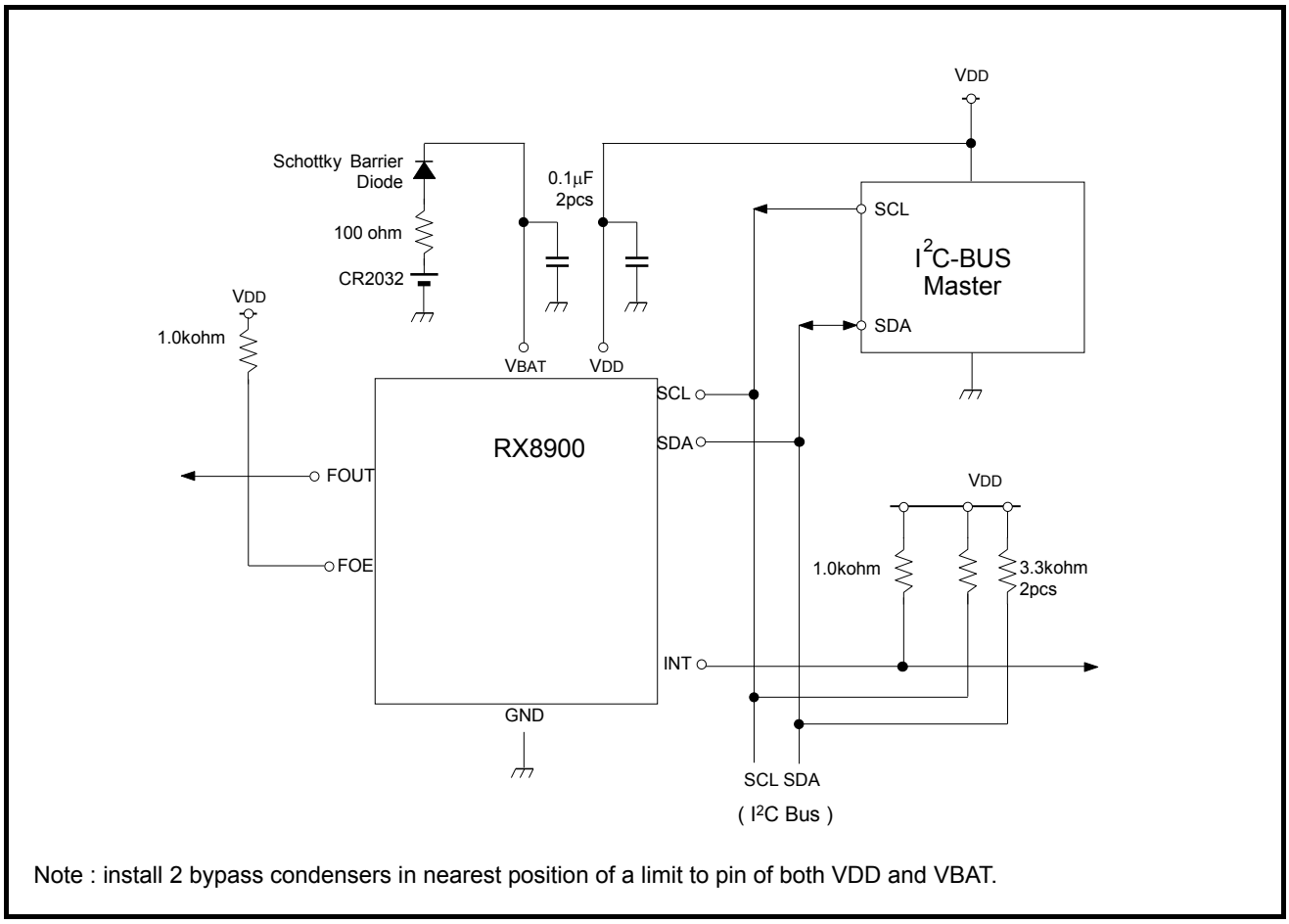
4) The reading of the clock and calendar



- Please complete access within 0.95 seconds
- At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end.
- The access to a clock calendar recommends to have access to continuation by a auto increment function.

Figure 8-37. The reading of the clock and calendar

8.13. Connection example with Typical Microcontroller



Note : install 2 bypass condensers in nearest position of a limit to pin of both VDD and VBAT.

Figure 8-38. Connection example with Typical Microcontroller

8.14. Connection RTC used as a clock source (32 kHz-TCXO)

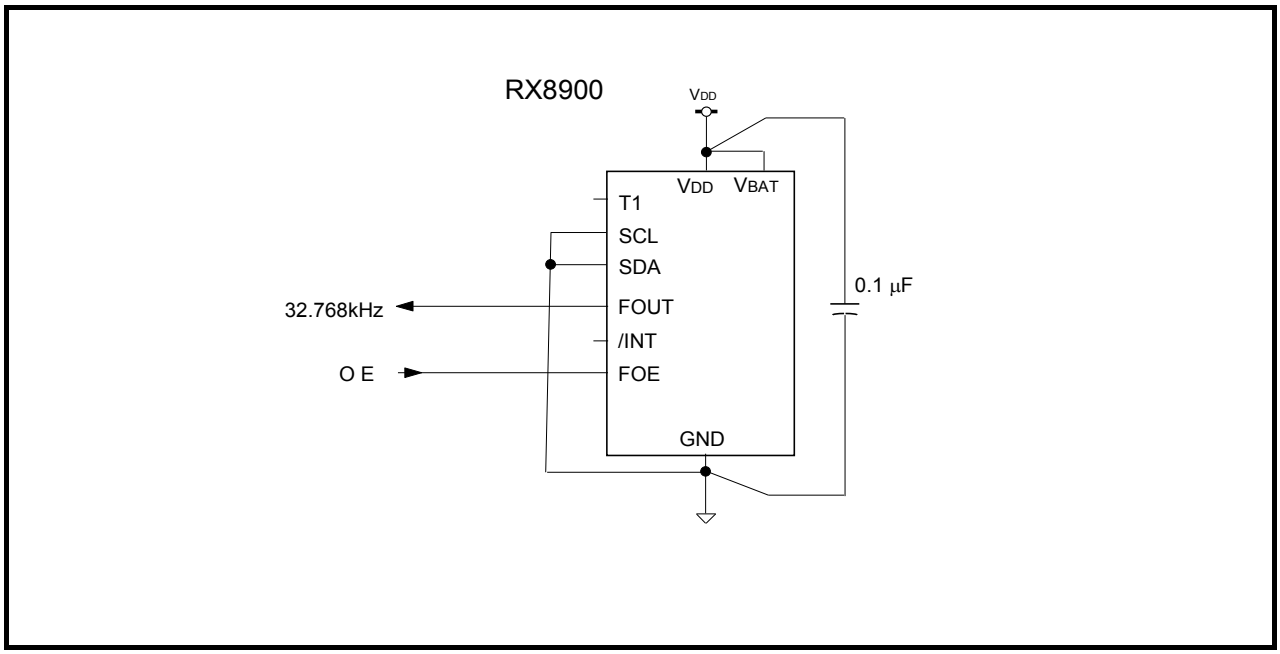


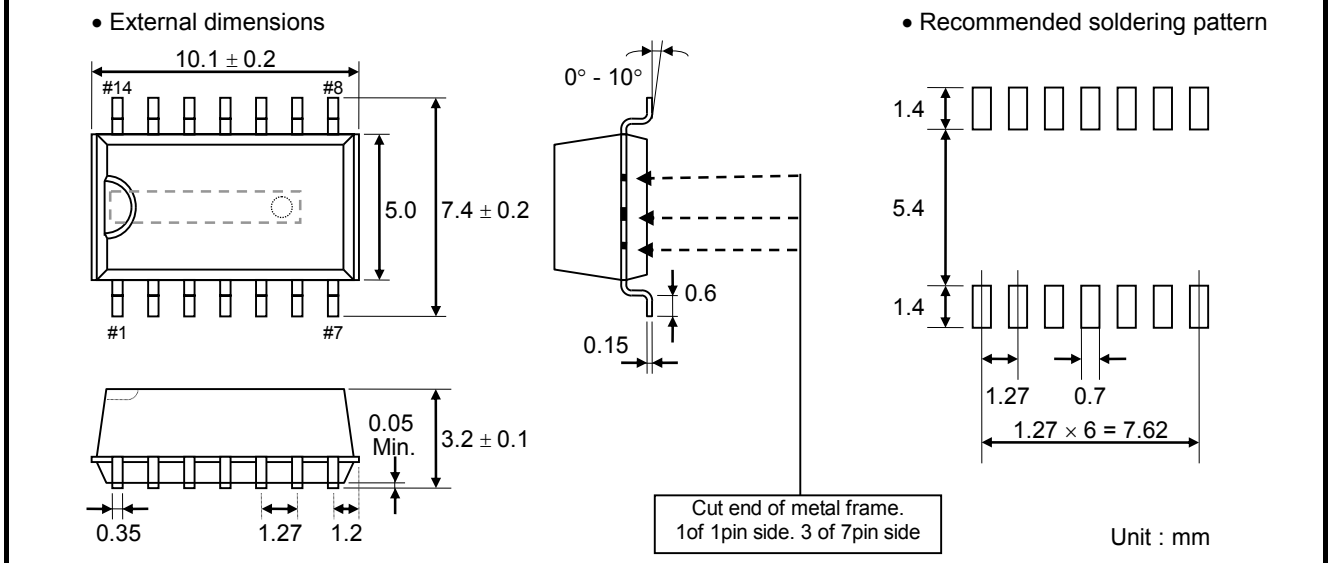
Figure 8-39. Connection RTC used as a clock source (32 kHz-TCXO)

9. External Dimensions / Marking Layout

9.1. RX8900SA

9.1.1. External dimensions

RX8900SA (SOP – 14pin)

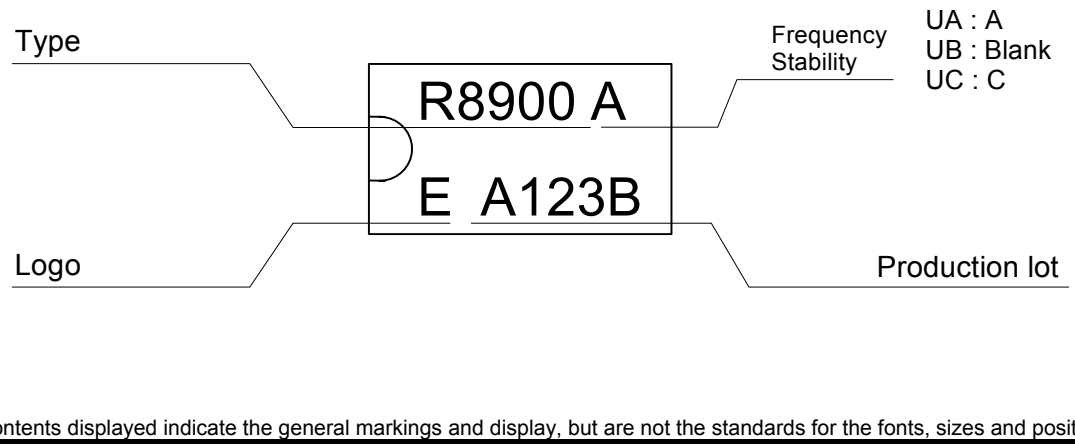


∗ The cylinder of the crystal oscillator can be seen in this area (front) but it has no effect on the performance of the device.
In the short side of package, some small cut end of metal frame appears. these cut ends are connected to inside circuit of crystal oscillator. Don't touch anything to these cut ends. it has risk of crystal stop.

Figure 9-1. RX8900SA package

9.1.2. Marking layout

RX8900SA (SOP – 14pin)



∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

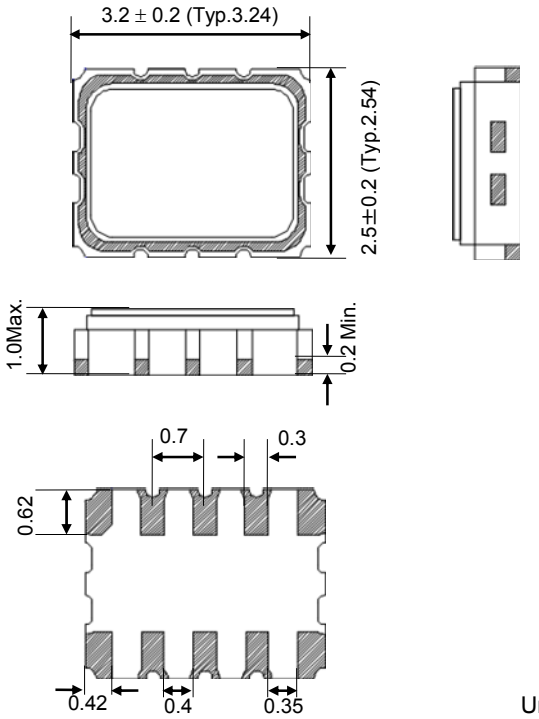
Figure 9-2. RX8900SA Marking layout

9.2. RX8900CE

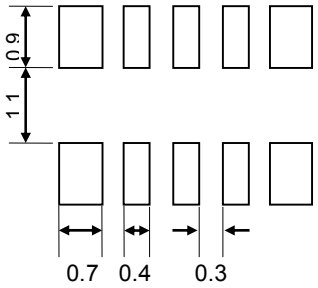
9.2.1. External dimensions

RX8900CE

• External dimensions



• Recommended soldering pattern



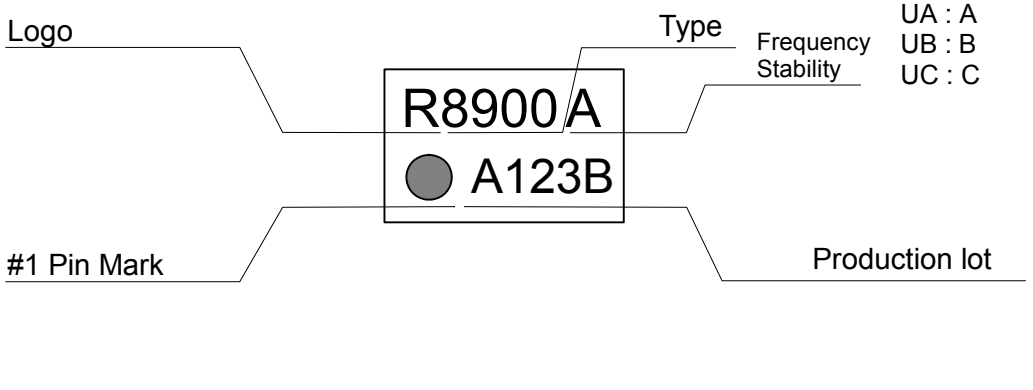
Unit : mm

The small metal pads on the short side of the ceramic package are used to test the crystal.
When assembling the part, please be careful not to connect or short circuit this pad.
In addition, please avoid short circuit between these metal parts by dew condensation or particle adhesion.

Figure 9-3. RX8900CE package

9.2.2. Marking layout

RX8900CE



∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

Figure 9-4. RX8900CE Marking layout

10 Application Notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity
While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise
If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.
* Do not layout signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins
When the mid-voltage(near to 50% of VDD) is applied to input-pins, it may occur the current increase, decrease of the margin of noise, and invites a error of functions. should apply near voltage of VDD or GND.

(4) Handling of unused pins
Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, please apply the voltage level to near of VDD or GND.

(5) Installation of charged battery.
When a charged backup battery is installed by soldering, battery connection terminal of RTC should connect to GND, beforehand.

2) Notes on packaging

(1) Soldering heat resistance.
If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.
* See Fig. 2 profile for our evaluation of Soldering heat resistance for reference.

(2) Mounting equipment
While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning
Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation
This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins
Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

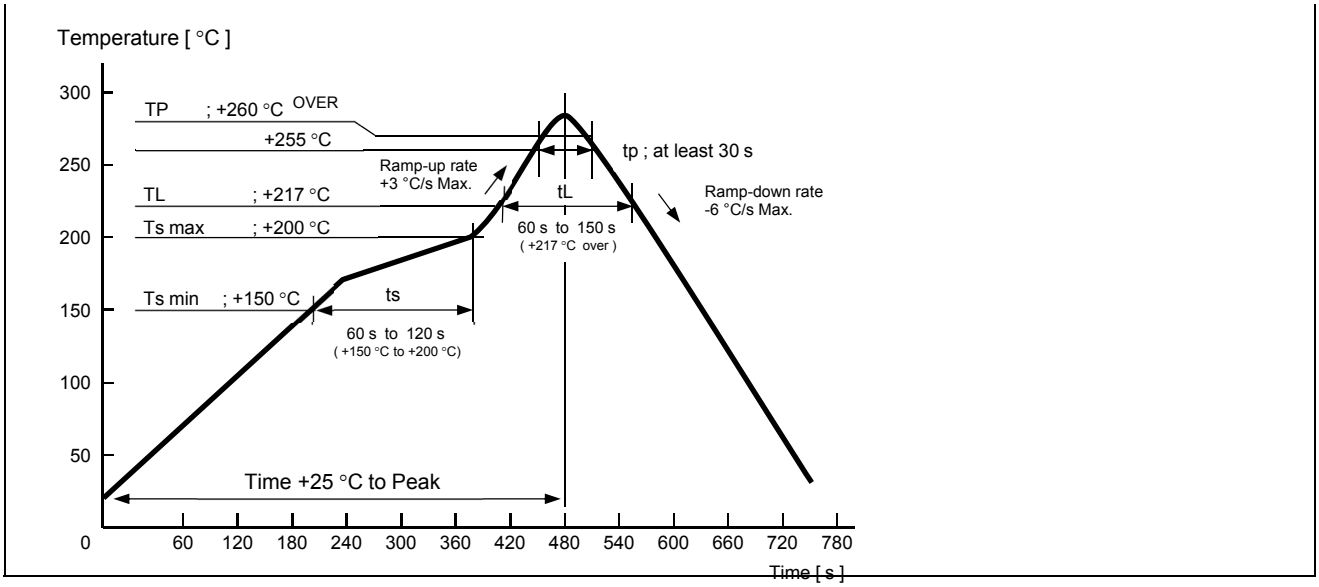


Figure 12-1. Reference profile for

11. Tables

12. Figures

Application Manual

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Distributor

Electronic devices information on WWW server

www5.epsondevice.com/en/

MICRO DEVICES

Click to add text

Product Configuration Guide

Product Configuration System

Real Time Clock Modules – I²C-Bus

RA-8581SA : B 0 : PURE SN

Base Model	Pkg.	Status
RA-8581SA	SOP 14 PIN	Discontinued
RTC-8564JE	VSOJ 20 PIN	Active
RTC-8564NB	SON 22 PIN	Active
RX8010SJ	SOP 8 PIN	Active
RA4803SA RA8803SA	SOP 14 PIN SOP 14 PIN	Active
RX8900SA RA8900SA	SOP 14 PIN	Active
RX8900CE RA8900CE	3.2x2.5mm 10 PIN Ceramic	Active

Frequency Tolerance:	
RA-8581SA	B=5+/-23PPM
RTC-8564JE	B=5+/-23PPM
RTC-8564NB	B=5+/-23PPM
RX8010SA	B=5+/-23PPM
RX4803SA and RX8803SA	UA= +/-3.4PPM -40°C to 85°C UB= +/-5.0PPM -40°C to 85°C UC=+/- 5PPM -30°C to 70°C AA=5+/-5PPM 25°C
RX8900SA RA8900SA and RX8900CE RX8900CE	UA=+/-3.4PPM -40°C to 85°C UB=+/-5PPM -40°C to 85°C UC=+/-5PPM -30°C to 70°C

Tape & Reel Qty
SOP Package Type Only
B: Bulk
0: 1000 pcs. per reel
3: 250 pcs. per reel

Blank : CE Package
RX8010SJ: PURE SN
RA4803SA: PURE SN
RX8803SA: PURE SN
RX8900SA: PURE SN
RA-8581SA: ROHS or PURE SN
RTC-8564JE: ROHS
RTC-8564NB: ROHS or PURE SN

Note:
Model P/N in RED font = DISCONTINUED

EPSON