Technology Development

of Infineon's automotive Power MOSFETs

About this document

Scope and purpose

This document provides a historical summary about Infineon's technology development of automotive power MOSFETs.

Intended audience

This document is intended for engineers designing automotive applications.

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1 Introduction

Power semiconductors are not only used in newer battery electric driven cars but have always been required in a broad spectrum of automotive applications. Beside IGBTs and wide bandgap switches the power MOSFETs play an important role in a wide variety of systems in the group of controllable power semiconductors.

Power MOSFETs are needed in many body power applications. Typical examples are DC/AC inverters for driving the motors of oil, fuel or water pumps, for window lifters or seat belt pretensioners, whereas DC/DC converters are needed for light systems. Electric breaking, electric power steering and vehicle stability control systems use MOSFETs to drive the actuators in the chassis segment. All applications mentioned are independent of the used drive train of the car. They operate with combustion engines as well as in battery driven cars.

The transition from combustion engines to battery electric vehicles expands the demand for MOSFETs in applications that ensure the power distribution. A high voltage to low voltage DCDC converter supplies the low voltage domain of an electric vehicle and ensures the isolation between the high voltage battery and the low voltage domain, usually 12V DC. The MOSFETs operate in highly efficient circuits on the primary (high voltage MOSFETs) as well as on the secondary side in rectifier circuits (low voltage MOSFETs) of the DCDC converter. Specific thermal management systems are required to ensure full performance of other systems under all possible environmental conditions. Therefore, MOSFETs also are required to drive additional loads such as blowers, fans and pumps in an electric vehicle as well.

Infineon as a leading manufacturer for automotive power semiconductors provides a broad portfolio of high power MOSFETs to fulfill the individual requirements of all above mentioned applications. Constantly changing requirements to the MOSFETs caused by the evolution of the system needs in a modern car, and new applications resulting from transition from the combustion engine to battery electric vehicles, are influencing the development of Infineon's MOSFET technologies in the last few decades. In order to perfectly match the application requirements, the development of MOSFET technologies cover both, frontend, e.g. wafer and backend, e.g. package technologies.

This document gives a concise but comprehensive overview of Infineon's automotive MOSFET technologies and describes the driving factors behind the technology evolution.

For more information please visit our dedicated Infineon automotive MOSFET website [1].

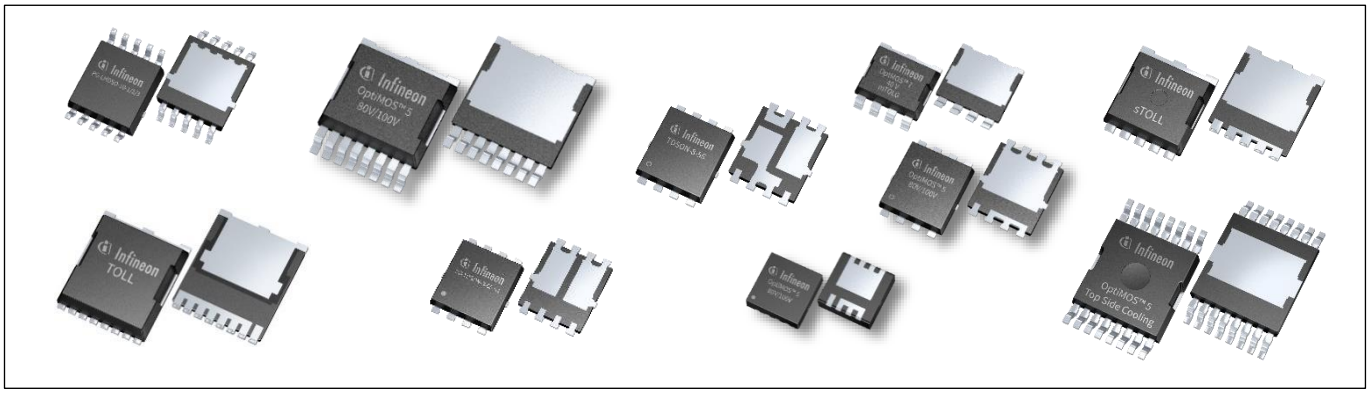


Figure 1 Automotive High Power MOSFETs from Infineon

2 Technology Roadmap

An overview about the different MOSFET technologies introduced by Infineon over the last two decades is given in Figure 2. The graph covers n-channel MOSFET technologies with Infineon's first OptiMOS™ technology and ends with the latest OptiMOS™-7 technology.

In 2015 Infineon acquired International Rectifier (IR) increasing its portfolio of high power MOSFETs for automotive applications. The second path with legacy IR technologies is shown at the bottom of Figure 2.

There are technologies older than Infineon's OptiMOS technology, but MOSFETs based on these technologies are discontinued for new project designs and therefore beyond the scope of this paper. Likewise, the relatively small portion of p-channel MOSFET is not included in Figure 2 although Infineon provides p-Channel MOSFETs in different voltage classes and package types. Furthermore, the timeline depicts released technologies only. Of course, Infineon will continue to develop and release new technologies to the market extending its MOSFET portfolio to provide products that are fitting the constantly evolving requirements of automotive applications.

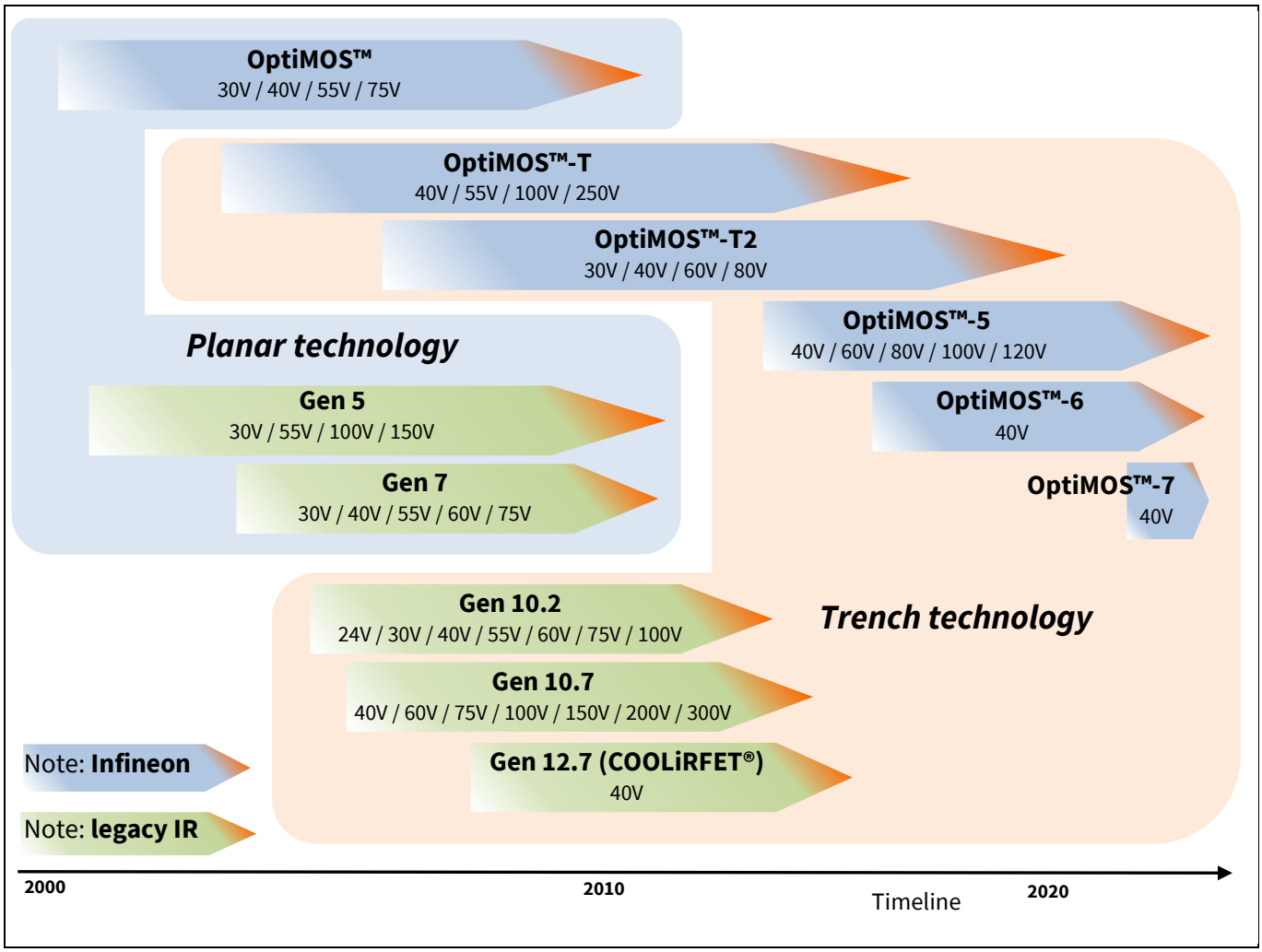


Figure 2 High Power MOSFET Technology evolution for automotive MOSFETs

Typical power MOSFETs are characterized by their vertical current flow. Source and Gate are located on top side of the die and connected via bond wires and/or copper-clips to the leads. The Drain is on the bottom side of the die and connected to the lead frame by solder die attach or conductive glue. The MOSFET and its contacts are encapsulated by mold compound forming the package. Applying a positive potential between Gate and Source (n-channel MOSFET) creates a conducting channel between Drain and Source.

Older power MOSFET technologies are based on a planar cell concept. Figure 3 shows a cross section of Infineon's OptiMOS planar cell. To achieve the desired $R_{DS(on)}$ of the MOSFET many of these individual cells are connected in parallel to form the active area of the die. In the MOSFET on-state, current flows from Drain through the substrate n^+, the epitaxial area n^-, the JFET area between the p-doped regions and finally through the channel region in horizontal direction underneath the planar designed gate of the cell to the Source metallization. Each single cell region contributes its portion to the overall Drain-to-Source on-state resistance. The lower n^- doped epitaxial layer is needed to achieve the required electric breakdown voltage of the MOSFET. As an example, a thicker epitaxial layer with lower doping will increase the breakdown voltage but also significantly increase resistance contribution to the overall on-state resistance from the R_{EPI} of this layer.

As mentioned previously, to achieve the desired $R_{DS(on)}$ of the MOSFET many of these individual cells are connected in parallel to form the active area of the die. For the final product the package resistance contributions from bond wires or copper clips, lead frame and leads have to be considered as well. Due to process constraints for electric contacts and a minimum length requirement for the channel for a robust device the cell structure cannot be shrunk arbitrarily below a dimensional limit.

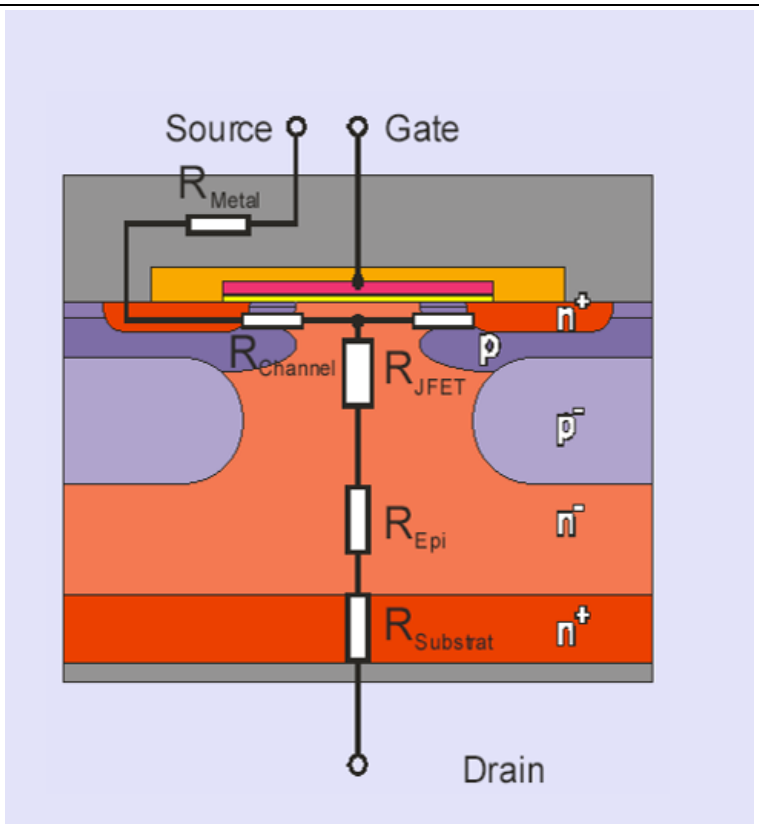


Figure 3 Planar MOSFET cell (OptiMOS™)

To overcome these space constraints of the planar MOSFET, the channel region can be transferred to a vertical design forming a trench MOSFET, see Figure 4 (a). The channel orientation changes from lateral to vertical along the walls of the trench. With this cell topology the resistive contribution of R_{JFET} between the p^- regions underneath the gate pad is eliminated. The trench cell requires significantly less surface area while maintaining the requirement for the gate length. As a result the cell pitch is smaller and more cells can be paralleled on the same area and a lower $R_{DS(on)}$ can be realized. The portions of resistance coming from metallization areas on top and bottom of the die and the resistive portion of epitaxial and substrate layer are not affected by transition from planar to trench technology.

Figure 4 (b) shows the cross section of the next evolution step, the field plate trench concept. The cell architecture is characterized by a trench reaching deep into the epitaxial layer, in an extreme realization all the way into the substrate layer. The trench is coated with an insulating oxide layer and then filled with a conductive material (typically doped poly silicon) which is connected to the gate. The structure acts like a field plate giving the concept its name. If a reverse bias is applied to the structure, the field plate will push out free charges in the n^- region. The great benefit of this construction is that for the same breakdown voltage the doping of the n^- epitaxial layer can be significantly increased, thus reducing the resistance R_{EPI}. The benefit of the field plate is so large that the area requirement of the trench, which is not contributing to the current flow, is by far overcompensated by the reduction of R_{EPI}. The first Infineon technology using the field plate trench was the 55V OptiMOS™-T technology.

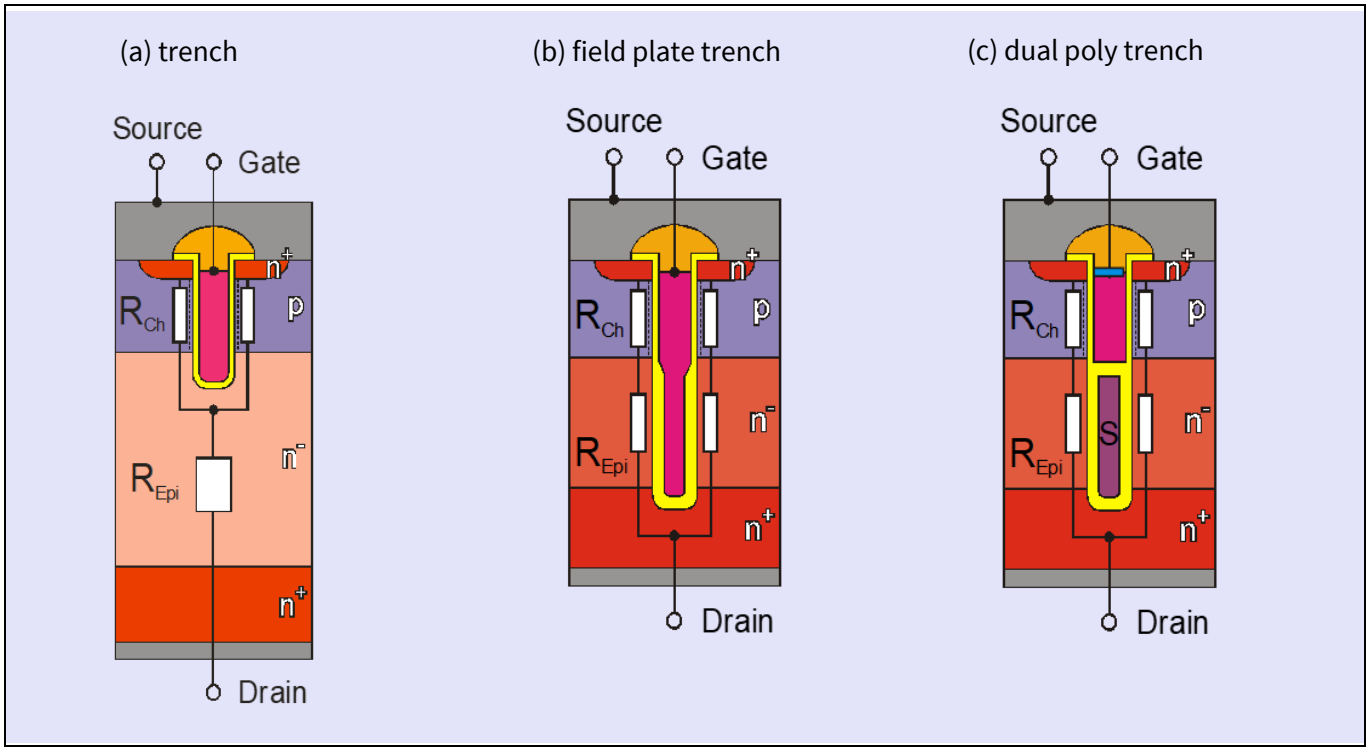


Figure 4 Technologies for trench MOSFET

The extended trench depth of the field plate concept however leads to a significant drawback. The built- in Gate-to-Drain capacitance C_{rss}, also referred as Miller capacitance, increases significantly limiting the potential use of such switches in applications requiring higher switching speed and/or frequencies (such as DCDC converters). To overcome this problem the next evolutionary step splits the poly inside the trench into two isolated parts. The lower part of trench poly is connected to the Source potential, whereas the upper part is connected to the Gate.

By this measure the capacitance between Gate and Drain becomes very small again, enabling the MOSFET for applications requiring high switching speed. Figure 4 (c) shows cross section of the dual poly trench concept. The OptiMOS™-T2 and all following technologies use the dual poly concept.

3 Technology Driver

The development of new MOSFET technologies is driven by the ever-increasing demands of the broad spectrum of automotive applications for higher power density and, above all, cost optimization. Thereby the evolution of new MOSFET products covers new semiconductor technology nodes but includes also the design and development of new packages.

Each technology generation enables smaller die sizes for the same Drain-to-Source on-state resistance $R_{DS(on)}$. This also means that the use of the same die size in a new generation results in a significant reduction of lowest achievable $R_{DS(on)}$. Figure 5 shows the reduction of the specific Drain-to-Source on-state resistance $R_{DS(on)}$*A from technology OptiMOS™ to OptiMOS™-7 (for 40V normal level MOSFETs). The values in the diagram are normalized with respect to the OptiMOS technology.

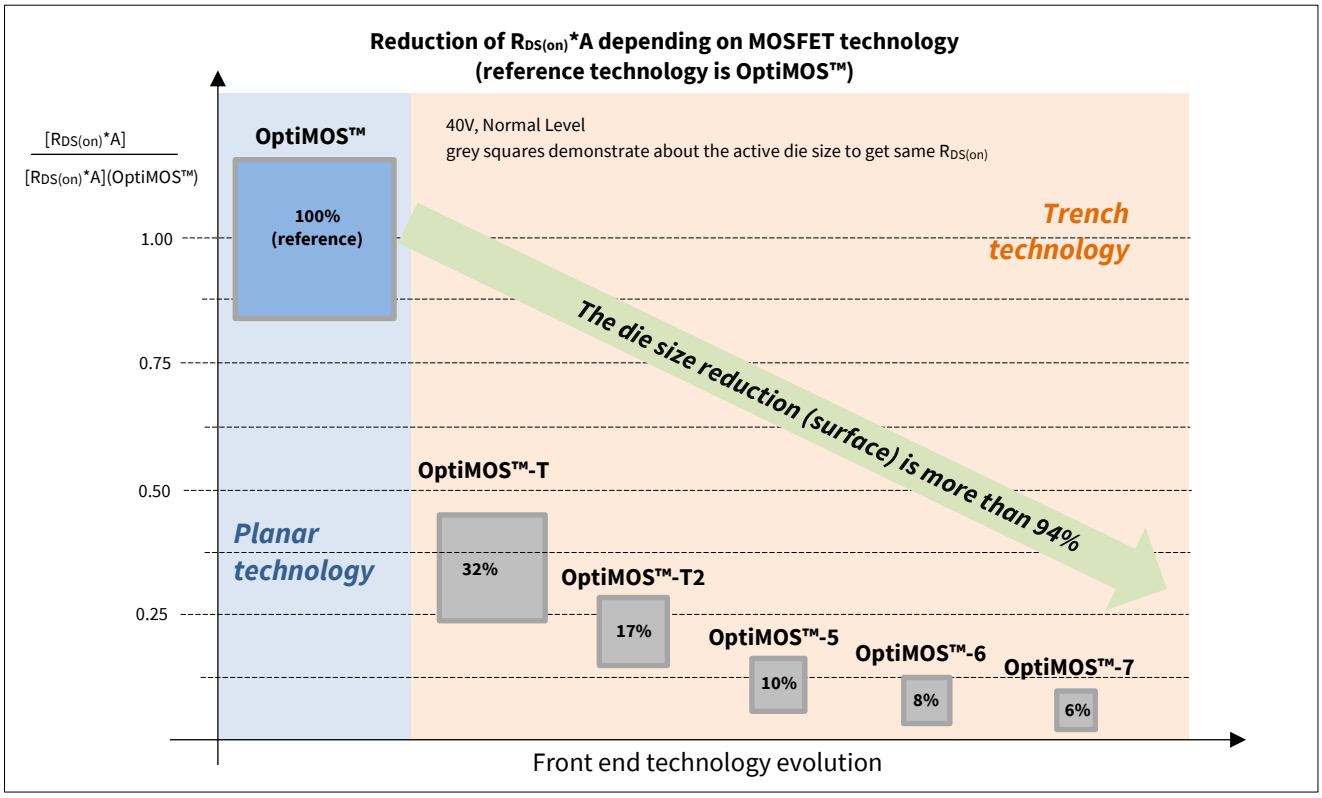


Figure 5 Reduction of $R_{DS(on)}$*A

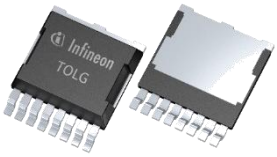
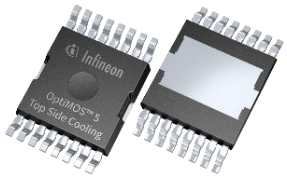
The improved $R_{DS(on)}$ of each new MOSFETs generation offers various advantages. On the one hand there is the possibility to increase the output power of an application in a given factor because the overall power losses can be reduced by using lower $R_{DS(on)}$ products in same package. On the other hand, it is possible to realize the same performance but in a more compact form factor by smaller packages. The associated cost savings on application level are the main driver for the development of new MOSFET technologies.

It must be mentioned that the development of new package types is inextricably linked to the development of new frontend technologies to optimize the performance of the die. The higher current densities possible in each new generation drive the development of new interconnect techniques as the link to the PCB. Thicker bond wires extend the current limits from the package pins to the silicon. As current densities for the latest MOSFET

technology generations become more than 10A/mm^2 bond wires are replaced by copper clips. The required special metallization schemes enable a soldered interconnect of the clip to the die.

Specific package families are designed for specific application requirements. Standard TO-leadless packages are very compact and are available in different package sizes. Due to the exposed pad on bottom side, the heat dissipation to a connected cooling system is excellent. The leadless design allows lowest possible package resistance and significant reduction of parasitic inductances. Variants offering two MOSFETs in one package support applications with critical space. Half-bridge package allows an EMC optimized board layout especially in low power motor applications. Leaded packages supplement the leadless packages portfolio, in cases where an extraordinary second level reliability is required due to extreme mismatches in Coefficient of Thermal Expansion (CTE) or PCB bending. The flexible leads reduce the thermo-mechanical stress of the solder joints between MOSFET pins and PCB. Top-side cooled packages provide the (exposed) drain pad on the top side of the package. A heat sink can be attached using an isolating thermal interface material (TIM) directly to the drain pad. Top side cooled packages are a perfect choice if superior thermal performance is required. The Table 1 gives an overview of Infineon's modern package portfolio.

Table 1 Modern MOSFET package types

Name	description
PG-HSOF-8 	10mm x 12mm TO leadless package, 8 terminals, exposed paddle
PG-HSOG-8 	10mm x 12mm TO leaded package, 8 terminals, exposed paddle
PG-HDSOP-16 	10mm x 15mm TO leaded package, 16 terminals, exposed paddle, top side cooled
PG-HSOG-4 	8mm x 8mm TO leaded package, 4 terminals, exposed paddle
PG-HSOF-5 	7mm x 8mm TO leadless package, 5 terminals, exposed paddle
PG-TDSON-8 	5mm x 6mm TO leadless package, 8 terminals, exposed paddle
PG-LHDSO-10 	5mm x 7mm TO leaded package, 10 terminals, exposed paddle, top side cooled
PG-TDSON-8 dual 	5mm x 6mm TO leadless package, 8 terminals, exposed paddles, dual configuration
PG-TDSON-8 half-bridge 	5mm x 6mm TO leadless package, 8 terminals, exposed paddles, half- bridge configuration
PG-TSDSON-8 	3.3mm x 3.3mm TO leadless package, 8 terminals, exposed paddle

4 MOSFET Parameter Comparison

The easiest way to compare the behavior of different MOSFET technologies in an application is looking at products with comparable $R_{DS(on)}$ ratings. Table 2 gives an overview on the MOSFET types selected for this exercise. In case a MOSFET with the exact same $R_{DS(on)}$ rating was not available the nearest product was chosen.

Table 2 MOSFETs for parameter comparison

Type	Technology	Package	$R_{DS(on)}$ max. [mΩ]
IPB180N04S3-02	OptiMOS™-T	PG-TO263-7-3	1.5
IPB160N04S4-H1	OptiMOS™-T2	PG-TO263-7-3	1.6
IAUA120N04S5N014	OptiMOS™-5	PG-HSOF-5-2	1.4
IAUC100N04S6N015	OptiMOS™-6	PG-TDSON-8	1.5
IAUCN04S7N015	OptiMOS™-7	PG-TDSON	1.5

Figure 6 shows an overview of key parameters of MOSFETs in different technology generations. In the following chapters we will have a detailed look at the individual parameters based on the MOSFETs selected in table 2.

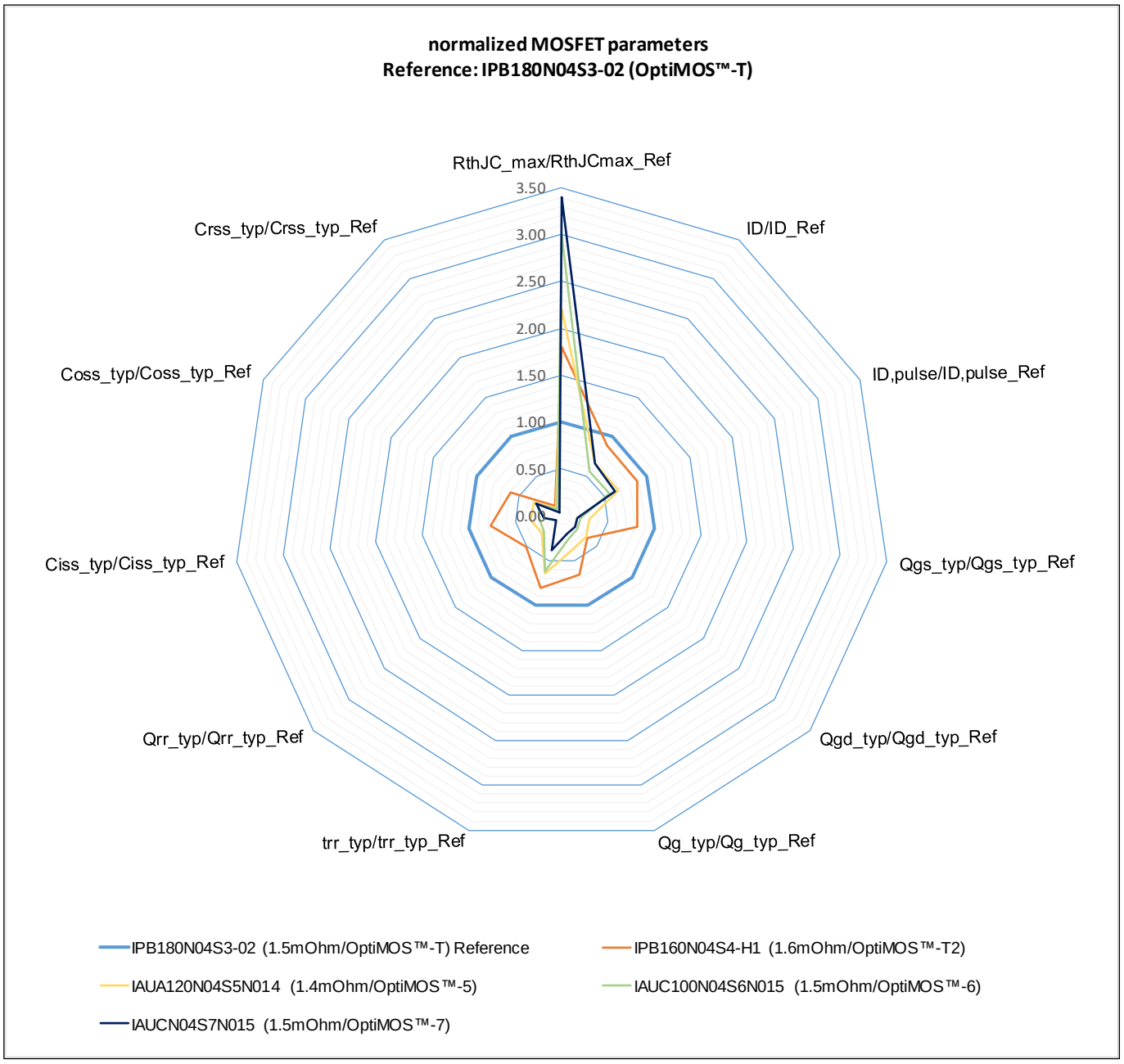


Figure 6 Normalized parameters of MOSFETs[1]

[1] OptiMOS™-7: capacitances C_{iss}, C_{oss}, C_{rss}: condition V_{DS}=25V (differs from data sheet condition); charge Q_{gs}, Q_{gd}, Q_g: condition V_{DD}=32V (differs from data sheet condition) ⇨ conditions changed to have the same conditions for all MOSFET technologies

4.1 Chip Size

The reduction of the die size while maintaining the same drain-source on-state resistance $R_{DS(on)}$ is clearly visible, the die size from OptiMOS-T to OptiMOS7 is reduced to nearly a seventh of the original size. Accordingly, the use of smaller packages for the newer technologies becomes feasible. While the OptiMOS™-T and OptiMOS™-T2 MOSFETs are implemented in a 7-pin D2PAK package (PG-TO263, footprint size on PCB about 174mm^2), the OptiMOS™-5 MOSFET is equipped in a leadless sTOLL package (PG-HSOF-5, footprint size about 65mm^2) and the OptiMOS™-6 or OptiMOS™-7 device is offered in the leadless SS08 package (PG-TDSON-8, footprint size on PCB about 34mm^2). The potential for more compact application designs is obvious.

Table 3 Normalized die size

Type	Technology	Normalized die size (Reference OptiMOS™-T)
IPB180N04S3-02	OptiMOS™-T	100%
IPB160N04S4-H1	OptiMOS™-T2	50%
IAUA120N04S5N014	OptiMOS™-5	29%
IAUC100N04S6N015	OptiMOS™-6	22%
IAUCN04S7N015	OptiMOS™-7	15%

4.2 Thermal Resistance

The benefit of smaller dies in smaller packages however comes at a price. The thermal resistance of a MOSFET is directly linked to its die and package size. Heat is generated at the junction at the top of the MOSFET die. The most efficient path for heat transfer is through the silicon die, into the coper leadframe, then into the Printed Circuit Board (PCB) and thermal management system (i.e. heat sink). Smaller packages decrease the efficiency of heat transfer from the MOSFET to the PCB. Likewise, the capability to prevent junction temperatures above the allowed maximum limit resulting from transient events with high power losses like short circuit, inrush events or linear operation within SOA (see below) is reduced. This behavior is also reflected in higher values of the transient thermal impedance. Note however that this is only an indirect result of the different frontend technologies due to the changed dimensions of the die and the package. Figure 7 shows the thermal resistance R_{thJC} of the 5 MOSFET devices, Figure 8 shows the maximum thermal impedance of the largest die/package in comparison to the smallest one. As expected, the larger OptiMOS™-T product in the huge TO263 footprint dissipates heat power losses more efficient than the small outline of the OptiMOS™-6 MOSFET in the TDSON-8 footprint. The impact of using a newer MOSFET technology with a smaller die or package must be evaluated by the designer and if necessary, the thermal management system of the application (i.e. PCB layer stack up, thermal vias, heat sink) may need to be adjusted. It is important to note that reduction in thermal resistance of the MOSFET is typically fairly small when compared to the contribution of the thermal management system and the loss of thermal performance can be compensated if one selects a device with a slightly lower $R_{DS(on)}$ resulting in lower power losses.

The thermal resistance and thermal impedance affect several other MOSFET parameters as well, which the developer of an application has to consider when choosing the best fitting device for his specific application. Typical examples of such parameters are the continuous and pulsed drain current (I_D, I_{D_pulse}) and the power dissipation (P_{tot}). In case of continuous operation the complete system influences the capability to dissipate the power losses from MOSFET to ambient. In this case, the thermal resistance from case to ambient (containing PCB, heat sink, cooling system etc.) has significant importance for the selection of the best fitting MOSFET for the specific application requirements. See Figure 7 below. The thermal impedance Z_{thJC} also plays an important role in the assessment of pulse conditions which lead to high power losses at the MOSFET junction (short circuit, inrush current of a motor, avalanche etc.). Under such conditions the designer must ensure that the MOSFET operates within the allowed limits regarding junction temperature because the heat generated by the power losses in the die can't be transferred fast enough out of the MOSFET. See Figure 8 below.

For more information about thermal resistance see [2].

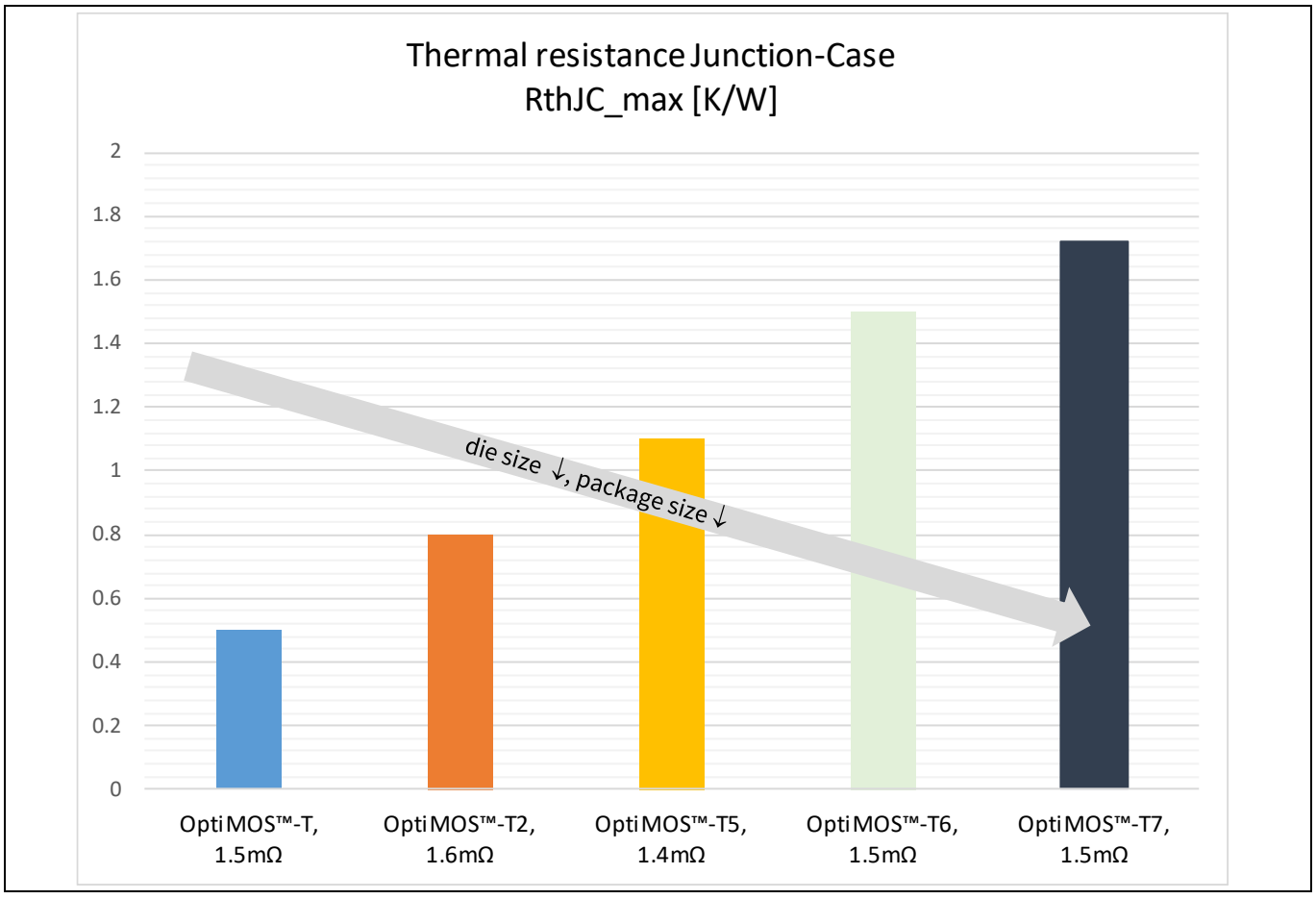


Figure 7 Maximum thermal resistance, junction-case R_{thJC} (maximum data sheet value)

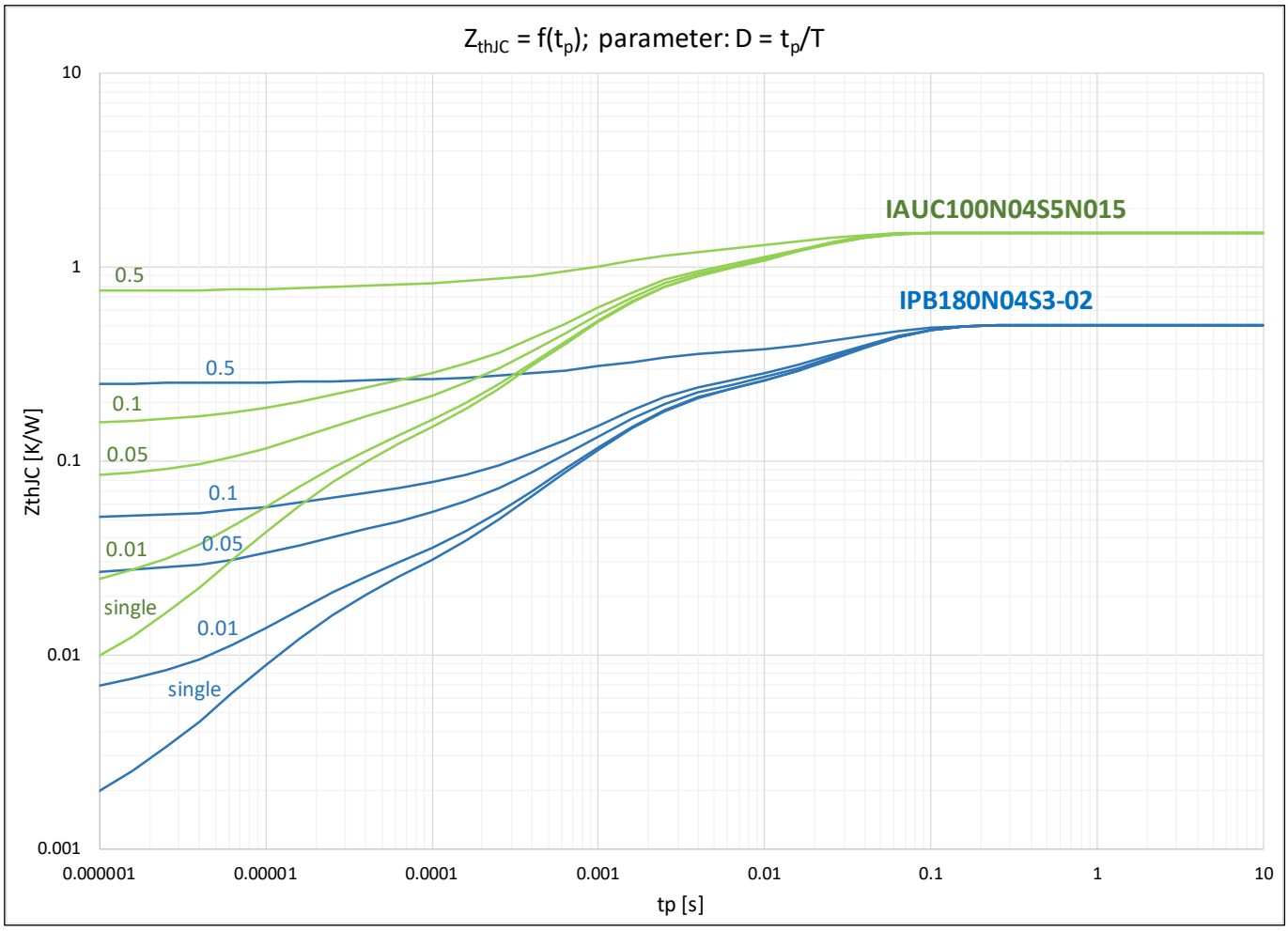


Figure 8 Maximum transient thermal impedance Z_{thJC} (IPB180N04S3-02 versus IAUC100N04S6N015)

4.3 Safe Operating Area

Figure 9 compares the SOA performance of OptiMOS™-T and OptiMOS™-6 MOSFETs. The impact of the different frontend technology and package is clearly visible. The linear rise of the SOA in section (A) is limited by on-state resistance $R_{DS(on)}$ and the voltage drop V_{DS} simply the result I_D* $R_{DS(on)}$.

The $R_{DS(on)}$ limit ends at the maximum pulse current limit (B). Up to OptiMOS™-T this limit is defined by 4 times the nominal current, e.g. 720A for OptiMOS™-T and 400A for OptiMOS™-6. This limitation was in part due to the package construction which used Aluminum bond wires for the source connection. Recent investigations have shown that for new packages that use copper clips for the source connection (OptiMOS™-5 and later) the maximum power is only limited by the maximum junction temperature T_{j_max}.

This limit is represented by section (C). As the maximum junction temperature may not exceed 175°C the maximum current can directly be calculated using the Z_{th} diagram, the required pulse length and drain voltage. Thus, the slope of this region is -1.

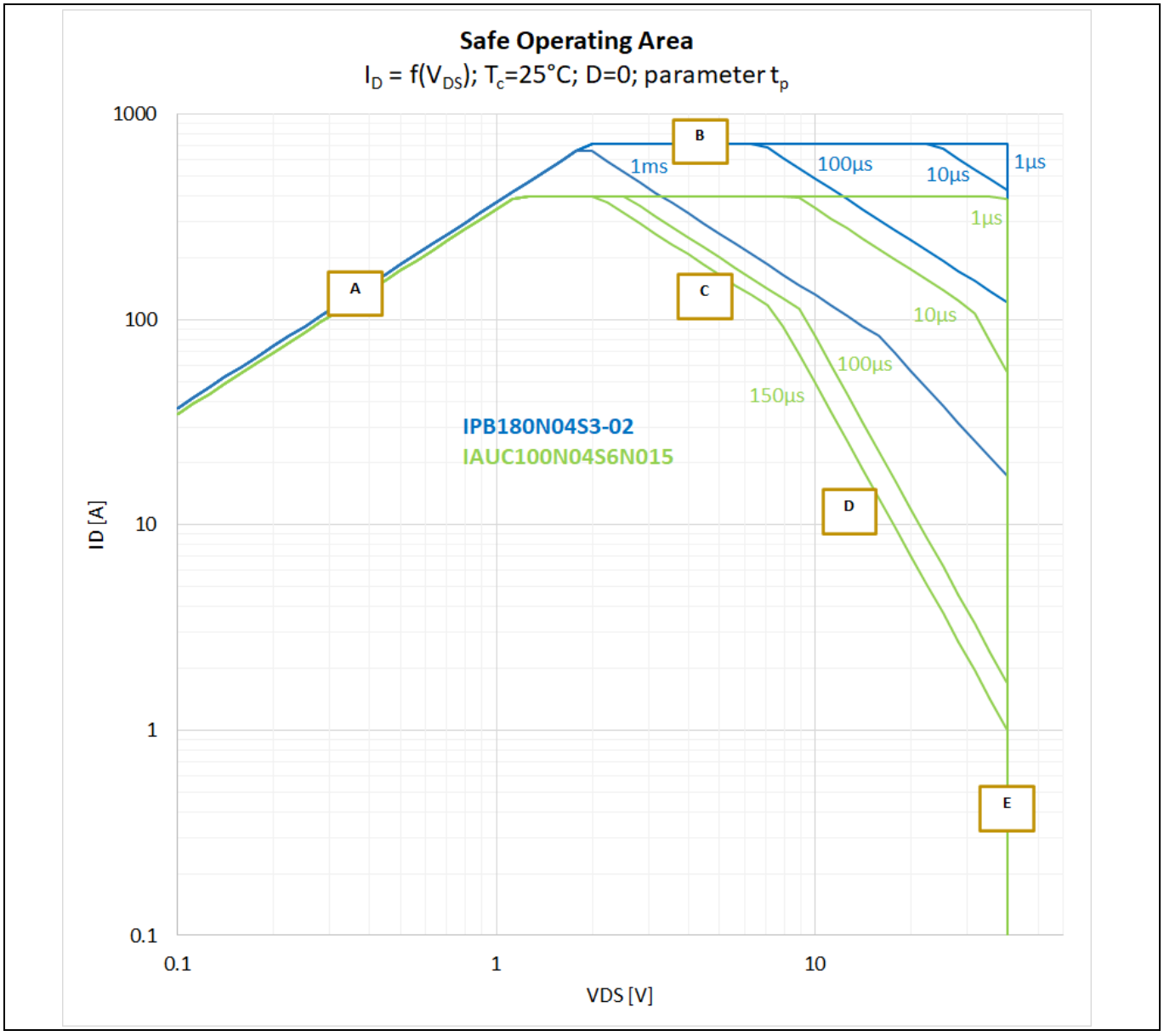


Figure 9 Safe Operating Area (IPB180N04S3-02 versus IAUC100N04S6N015)

However, SOA is not stable under all circumstances, in particular regarding the pulse length. The steeper decline of section (D) refers to the limit of thermal stability and considers the effect of an unbalanced current density inside the active area of the chip. The effect can be best understood when looking at the transfer characteristic of the device (see Figure 10). Above the so called zero-temperature coefficient (ZTC) with V_{gs} > 4.9V, the current in the device will decline with increasing junction temperature, whereas below this point the current will increase. The current density at the ZTC is increasing with each new technology generation and meanwhile so high, that typical application currents are always below the zero-temperature coefficient with V_{gs} < 4.9V. For the SOA this has a dramatic impact: any thermal inhomogeneity in the die, in the package, even on the PCB can result in a local overheating and thus in a thermal runaway of the device. As the risk increases with the pulse length Infineon has decided to limit the guaranteed SOA to pulse below 1ms for V_{gs} below the ZTC.

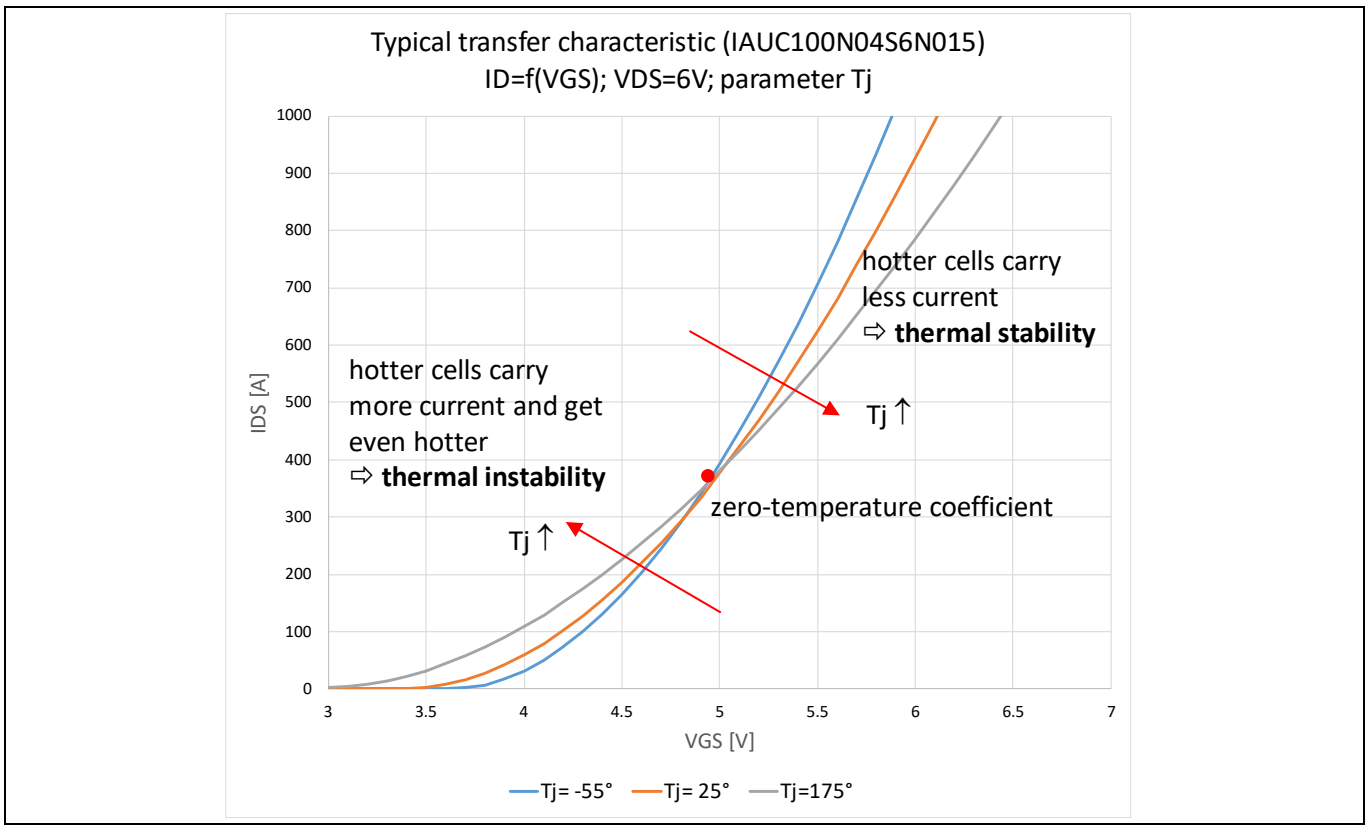


Figure 10 Typical transfer characteristic (IAUC100N04S6N015)

4.4 Avalanche

In case the application requires avalanche operation, there are differences depending on the used frontend technology.

The newer MOSFET technologies (e.g. dual poly trench) are rated for single event avalanche energy. This allows for avalanche operation up to a certain limit of avalanche charge and events depending on the conditions and particular MOSFET technology chosen. The avalanche capability is fully tested for all devices at the end of line test in production for all technologies. Due to the high power losses which occur in avalanche operation, the thermal performance affects the capability of a MOSFET to handle a certain avalanche energy. This means smaller dies in smaller packages can handle lower avalanche energies. Designers must take this into consideration when selecting a new generation MOSFET that shall replace an older, planar based MOSFET.

During avalanche the oxide of the dual poly trench can begin to collect charge (hot carrier injection). Overtime when exposed to multiple or repetitive avalanche events this can lead to premature failure. Therefore trench based MOSFET technologies are not recommended to operate in applications requiring recurring or repetitive avalanche. These MOSFETs can handle a certain amount of avalanche energy, but in applications requiring repetitive avalanche without any limits regarding avalanche energy, frequency, or number of events, specific measures are needed to prevent avalanche operation (for example using a TVS diode).

4.5 Capacitance C_{iss}, C_{oss} and C_{rss}

Direct $R_{DS(on)}$ equal comparison of different frontend technology generations shows the absolute value of the capacitances becomes usually smaller which each new technology step. At first glance one would expect the capacitance to increase with reduction of the cell pitch as more trenches (more capacitance) are placed in the same area. As mentioned above however the lower $R_{DS(on)}$ allows for smaller devices. Both effects are typically cancelling each other and the capacitances become smaller. Figure 11 and Figure 12 show the input capacitance C_{iss} and output capacitance C_{oss}. It should be mentioned that the output capacitance C_{oss} of the OptiMOS™-7 MOSFET slightly increases again contrary to the trend in comparison with OptiMOS™-5 and OptiMOS™-6. The reason for this is that there is some degree of freedom in the cell design for tradeoff between $R_{DS(on)}$ reduction and the capacitance values. For the OptiMOS™-7 technology we put more focus on $R_{DS(on)}$ reduction by increasing C_{oss}. The output capacitance C_{oss} can act as a snubber which is some advantages particularly in switching applications such as motor control.

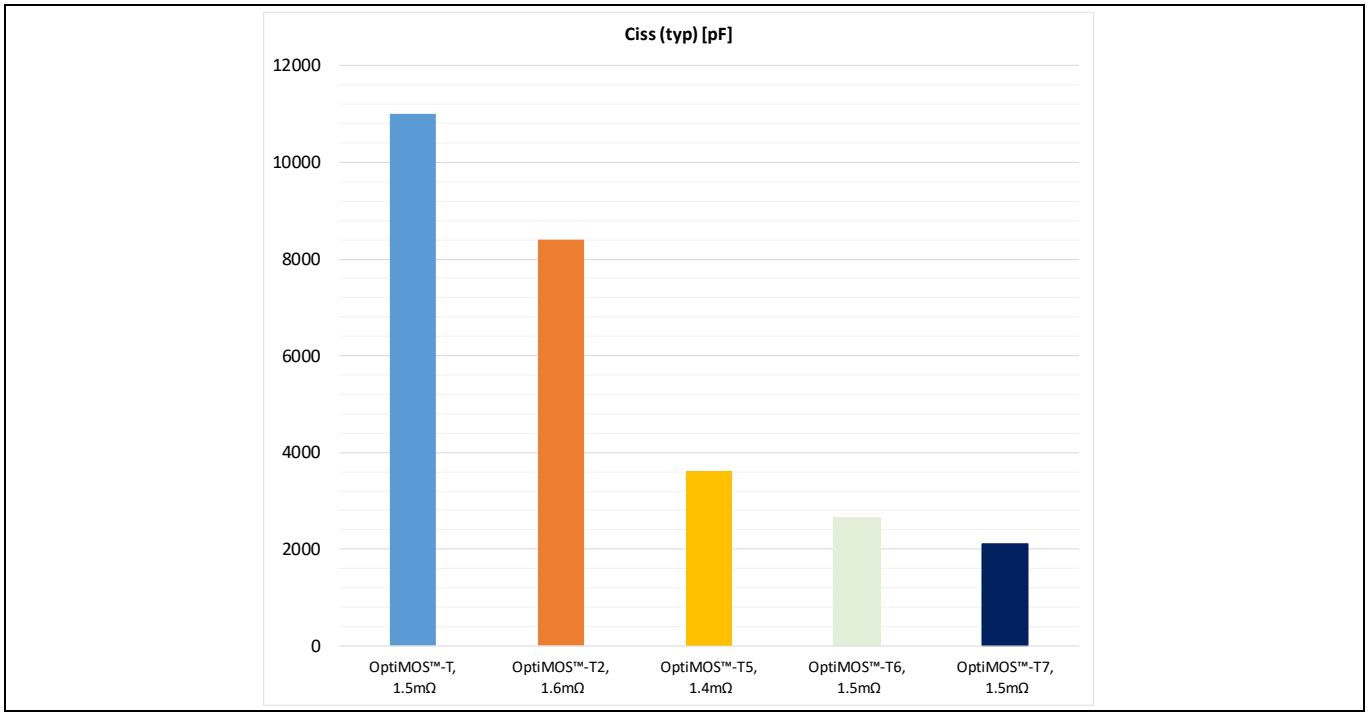


Figure 11 Input capacitance C_{iss}[1]

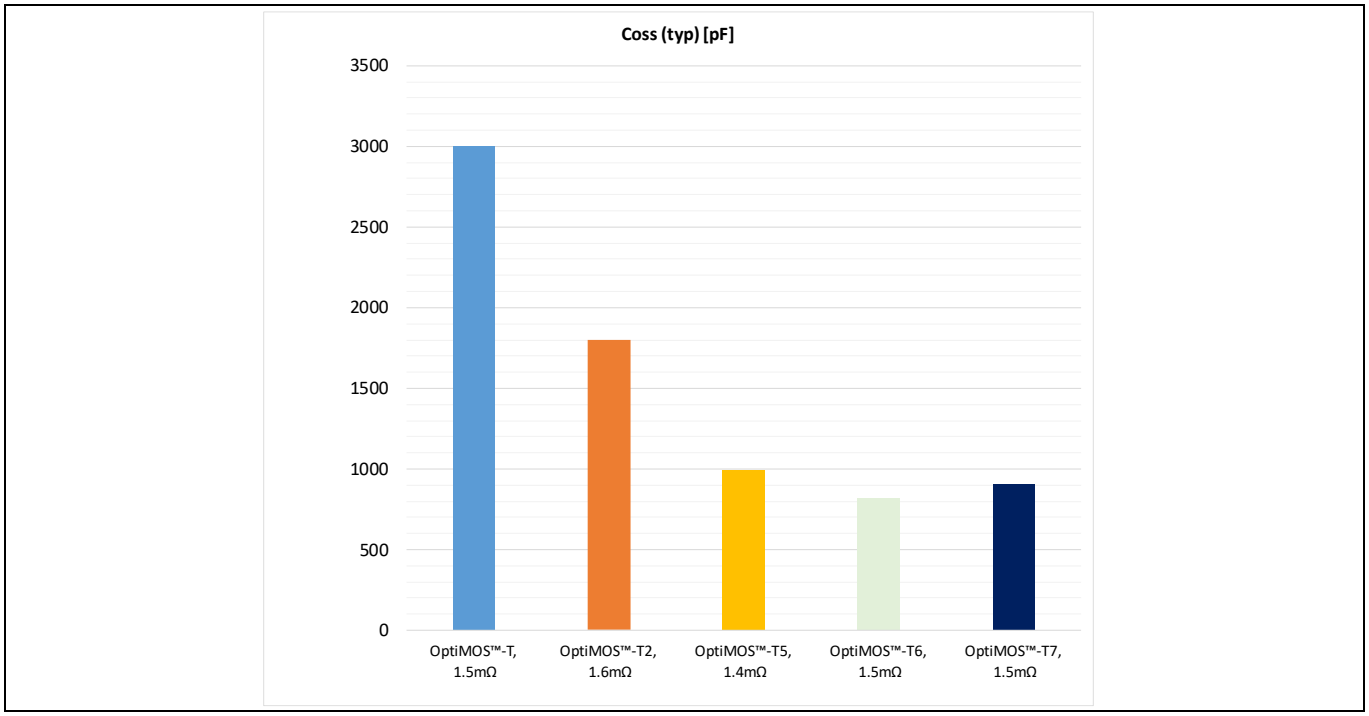


Figure 12 Output capacitance C_{oss}[2]

[1,2] OptiMOS™-7: capacitances C_{iss}, C_{oss}, C_{rss}: condition V_{DS}=25V (differs from data sheet condition) ⇨ condition changed to have the same conditions for all MOSFET technologies

MOSFETs based on the single field-plate-trench technology such as OptiMOS™-T are characterized by large values of reverse transfer capacitance C_{rss}. The gate-poly inside the trench and the drain region of MOSFET form a capacitor with the trench-oxide as insulator. This specific geometry provokes high values of reverse transfer capacitance C_{rss}.

In contrary, for MOSFETs based on dual-poly trench technology such as OptiMOS™-T2 and later, the reverse transfer capacitance C_{rss} is low due to the source potential in the poly in lower part of the trench. Thus, the overlap between gate and drain is dramatically reduced, resulting in a small C_{rss}. This effect makes dual-poly-trench based MOSFETs particularly suitable for fast switching applications. Figure 13 illustrates the relationship between technology and capacitance C_{rss}. The MOSFET IPB180N04S3-02 with the OptiMOS™-T technology has significant larger reverse transfer capacitance C_{rss}.

Again, OptiMOS™-7 technology was designed with a focus towards switching applications such as motor control and DCDC power conversion applications. These require a very low variation of C_{rss} for optimized dead time control, e.g. a slightly higher value of C_{rss} is preferred over a larger absolute variation.

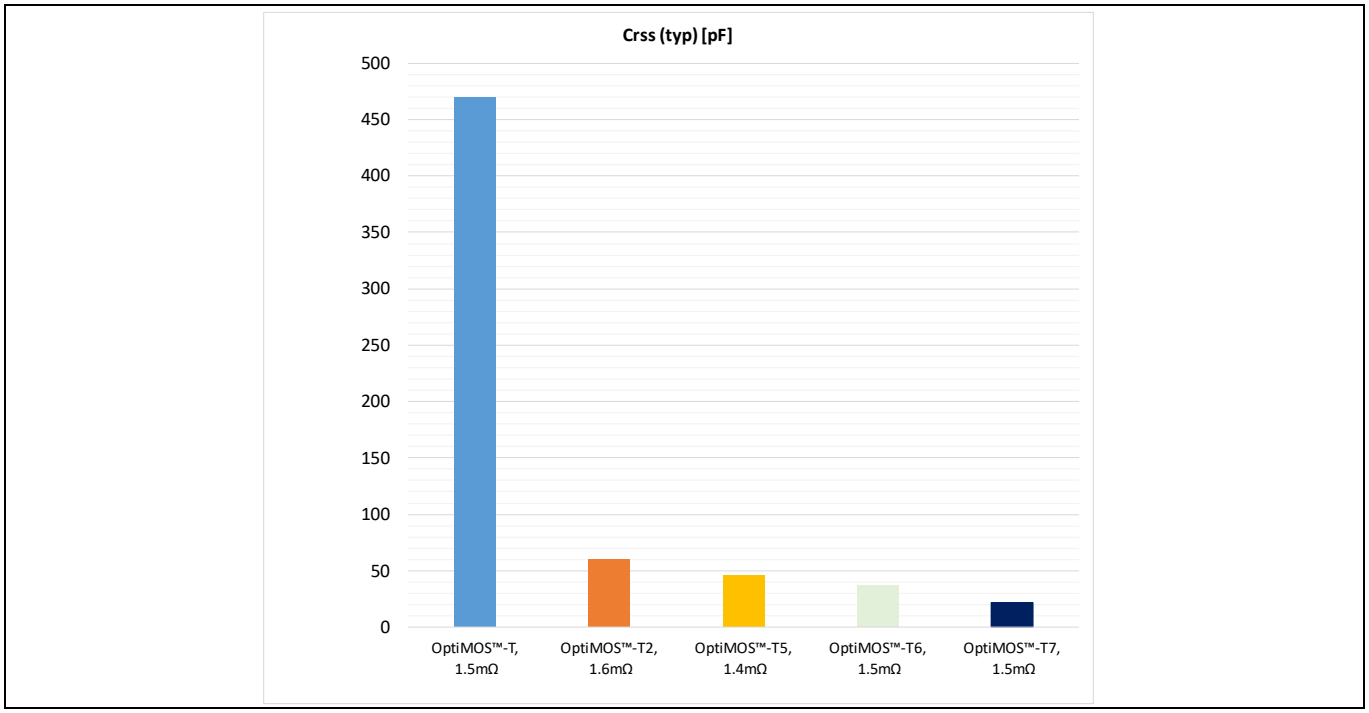


Figure 13 Reverse transfer capacitance C_{rss}[1]

[1] OptiMOS™-7: capacitances C_{iss}, C_{oss}, C_{rss}: condition V_{DS}=25V (differs from data sheet condition) ⇨ condition changed to have same conditions for all MOSFET technologies

4.6 Total Gate Charge

Shrinking die size of newer MOSFET results also in lower values for total gate charge Q_g. Therefore, when replacing a MOSFET of older technology with a newer one, an adjustment of the gate driver configuration necessary to achieve the same switching behavior. The Figure 14 shows the reduction of total gate charge Q_g from technology OptiMOS™-T to about a fifth of total gate charge for OptiMOS™-7.

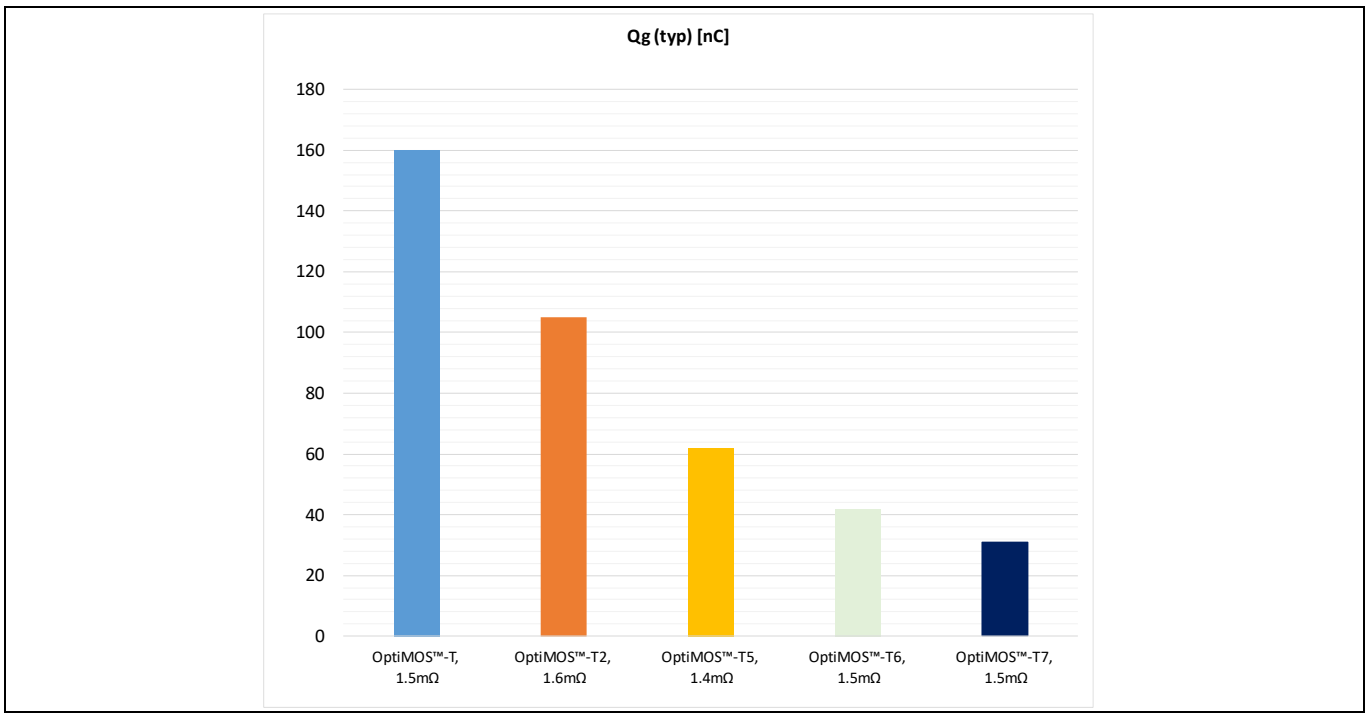


Figure 14 Gate charge total Q_g[1]

[1] OptiMOS™-7: capacitances Q_g: condition V_{DD}=32V (differs from data sheet condition) ⇨ condition changed to have same conditions for all MOSFET technologies

4.7 Reverse Recovery Behavior

The internal body diode of newer MOSFET technology generations have a lower reverse recovery charge Q_{rr} due to the reduced area of the diode inside the die structure. The lower value of Q_{rr} reduces the reverse recovery time which is needed to change the operation of the diode from conductive to blocking state. This benefit leads to a shorter reverse recovery time in applications using the internal body in reverse conduction for faster switching. Figure 15 exhibits the correlation between reverse recovery charge and the smaller die size in newer frontend technologies.

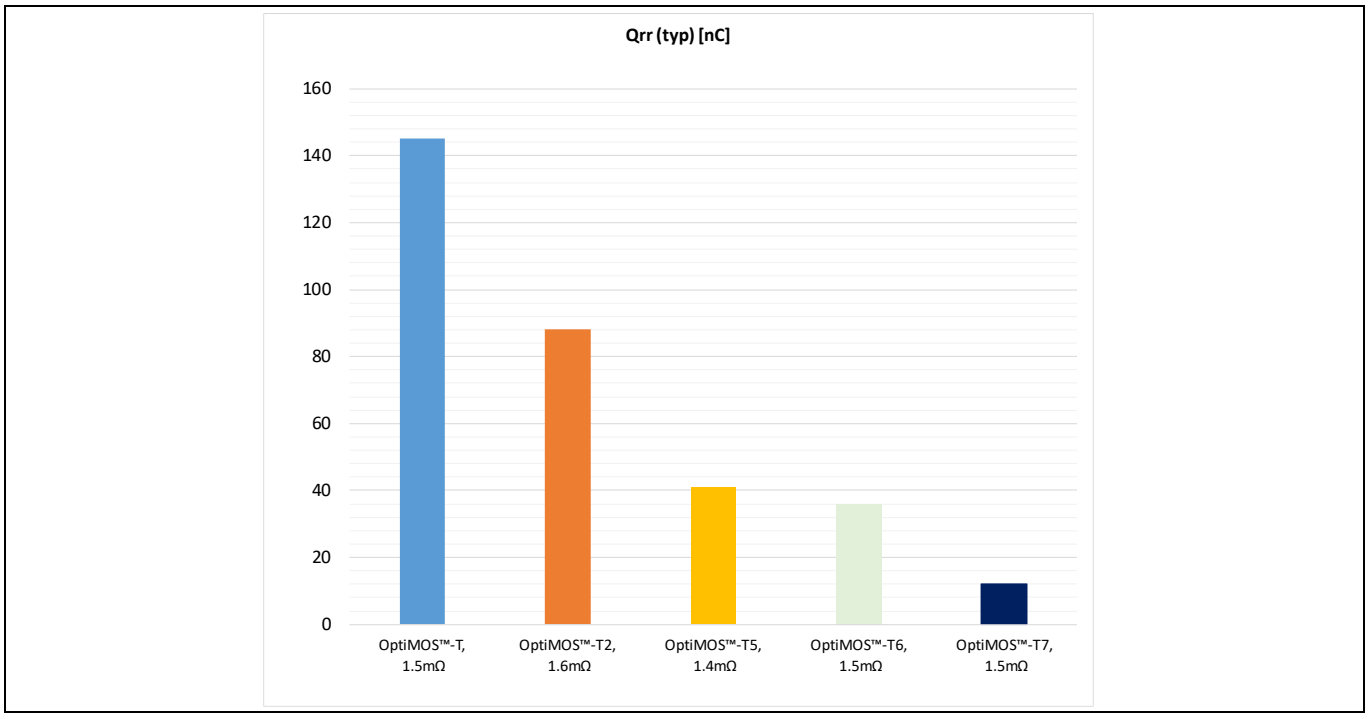


Figure 15 Reverse recovery charge Q_{rr} [1]

[1] Condition V_R=20V, I_F=50A, dI_F/dt =-100A/µs, for details see data sheet of corresponding MOSFET

4.8 Summary Parameter Comparison

Infineon's new MOSFET technologies provide a multitude of advantages in comparison to their predecessors. The most important benefit is coming from the reduced drain-source on-state resistance per chip size. More powerful dies in smaller, low inductive packages enable the realization of highly efficient applications providing maximum power density. When changing from one MOSFET technology generation to the next some specifics need to be considered, in particular regarding thermal constraints. In general, each parameter provided in the data sheet should be checked thoroughly for match with the application requirements. The possibility of modern MOSFET generations, however, to provide higher output power, to reduce the effort for cooling or to minimize the size and the weight are key in fulfilling the ambitious requirements of the automotive market from technical as well as commercial point of view in the future.

5 Automotive MOSFET Naming System

In order to quickly identify an Infineon MOSFET, a naming system has been introduced, which is explained here.

5.1 MOSFET Technology Naming System up to OptiMOS™-5

Infineon Automotive MOSFET technologies up to OptiMOS™-5 40V portfolios have the following naming system. The part number (e.g. IPD90N04S4L-05) reveals already important key parameters of the product which are explained in Figure 16.

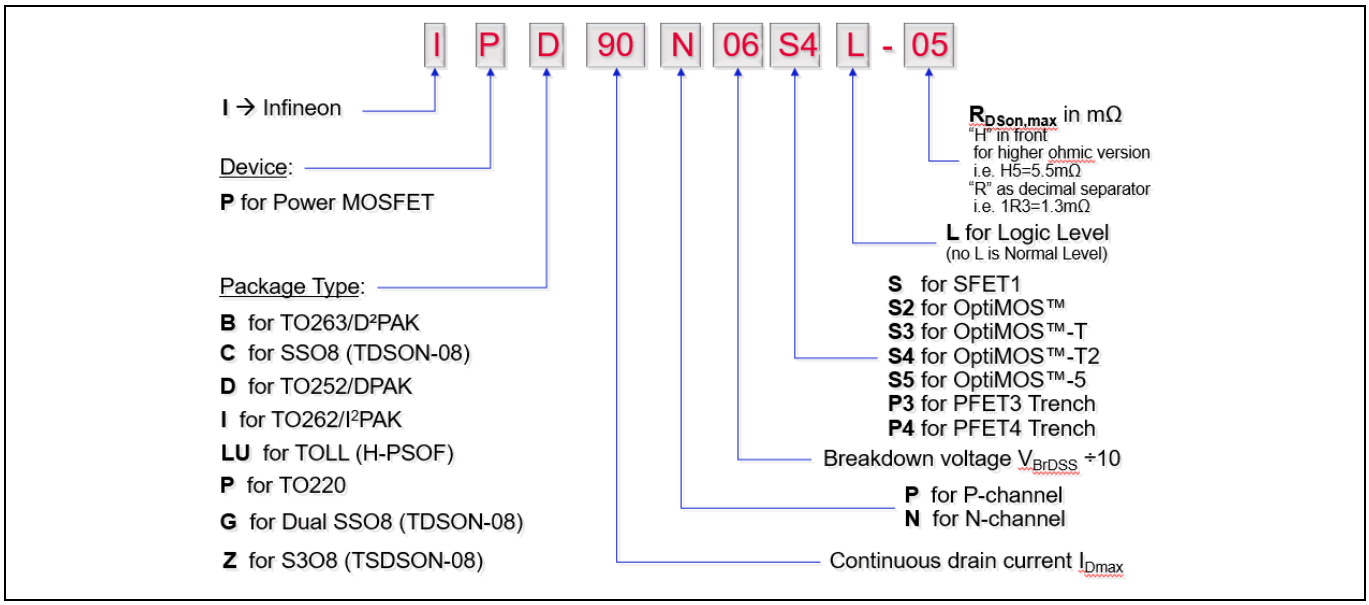


Figure 16 MOSFET Technology Naming System up to OptiMOS™-5

5.2 MOSFET OptiMOS ™-6 Technology Naming System

For bottom side cooled MOSFETs using OptiMOS™-6 technology, as well as the higher voltage classes of OptiMOS™-5 (e.g. 60V, 80V or 120V), a newer naming system is applied to identify explicitly the automotive grade and account for $R_{DS(on)}$ ratings below 1mΩ. As an example the MOSFET IAUC100N08S5N055X demonstrates the naming system in Figure 17.

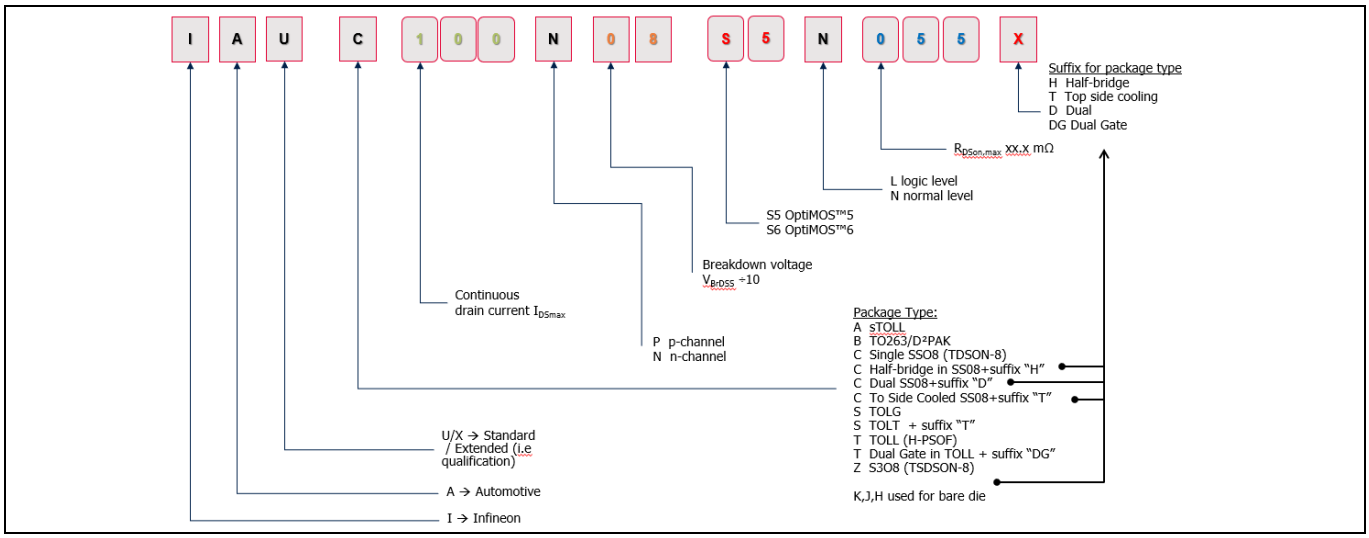


Figure 17 MOSFET Technology Naming System OptiMOS™-6

5.3 The MOSFET Technology Naming System for New Products

Based on the market feedback and benchmark with competitors, another update of the naming system will be used for upcoming MOSFET products. The naming system is applied to all products based on OptiMOS™-7 technology and future technologies. Additionally for some products in certain package configurations and equipped with older front-end technologies this naming system is also used. An example to explain this naming system shown in Figure 18 with the OptiMOS™-7 MOSFET IAUCN08S7N055X. The main change compared to the previous naming systems is that maximum continuous current (I_D) is removed from the part number to avoid misunderstanding in device selection. Instead, a more detailed continuous drain current capability information for the MOSFET is provided in the data sheet.

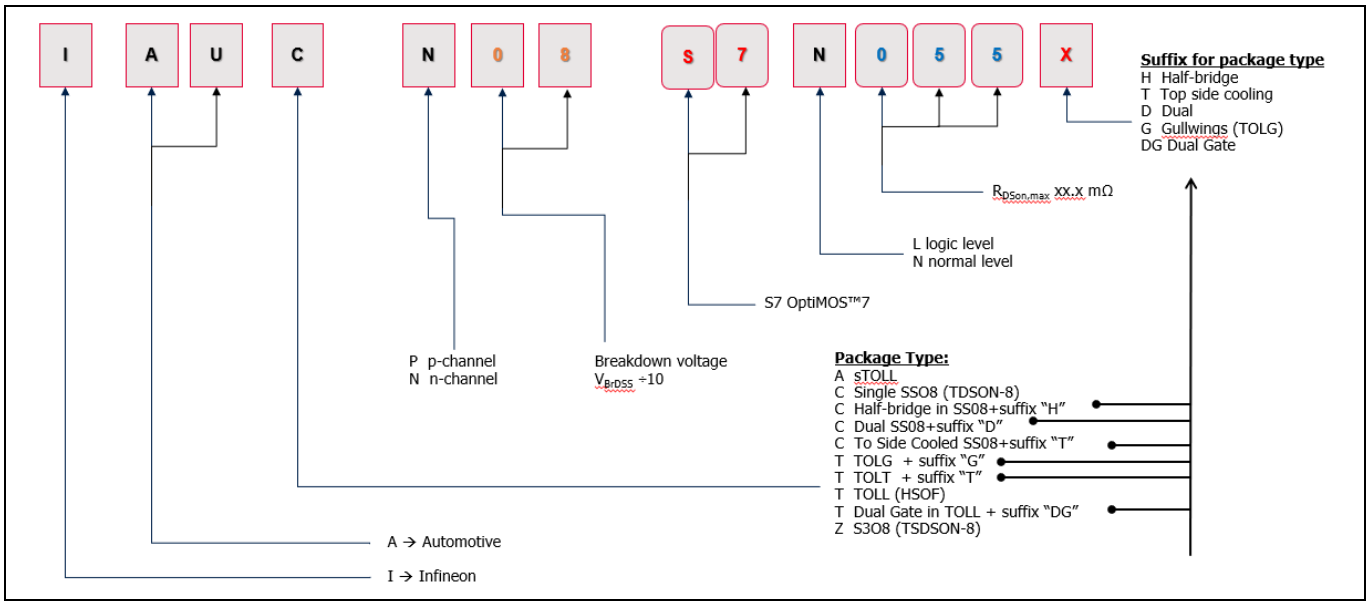


Figure 18 The MOSFET Technology Naming System OptiMOS™-7

5.4 Legacy IR Naming System

Infineon acquired International Rectifier known as IR to enhance its market leadership in power semiconductor. For MOSFETs coming from legacy IR, the part number is described in Figure 19.

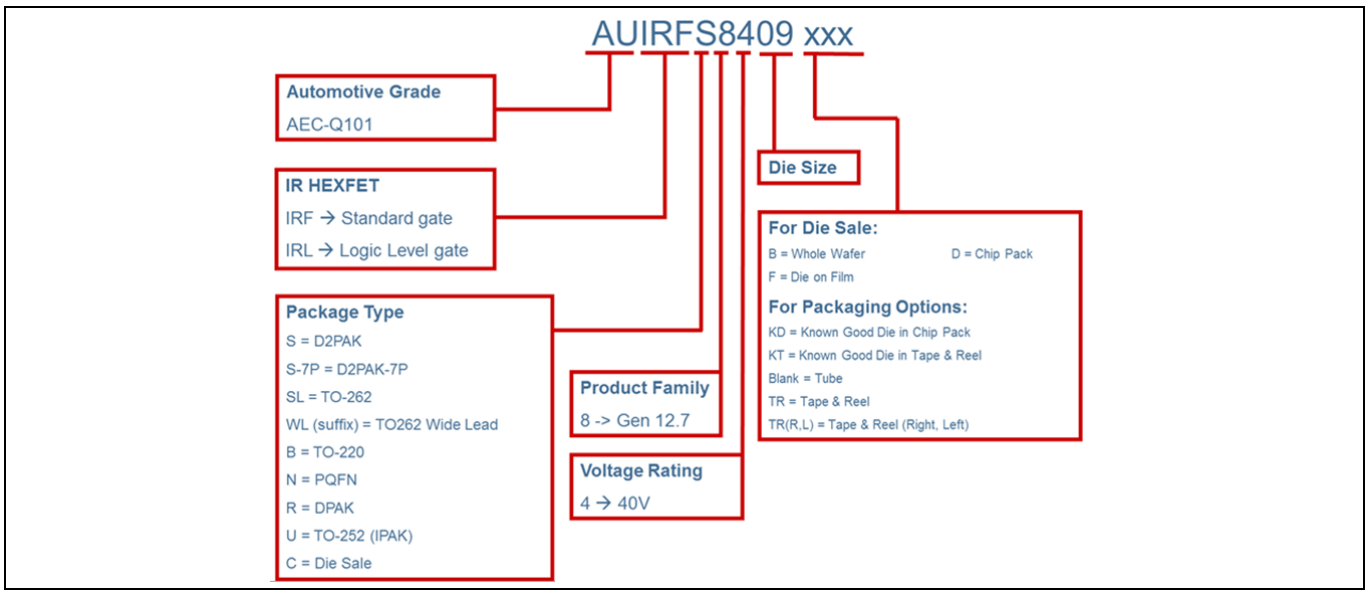


Figure 19 The legacy IR Naming System

6 Abbreviations and definitions

Table 4 Abbreviations

Abbreviation	Definition
AC	Alternating Current
DC	Direct Current
EMC	Electromagnetic Compatibility
IGBT	Insulated-Gate Bipolar Transistor
IR	International Rectifier
JFET	Junction-gate Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
$R_{DS(on)}$	Drain-Source on-state resistance
SOA	Safe Operating Area
TIM	Thermal Interface Material
TOLx	TOLL, TOLG, TOLT
TVS	Transient Voltage Suppressor
ZTC	Zero Temperature Coefficient

7 Reference documents

This document should be read in conjunction with the following documents:

[1] Infineon website Automotive MOSFET,
https://www.infineon.com/cms/en/product/power/mosfet/automotive-mosfet/

[2] Infineon Special Subject Book January 2000 'Thermal Resistance Theory and Practice',
https://www.infineon.com/dgdl/smdpack.pdf?fileId=db3a304330f6860601311905ea1d4599

[3] IPB180N04S3-02 datasheet, Infineon Technologies AG,
https://www.infineon.com/cms/en/product/power/mosfet/automotive-mosfet/ipb180n04s3-02/

[4] IPB160N04S4-H1 datasheet, Infineon Technologies AG,
https://www.infineon.com/cms/en/product/power/mosfet/automotive-mosfet/ipb160n04s4-h1/

[5] IAUA120N04S5N014 datasheet, Infineon Technologies AG,
https://www.infineon.com/cms/en/product/power/mosfet/automotive-mosfet/iaua120n04s5n014/

[6] IAUC100N04S6N015 datasheet, Infineon Technologies AG,
https://www.infineon.com/cms/en/product/power/mosfet/automotive-mosfet/iauc100n04s6n015/

Revision history

Document version	Date of release	Description of changes
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