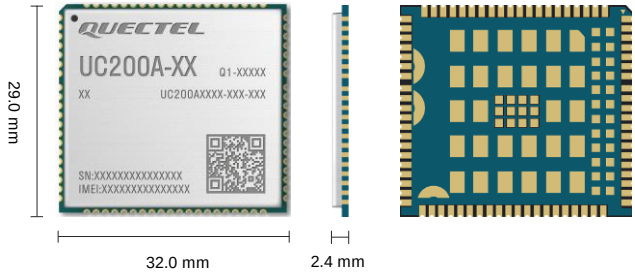
# Quectel UC200A-GL

## UMTS/HSPA+ Module




Quectel UC200A-GL is a cost-effective and high-performance UMTS/HSPA+ module with data rates of up to 21 Mbps downlink and up to 5.76 Mbps uplink. UC200A-GL is compatible with UMTS/HSPA+ UC200T series and LTE Standard EC2x series (EC25 series and EC21 series), EC200x series (EC200T series and EC200U series), EC20-CE, EC200D-CN and EC200N-CN in SMT package, which ensures a smooth transition between 3G and 4G networks. In addition, UC200A-GL is also fully backward compatible with existing GSM/GPRS/EDGE networks.

In UMTS/HSPA+ connectivity, UC200A-GL is suited for global networks. UC200A-GL adopts the laser engraving process to ensure more good-looking appearance, strong metallic texture, better heat dissipation and durable label information, which makes it more suitable for automation requirements.

A rich set of Internet protocols, industry-standard interfaces and abundant functionalities (USB drivers for Windows 7/8/8.1/10, Linux and Android) extend the applicability of the module to a wide range of M2M applications, such as automation, smart metering, tracking systems, security solutions, routers, wireless POS, mobile computing devices, PDA phones and tablet PC.

## Key Features

- Worldwide UMTS/HSPA+ and GSM/GPRS/EDGE coverage
- Low design cost
- High-performance and multi-feature interfaces
- High-quality data and image transmission even in harsh conditions
- Compatible with UMTS/HSPA+ UC200T Series and multiple LTE Standard modules in package

Dual-mode & Multi-band for UMTS & GSM

Max. 21 Mbps (DL)
Max. 5.76 Mbps (UL)

Android OS

LCC Package

Embedded Abundant Protocols

DFOTA

USB 2.0 High Speed Interface

Quectel Enhanced AT Commands

# Quectel UC200A-GL

| UMTS/HSPA+ | UC200A-GL |
|---|---|
| **Region/Operator** | Global |
| **Dimensions (mm)** | 29.0 × 32.0 × 2.4 |
| **Temperature Range** | |
| **Operating Temperature** | -35 °C to +75 °C |
| **Extended Temperature** | -40 °C to +85 °C |
| **Frequency Bands** | |
| **WCDMA** | B1/B2/B5/B8 |
| **GSM/EDGE** | B2/B3/B5/B8 |
| **Certifications** | |
| **Regulatory** | **Europe:** CE<br>**America:** FCC<br>**Australia/New Zealand:** RCM<br>**Brazil:** Anatel* |
| **Data Rates** | |
| **HSPA+ (Mbps)** | 21 (DL)/5.76 (UL) |
| **WCDMA (kbps)** | 384 (DL)/384 (UL) |
| **EDGE (kbps)** | 236.8 (DL)/236.8 (UL) |
| **GPRS (kbps)** | 85.6 (DL)/85.6 (UL) |
| **Interfaces** | |
| **USB 2.0** | × 1 |
| **Audio Digital (PCM)*** | × 1 |
| **(U)SIM** | × 1 (1.8/ 3.0 V) |
| **NETLIGHT** | × 2 (NET_STATUS and NET_MODE) |
| **UART** | × 2 (Main UART and Debug UART) |
| **ADC** | × 2 (12 bits) |
| **SDIO** | × 1 (Use for connecting SD card) |
| **STATUS** | × 1 (ON/OFF Status Indication) |
| **I2C** | × 1 |
| **RESET** | × 1 (Active low) |
| **PWRKEY** | × 1 (Active low) |
| **Voice** | |
| **Speech Codec Modes** | HR/FR/EFR/AMR/AMR-WB |
| **Echo Arithmetic** | Echo Cancellation/ Noise Reduction |
| **Enhanced Features** | |
| **DFOTA** | ● |
| **Firmware Upgrade via USB or UART** | ● |
| **QuecLocator®** | ● |
| **(U)SIM Detection** | ● |
| **Software Features** | |
| **Protocols** | TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS/SMTP/SMTPS |
| **Drivers** | |
| **USB Serial Driver** | Windows 7/8/8.1/10,<br>Linux 2.6–5.12,<br>Android 4.x–11.x |
| **RIL Driver*** | Android 4.x–11.x |
| **USB ECM Driver** | Linux 2.6–5.12 |
| **USB RNDIS Driver*** | Windows 7/8/8.1/10<br>Linux 2.6–5.12 |
| **Electrical Features** | |
| **Supply Voltage Range** | 3.4–4.5 V, typ. 3.8 V |
| **Power Consumption (Typical)** | 17 µA @ Power off<br>1 mA @ Sleep |

NOTE:
1. *: under development.
2. ●: supported.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# UC200A&UC200T Series

# Compatible Design

**UMTS/HSPA+ Module Series**

Version: 1.0.0

Date: 2021-12-13

Status: Preliminary

**At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:**

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# About the Document

## Revision History

| Version | Date | Author | Description |
|---|---|---|---|
| - | 2021-12-13 | Johen SUN | Creation of the document |
| 1.0.0 | 2021-12-13 | Johen SUN | Preliminary |

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# 1 Introduction

Quectel UMTS/HSPA+ UC200A series and UC200T series modules are compatible with each other. This document briefly describes the compatible design among these modules.

## 1.1. Special Mark

**Table 1: Special Mark**

| Mark | Definition |
|---|---|
| * | Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable. |

# 2 General Descriptions

## 2.1. Product Description

The supported network modulation and Rx-diversity of UC200A and UC200T series are shown in the following table, you can choose suitable products as terminal applications for your specific applications.

**Table 2: Supported Network Modulation and Rx-diversity of the Modules**

| Module | WCDMA | TD-SCDMA | EVDO | CDMA | GSM | Rx-diversity |
|---|---|---|---|---|---|---|
| UC200A Series | √ | - | - | - | √ | - |
| UC200T Series | √ | - | - | - | √ | - |

### 2.1.1. Brief Introduction of the Modules

**Table 3: Brief Introduction of the Module**

| Module | Picture | Packaging | Dimensions (mm) | Description |
|---|---|---|---|---|
| UC200A Series |  | 80 LCC pins<br>64 LGA pins | 29.0 × 32.0 × 2.4 | UMTS/HSPA+ module |
| UC200T Series |  | 80 LCC pins<br>64 LGA pins | 29.0 × 32.0 × 2.4 | UMTS/HSPA+ module |

### 2.1.2. Frequency Bands

**Table 4: Frequency Bands**

| Module | UMTS | EVDO/CDMA | GSM | GNSS [1] |
|---|---|---|---|---|
| **UC200A Series** | | | | |
| **UC200A-GL** | WCDMA: B1/B2/B5/B8 | - | 850/900/1800/1900 MHz | - |
| **UC200T Series** | | | | |
| **UC200T-GL** | WCDMA: B1/B2/B5/B6/B8 | - | 850/900/1800/1900 MHz | - |
| **UC200T-EM** | WCDMA: B1/B8 | - | 900/1800 MHz | - |

[1] GNSS function is optional.

## 2.2. Feature Overview

The following table compares the general features of UC200A & UC200T series.

**Table 5: Feature Overview**

| Function | UC200A Series | UC200T Series |
|---|---|---|
| Power Supply | Supply voltage: 3.4–4.5 V<br>Typ. 3.8 V | Supply voltage: 3.4–4.5 V<br>Typ. 3.8 V |
| Peak Current | VBAT: max. 2.3 A | VBAT: max. 2.0 A |
| Sleep Current | < 1.2 mA @ **AT+CFUN=0** (USB disconnected) | < 1.2 mA @ **AT+CFUN=0** (USB disconnected) |
| Operating Temperature | Operating Temperature Range: -35 °C – +75 °C [2]<br>Extended Operating Temperature Range: -40 °C – +85 °C [3]<br>Storage temperature range: -40 °C - +90 °C | Operating Temperature Range: -35 °C to +75 °C [2]<br>Extended Operating Temperature Range: -40 °C – +85 °C [3]<br>Storage temperature range: -40 °C - +90 °C |
| UART Interfaces | **Main UART:**<br>● Used for AT command communication and data transmission.<br>● Baud rates: reach 921600 bps, 115200 bps by default.<br>● Supports RTS and CTS hardware flow control.<br>**Debug UART:**<br>● Used for the output of partial logs.<br>● Baud rates: 115200 bps. | **Main UART:**<br>● Used for AT command communication and data transmission.<br>● Baud rates: reach 1 Mbps, 115200 bps by default.<br>● Supports RTS and CTS hardware flow control.<br>**Debug UART:**<br>● Used for the output of partial logs.<br>● Baud rates: 115200 bps. |
| (U)SIM Interfaces | Supports(U)SIM card: 1.8/3.0 V | Supports(U)SIM card: 1.8/3.0 V |
| PCM Interface | ● Used for audio function with external Codec<br>● Supports 16-bit linear data format<br>● Supports short frame synchronization mode<br>● Supports master and slave modes | ● Used for audio function with external Codec<br>● Supports 16-bit linear data format<br>● Supports short frame synchronization mode<br>● Supports master and slave modes |
| USB Interface | Supports USB 2.0 (slave only), with transmission rates up to 480 Mbps | Supports USB 2.0 (slave only), with transmission rates up to 480 Mbps |
| SD Card Interface | Under development | Under development |
| ADC interface | The module provides two analog-to-digital converter interfaces.<br>Voltage range: 0–VBAT_BB<br>Resolution: 12 bits | The module provides two analog-to-digital converter interfaces.<br>Voltage range: 0–VBAT_BB<br>Resolution: 12 bits |
| Network Indication | Two pins NET_MODE and NET_STATUS to indicate network status. | Two pins NET_MODE and NET_STATUS to indicate network status. |
| Antenna Interface | ANT_MAIN | ANT_MAIN |
| Firmware Upgrade | USB interface or DFOTA. | USB interface or FOTA. |

[2] Within the operating temperature range, the module meets 3GPP specifications.

[3] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as $P_{out}$, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

## 2.3. Pin Assignment

The following figures show the pin assignment of UC200A series, UC200T series.

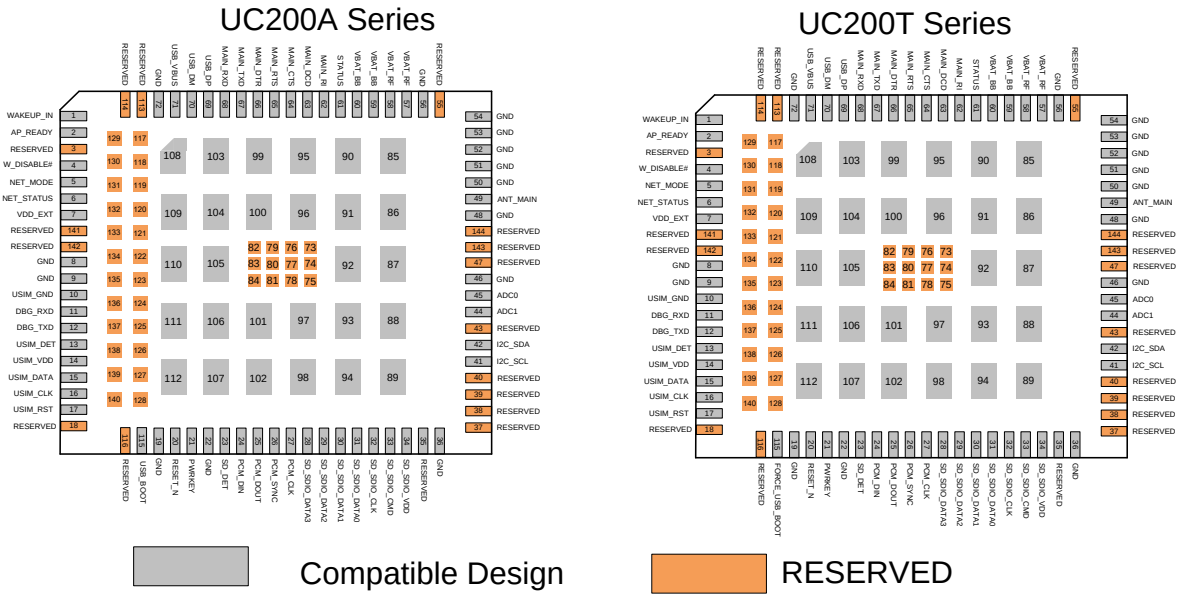


**Figure 1: Pin Assignment (Top View)**

**NOTE**

USB_BOOT of UC200A series and FORCE_USB_BOOT of UC200T series cannot be pulled up before the module startup.

# 3 Pin Description

This chapter describes the pin definition of UC200A and UC200T series.

**Table 6: I/O Parameters Definition**

| Type | Description |
|---|---|
| AI | Analog Input |
| AIO | Analog Input/Output |
| DI | Digital Input |
| DO | Digital Output |
| DIO | Digital Input/Output |
| OD | Open Drain |
| PI | Power Input |
| PO | Power Output |

The following table describes the pin functions and DC characteristics of UC200A series and UC200T series modules.

**Table 7: Pin Comparison**

| UC200A Series | | | | UC200T Series | | | |
|---|---|---|---|---|---|---|---|
| **Pin No.** | **Pin Name** | **I/O** | **Power Domain** | **Pin No.** | **Pin Name** | **I/O** | **Power Domain** |
| 1 | WAKEUP_IN | DI | 1.8 V | 1 | WAKEUP_IN | DI | 1.8 V |
| 2 | AP_READY | DI | 1.8 V | 2 | AP_READY | DI | 1.8 V |
| 4 | W_DISABLE# | DI | 1.8 V | 4 | W_DISABLE# | DI | 1.8 V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 5 | NET_MODE | DO | 1.8 V | 5 | NET_MODE | DO | 1.8 V |
| 6 | NET_STATUS | DO | 1.8 V | 6 | NET_STATUS | DO | 1.8 V |
| 7 | VDD_EXT | PO | 1.8 V | 7 | VDD_EXT | PO | 1.8 V |
| 8, 9 | GND | - | GND | 8 | GND | - | GND |
| 10 | USIM_GND | - | GND | 10 | USIM_GND | - | GND |
| 11 | DBG_RXD | DI | 1.8 V | 11 | DBG_RXD | DI | 1.8 V |
| 12 | DBG_TXD | DO | 1.8 V | 12 | DBG_TXD | DO | 1.8 V |
| 13 | USIM_DET | DI | 1.8 V | 13 | USIM_DET | DI | 1.8 V |
| 14 | USIM_VDD | PO | 1.8/3.0 V | 14 | USIM_VDD | PO | 1.8/3.0 V |
| 15 | USIM_DATA | DIO | 1.8/3.0 V | 15 | USIM_DATA | DIO | 1.8/3.0 V |
| 16 | USIM_CLK | DO | 1.8/3.0 V | 16 | USIM_CLK | DO | 1.8/3.0 V |
| 17 | USIM_RST | DO | 1.8/3.0 V | 17 | USIM_RST | DO | 1.8/3.0 V |
| 19 | GND | - | GND | 19 | GND | - | GND |
| 20 | RESET_N | DI | 1.8 V | 20 | RESET_N | DI | 1.8 V |
| 21 | PWRKEY | DI | VBAT Power domain | 21 | PWRKEY | DI | VBAT Power domain |
| 22 | GND | - | GND | 22 | GND | - | GND |
| 23 | SD_DET* | DI | 1.8 V | 23 | SD_DET* | DI | 1.8/2.8 V |
| 24 | PCM_DIN | DI | 1.8 V | 24 | PCM_DIN | DI | 1.8 V |
| 25 | PCM_DOUT | DO | 1.8 V | 25 | PCM_DOUT | DO | 1.8 V |
| 26 | PCM_SYNC | DIO | 1.8 V | 26 | PCM_SYNC | DIO | 1.8 V |
| 27 | PCM_CLK | DIO | 1.8 V | 27 | PCM_CLK | DIO | 1.8 V |
| 28 | SD_SDIO_ DATA3* | DIO | 1.8/2.8 V | 28 | SD_SDIO_ DATA3* | DIO | 1.8/2.8 V |
| 29 | SD_SDIO_ DATA2* | DIO | 1.8/2.8 V | 29 | SD_SDIO_ DATA2* | DIO | 1.8/2.8 V |
| 30 | SD_SDIO_ DATA1* | DIO | 1.8/2.8 V | 30 | SD_SDIO_ DATA1* | DIO | 1.8/2.8 V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 31 | SD_SDIO_DATA0* | DIO | 1.8/2.8 V | 31 | SD_SDIO_DATA0* | DIO | 1.8/2.8 V |
| 32 | SD_SDIO_CLK* | DO | 1.8/2.8 V | 32 | SD_SDIO_CLK* | DO | 1.8/2.8 V |
| 33 | SD_SDIO_CMD* | DIO | 1.8/2.8 V | 33 | SD_SDIO_CMD* | DIO | 1.8/2.8 V |
| 34 | SD_SDIO_VDD* | PO | 1.8/2.8 V | 34 | SD_SDIO_VDD* | PO | 1.8/2.8 V |
| 36 | GND | - | GND | 36 | GND | - | GND |
| 41 | I2C_SCL | OD | An external 1.8 V pull-up resistor is needed. | 41 | I2C_SCL | OD | An external 1.8 V pull-up resistor is needed. |
| 42 | I2C_SDA | OD | An external 1.8 V pull-up resistor is needed. | 42 | I2C_SDA | OD | An external 1.8 V pull-up resistor is needed. |
| 44 | ADC1 | AI | 0 V–VBAT_BB | 44 | ADC1 | AI | 0 V–VBAT_BB |
| 45 | ADC0 | AI | 0 V–VBAT_BB | 45 | ADC0 | AI | 0 V–VBAT_BB |
| 46 | GND | - | GND | 46 | GND | - | GND |
| 48 | GND | - | GND | 48 | GND | - | GND |
| 49 | ANT_MAIN | AIO | - | 49 | ANT_MAIN | AIO | - |
| 50–54 | GND | - | GND | 50–54 | GND | - | GND |
| 56 | GND | - | GND | 56 | GND | - | GND |
| 57 | VBAT_RF | PI | 3.4–4.5 V | 57 | VBAT_RF | PI | 3.4–4.5 V |
| 58 | VBAT_RF | PI | 3.4–4.5 V | 58 | VBAT_RF | PI | 3.4–4.5 V |
| 59 | VBAT_BB | PI | 3.4–4.5 V | 59 | VBAT_BB | PI | 3.4–4.5 V |
| 60 | VBAT_BB | PI | 3.4–4.5 V | 60 | VBAT_BB | PI | 3.4–4.5 V |
| 61 | STATUS | OD | - | 61 | STATUS | OD | - |
| 62 | MAIN_RI | DO | 1.8 V | 62 | MAIN_RI | DO | 1.8 V |
| 63 | MAIN_DCD | DO | 1.8 V | 63 | MAIN_DCD | DO | 1.8 V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 64 | MAIN_CTS | DO | 1.8 V | 64 | MAIN_CTS | DO | 1.8 V |
| 65 | MAIN_RTS | DI | 1.8 V | 65 | MAIN_RTS | DI | 1.8 V |
| 66 | MAIN_DTR | DI | 1.8 V | 66 | MAIN_DTR | DI | 1.8 V |
| 67 | MAIN_TXD | DO | 1.8 V | 67 | MAIN_TXD | DO | 1.8 V |
| 68 | MAIN_RXD | DI | 1.8 V | 68 | MAIN_RXD | DI | 1.8 V |
| 69 | USB_DP | AIO | - | 69 | USB_DP | AIO | - |
| 70 | USB_DM | AIO | - | 70 | USB_DM | AIO | - |
| 71 | USB_VBUS | AI | 3.0–5.25 V | 71 | USB_VBUS | AI | 3.0–5.25 V |
| 72 | GND | - | GND | 72 | GND | - | GND |
| 85–112 | GND | - | GND | 85–112 | GND | - | GND |
| 115 | USB_BOOT | DI | 1.8 V | 115 | FORCE_USB_BOOT | DI | 1.8 V |
| 3<br>18<br>35<br>37–40<br>43<br>47<br>55<br>73–84<br>113<br>114<br>116–144 | RESERVED | - | - | 3<br>18<br>35<br>37–40<br>43<br>47<br>55<br>73–84<br>113<br>114<br>116–144 | RESERVED | - | - |

**NOTE**

1. Pins in **blue** are compatible pins with different functionality or power domain; Pins in **black** are compatible pins with same functionality.
2. Keep all RESERVED pins and unused pins unconnected.
3. For more information about the pins on UC200A and UC200T series, refer to the relevant hardware design.

# 4 Hardware Interfaces Design

This chapter mainly introduces the compatible design among UC200A and UC200T series modules in terms of main functionalities.

## 4.1. Power Supply

### 4.1.1. Operating Voltage

The following table shows the operating voltage range of UC200A and UC200T series modules.

**Table 8: Difference of Operating Voltage Range**

| Module | Power Supply Pins | Min. | Typ. | Max. | Unit | Description |
|---|---|---|---|---|---|---|
| UC200A Series | VBAT_BB & VBAT_RF | 3.4 | 3.8 | 4.5 | V | The actual input voltages must be kept between the minimum and maximum values. |
| UC200T Series | VBAT_BB & VBAT_RF | 3.4 | 3.8 | 4.5 | V | |

In compatible design, please ensure that the input voltage is between 3.4 V and 4.5 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop in 3G and 4G network is smaller than that in 2G network.

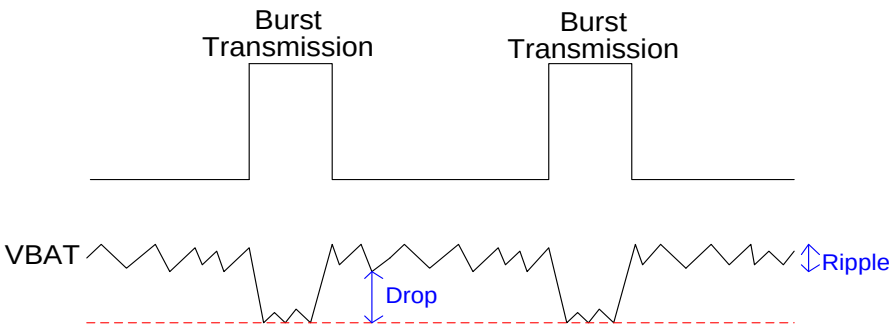


**Figure 2: Power Supply Limits During Burst Transmission**

To decrease voltage ‘s drop, a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source and can be expanded to two sub paths with the star structure. The width of VBAT_BB trace should be no less than 1 mm. The width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to ensure the stability of power source, it is suggested that a WS4.5D3HV TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. A simple reference circuit is illustrated in the following figure.

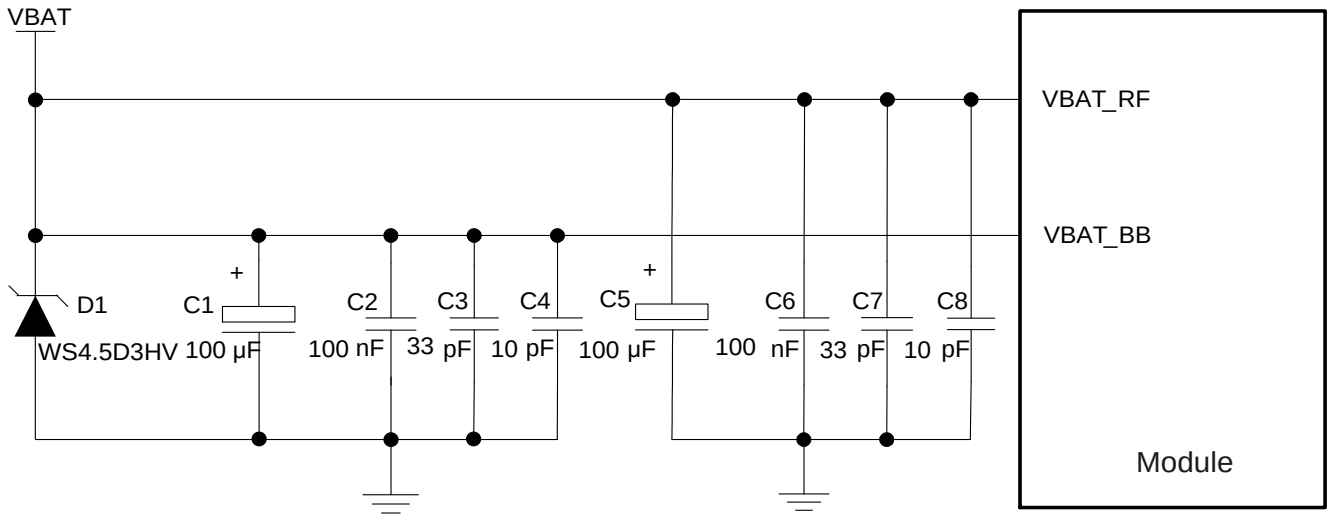


**Figure 3: Reference Circuit of Power Supply**

### 4.1.2. Power Supply

Power design is critical for the module’s performance. The power supply of UC200A series should be able to provide sufficient current at least 2.3 A (the power supply of UC200T series should be able to provide sufficient current at least 2.0 A). If the voltage drops between input and output is not too high, it is suggested that an LDO should be used to supply power to the module. If there is a big voltage difference between the input source and the desired output, a buck converter is recommended.

The following figure illustrates a reference design for +5 V input power source.

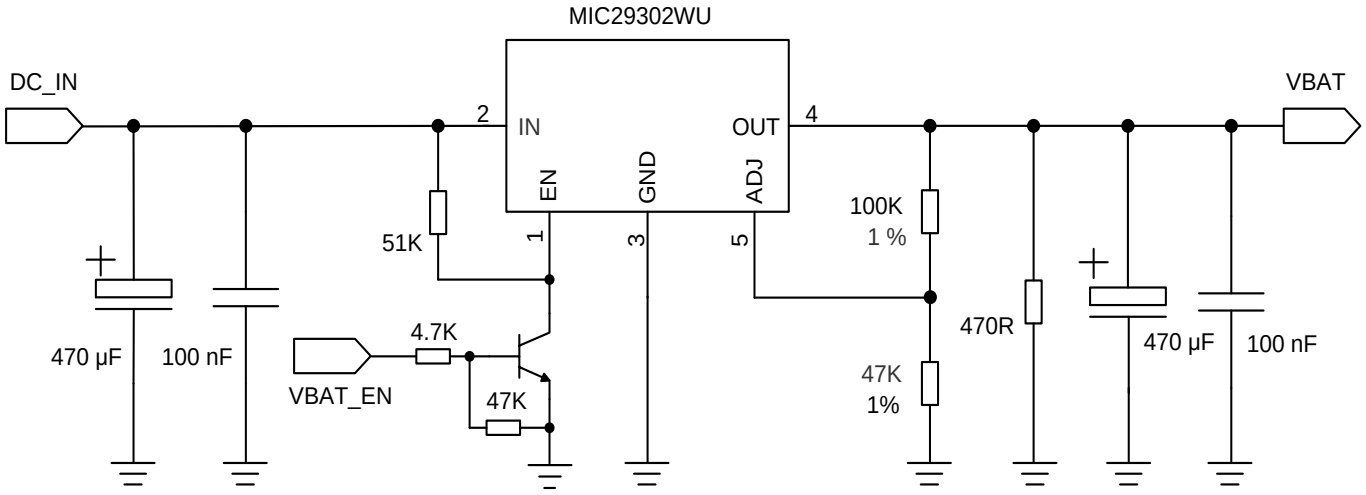


**Figure 4: Power Supply Reference Design**

## 4.2. Turn on/off

### 4.2.1. Turn on/off with PWRKEY

The turn-on/off methods of UC200A series are the same as UC200T series.

The modules can be turned on or turned off after pressing PWRKEY for a certain time. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

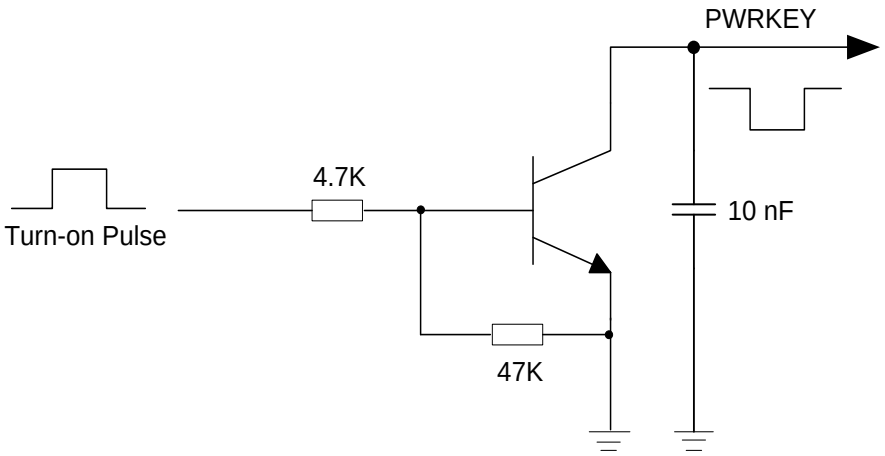


**Figure 5: Turn on/off the Module with a Driving Circuit**

Another way to control the PWRKEY is using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection.

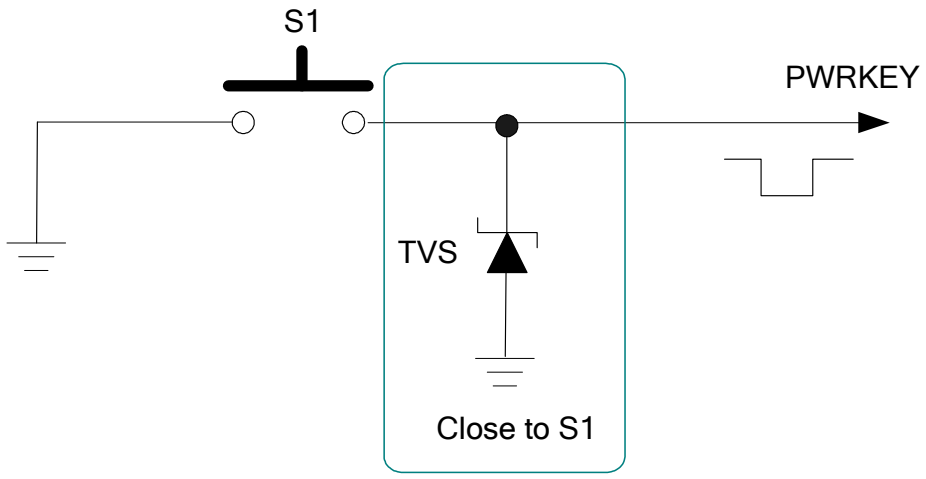


**Figure 6: Turn on/off the Module with a Button**

The power-up scenario is illustrated in the following figure.

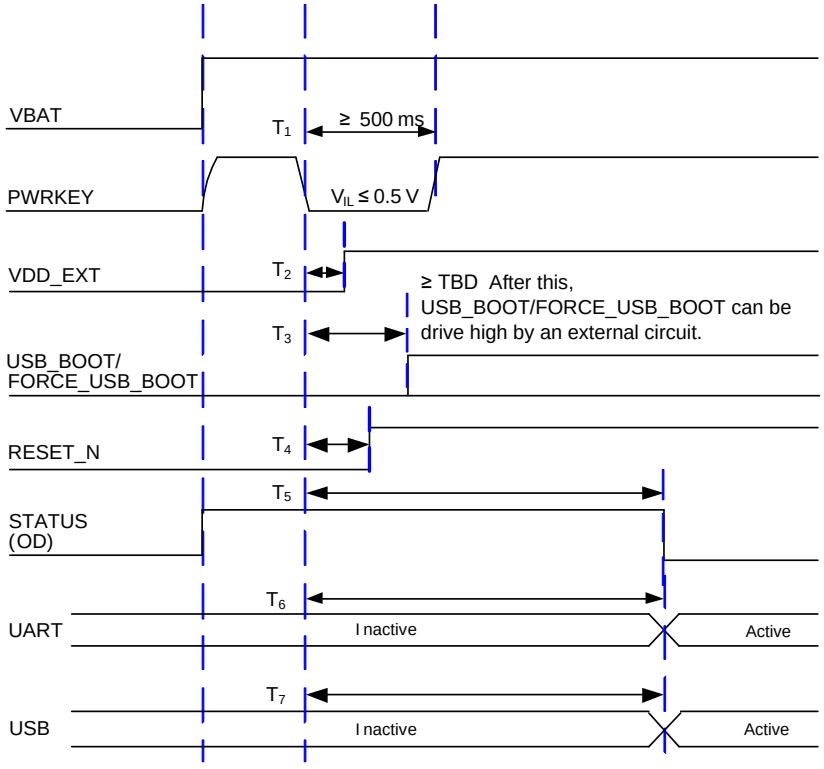


**Figure 7: Power-up Timing (UC200A & UC200T Series)**

The power-up timing of UC200A and UC200T series is illustrated in the table below.

**Table 9: Power-up Timing of UC200A &UC200T series**

| Module | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_5$ | $T_6$ | $T_7$ |
|---|---|---|---|---|---|---|---|
| UC200A Series | ≥ 500 ms | Typ. 5 ms | ≥ 100 ms | Typ. 22 ms | ≥ 10 s | ≥ 10 s | ≥ 10 s |
| UC200T Series | ≥ 500 ms | Typ. 5 ms | ≥ 100 ms | Typ. 22 ms | ≥ 10 s | ≥ 10 s | ≥ 10 s |

**NOTE**

1. Make sure that the VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 4.7 kΩ resistor if the module needs to be powered on automatically and shutdown is not needed.

The following are reference design circuits of the power-down for UC200A and UC200T series.

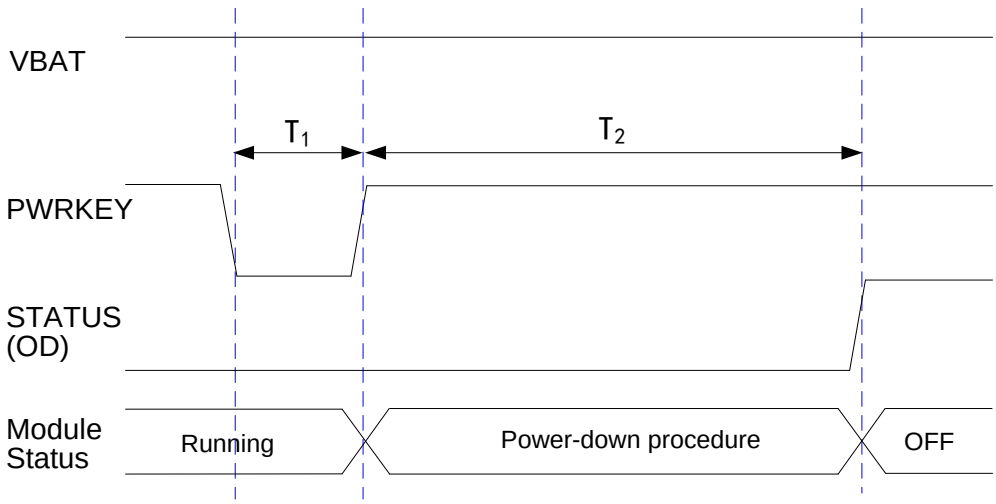


**Figure 8: Power-down Timing (UC200A &UC200T Series)**

The power-down timing of UC200A and UC200T series is illustrated in the table below.

**Table 10: Power-down Timing of UC200A & UC200T Series**

| Module | $T_1$ | $T_2$ |
|---|---|---|
| UC200A Series | ≥ 650 ms | ≥ 2 s |

| | | |
|---|---|---|
| UC200T Series | ≥ 650 ms | ≥ 2 s |

### 4.2.2. Turn off with AT Command

It is safe to use **AT+QPOWD** to turn off the module**,** which is similar to turning off the module via PWRKEY Pin. See ***document [1]*** for details about **AT+QPOWD**.

**NOTE**

1. To avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off module with AT command, please keep PWRKEY at a high level after the execution of power-off command. Otherwise, the module will be turned on again after successfully turn-off.

## 4.3. Reset

UC200A and UC200T series modules can be reset by driving RESET_N to a low level voltage for a certain time. An open drain/collector driver can be used to control the RESET_N.

A simple reference circuit is illustrated in the following figure.

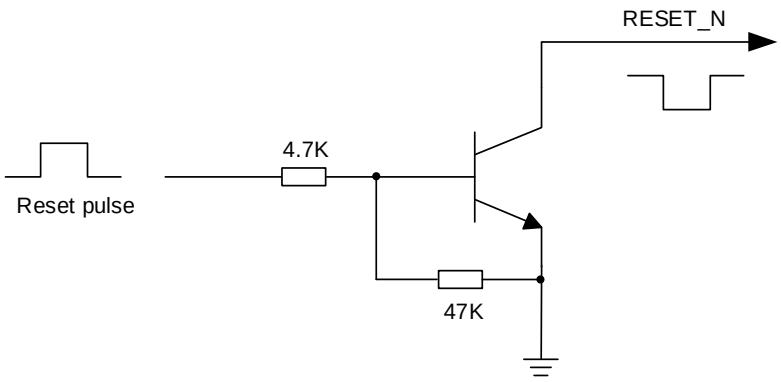


**Figure 9: Reference Circuit of RESET_N with a Driving Circuit**

Another way to control RESET_N is using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection.

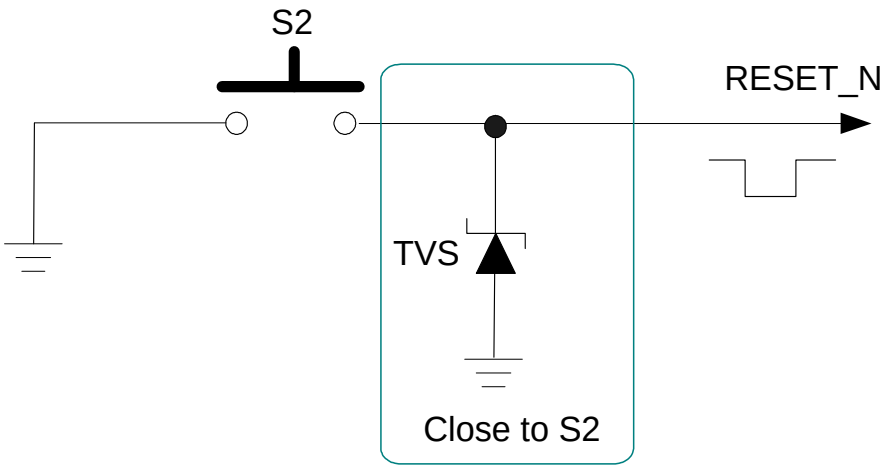


**Figure 10: Reference Circuit of RESET_N with Button**

The reset scenario is illustrated in the following figure.

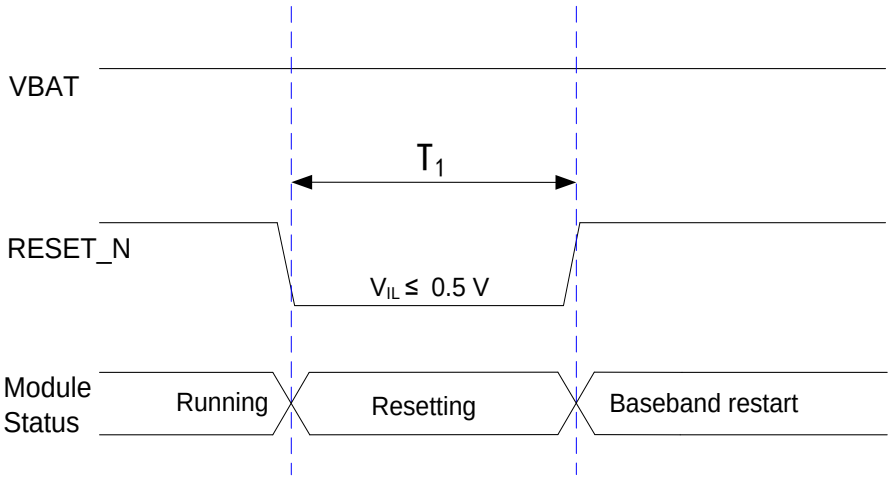


**Figure 11: Reset Timing (UC200A & UC200T Series)**

The reset timing of UC200A and UC200T series is illustrated in the table below.

**Table 11: Reset Timing of UC200A & UC200T Series**

| Module | $T_1$ |
|---|---|
| UC200A Series | ≥ 300 ms |
| UC200T Series | ≥ 300 ms |

**NOTE**

1. For UC200A & UC200T series, driving RESET_N low will only reset the BB chip inside the modules, power management chip will not be reset.
2. For UC200A & UC200T series, the BB chip is in reset state when driving RESET_N low, and the chip system will restart after releasing.
3. For UC200A & UC200T series, the voltage of REST_N will rise after driving RESET_N low.
4. Please ensure that there is no large capacitance with the maximum value exceeding 10 nF on PWRKEY and RESET_N pins.

## 4.4. (U)SIM interfaces

UC200A and UC200T series modules both support 1.8/3.0 V (U)SIM card by default.

(U)SIM interfaces of UC200A and UC200T series are compatible with each other, and the modules support (U)SIM card hot-plug via the USIM_DET pin.

The following figure shows a compatible design for (U)SIM interface with an 8-pin (U)SIM card connector.

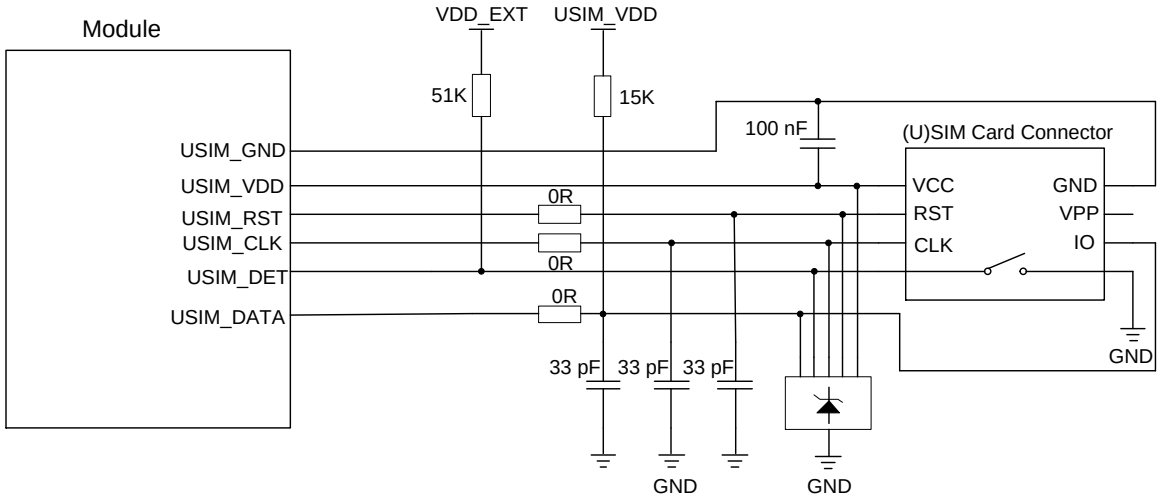


**Figure 12: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector**

If (U)SIM card detection function is not needed, please keep USIM_DET disconnected. The following figure shows a compatible design for (U)SIM interface with a 6-pin (U)SIM card connector.

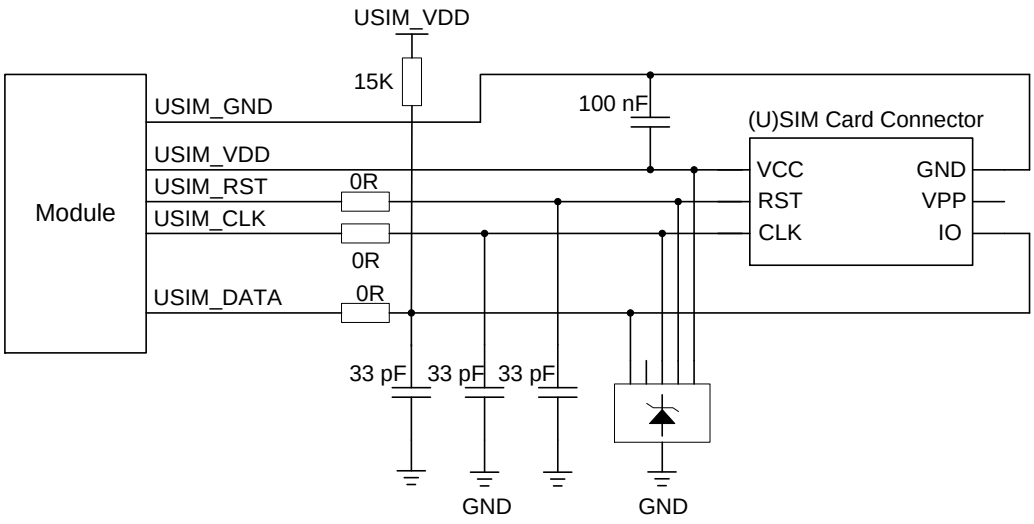


**Figure 13: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector**

## 4.5. USB Interface

UC200A/UC200T series modules contain one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high speed (480 Mbps) and full speed (12 Mbps) modes. It is recommended to reserve test points for debugging and firmware upgrade in your designs.

The following figure shows a reference circuit of USB interface.

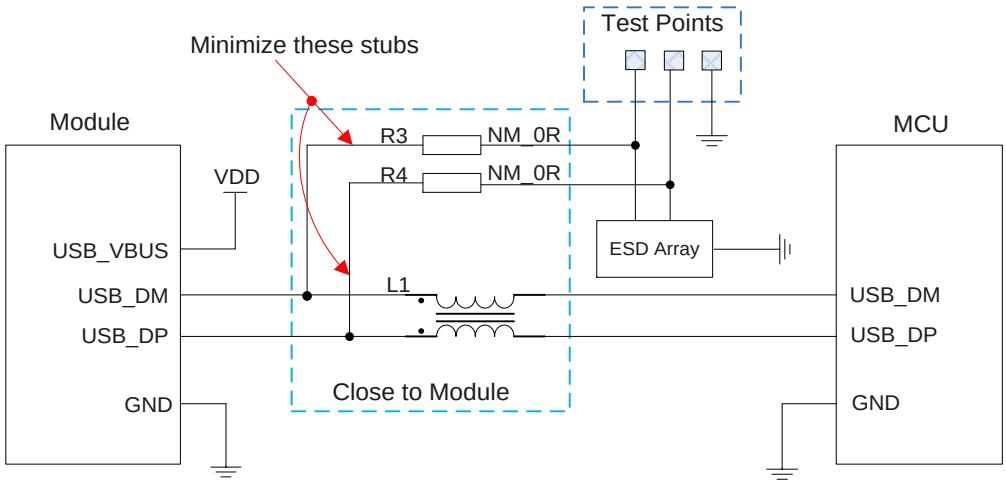


**Figure 14: Reference Circuit of USB Interface**

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series

between the module and the test points to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1, R3 and R4 components must be placed close to the module, and R3 and R4 should be placed close to each other, and the extra stubs of trace must be as short as possible.

The following principles should be complied with when designing the USB interface, to meet USB specifications.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Pay attention to the selection of the ESD component on the USB data line. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB interface.

## 4.6. UART Interfaces

UC200A and UC200T series modules provide two UART interfaces: main UART interface and debug UART interface. The following shows their features:

- Main UART: supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps baud rates. Its baud rate is 115200 bps by default. It is used for data transmission and AT command communication.
- Debug UART: supports 115200 bps baud rate. It is used for the output of partial logs on UC200A and UC200T series.
- UC200A and UC200T series both support RTS and CTS hardware flow control.

UC200A and UC200T series modules provide 1.8 V UART interfaces. A voltage-level translator should be used if the application is equipped with a 3.3 V UART interface. The following figure shows a reference design.

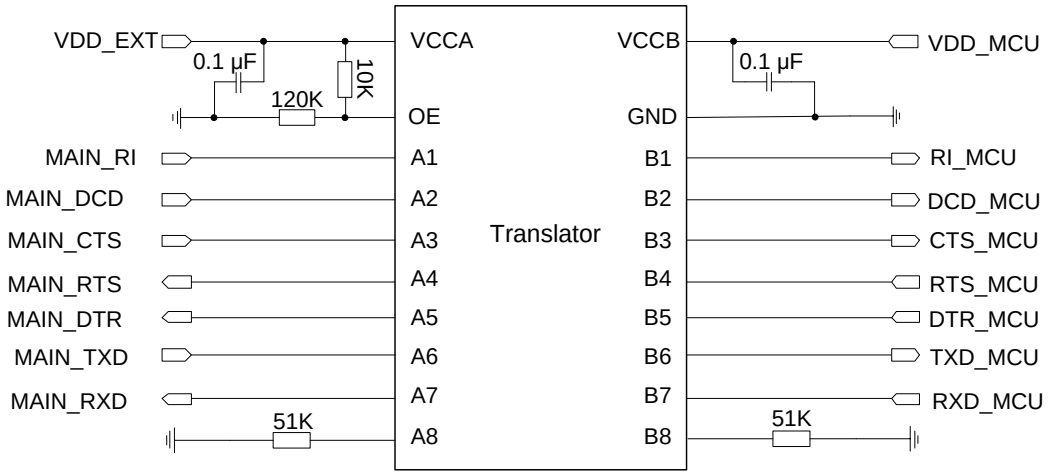


**Figure 15: Reference Circuit with Translator Chip**

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

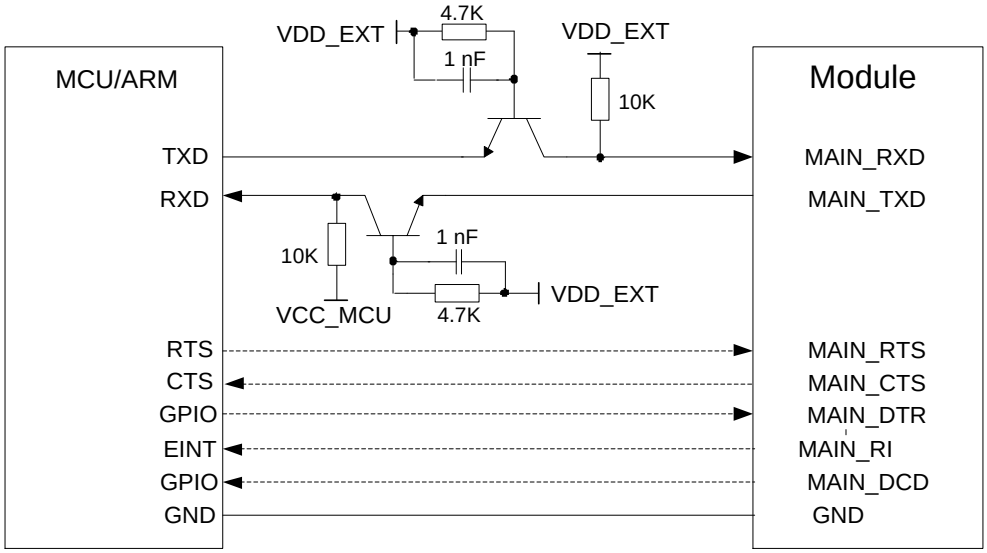


**Figure 16: Reference Circuit with Transistor Circuit**

**NOTE**

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the host's CTS, and the module's RTS is connected to the host's RTS and pay attention to the direction of input and output.

## 4.7. PCM and I2C Interfaces

UC200A & UC200T series modules provide one I2C interface and one Pulse Code Modulation (PCM) interface. The following table shows the difference.

**Table 12: Pin Difference of PCM Interface**

| Function | UC200A Series | UC200T Series |
|---|---|---|
| PCM Interface | ● Used for audio function with external Codec<br>● Supports 16-bit linear data format<br>● Supports short frame synchronization mode<br>● Supports master and slave modes | ● Used for audio function with external Codec<br>● Supports 16-bit linear data format<br>● Supports short frame synchronization mode<br>● Supports master and slave modes |

The following figure shows a reference design of PCM and I2C interfaces with external Codec IC.

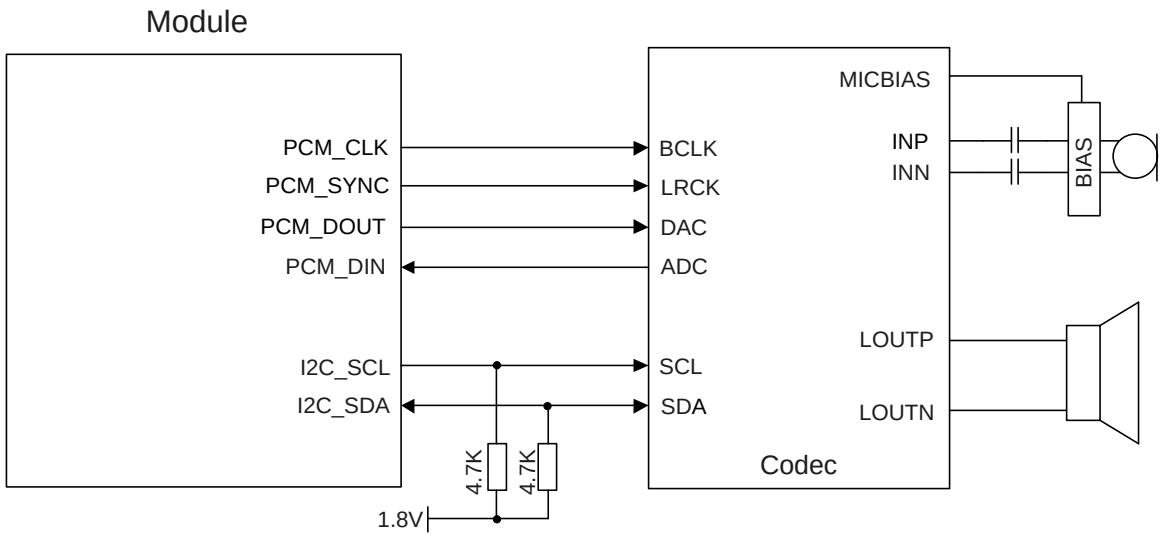


**Figure 17: Reference Circuit of PCM and I2C Interfaces**

**NOTE**

1. It is recommended to reserve RC (R = 22 Ω, C = 22 pF) circuit on PCM signal traces, and place it close to Codec, especially on PCM_CLK.
2. UC200A and UC200T series modules can only act as master device in applications related to I2C interface.

## 4.8. ADC interface

The following table compares the ADC interface of UC200A and UC200T series.

**Table 13: Pin Difference of ADC interface**

| Function | UC200A Series | UC200T Series |
|---|---|---|
| ADC interface | ● The modules provide two analog-to-digital converter interfaces.<br>● Voltage range: 0–VBAT_BB<br>● Resolution: 12 bits | ● The modules provide two analog-to-digital converter interfaces.<br>● Voltage range: 0–VBAT_BB<br>● Resolution: 12 bits |

**NOTE**

1. It is recommended to use resistor divider circuit for ADC application.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. The input voltage of ADC should not exceed its corresponding voltage range.

## 4.9. Network Status Indication

UC200A and UC200T series modules provide two pins: NET_MODE and NET_STATUS. The network indication pins can drive the network status indicators.

The following tables describe logic level changes in different network status.

**Table 14: Working State of the Network Connection Status/Activity Indication**

| Pin Name | Working State | Indicate Indication Network Status |
|---|---|---|
| NET_MODE | Always High | Registered on LTE network |
| | Always Low | Others |
| NET_STATUS | Flicker slowly (200 ms High/1800 ms Low) | Network searching |
| | Flicker slowly (1800 ms High/200 ms Low) | Idle |
| | Flicker quickly (125 ms High/125 ms Low) | Data transfer is ongoing |

| | |
|---|---|
| Always high | Voice calling |

A reference circuit is shown as below.

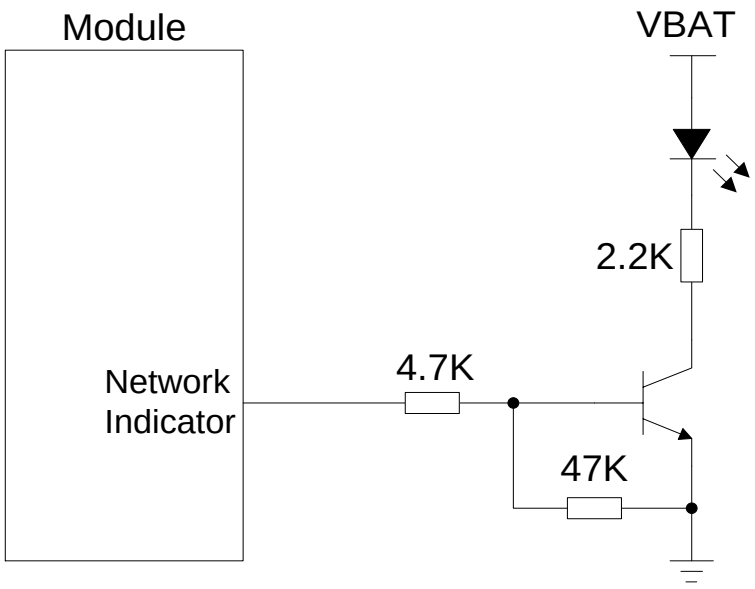


**Figure 18: Reference Circuit of the Network Status Indication**

## 4.10. STATUS

The STATUS pin of UC200A and UC200T series is an open drain output for the module's operation status indication.

It can be connected to a GPIO of DTE with a pulled-up resistor, or as an LED indication circuit as below. It will output low level when module is powered on successfully. Otherwise, STATUS will be in high-impedance state.

The following figure shows different circuit designs of STATUS, and you can choose either one according to the application demands.

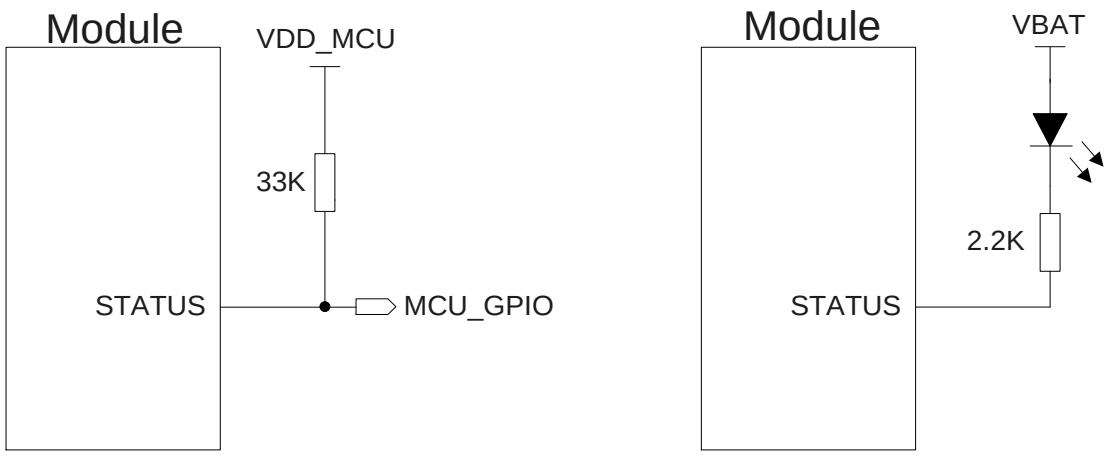


**Figure 19: Reference Circuits of STATUS (UC200A & UC200T Series)**

**NOTE**

STATUS cannot indicate the modules' shutdown status when VBAT is removed.

## 4.11. FORCE_USB_BOOT/USB_BOOT Interface

FORCE_USB_BOOT and USB_BOOT have the same function. UC200A and UC200T series support the function of FORCE_USB_BOOT/USB_BOOT. Developers can pull up FORCE_USB_BOOT to 1.8 V before VDD_EXT is powered on, and the module will enter emergency download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

The following circuits show reference circuit of FORCE_USB_BOOT/USB_BOOT in UC200A and UC200T series.

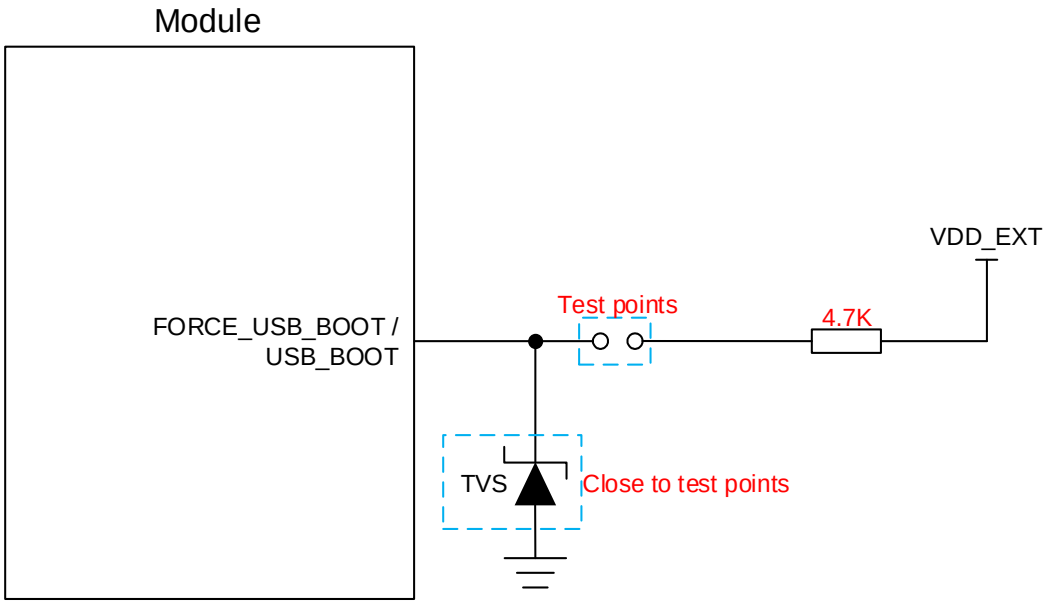


**Figure 20: Reference Circuit of FORCE_USB_BOOT/USB_BOOT Interface**

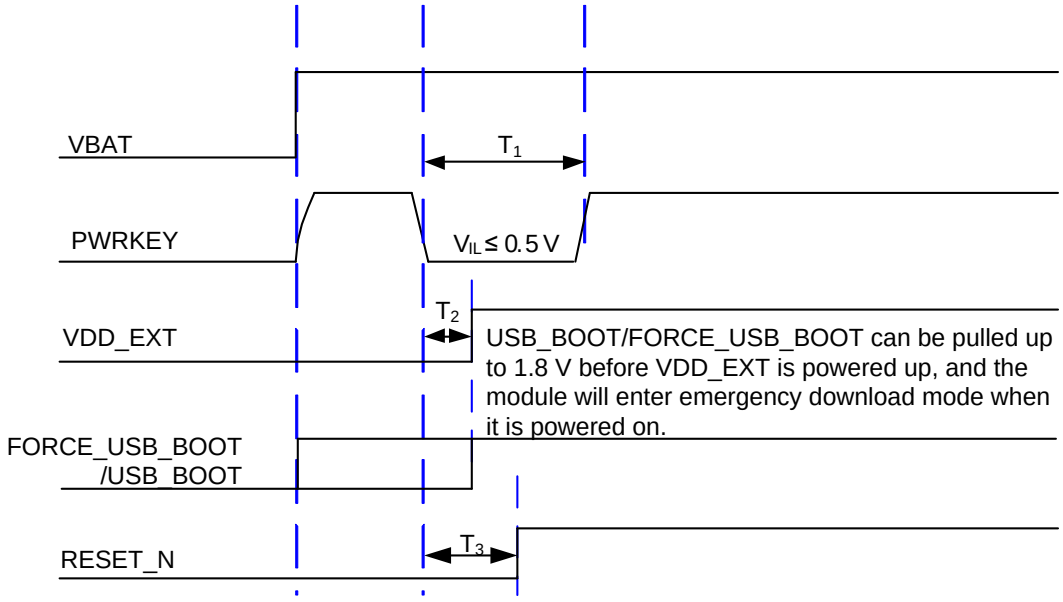


**Figure 21: Timing Sequence for Entering Emergency Download Mode (UC200A & UC200T Series)**

**NOTE**

1. Ensure VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up FORCE_USB_BOOT to 1.8 V before

powering up VBAT. Directly connect the test points as shown in ***Figure 20*** can manually force the module into download mode.

3. FORCE_USB_BOOT/USB_BOOT cannot be pulled up before startup.

## 4.12. Antenna Interface

Reference circuit of ANT_MAIN of UC200A and UC200T series is illustrated in the following figure. It is recommended to reserve a π-type matching circuit for better RF performance. The capacitors are not mounted by default.

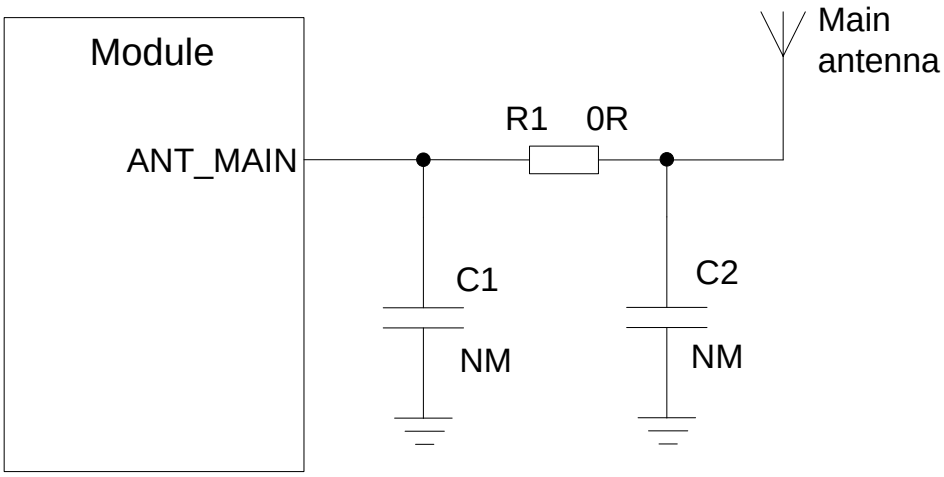


**Figure 22: RF Antenna Interface (UC200A & UC200T Series)**

**NOTE**

1. For better Rx sensitivity, the distance between the main antenna and the Rx-diversity antenna should be appropriate.
2. The π-type matching components (R1, C1, C2) should be placed as close to the antenna as possible.

# 5 Mechanical Information

This chapter mainly introduces the recommended footprint and stencil design for UC200A and UC200T series modules. All dimensions are measured in mm, and the dimensional tolerances are ±0.2 mm unless otherwise specified.

The thickness of stencil for UC200A and UC200T series modules is recommended to be 0.18–0.20 mm. For more details, see ***document [2]***.

## 5.1. Recommended Compatible Footprint

The following figure shows the bottom views of UC200A and UC200T series.

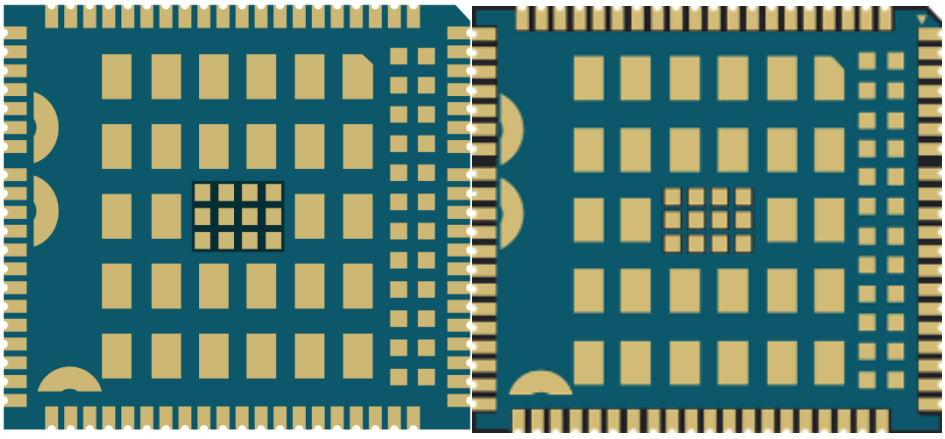

**Figure 23: Bottom Views of UC200A/UC200T Series**

**NOTE**

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

The following figure shows the recommended compatible footprint of UC200A and UC200T series.

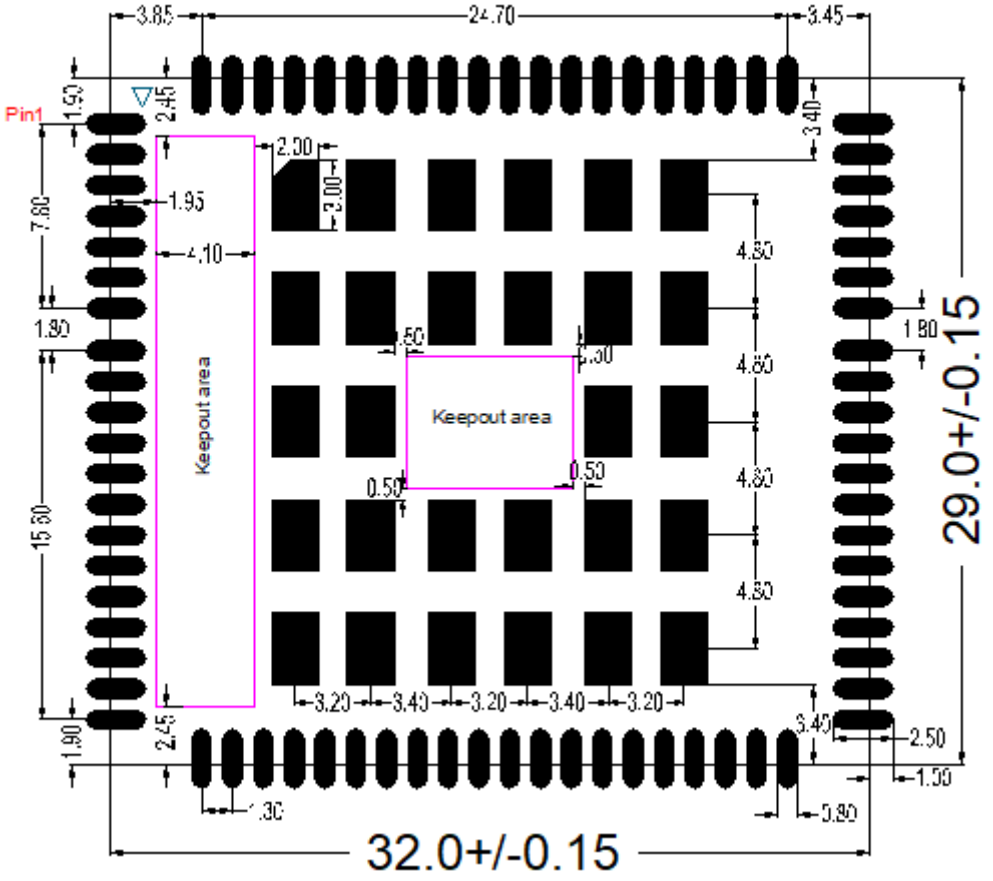


**Figure 24: Recommended Footprint of UC200A/UC200T Series (Top View)**

**NOTE**

1. The pad size of UC200A and UC200T series are the same.
2. The actual size of UC200A and UC200T is 29.0 mm × 32.0 mm × 2.4 mm.
3. The pin of 73–84, 117–140 included in the keepout area should not be used when designing schematics and PCB layout.
4. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

# 6 Appendix References

**Table 15: Related Documents**

| Document Name |
|---|
| [1] Quectel_UC200T_AT_Command_Manual |
| [2] Quectel_Module_Secondary_SMT_Application_Note |
| [3] Quectel_UC200T_Series_Hardware_Design |
| [4] Quectel_UC200A_Series_Hardware_Design |

**Table 16: Terms and Abbreviations**

| Abbreviation | Description |
|---|---|
| ADC | Analog-to-Digital Converter |
| bps | Bits Per Second |
| CDMA | Code Division Multiple Access |
| CTS | Clear To Send |
| ESD | Electrostatic Discharge |
| EVDO | Evolution-Data Optimized |
| FDD | Frequency Division Duplex |
| GSM | Global System for Mobile Communications |
| HSPA | High Speed Packet Access |
| LDO | Low-dropout Regulator |
| LTE | Long Term Evolution |
| PCB | Printed Circuit Board |

| | |
|---|---|
| PCM | Pulse Code Modulation |
| RF | Radio Frequency |
| RTS | Request To Send |
| TDD | Time Division Duplexing |
| TD-SCDMA | Time Division-Synchronous Code Division Multiple Access |
| UART | Universal Asynchronous Receiver/Transmitter |
| USB | Universal Serial Bus |
| (U)SIM | (Universal) Subscriber Identity Module |
| WCDMA | Wideband Code Division Multiple Access |
| WLAN | Wireless Local Area Network |