TOSHIBA

Date : June 15, 2022
Specification number : H22293193

SPECIFICATION

Your product number : 0087-0426-2
Product number : TMPM3HNFDFG(DBB)

This specification is approved and confirmed by both

ELECTRONICS SOURCE CO., LTD.

and TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION.

ELECTRONICS SOURCE CO., LTD.

TOSHIBA ELECTRONIC DEVICES &
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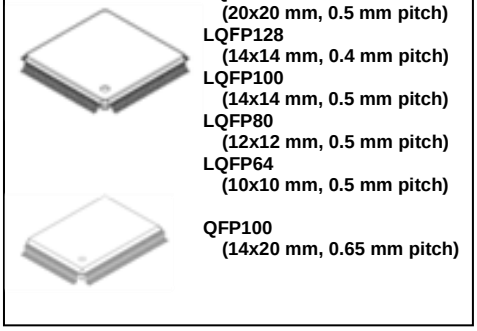
CMOS Digital Integrated Circuit Silicon Monolithic

TMPM3H Group(2)



LQFP144
(20x20 mm, 0.5 mm pitch)
LQFP128
(14x14 mm, 0.4 mm pitch)
LQFP100
(14x14 mm, 0.5 mm pitch)
LQFP80
(12x12 mm, 0.5 mm pitch)
LQFP64
(10x10 mm, 0.5 mm pitch)

QFP100
(14x20 mm, 0.65 mm pitch)

General Description

- Arm ® Cortex®-M3 core. Operation frequency: 1 to 80 MHz.
  Operation voltage: 2.7 to 5.5V
- Code flash: 256KB to 512KB. Data flash: 32KB.
- Package: 64-pin to 144-pin. 6 types of packages are available.

Applications

Widely used for consumer products and industrial products including home appliances, OA equipment, household equipment, AV devices, and motor control devices.

Features

- ARM Cortex-M3 core
  - Operation frequency: 1 to 80 MHz
  - Memory Protection Unit (MPU)
- Low-power consumption mode
  - Operation voltage: 2.7 to 5.5V
  - Low-power consumption operation: IDLE, STOP1,STOP2
- Operation temperature: -40 to +85°C
- Internal memory
  - Code flash: 256KB to 512 KB, rewritable up to 10,000 times
  - Data flash: 32 KB, rewritable up to 100,000 times
  - Data flash is rewritable in parallel with instruction execution
  - RAM: 64KB(with Parity) and Backup RAM 2 KB
- Clock
  - External High-speed Oscillator: 6 MHz to 12 MHz(Ceramic, Crystal)
  - External High-speed clock input: 6 to 20 MHz
  - Internal High-speed Oscillator (IHOSC1): 10 MHz, user trimming function
  - PLL: 80 MHz output
  - External Low-speed Oscillator: 32.768kHz
- Oscillation Frequency Detector (OFD): Abnormal system clock detection
- Voltage Detection circuit (LVD): 8 level, Generate interrupts and reset outputs
- Interruption
  - External: 12 to 32 factors, with DNF
  - internal: 116 to 136 factors
- I/O ports: GPIO: 56 to 134 (Include Input only: 4, Output only: 1)
  - pull-up/pull-down resistor,Open-drain,5V-tolerant
- On chip Debug(JTAG/SW)
- Trigger Selection Circuit(TRGSEL)
  - Expand Trigger request for DMAC, Timer, others
- DMA Controller(DMAC)
  - DMA requests: 2units,62 to 64 factors, internal/external triggers
- Universal Asynchronous Receiver Transmitter(UART): 6 channels
  - 2.5Mbps(Max),FIFO(Send 8-stage, Receive 8-stage)
- Serial Peripheral Interface(TSPI): 1 to 5 channels
  - SIO/SPI mode,20Mbps(MAX),FIFO(Send 16bitx8,Receive 16bitx8)
- I^2C Interface(I2C): 2 to 4 channels
  - Multi Master, Release function for Low Power Mode
- Comparator: 1 channels. EMG signal output to A-PMD
- 8-bit DA Converter(DAC): 2 channels
- 12-bit ADC(ADC): 10 to 21 channels analog inputs
  - Sample-and-hold circuit
  - Conversion time: 1.5μs@ADCLK=40MHz
  - Self-diagnosis support function
- Advanced Programmable Motor Control Circuit (A-PMD): 1 channel
  - 3 phase PWM output, Synchronized with 12-bit ADC
  - Emergency stop function by external inputs (EMG0 pin, OVV0 pin)
- Advanced Encoder Input Circuit (A-ENC): 1 channel
  - Encoder/sensor (3 types)/Timer /Phase counter mode
- 32bit Timer Event Counter (T32A)
  - 8 channels as 32-bit Timers:16 channels as 16-bit Timers
  - Interval Timer, event counter, input capture, phase difference input, PPG output, Sync Start, Trigger Start
- Real Time Clock (RTC): 1 channel
- Watchdog Timer (SIWDT): 1 channel
  - Clock system other than the system clock can be selected
  - Clear window, interrupts and reset output
- Remote control signal preprocessor (RMC): 1 channel
- CRC calculation circuit(CRC): 1channel, CRC32, CRC16

Commercial Production Date: 2018-03

Products Lists Categorized by Functions

The product under development is contained in this table.
For the newest status of each product, Please contact your sales representative.

Table 1 Products List

Built-in Functions		TMPM3HQFDFG TMPM3HQFZFG TMPM3HQFYFG	TMPM3HPFDFG TMPM3HPFZFG TMPM3HPFYFG	TMPM3HNFDFG TMPM3HNFZFG TMPM3HNFYFG	TMPM3HNFDDFG TMPM3HNFZDFG TMPM3HNFYDFG	TMPM3HMFDFG TMPM3HMFZFG TMPM3HMFYFG	TMPM3HLFDUG TMPM3HLFZUG TMPM3HLFYUG
Memory	Code Flash (KB)	512 384 256	512 384 256	512 384 256	512 384 256	512 384 256	512 384 256
	Data Flash (KB)	32 32 32	32 32 32	32 32 32	32 32 32	32 32 32	32 32 32
	RAM (KB)	64 64 64	64 64 64	64 64 64	64 64 64	64 64 64	64 64 64
	Backup RAM (KB)	2	2	2	2	2	2
I/O port	PORT (Pin)	134	118	92	92	72	56
External interrupt	INT (Pin)	32	29	19	19	15	12
DMA	DMAC (ch)	64	64	64	64	62	54
Timer function	T32A (ch)	8	8	8	8	8	8
	RTC (ch)	1	1	1	1	1	1
Serial communication function	UART (ch)	6	6	6	6	6	6
	I^2C (ch)	4	4	3	3	3	2
	TSPI (ch)	5	5	4	4	4	1
Analog function	12-bit ADC (ch)	21	19	13	13	10	10
	8-bit DAC (ch)	2	2	2	2	2	2
	Comparator(ch)	1	1	1	1	1	1
Motor Control Receiver peripherals	A-ENC (ch)	1	1	1	1	1	1
	A-PMD (ch)	1	1	1	1	1	1
Remote Control Receiver peripherals	RMC (ch)	1	1	1	1	1	1
Other peripherals	CRC(ch)	1	1	1	1	1	1
System function	LVD (ch)	1	1	1	1	1	1
	SIWDT (ch)	1	1	1	1	1	1
	OFD (ch)	1	1	1	1	1	1
	POR	1	1	1	1	1	1
Debug interface	Debug	JTAG/SW TRACE(4bit)	JTAG/SW TRACE(4bit)	JTAG/SW TRACE(4bit)	JTAG/SW TRACE(4bit)	JTAG/SW TRACE(2bit)	JTAG/SW
Package	Package type	LQFP144 (20 mm x 20 mm, 0.5 mm pitch)	LQFP128 (14 mm x 14 mm, 0.4 mm pitch)	LQFP100 (14 mm x 14 mm, 0.5 mm pitch)	QFP100 (14 mm x 20 mm, 0.65 mm pitch)	LQFP80 (12 mm x 12 mm, 0.5 mm pitch)	LQFP64 (10 mm x 10 mm, 0.5 mm pitch)
	Package name	P-LQFP144-2020 -0.50-002	P-LQFP128-1414 -0.40-001	P-LQFP100-1414 -050-002	P-QFP100-1420 -0.65-001	P-LQF80-1212 - 0.50-003	P-LQFP64-1010 - 0.50-003

Preface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the "0b" when the number of bit can be distinctly understood from a sentence.
- "_N" is added to the end of signal names to indicate low active signals.
- It is called "assert" that a signal moves to its active level, "deassert" to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- "n" substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, "x" means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] →[ADxCR0]***
  In case of channel, "x" means 0, 1, and 2 . . .
  Example: [***T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

The flash memory uses the Super Flash® technology licensed from Silicon Storage Technology(SST), Inc.
Super Flash® is registered trademark of Silicon Storage Technology, Inc.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

The following words are terms or abbreviations mainly used in this datasheet.

ADC	Analog to Digital Converter
A-ENC	Advanced Encoder input Circuit
A-PMD	Advanced Programmable Motor Control Circuit
COMP	Comparator
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DMAC	Direct Memory Access Controler
DNF	Digital Noise Filter
EHOSC	External High speed Oscillator
ELOSC	External Low speed Oscillator
Fm	I^2C Fast Mode
IHOSC	Internal High speed Oscillator
INT	Interrupt
I^2C	Inter-Integrated Circuit
I2CS	I^2C wake-up circuit from Stand-by mode
LVD	Voltage Detection Circuit
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
RAMP	RAM Parity
RMC	Remote control signal preprocessor
RTC	Real Time Clock
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection circuit
TRM	Trimming circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Block Diagram

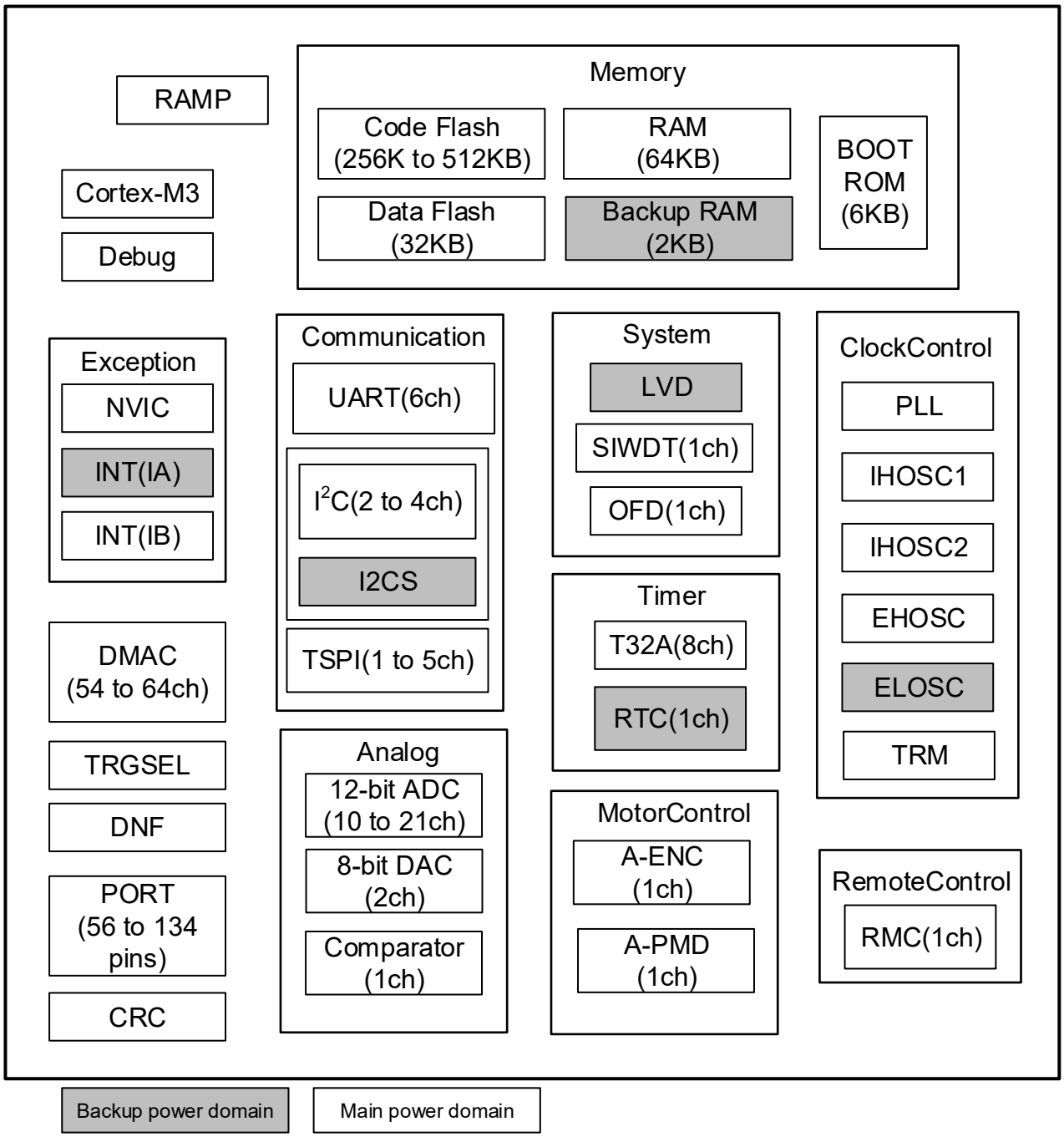
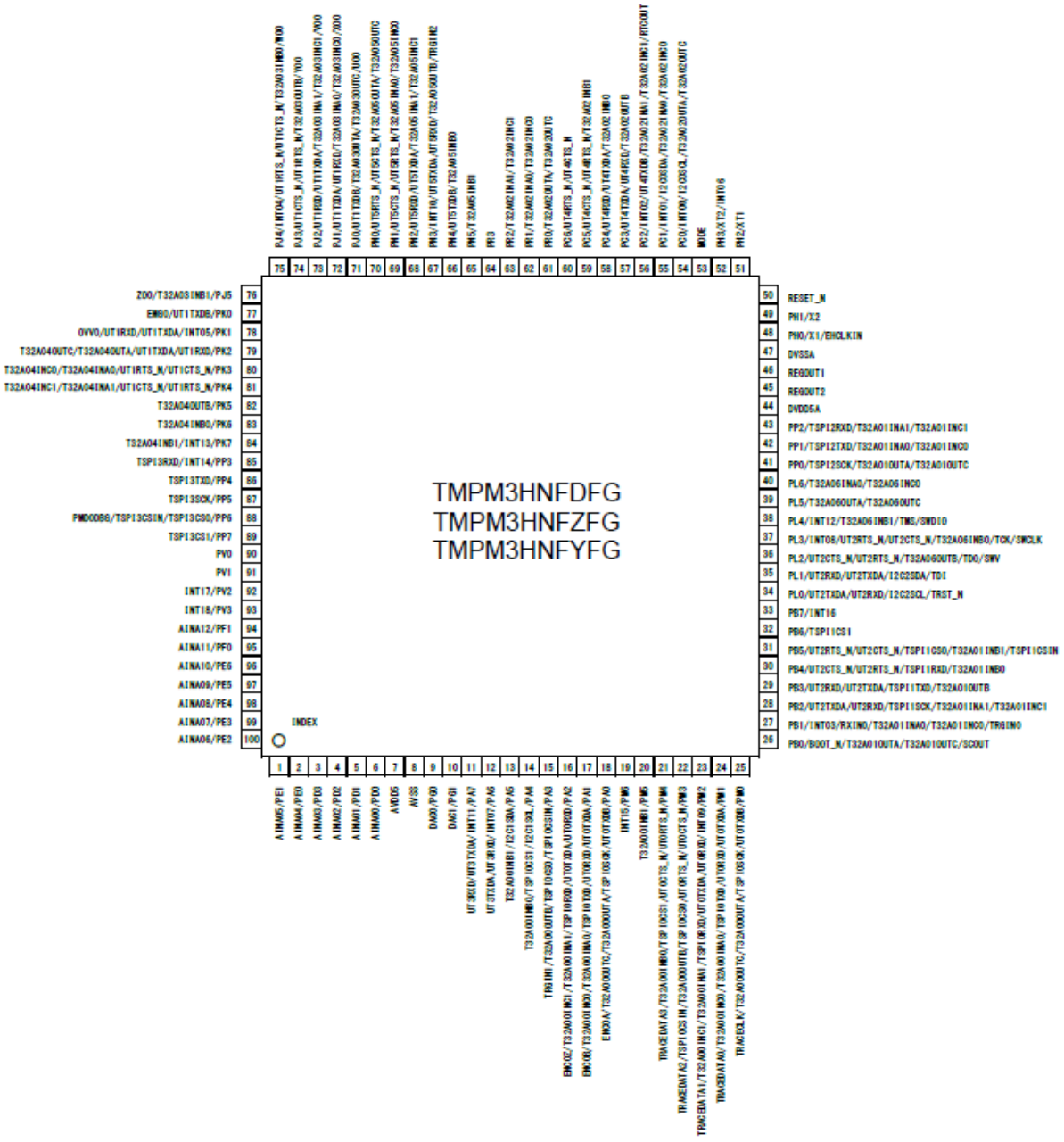


Figure 1.1 Block diagram of the TMPM3H Group(2)

2.Pin Assignment

2.1. LQFP100



3. Memory Map

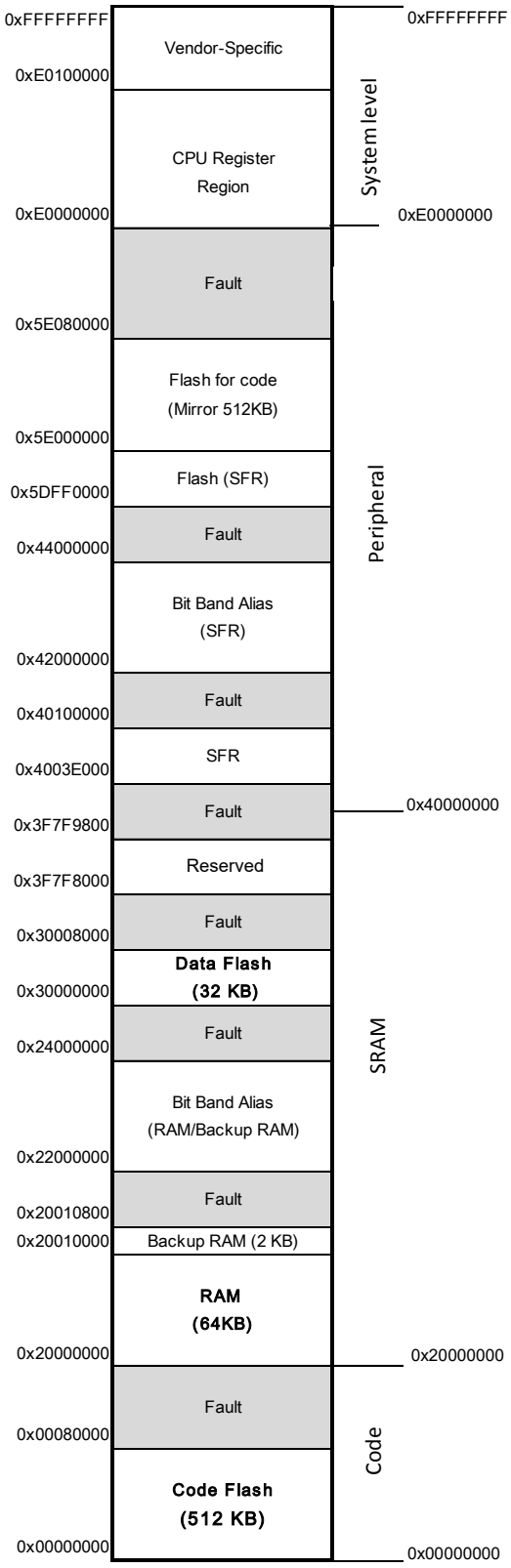


Figure 3.1 Example of the TMPM3HQFDFG

3.1. List of Memory Sizes

Table 3.1 Memory sizes and addresses

Products			TMPM3HQFDFG TMPM3HPFDFG TMPM3HNFDFG TMPM3HNFDDFG TMPM3HMFDFG TMPM3HLFDUG	TMPM3HQFZFG TMPM3HPFZFG TMPM3HNFZFG TMPM3HNFZDFG TMPM3HMFZFG TMPM3HLFZUG	TMPM3HQFYFG TMPM3HPFYFG TMPM3HNFYFG TMPM3HNFYDFG TMPM3HMFYFG TMPM3HLFYUG
Peripheral region	Code Flash (Mirror)	Size	512KB	384KB	256KB
		START	0x5E000000	0x5E000000	0x5E000000
		END	0x5E07FFFF	0x5E05FFFF	0x5E03FFFF
SRAM region	Data Flash	Size	32KB		
		START	0x30000000		
		END	0x30007FFF		
	Backup RAM	Size	2KB		
		START	0x20010000		
		END	0x200107FF		
	RAM	Size	64KB		
		START	0x20000000		
		END	0x2000FFFF		
Code Region	Code Flash	Size	512KB	384KB	256KB
		START	0x00000000	0x00000000	0x00000000
		END	0x0007FFFF	0x0005FFFF	0x0003FFFF

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 7.1 Absolute maximum ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		DVDD5A DVDD5B	-0.3 to 6.0	V
		AVDD5	-0.3 to DVDD5 (Note1)	
Capacitor pin voltage for voltage maintenance		REGOUT1	-0.3 to 1.7	V
		REGOUT2	-0.3 to 3.9	
Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PR0 to 7, PV0 to 7, PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 7, PT0 to 7, PU0 to 5, MODE, RESET_N,BOOT_N	V_{IN1} V_{IN2}	-0.3 to DVDD5+0.3(≤6.0V) (Note1)	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{IN3}	-0.3 to AVDD5+0.3(≤6.0V)	
	PA4 to 5	V_{IN4}	-0.3 to 6.0	
Low level output current	Per Pin, PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PR0 to 7, PV0 to 7, PA0 to 3, PA6 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 7, PT0 to 7, PU0 to 5, PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	I_{OL}	5	mA
	Per Pin, PA4 to 5	I_{OL4}	25	
	Total	ΣI_{OL}	50	
High level output current	Per pin, PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PR0 to 7, PV0 to 7, PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 7, PT0 to 7, PU0 to 5, PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	I_{OH}	-5	
	Total	ΣI_{OH}	-50	
Power consumption (Ta= 85°C)		PD	600	mW
Soldering temperature		T_{SOLDER}	260	°C
Storage temperature		T_{STG}	-55 to 125	°C
Operational temperature		T_{OPR}	-40 to 85	°C

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B. Apply the same voltage to DVDD5 and AVDD5.

Note2: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

7.2. DC Electrical Characteristics (1/2)

4.5V ≤ DVDD5=AVDD5 ≤ 5.5V
DVSS = AVSS=0V
Ta=-40 to 85 °C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A,DVDD5B, AVDD5	VDD	f_{OSC} = 6 to 12MHz f_{sys} = 1 to 80MHz fs = 30 to 34kHz	4.5	-	5.5	V
Low level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N,	V_{IL1}		-0.3	-	DVDD5×0.25	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, BOOT_N	V_{IL2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{IL3}				AVDD5×0.25	
	PA4 to 5	V_{IL4}				DVDD5×0.3	
High level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N,	V_{IH1}		DVDD5×0.75	-	DVDD5+0.3	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, BOOT_N	V_{IH2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{IH3}		AVDD5×0.75		AVDD5+0.3	
	PA4 to 5	V_{IH4}		DVDD5×0.7		DVDD5+0.3	
Low level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 3, PA6 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5,	V_{OL1} V_{OL2}	DVDD5=4.5V I_{OL} = 1.6mA	-	-	0.4	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{OL3}	AVDD5=4.5V I_{OL}=1.6mA	-	-	0.4	
	PA4 to 5	V_{OL4}	DVDD5=4.5V I_{OL}=8mA	-	-	1.0	
High level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5,	V_{OH1} V_{OH2}	DVDD5=4.5V I_{OH}=-1.6mA	DVDD5-0.4	-	-	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{OH3}	AVDD5=4.5V I_{OH}=-1.6mA	AVDD5-0.4	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5V, unless otherwise noted.

Note 3: Apply the same voltage to DVDD5 and AVDD5.

4.5V ≤DVDD5=AVDD5≤ 5.5 V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	0.05	5	μA
Output leak current		I_{LO}	0.2 ≤VIN ≤DVDD5-0.2 0.2 ≤ VIN ≤ AVDD5-0.2	-10	0.05	10	
Schmitt trigger Input width		VTH	DVDD5=AVDD5=5V	-	1	-	V
Reset pull-up resistor		R_{RST}		25	30	100	kΩ
Programmable pull-up/-down resistor		P_{KH}	Pull-up	25	30	100	kΩ
			Pull-down	25	50	100	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin except below ports	I_{OL}	DVDD5=5V AVDD5=5V	-	-	2 (Note4)	mA
	Per pin PA4 to 5	I_{OL4}	DVDD5=5V	-	-	12 (Note4)	
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7	ΣI_{OL1}	DVDD5=5V	-	-	35 (Note5)	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5	ΣI_{OL2}	DVDD5=5V	-	-	35 (Note5)	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	ΣI_{OL3}	AVDD5=5V	-	-	20 (Note5)	
High level output current	Per pin	I_{OH}	DVDD5=5V AVDD5=5V	-2 (Note4)	-	-	mA
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7	ΣI_{OH1}	DVDD5=5V	-35 (Note5)	-	-	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5	ΣI_{OH2}	DVDD5=5V	-35 (Note5)	-	-	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	ΣI_{OH3}	AVDD5=5V	-20 (Note5)	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5V, unless otherwise noted

Note 3: Apply the same voltage to DVDD5 and AVDD5.

Note 4: The current sum total of a terminal should not exceed the sum total of each group current.

Note 5: The sum total of each group current should not exceed absolute maximum rating.

2.7V ≤ DVDD5=AVDD5< 4.5V
DVSS = AVSS=0V
Ta=-40 to 85 °C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD5A,DVDD5B, AVDD5	VDD	f_{OSC} = 6 to 12MHz f_{sys} = 1 to 80MHz fs = 30 to 34kHz	2.7	-	4.5	V
Low level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N,	V_{IL1}		-0.3	-	DVDD5×0.25	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, BOOT_N	V_{IL2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{IL3}				AVDD5×0.25	
	PA4 to 5	V_{IL4}				DVDD5×0.3	
High level Input voltage	PC0 to 6, PH0 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 7, PR0 to 7, PV0 to 7, MODE, RESET_N,	V_{IH1}		DVDD5×0.75	-	DVDD5+0.3	V
	PA0 to 3, PA6 to 7, PB1 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5, BOOT_N	V_{IH2}					
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{IH3}		AVDD5×0.75		AVDD5+0.3	
	PA4 to 5	V_{IH4}		DVDD5×0.7		DVDD5+0.3	
Low level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 3, PA6 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5,	V_{OL1} V_{OL2}	DVDD5=2.7V I_{OL} = 0.8mA	-	-	0.4	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{OL3}	AVDD5=2.7V I_{OL}= 0.8mA	-	-	0.4	
	PA4 to 5	V_{OL4}	DVDD5=2.7V I_{OL}= 4mA	-	-	1.0	
High level output voltage	PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP0 to 7, PR0 to 7, PV0 to 7, PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PT0 to 7, PU0 to 5,	V_{OH1} V_{OH2}	DVDD5=2.7V I_{OH}= -0.8mA	DVDD5-0.4	-	-	V
	PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	V_{OH3}	AVDD5=2.7V I_{OH}= -0.8mA	AVDD5-0.4	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3V, unless otherwise noted.

Note 3: Apply the same voltage to DVDD5 and AVDD5.

2.7V ≤DVDD5=AVDD5< 4.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD5 0.0V ≤ VIN ≤ AVDD5	-5	0.05	5	μA
Output leak current		I_{LO}	0.2 ≤VIN ≤DVDD5-0.2 0.2 ≤ VIN ≤ AVDD5-0.2	-10	0.05	10	
Schmitt trigger Input width		VTH	DVDD5 =AVDD5= 3V	-	0.5	-	V
Reset pull-up resistor		R_{RST}		25	100	200	kΩ
Programmable pull-up/-down resistor		P_{KH}	Pull-up	25	100	200	
			Pull-down	25	100	200	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin except below ports	I_{OL}	DVDD5=3V AVDD5=3V	-	-	1 (Note4)	mA
	Per pin PA4 to 5	I_{OL4}	DVDD5=3V	-	-	6 (Note4)	
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 4, PR0 to 7, PV0 to 7	ΣI_{OL1}	DVDD5=3V	-	-	18 (Note5)	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5	ΣI_{OL2}	DVDD5=3V	-	-	18 (Note5)	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	ΣI_{OL3}	AVDD5=3V	-	-	10 (Note5)	
High level output current	Per pin	I_{OH}	DVDD5=3V AVDD5=3V	-1 (Note4)	-	-	mA
	Total of PC0 to 6, PH4 to 7, PJ0 to 5, PK0 to 7, PN0 to 5, PP3 to 4, PR0 to 7, PV0 to 7	ΣI_{OH1}	DVDD5=3V	-18 (Note5)	-	-	
	Total of PA0 to 7, PB0 to 7, PG2 to 7, PL0 to 7, PM0 to 7, PP0 to 2, PT0 to 7, PU0 to 5	ΣI_{OH2}	DVDD5=3V	-18 (Note5)	-	-	
	Total of PD0 to 5, PE0 to 6, PF0 to 7, PG0 to 1	ΣI_{OH3}	AVDD5=3V	-10 (Note5)	-	-	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 3.0V, unless otherwise noted.

Note 3: Apply the same voltage to DVDD5 and AVDD5.

Note 4: The current sum total of a terminal should not exceed the sum total of each group current.

Note 5: The sum total of each group current should not exceed absolute maximum rating.

7.3. DC Electrical Characteristics (2/2)

Consumption current

Ta =-40 to 85°C

Parameter	Symbol	Conditions				Min	Typ. (Note2)	Max	Unit
		Supply voltage	High-speed oscillator	Low-speed oscillator	Operating condition				
Normal	I_{DD}	DVDD5= AVDD5= 5.5V	Refer to the table 7.2 and 7.3 for detail			-	19.6	27.4	mA
IDLE			Oscillation	Oscillation	Refer to the table 7.2 and 7.3 for detail	-	3.2	12.2	
STOP1			Stop	Oscillation		-	220	5200	μA
STOP2						-	18	300	
				Stop		-	17	300	

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5V, unless otherwise noted.

Note 3: Apply the same voltage to DVDD5 and AVDD5.

Note 4: Input pin is fixed level, Output pin is open.

Table 7.2 IDD measurement condition (Pin setting, Oscillation Circuit)

		NORMAL	IDLE	STOP1	STOP2	
				ELOSC run		ELOSC stop
Pin setting	DVDD5= AVDD5=	5.0V(Typ.), 5.5V(max)				
	X1,X2	Oscillator connected (10MHz)				
	XT1,XT2	Oscillator connected(32.768kHz)				
	Input pins	Fixed				
	Output pins	Open				
Operation condition (Oscillation Circuit)	System clock (fsys)	80MHz		Stop		
	External High speed frequency oscillator (EHOSC)	Oscillation		Stop		
	Internal High speed frequency oscillator1 (IHOSC1)	Stop				
	PLL	run(8times)		Stop		
	External low speed oscillator (ELOSC)	Oscillation				Stop

Table 7.3 IDD measurement condition (CPU, Peripheral)

Peripheral	unit number	NORMAL	IDLE	STOP1	STOP2
				LOSC oscillation	LOSC stop
CPU	1	Run (Dhrystone Ver.2.1)	Stop		
DMAC	1	(Request from UARTch0 TX, destination: RAM)	Stop		
ADC	1	Run (1.5μs, Repeated conversion)	Stop		
DAC	2	Run	Stop		
T32A	6	All Ch: Run	Stop		
A-PMD	1	Run	Stop		
A-ENC	1	Run	Stop		
RTC	1	Run			
SIWDT	1	Run	Stop		
UART	6	All Ch: UART, Transmission(2.5Mbps)	Stop		
I2C	4	Stop			
TSPI	5	Ch0, Ch1: Transmission(20MHz)	Stop		
RMC	1	Run	Stop		
LVD	1	Stop			
OFD	1	Stop			
Input Output Port	-	Run	Stop		

7.4. 12-bit AD Converter Characteristics

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	AVDD5 (VREFH)		AVDD5-0.3	-	AVDD5+0.3	V
Analog input voltage	VAIN		AVSS (VREFL)	-	AVDD5 (VREFH)	V
Integral nonlinearity error (INL)	-	4.5 ≤ AVDD5 ≤ 5.5 AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 1.5μs	-2.5	-	2.5	LSB
Differential nonlinearity error (DNL)			-2	-	1.5	
Zero-scale error			-1	-	3	
Full-scale error			-2	-	3	
Total errors			-3	-	3	
Integral nonlinearity error (INL)	-	2.7 ≤ AVDD5 < 4.5 AIN load resistor = 600 Ω AIN load capacity ≥ 0.1μF Conversion time = 2.95μs	-3	-	3	LSB
Differential nonlinearity error (DNL)			-2	-	1.5	
Zero-scale error			-4	-	4.5	
Full-scale error			-4	-	4.5	
Total errors			-5.5	-	4	
Stable time	t_{sta}	After ***[ADMOD0]***<DACON>= 1 is set.	3	-	-	μs
Conversion time (Note3)	t_{conv}	4.5V ≤ AVDD5 ≤ 5.5V SCLK=40MHz	1.5	-	16.3	
		2.7V ≤ AVDD5 < 4.5V SCLK=40MHz	2.95	-	16.65	

Note1: 1LSB = (AVDD5(VREFH) - AVSS(VREFL)) / 4096 [V]

Note2: The characteristic when single unit AD converter operates only.

Note3: For detail of setting, refer to “Analog to Digital Converter” of the reference manual.

DVDD5=AVDD5=2.7Vto 5.5V
DVSS=AVSS=0V
Ta= -40to 85°C

Parameter	Conditions	Min	Typ.	Max	Unit
Reference power	ch23 selected	1.1	-	1.3	V

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.5. 8-bit DA Converter Characteristics

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	AVDD5 (VREFH)		AVDD5-0.3	-	AVDD5+0.3	V
Integral nonlinearity error (INL)	-	4.5V ≤ AVDD5 ≤ 5.5V Rload = 10MΩ	-1	-	+1	LSB
Differential nonlinearity error (DNL)			-1	-	+1	
Total errors			-1	-	+1	
Integral nonlinearity error (INL)	-	2.7V ≤ AVDD5 < 4.5V Rload = 10MΩ	-2	-	+2	LSB
Differential nonlinearity error (DNL)			-1	-	+1	
Total errors			-2	-	+2	
Stable time	t_{sta}	Cload = 20pF	4.5	-	-	μs

Note 1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDD5 = 5V, unless otherwise noted.
Note 3: 1LSB = (AVDD5(VREFH) - AVSS(VREFL)) / 256 [V]
Note 4: This is the characteristic in case only DA converter is operating.
Note 5: When using DAC0 as the reference voltage of Comparator, DAC0 pin should be open.

7.6. Comparator Characteristics

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
AIN Input voltage Range	VINC		VREF-1.5	-	VREF+1.5	V
Reference Voltage Range (Note1)	VREFC		0.2	-	AVDD5-0.5	V
Response time(Note2)			-	-	0.7	μs
Comparator Start-up time	Tsta		-	-	5	μs

Note 1: Output of On-chip 8-bit DA converter (DAC0)
Note 2: In case of the VIN change from VREF-100mV to +100mV, or from VREF+100mV to -100mV.
Note 3: This is the characteristic in case only Comparator is operation.

7.7. Characteristics of Internal processing at RESET

DVSS=AVSS=0V
Ta= -40to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal Initialized time	T_{IINIT}	Power-On	-	-	2.15	ms
		STOP2 Release by RESET with RESET_N	-	-	1.8	
		STOP2 Release by Interrupt	-	-	1.55	
Internal processing time for Reset	T_{IRST}		0.16	-	0.2	
Waiting time till CPU running	T_{CPUWT}	Cold Reset	12	-	15	µs
		Warm Reset	70	-	90	
Power-on rising gradient	V_{PON}		0.01	-	100	mV/µs

7.8. Characteristics of Power On Reset

DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PREL}	Power-up	2.25	2.4	2.55	V
	V_{PDET}	Power-down	2.2	2.35	2.5	
Detection pulse width	T_{PDET}		200	-	-	µs

7.9. Characteristics of Voltage Detection Circuit

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{LVL0}	Power-up	2.55	2.65	2.75	V
		Power-down	2.5	2.6	2.7	
	V_{LVL1}	Power-up	2.65	2.75	2.85	V
		Power-down	2.6	2.7	2.8	
	V_{LVL2}	Power-up	2.75	2.85	2.95	V
		Power-down	2.7	2.8	2.9	
	V_{LVL3}	Power-up	2.85	2.95	3.05	V
		Power-down	2.8	2.9	3.0	
	V_{LVL4}	Power-up	3.75	3.85	3.95	V
		Power-down	3.7	3.8	3.9	
	V_{LVL5}	Power-up	3.95	4.05	4.15	V
		Power-down	3.9	4.0	4.1	
	V_{LVL6}	Power-up	4.15	4.25	4.35	V
		Power-down	4.1	4.2	4.3	
	V_{LVL7}	Power-up	4.35	4.45	4.55	V
		Power-down	4.3	4.4	4.5	
Detection response time	t_{VDDT1}	Power-down	-	50	200	μs
Detection Release time	t_{VDDT2}	Power-up	-	250	-	
setup time	t_{LVDEN}		-	-	100	
Detection Minimum pulse width	t_{LVDPW}		200	-	-	

7.10. AC Electrical Characteristics

7.10.1. Serial Peripheral Interface (TSPI)

7.10.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40 to 85°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

The number of cycles can be 1 to 16. It is specified with TSPIxSCK. The value of k1 is specified with ***[TSPIxFMTR0]***<CSSCKDL[3:0]>; the value of k2 is specified with ***[TSPIxFMTR0]***<SCKCSDL[3:0]>. These values are 1 to 16.

(1) Master in SPI mode (TSPI1/2/3/4)

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 13	-	12	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 13	-	12	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} x k1) - 20	(t_{CYC} x k1) + 9	30	59	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	(t_{CYC} x (k2 + 0.5))-20	-	55	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35 - 2x T(Note1)	-	10	-	
		35 - T(Note2)				
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2xT - 10.5 (Note1)	-	14.5	-	
		T-10.5 (Note2)		14.5		
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} x (k1 - 0.5))-25	(t_{CYC} x (k1 - 0.5))+9	0	34	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1 ,fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0 ,fsys=40MHz

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 16	-	9	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 16	-	9	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} x k1) - 20	(t_{CYC} x k1) + 11	30	61	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	(t_{CYC} x (k2 + 0.5))-20	-	55	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45 - 2xT (Note1)	-	20	-	
		45 - T(Note2)		20		
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2xT-10.5 (Note1)	-	14.5	-	
		T- 10.5 (Note2)	-	14.5		
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} x (k1 - 0.5))-25	(t_{CYC} x (k1 - 0.5))+13	0	38	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1 ,fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0 ,fsys=40MHz

(2) Master in SPI mode (TSPI0)

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	5.88	-	5.88	MHz
TSPIxSCK output cycle	t_{CYC}	170	-	170	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 13	-	72	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 13	-	72	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} x k1) - 140	(t_{CYC} x k1) + 9	30	179	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	(t_{CYC} x (k2 + 0.5))-20	-	235	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35 - 2x T(Note1)	-	10	-	
		35 - T(Note2)		10		
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2xT - 10.5 (Note1)	-	14.5	-	
		T - 10.5(Note2)	-	14.5		
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} x (k1- 0.5))-145	(t_{CYC} x (k1- 0.5))+9	-60	94	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1, fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0, fsys=40MHz

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	4.34	-	4.34	MHz
TSPIxSCK output cycle	t_{CYC}	230	-	230	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 16	-	99	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 16	-	99	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} x k1) - 200	(t_{CYC} x k1) + 9	30	239	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	(t_{CYC} x (k2 + 0.5))-20	-	325	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45 - 2xT (Note1)	-	20	-	
		45 - T(Note2)	-	20		
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2xT-10.5 (Note1)	-	14.5	-	
		T-10.5(Note2)	-	14.5		
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSn fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} x (k1-0.5))-211	(t_{CYC} x (k1-0.5))+13	-96	128	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1, fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0, fsys=40MHz

(3) Slave in SPI mode(TSPI0/1/2/3/4)

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level Input pulse width	t_{WH}	37	-	37	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU1}	(t_{CYC} x (k1 + 0.5)) +15	-	170	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU2}	(t_{CYC} x k1) - 15	-	80	-	
TSPIxSCK rise/fall time → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	49	-	49	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	(t_{CYC} x (k1 - 0.5)) +5	-	55	
TSPIxCSIN high level input pulse width	t_{WDIS}	T x 2 + 20	-	45	-	

2.7V ≤DVDD5=AVDD5<4.5V

Parameter	Symbol	Equation		fsys = 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	37	-	37	-	
TSPIxSCK high level Input pulse width	t_{WH}	37	-	37	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU1}	(t_{CYC} x (k1 + 0.5)) +15	-	170	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU2}	(t_{CYC} x k1) - 15	-	80	-	
TSPIxSCK rise/fall time → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	55	-	55	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	-	(t_{CYC} x (k1 - 0.5)) +5	-	55	
TSPIxCSIN high level input pulse width	t_{WDIS}	T x 2 + 20	-	45	-	

(4) Master in SIO Mode (TSPI0/1/2/3/4)

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Equation		fsys= 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Output Frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK Output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK Low level Output pulse width	t_{WL}	(t_{CYC}/2)-13	-	12	-	
TSPIxSCK High level Output pulse width	t_{WH}	(t_{CYC}/2)-13	-	12	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35-2×T (Note1)	-	10	-	
		35-T (Note2)	-	10		
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	2×T-10.5 (Note1)	-	14.5	-	
		T -10.5 (Note2)	-	14.5		
TSPIxSCK rise/ fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK Rise/ fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1, fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0, fsys=40MHz

2.7V≤DVDD5=AVDD5<4.5V

Parameter	Symbol	Equation		fsys= 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Output Frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK Output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK Low level output pulse width	t_{WL}	(t_{CYC}/2)-16	-	9	-	
TSPIxSCK High level output pulse width	t_{WH}	(t_{CYC}/2)-16	-	9	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	45-2×T (Note1)	-	20	-	
		45-T (Note2)	-	20		
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	2×T-10.5 (Note1)	-	14.5	-	
		T- 10.5 (Note2)	-	14.5		
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	

Note 1: In this case ***[TSPIxCR2]***<RXDLY>=1, fsys=80MHz

Note 2: In this case ***[TSPIxCR2]***<RXDLY>=0, fsys=40MHz

(5) Slave in SIO mode (TSPI0/1/2/3/4)

4.5V ≤ DVDD5=AVDD5 ≤5.5V

Parameter	Symbol	Equation		fsys= 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input Frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input Cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK Low level Input Pulse Width	t_{WL}	37	-	37	-	
TSPIxSCK High level Input Pulse Width	t_{WH}	37	-	37	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← SPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	49	-	49	

2.7V ≤ DVDD5=AVDD5<4.5V

Parameter	Symbol	Equation		fsys= 80MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK Input Frequency	f_{CYC}	-	10	-	10	MHz
TSPIxSCK Input Cycle	t_{CYC}	100	-	100	-	ns
TSPIxSCK Low level Input Pulse Width	t_{WL}	37	-	37	-	
TSPIxSCK High level Input Pulse Width	t_{WH}	37	-	37	-	
TSPIxSCK rise/fall → TSPIxCSIN hold time	t_{CHD}	7	-	7	-	
TSPIxRXD Input ← SPIxSCK rise/fall time	t_{DSU}	7	-	7	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	10	-	10	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY1}	0	-	0	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	-	55	-	55	

(1) 1st clock edge sampling (Master)

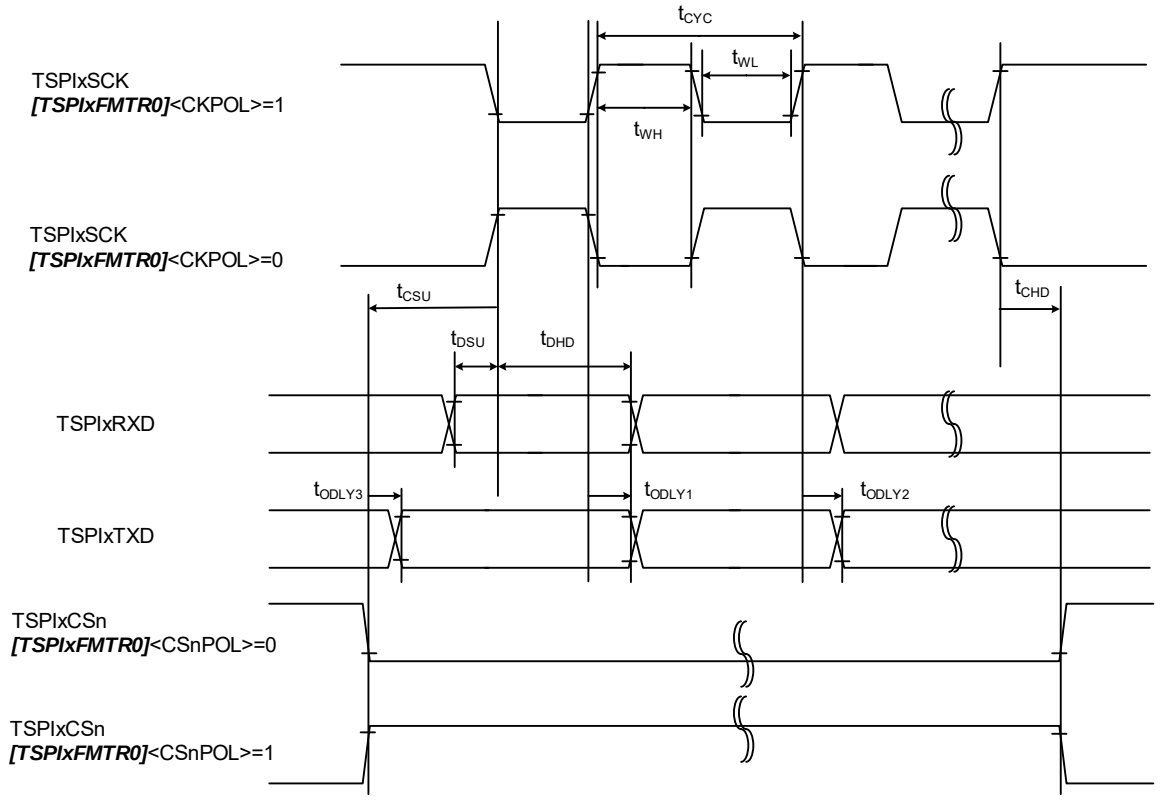


Figure 7.1 1st clock edge sampling (Master)

(2) 2nd clock edge sampling (Master)

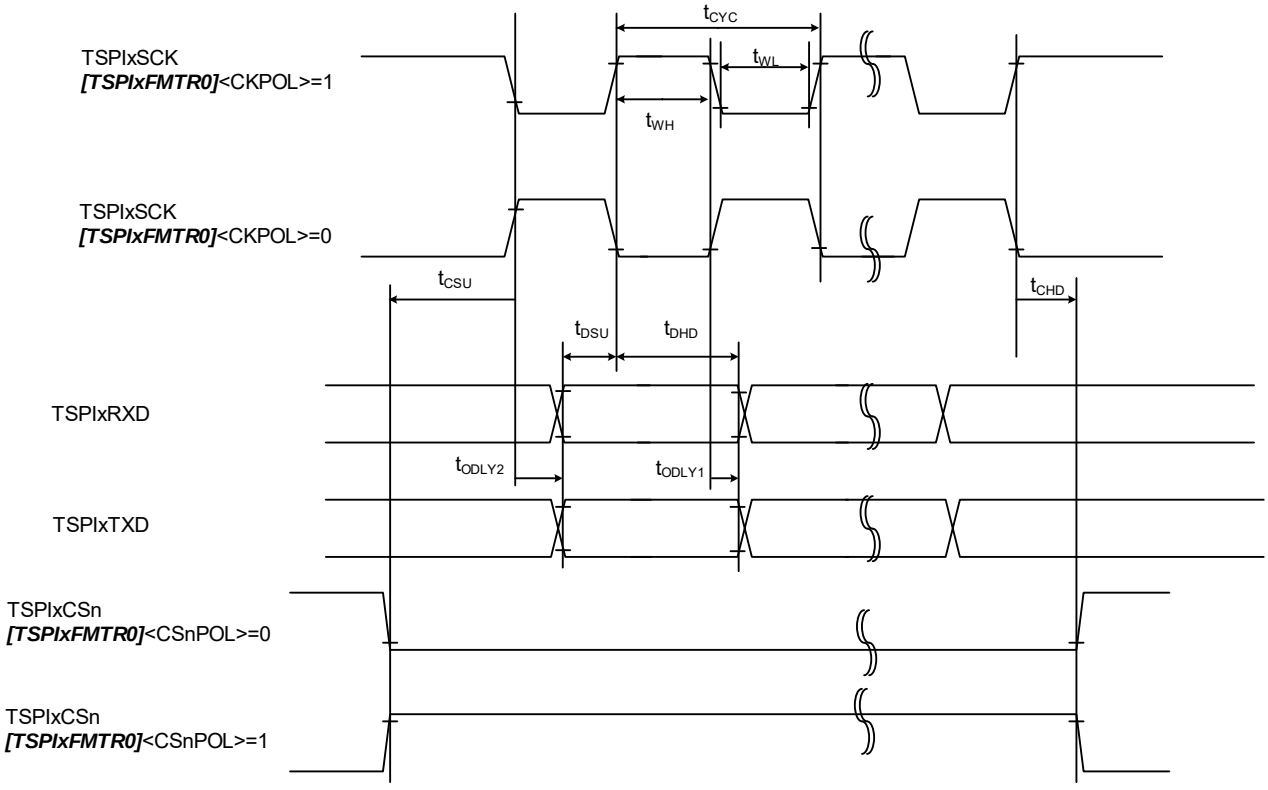


Figure 7.2 2nd clock edge sampling (Master)

(3) 2nd clock edge sampling (slave)

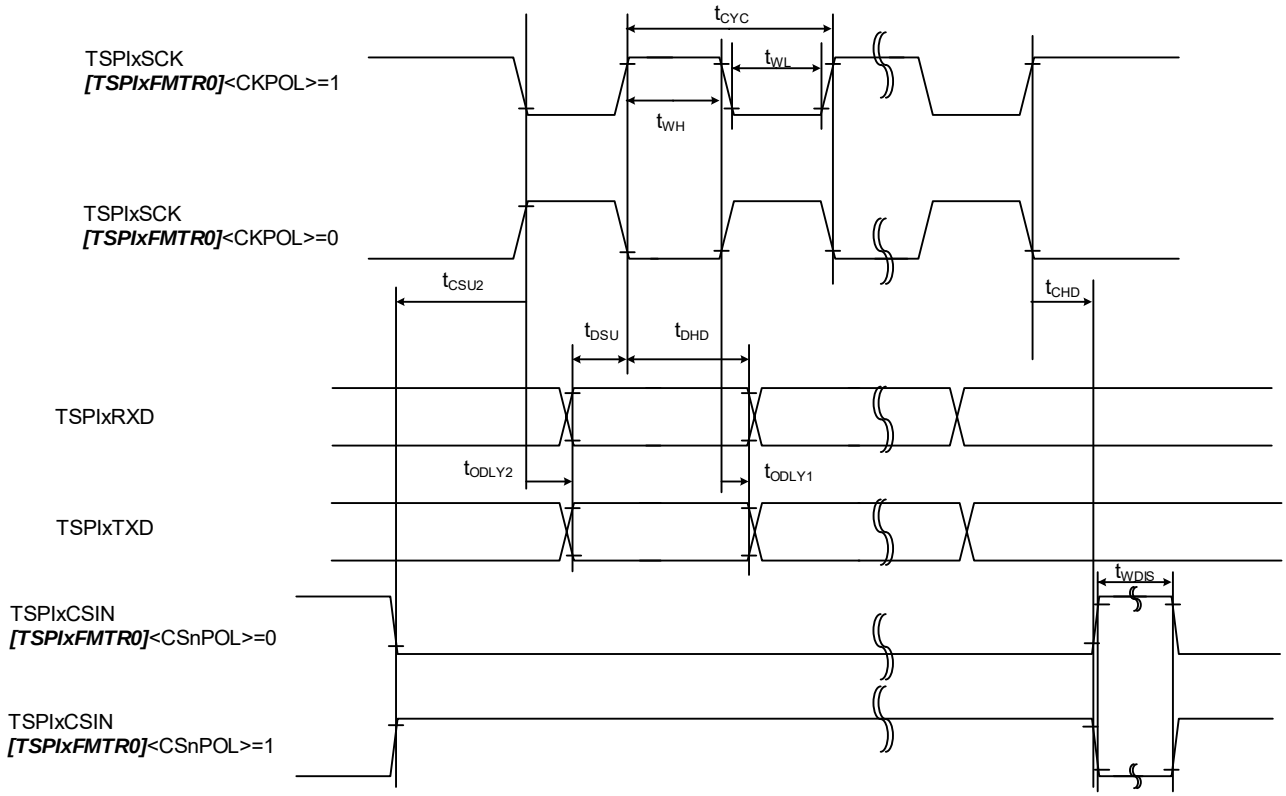


Figure 7.3 2nd clock edge sampling (Slave)

7.10.2. I^2C Interface (I^2C)

7.10.2.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7v to 5.5V
- Ta = -40 to 85°C
- Output level: Low = 0.4V
- Input level: High = 0.7 × DVDD5, Low = 0.3 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.2.2. AC Electrical Characteristics

T indicates the Operation clock cycle of I^2C.

The value of **n** is the SCL output clock frequency specified with ***[I2CxCR]***<SCK>.

The value of **p** is the prescaler dividing ratio specified with ***[I2CxPRS]***<PRSCK>.

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Start condition hold time	$t_{HD, STA}$	4.0	-	0.6	-	μs
SCL clock Low width (Input) (Note 1)	t_{LOW}	4.7	-	1.3	-	
SCL clock High width (Input) (Note 2)	t_{HIGH}	4.0	-	0.6	-	
Re-start condition setup time (Note 5)	$t_{SU, STA}$	4.7	-	0.6	-	
Data hold time (Input) (Note 3, 4)	$t_{HD, DAT}$	0	-	0	-	
Data setup time	$t_{SU, DAT}$	250	-	100	-	ns
Stop condition setup time	$t_{SU, STO}$	4.0	-	0.6	-	μs
Bus free time between stop condition and start condition (Note 5)	t_{BUF}	4.7	-	1.3	-	

Note1: SCL clock low level width (output): $p \times (2^{n+1}+10)/T$ (***[I2CxOP]***<NFSEL>=0)

Note2: SCL clock high level width (output): $p \times (2^{n+1}+6)/T$ (***[I2CxOP]***<NFSEL>=0)
On I^2C bus standard, the maximum speed of standard mode/fast mode is 100kHz/400 kHz respectively. Note that an internal SCL clock frequency is determined by the fsys and the calculation of Note 1 and Note 2 above-mentioned.

Note3: The data hold time (output) is equal to four cycles of the prescaler clock (Tprsck) started from the internal SCL.

Note4: On I^2C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that tr/tf on the SCL/SDA should be included in the data hold time.

Note5: Depends on software.

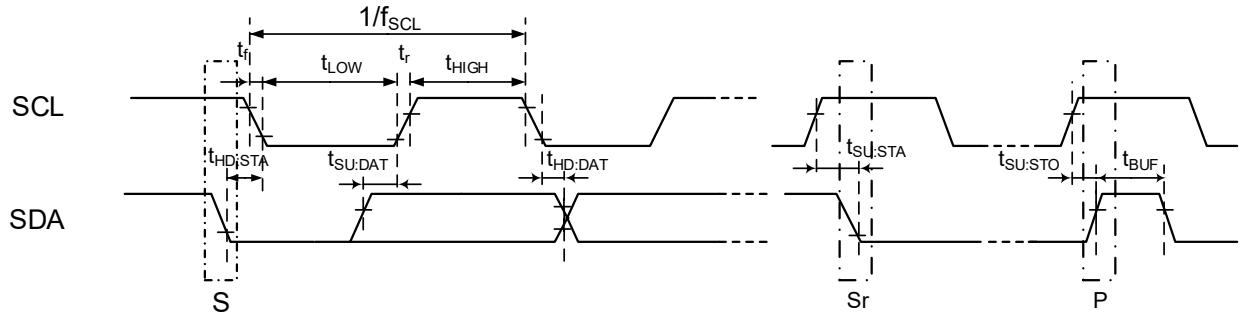


Figure 7.4 AC timing of I^2C

7.10.3. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

7.10.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.3.2. AC Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the ΦT0 clock. This cycle is depending on the Prescaler Clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Equation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{VCKL}	2T + 20	-	45	-	ns
High level pulse width	t_{VCKH}	2T + 20	-	45	-	

(2) At the pulse count

Parameter	Symbol	Equation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Pulse cycle	t_{DCYC}	1000	-	1000	-	ns
Low level pulse width	t_{PWL}	500	-	500	-	
High level pulse width	t_{PWH}	500	-	500	-	
Input setup	t_{ABS}	(NF+1)×T+20	-	82.5	-	
Input hold	t_{ABH}	(NF+1)×T+20	-	82.5	-	

NF Value is depending on the ***[T32AxPLSCR]***<NF[1:0]> setting as follows.

[T32AxPLSCR]<NF[1:0]>	NF Value of Formula
00	0
01	2
10	4
11	8

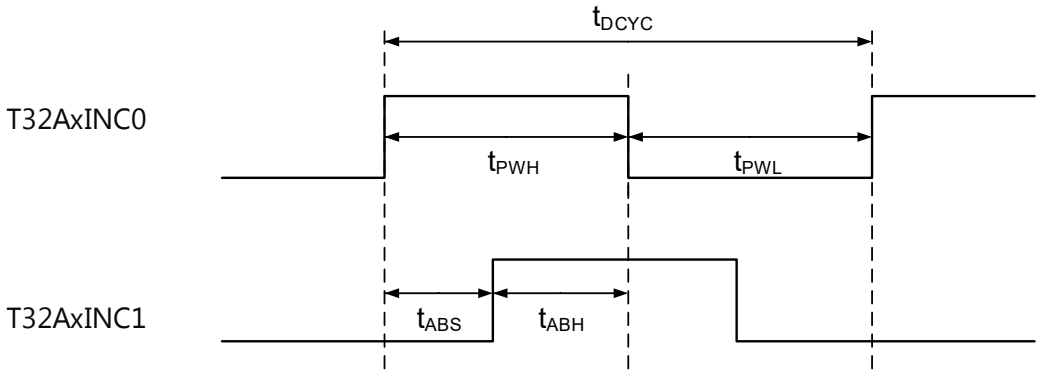


Figure 7.5 Count Pulse input

7.10.4. External Interrupt

7.10.4.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.4.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL, IDLE mode

Parameter	Symbol	Equation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTAL1}	T + 100	-	112.5	-	ns
High level pulse width	t_{INTAH1}	T + 100	-	112.5	-	

(4) STOP1, STOP2 mode

Parameter	Symbol	Equation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTCL2}	125	-	125	-	ns
High level pulse width	t_{INTCH2}	125	-	125	-	

7.10.5. Trigger Input (TRGINx)

7.10.5.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5 = 2.7V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.5.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

Parameter	Symbol	Equation		fsys=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{ADL}	2T + 20	-	45	-	ns
High level pulse width	t_{ADH}	2T + 20	-	45	-	

7.10.6. Debug Communication

7.10.6.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40 to 85°C
- Output level: High = 0.8 ×DVDD5, Low = 0.2×DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.6.2. SWD Interface

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold time from the rising edge of CLK	t_{d1}	4	-	
Output data valid time from the rising edge of CLK	t_{d2}	-	33	
Input data valid time from the rising edge of CLK	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold time from the rising edge of CLK	t_{d1}	4	-	
Output data valid time from the rising edge of CLK	t_{d2}	-	45	
Input data valid time from the rising edge of CLK	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

7.10.6.3. JTAG Interface

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold time from the rising edge of CLK	t_{d3}	4	-	
Output data valid time from the rising edge of CLK	t_{d4}	-	33	
Input data valid time from the rising edge of CLK	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
CLK cycle	t_{dck}	100	-	ns
Output data hold time from the rising edge of CLK	t_{d3}	4	-	
Output data valid time from the rising edge of CLK	t_{d4}	-	45	
Input data valid time from the rising edge of CLK	t_{ds}	20	-	
Input data hold time from the rising edge of CLK	t_{dh}	15	-	

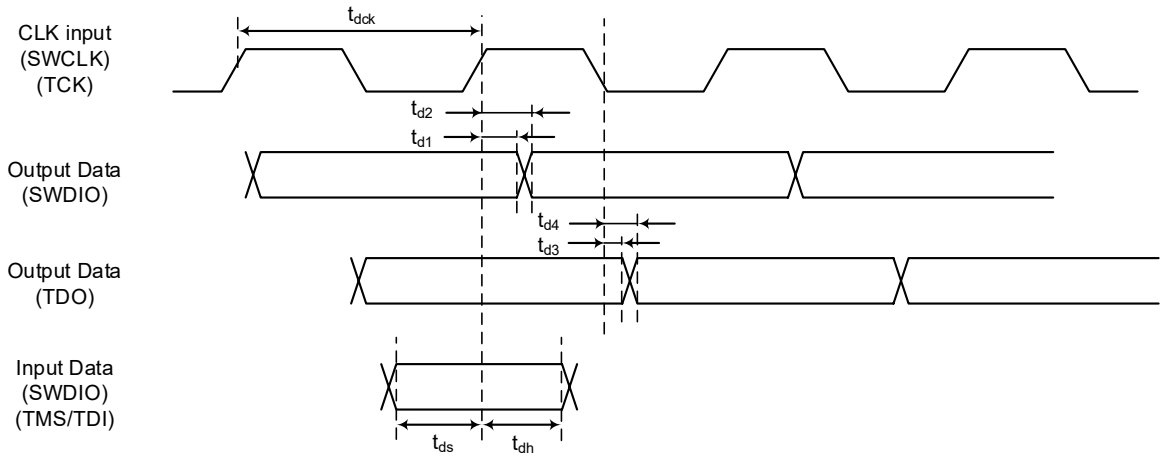


Figure 7.6 JTAG/SWD waveform

7.10.6.4. ETM Trace

4.5V≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	50	-	ns
Data valid time from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold time from the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid time from the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold time from the falling edge of TRACECLK	t_{holdf}	1	-	

2.7V ≤DVDD5=AVDD5< 4.5V

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	100	-	ns
Data valid time from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold time from the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid time from the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold time from the falling edge of TRACECLK	t_{holdf}	1	-	

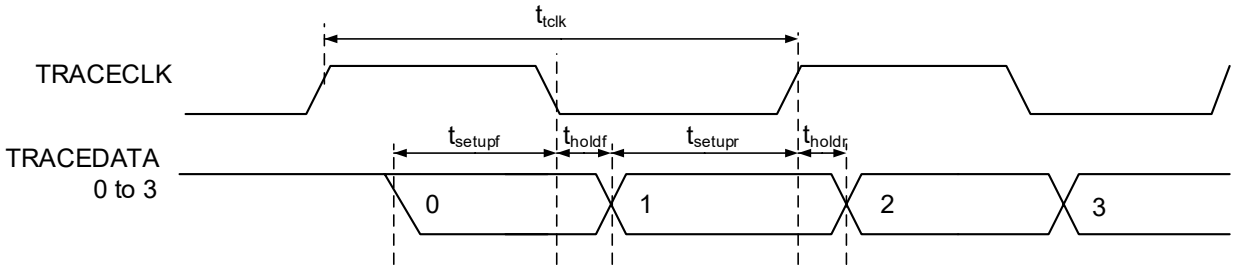


Figure 7.7 Trace signal waveform

7.10.7. SCOUT Pin

7.10.7.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5= AVDD5= 2.7V to 5.5V
- Ta = -40 to 85°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.7.2. AC Electrical Characteristics

"T" in the table indicates the cycle of the SCOUT output waveform.

Parameter	Symbol	Equation		SCOUT = 20MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{SCL}	0.5T- 10	-	15	-	ns
High level pulse width	t_{SCH}	0.5T- 10	-	15	-	

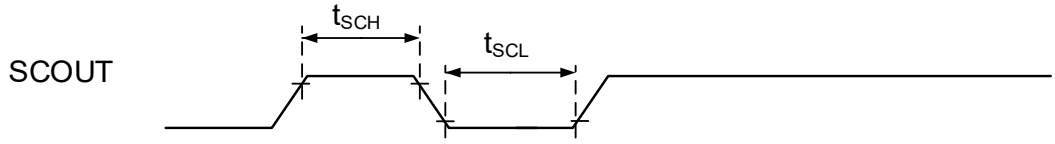


Figure 7.8 SCOUT wave output

7.10.8. Noise Filter Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Noise cancel width	-	15	30	60	ns

7.10.9. External Clock Input

7.10.9.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.10.9.2. AC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency($1/t_{ehcin}$)	$f_{EHCLKIN}$	6	-	20	MHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	10	ns
Clock fall time	t_f	-	-	10	ns

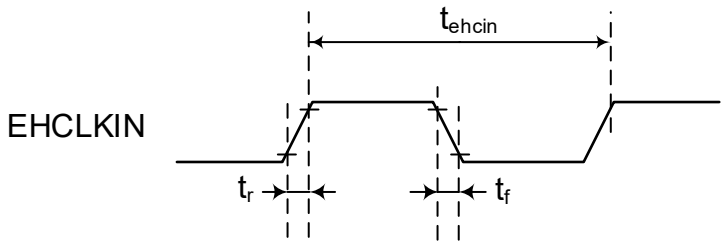


Figure 7.9 External clock input waveform

7.11. Flash Memory Characteristics

7.11.1. Code Flash

DVDD5=2.7V to 5.5V
Ta=-40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	-	-	-	10,000	cycles
Programming time	Word Program time	-	29.5	-	μs
Erase time	Page Erase time	1.1	-	4.3	ms
	Block Erase time	8.6	-	34	
	Area Erase time(Note2)	-	9.2	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note2: No block with effective protection.

7.11.2. Data Flash

DVDD5=2.7V to 5.5V
Ta=-40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance	-	-	-	100,000	cycles
Programing time	-	-	64.7	-	μs
Erase time	Page Erase time	1	-	3.9	ms
	Block Erase time	15.4	-	62.1	
	Area Erase time(Note2)	-	9.2	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note2: No block with effective protection.

7.11.3. Chip Erase

DVDD5= 2.7V to 5.5V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Chip Erase time	Erasing of Code Flash, Data Flash, Protect Bits(Code), Protect Bits(Data), User Information Area and Security bits	23.4	-	62.7	ms

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B.
Note2: When Chip Erase command executes, no block with effective protection.

7.12. Regulator

Parameter	Condition	Min	Typ.	Max	Unit
Capacitance of REGOUT1 capacitor	DVDD5=2.7Vto 5.5V Ta=-40 to 85°C	-	4.7	-	μF
Capacitance of REGOUT2 capacitor		-	4.7	-	

Note: DVDD5 is a generic name for DVDD5A, DVDD5B.

7.13. Oscillation Circuit

7.13.1. Internal Oscillator

DVDD5= 2.7V to 5.5V
Ta= -40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}	Factory out, IC data (Note2)	-	10	-	MHz
	f_{IHOSC2}		-	10	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note2: Not included the influence depend on the variations after Factory shipping. Please execute oscillator adjustment by the trimming register, if it is required.

7.13.2. External Oscillator

DVDD5= 2.7V to 5.5V
Ta= -40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{EHOSC}	-	6	-	12	MHz
	f_{ELOSC}		30	-	34	kHz

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B.

Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

7.13.3. Oscillation Circuit

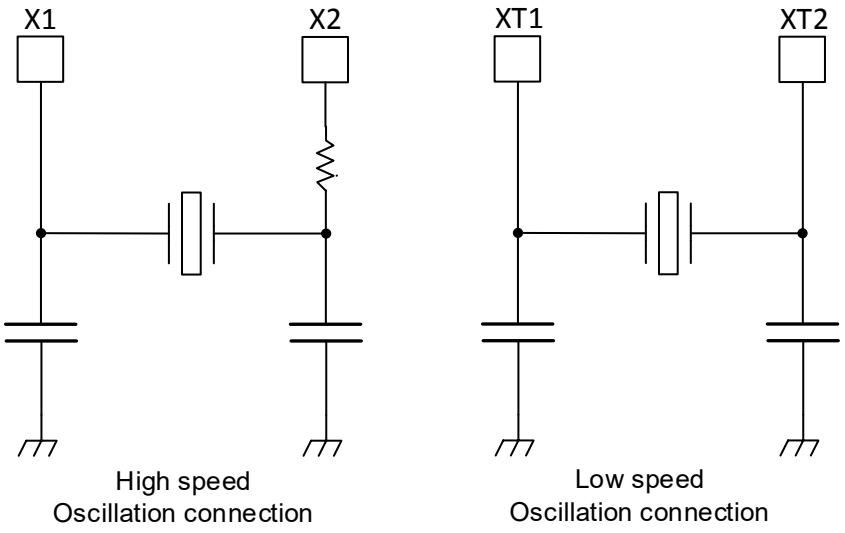


Figure 7.10 Oscillation circuit sample

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.

Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer to this information when selecting external parts.

7.13.4. Ceramic Oscillator

This product has been evaluated by the ceramic oscillator by Murata Manufacturing Co., Ltd.

Please refer to the Murata Website for details.

7.13.5. Crystal Oscillator

This product has been evaluated by the crystal oscillator by KYOCERA Corporation.

Please refer to the KYOCERA Website for details.

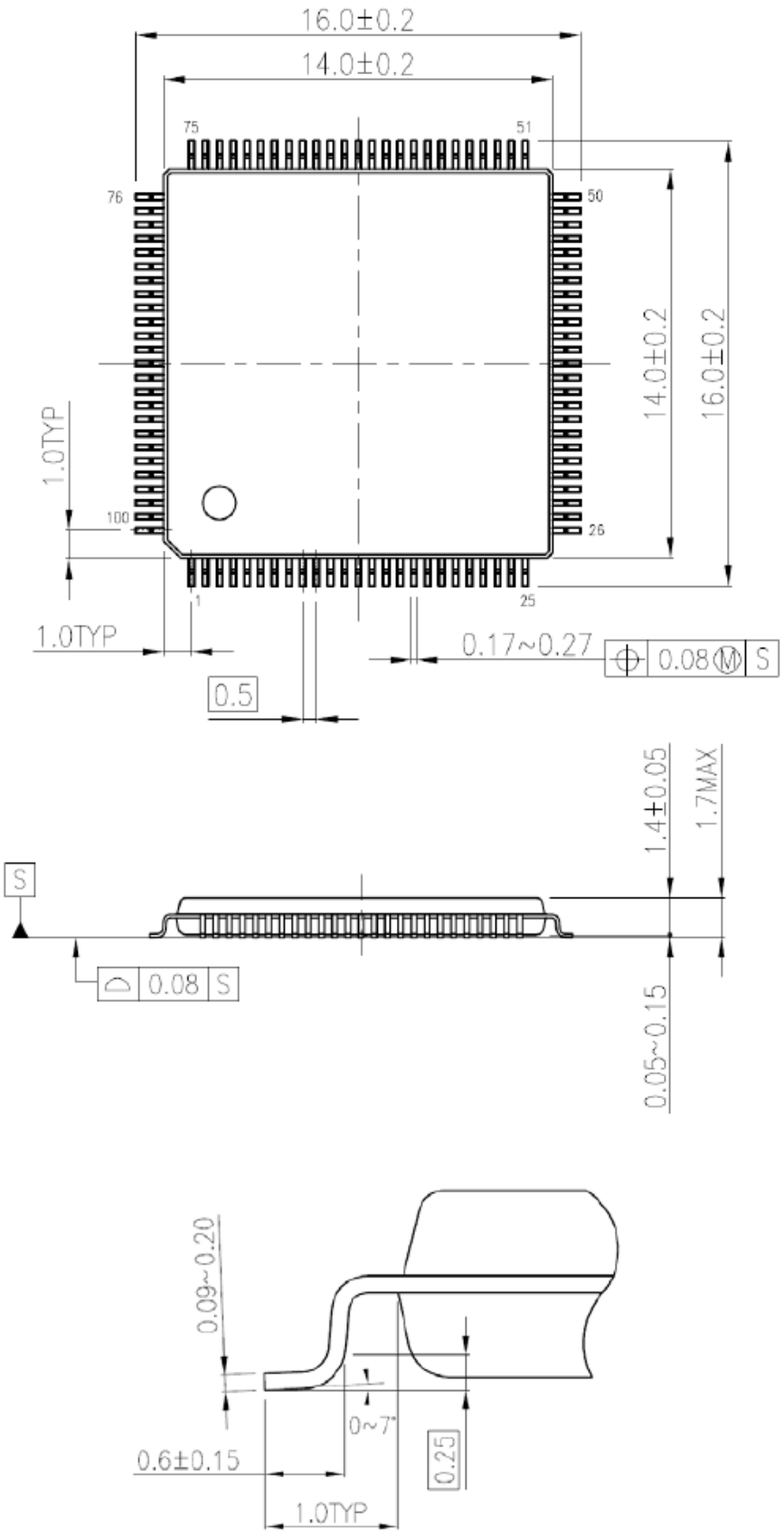
7.13.6. Precautions for designing printed circuit board

Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multi-layer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the oscillator vendor.

8. Package Dimensions

Unit: mm

P-LQFP100-1414-0.50-002



9. Precautions

This Page explains general precautions on the use of Toshiba MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of document has higher priority.

(1) The MCUs' operation at power-on

At power-on, internal state of the MCUs is unstable. Therefore, state of the pins is undefined until reset operation is completed.

When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is completed.

Also, when a reset is performed by the internal power-on reset, pins of the MCUs that use the internal power-on reset are undefined until power supply voltage reaches the voltage at which power- on reset is valid.

(2) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high-impedance.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch- up may occur in the internal LSI due to induced voltage influenced from external noise.

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(3) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the clock is stable.

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- Applied equipment : GPS driving equipment of in-vehicle equipment

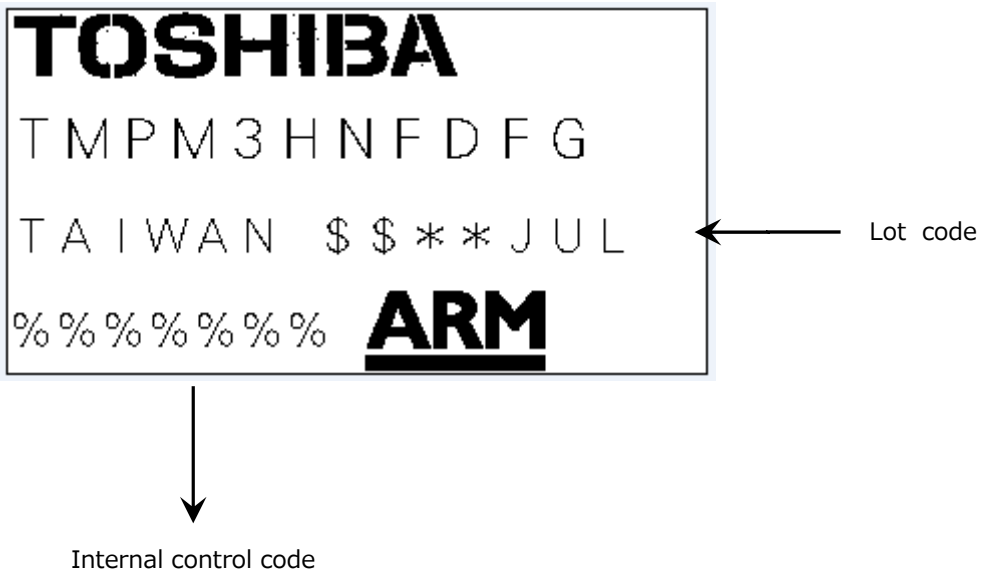
□Part Naming Conventions

TMP	M3	H	N	F	D	FG
①	②	③	④	⑤	⑥	⑦

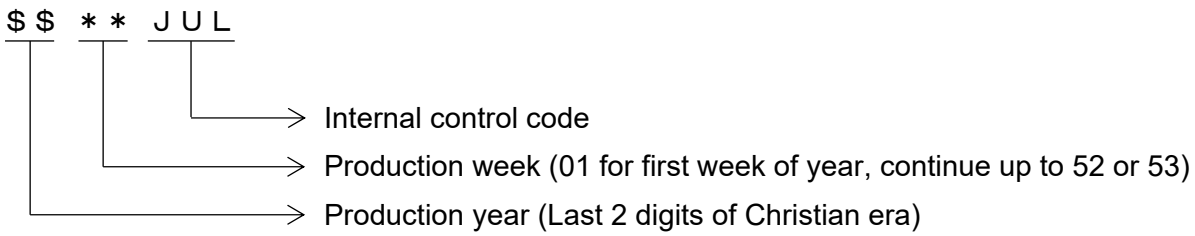
① The identification of Toshiba microcontrollers
② Core
③ Product Group
④ Pin Count
⑤ ROM Type
⑥ Memory Size
⑦ Package

（DBB)
D=Dropship
B=Pre-process
B=Post-process

○ Marking



Explanation for Lot code



TXZ™Family M3H Group

TOKYO—Toshiba Electronic Devices & Storage Corporation (“Toshiba”) has added the “M3H Group” to its “TXZ™ Family” of Arm® Cortex®-M-based microcontrollers for consumer and industrial equipment. The new microcontrollers are now in mass production.

The M3H Group has two groups based on their functional level. “M3H Group (1)” offers standard functions, while “M3H Group (2)” offers an expanded package line-up and memory size and supports high-speed processing (80MHz). Together, they offer a rich line-up with 13 packages (32 pins to 144 pins) and flash memory ranging from 32KB to 512KB.

Toshiba plans to release groups of microcontrollers for communications control for high-speed data processing, and devices equipped with high-precision analog circuits for control of low- to medium-speed motors. The Company continues to expand the TXZ family to meet the needs of the motor control and global sensing market.

Features

- High-performance ARM Cortex-M3 core, operating at up to 80MHz
- A comprehensive line-up of memory and package variations
- General-purpose microcontrollers for diverse applications

Applications

- Air-conditioners, washing machines, refrigerators, office automation equipment, housing and facility equipment, audio-visual equipment, motor control applications (consumer and industrial applications).

Product Specifications

Product series		TXZ3 Series	
Product group		M3H Group (1)	M3H Group (2)
CPU core		Arm Cortex-M3	
Maximum operating frequency		40MHz	80MHz
Internal oscillator		10MHz(±1%)*1	*1:Factory default setting
Built-in memory	Flash (code)	32K to 128KB	256K to 512KB
	Flash (data)	8K to 32KB	32KB
	RAM	8K to 18KB	66KB with parity
I/O port		24 to 87	56 to 134
CRC calculation circuit (CRC)		None	1 channel
Communication function	UART	2 to 3 channels	5 to 6 channels
	TSPI	1 to 2 channels	1 to 5 channels
	I^2C	1 to 3 channels	2 to 4 channels
12-bit AD converter (ADC)	Channel input	4 to 16 channels	19 to 21 channels
	Conversion time	1.5μs	
8-bit DA converter (DAC)		0 to 2 channels	2 channels
Programmable motor driver (PMD+)		1 channel	None
Advanced programmable motor driver (A-PMD)		None	1 channel
Advanced encoder input circuit (A-ENC)		1 channel	
Remote control signal processor (RMC)		0 to 1 channel	1 channel
Timer		Used as 32-bit timer : 6 channels Used as 16-bit timer × 2 channels: 12 channels	Used as 32-bit timer: 8 channels Used as 16-bit timer × 2 channels: 16 channels
Real time clock (RTC)		0 to 1 channel	1 channel
Watchdog timer (WDT)		1 channel	1 channel
DMA controller (DMAC)		32 channels / 1 unit	64 channels / 2 units
Operating temperature range		−40～+85℃	
Supply voltage		2.7 to 5.5V	
Number of pins		32 to 100 pins	64 to 144 pins

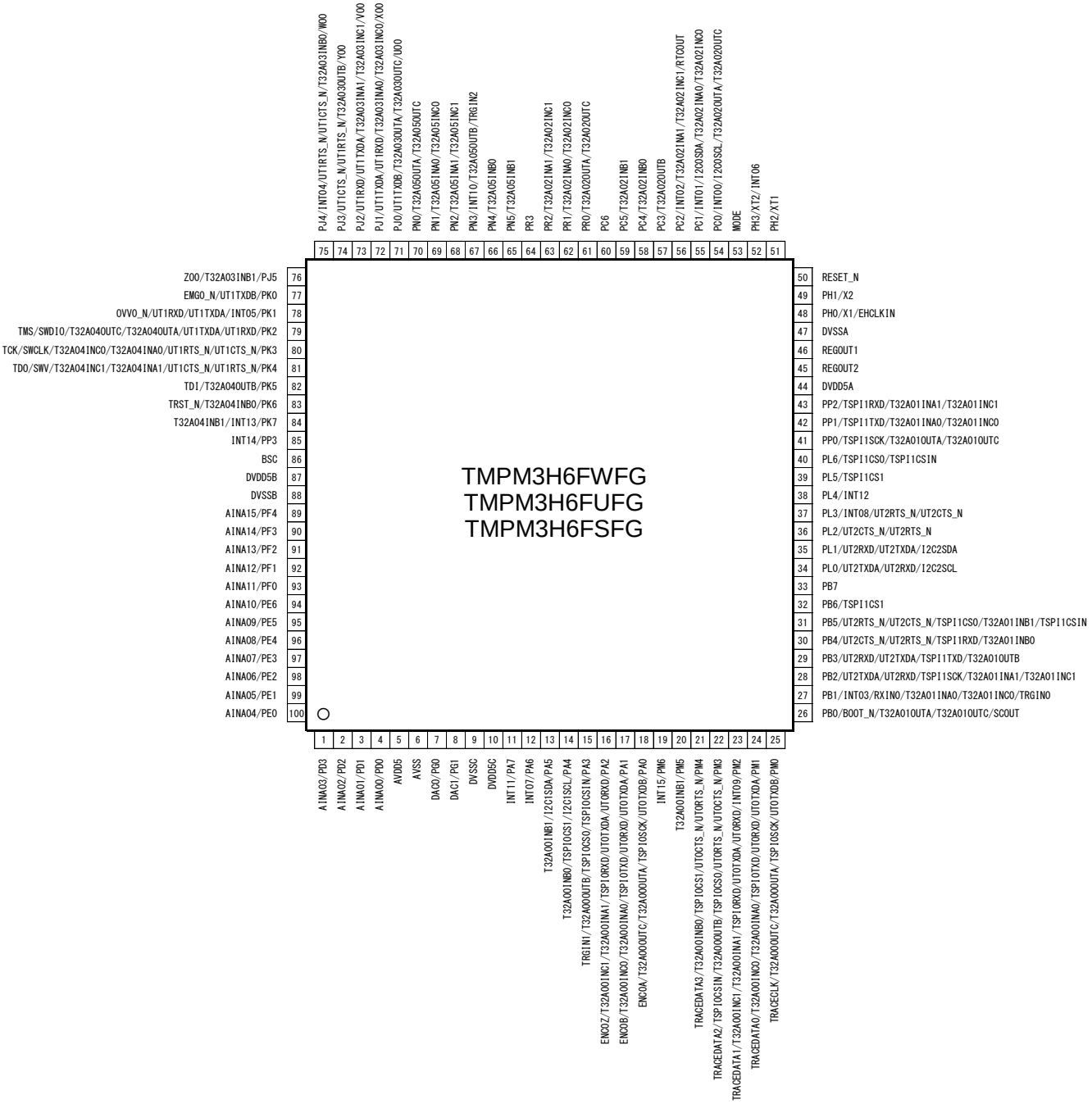
M3H Group (1) Lineup

Product Name	Memory				Package
	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Backup RAM (KB)	
TMPM3H6FWFG	128	32	16	2	LQFP100 (14mm x 14mm, 0.5mm pitch)
TMPM3H6FUFG	96	32	12		
TMPM3H6FSFG	64	16	8		
TMPM3H6FWDFG	128	32	16	2	QFP100 (14mm x 20mm, 0.65mm pitch)
TMPM3H6FUDFG	96	32	12		
TMPM3H6FSDFG	64	16	8		
TMPM3H5FWFG	128	32	16	2	LQFP80 (12mm x 12mm, 0.5mm pitch)
TMPM3H5FUFG	96	32	12		
TMPM3H5FSFG	64	16	8		
TMPM3H5FWDFG	128	32	16	2	LQFP80 (14mm x 14mm, 0.65mm pitch)
TMPM3H5FUDFG	96	32	12		
TMPM3H5FSDFG	64	16	8		
TMPM3H4FWUG	128	32	16	2	LQFP64 (10mm x 10mm, 0.5mm pitch)
TMPM3H4FUUG	96	32	12		
TMPM3H4FSUG	64	16	8		
TMPM3H4FWFG	128	32	16	2	LQFP64 (10mm x 10mm, 0.5mm pitch)
TMPM3H4FUFG	96	32	12		
TMPM3H4FSFG	64	16	8		
TMPM3H3FWUG	128	32	16	2	LQFP52 (10mm x 10mm, 0.65mm pitch)
TMPM3H3FUUG	96	32	12		
TMPM3H3FSUG	64	16	8		
TMPM3H2FWDUG	128	32	16	2	LQFP48 (7mm x 7mm, 0.5mm pitch)
TMPM3H2FUDUG	96	32	12		
TMPM3H2FSDUG	64	16	8		
TMPM3H2FWQG	128	32	16	2	VQFN48 (6mm x 6mm, 0.4mm pitch)
TMPM3H2FUQG	96	32	12		
TMPM3H2FSQG	64	16	8		
TMPM3H1FWUG	128	32	16	2	LQFP44 (10mm x 10mm, 0.8mm pitch)
TMPM3H1FUUG	96	32	12		
TMPM3H1FSUG	64	16	8		
TMPM3H1FPUG	48	8	6		
TMPM3H0FSDUG	64	16	8	2	LQFP32 (7mm x 7mm, 0.8mm pitch)
TMPM3H0FMDUG	32	8	6		

M3H Group (2) Lineup

Product Name	Memory				Package
	Code Flash (KB)	Data Flash (KB)	RAM (KB)	Backup RAM (KB)	
TMPM3HQFDFG	512	32	64	2	LQFP144 (20mm x 20mm, 0.5mm pitch)
TMPM3HQFZFG	384	32	64		
TMPM3HQFYFG	256	32	64		
TMPM3HPFDFG	512	32	64	2	LQFP128 (14mm x 14mm, 0.4mm pitch)
TMPM3HPFZFG	384	32	64		
TMPM3HPFYFG	256	32	64		
TMPM3HNFDFG	512	32	64	2	LQFP100 (14mm x 14mm, 0.5mm pitch)
TMPM3HNFZFG	384	32	64		
TMPM3HNFYFG	256	32	64		
TMPM3HNFDDFG	512	32	64	2	QFP100 (14mm x 20mm, 0.65mm pitch)
TMPM3HNFZDFG	384	32	64		
TMPM3HNFYDFG	256	32	64		
TMPM3HMFDFG	512	32	64	2	LQFP80 (12mm x 12mm, 0.5mm pitch)
TMPM3HMFZFG	384	32	64		
TMPM3HMFYFG	256	32	64		
TMPM3HLFDUG	512	32	64	2	LQFP64 (10mm x 10mm, 0.5mm pitch)
TMPM3HLFZUG	384	32	64		
TMPM3HLFYUG	256	32	64		

Pin Assignment



e.g. LQFP100

Application Circuit Example (Refrigerators)