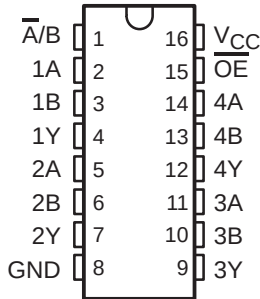


SN54LVC257A, SN74LVC257A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

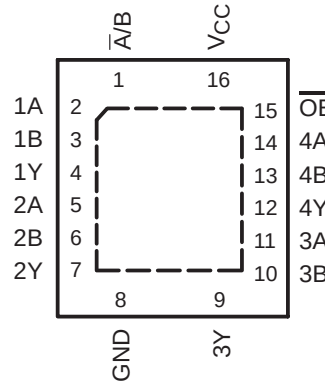
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- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.6 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
<0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
>2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

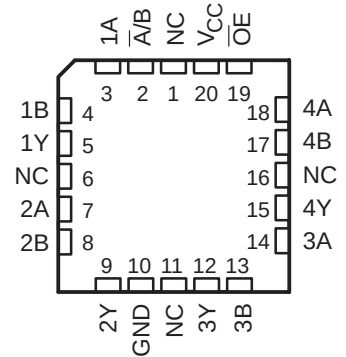
SN54LVC257A ... J OR W PACKAGE
SN74LVC257A ... D, DB, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC257A ... RGY PACKAGE
(TOP VIEW)



SN54LVC257A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These quadruple 2-line to 1-line data selectors/multiplexers are designed for 1.65-V to 3.6-V V_{CC} operation. The 'LVC257A devices are designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output-enable ($\overline{OE}$) input is at a high logic level.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC257ARGYR	LC257A
	SOIC – D	Tube of 40	SN74LVC257AD	LVC257A
		Reel of 2500	SN74LVC257ADR	
		Reel of 250	SN74LVC257ADT	
	SOP – NS	Reel of 2000	SN74LVC257ANSR	LVC257A
	SSOP – DB	Reel of 2000	SN74LVC257ADBR	LC257A
	TSSOP – PW	Tube of 90	SN74LVC257APW	LC257A
		Reel of 2000	SN74LVC257APWR	
		Reel of 250	SN74LVC257APWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC257AJ	SNJ54LVC257AJ
	CFP – W	Tube of 150	SNJ54LVC257AW	SNJ54LVC257AW
	LCCC – FK	Tube of 55	SNJ54LVC257AFK	SNJ54LVC257AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVC257A, SN74LVC257A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

WITH 3-STATE OUTPUTS

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description/ordering information (continued)

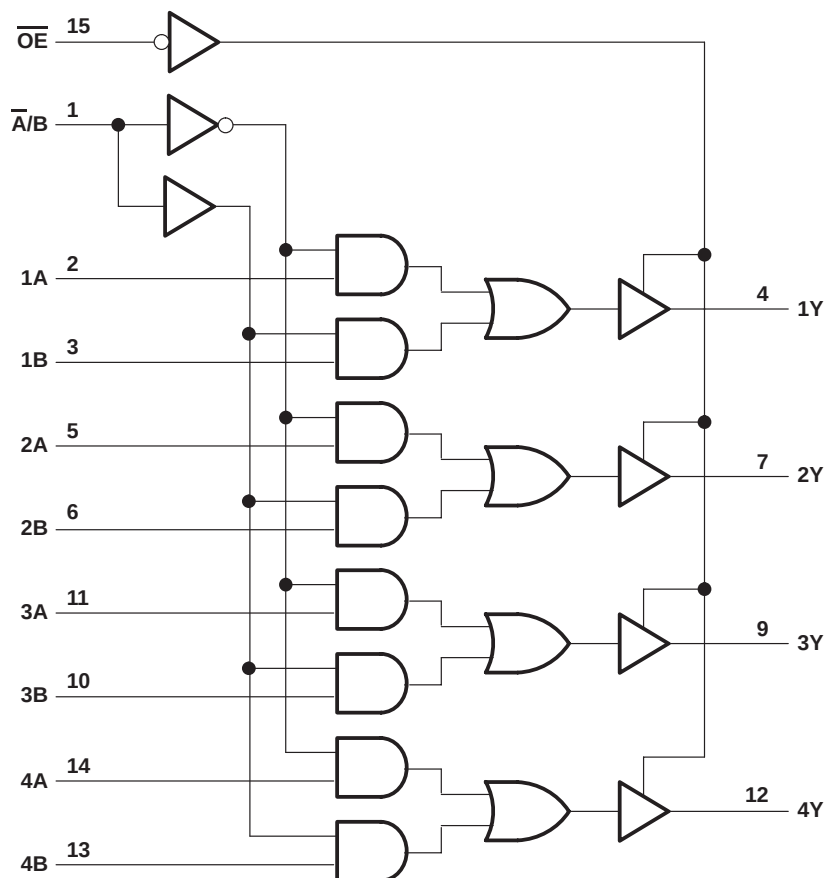
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

$\overline{OE}$	INPUTS			OUTPUT Y
	$\overline{A/B}$	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, NS, PW, RGY, and W packages.

SN54LVC257A, SN74LVC257A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
(see Note 3): DB package	82°C/W
(see Note 3): NS package	64°C/W
(see Note 3): PW package	108°C/W
(see Note 4): RGY package	39°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

		SN54LVC257A		SN74LVC257A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	Operating	2	3.6	1.65	3.6	V
	Data retention only	1.5		1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V			1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V			$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V			0.7		
	$V_{CC} = 2.7$ V to 3.6 V		0.8	0.8		
V_I Input voltage		0	5.5	0	5.5	V
V_O Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65$ V			–4		mA
	$V_{CC} = 2.3$ V			–8		
	$V_{CC} = 2.7$ V		–12	–12		
	$V_{CC} = 3$ V		–24	–24		
I_{OL} Low-level output current	$V_{CC} = 1.65$ V			4		mA
	$V_{CC} = 2.3$ V			8		
	$V_{CC} = 2.7$ V		12	12		
	$V_{CC} = 3$ V		24	24		
$\Delta t/\Delta v$ Input transition rise or fall rate			10		10	ns/V
T_A Operating free-air temperature		–55	125	–40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVC257A, SN74LVC257A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC257A			SN74LVC257A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V				V _{CC} -0.2			V
	I _{OH} = -100 μA	2.7 V to 3.6 V	V _{CC} -0.2						
	I _{OH} = -4 mA	1.65 V				1.2			
	I _{OH} = -8 mA	2.3 V				1.7			
	I _{OH} = -12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
	I _{OH} = -24 mA	3 V	2.2			2.2			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I _{OL} = 4 mA	1.65 V				0.45			
	I _{OL} = 8 mA	2.3 V				0.7			
	I _{OL} = 12 mA	2.7 V	0.4			0.4			
	I _{OL} = 24 mA	3 V	0.55			0.55			
I _I	V _I = 5.5 V or GND	3.6 V	±5			±5			μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±15			±10			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10			10			μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5			5			pF
C _O	V _O = V _{CC} or GND	3.3 V	5			5			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC257A				UNIT
			V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	5.4		1	4.6	ns
	$\overline{A/B}$		7.5		1	6.4	
t _{en}	$\overline{OE}$	Y	6.7		1	5.6	ns
t _{dis}	$\overline{OE}$	Y	4.7		0.5	4.3	ns
t _{sk(o)}					1		ns

SN54LVC257A, SN74LVC257A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC257A								UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1	13.5	1	7.4	1	5.4	1	4.6	ns
	$\overline{A/B}$		1	15.6	1	9.5	1	7.5	1	6.4	
t _{en}	$\overline{OE}$	Y	1	14.6	1	8.7	1	6.7	1	5.6	ns
t _{dis}	$\overline{OE}$	Y	1	15.4	1	6.7	1	4.7	1	4.3	ns
t _{sk(o)}									1		ns

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	13.5	14.5	15.5	pF



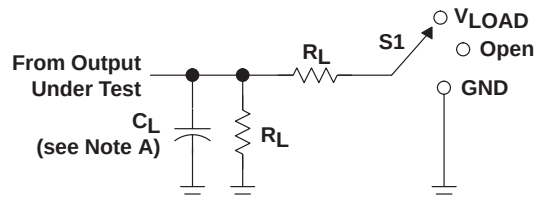
SN54LVC257A, SN74LVC257A

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

WITH 3-STATE OUTPUTS

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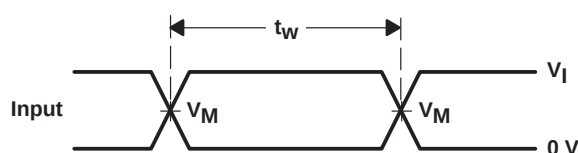
PARAMETER MEASUREMENT INFORMATION



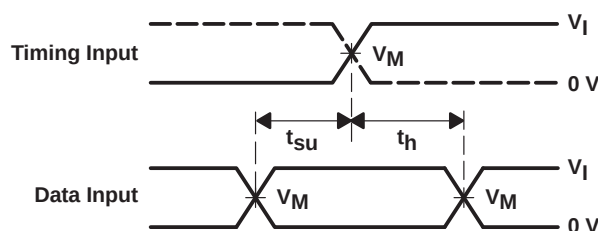
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

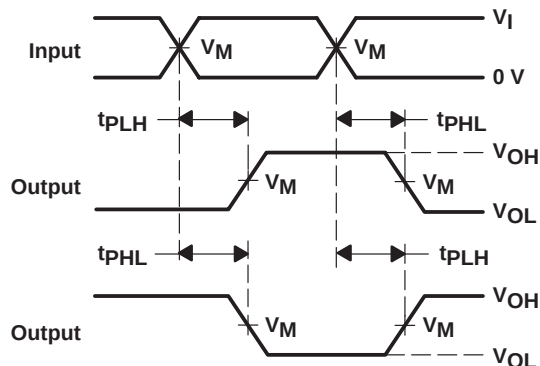
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



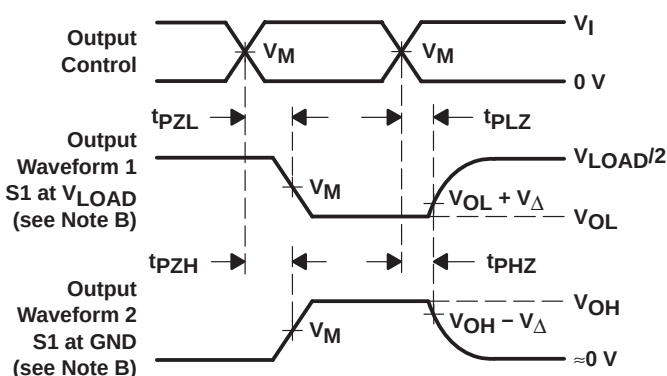
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

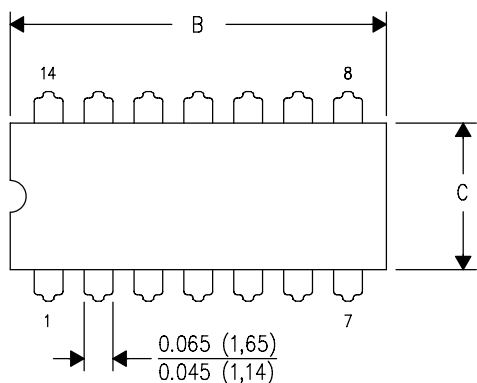


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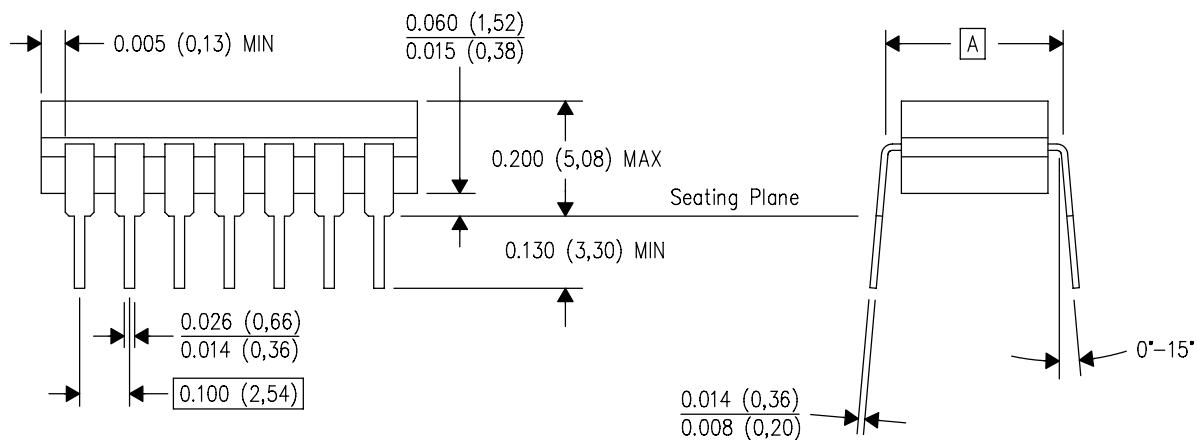
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

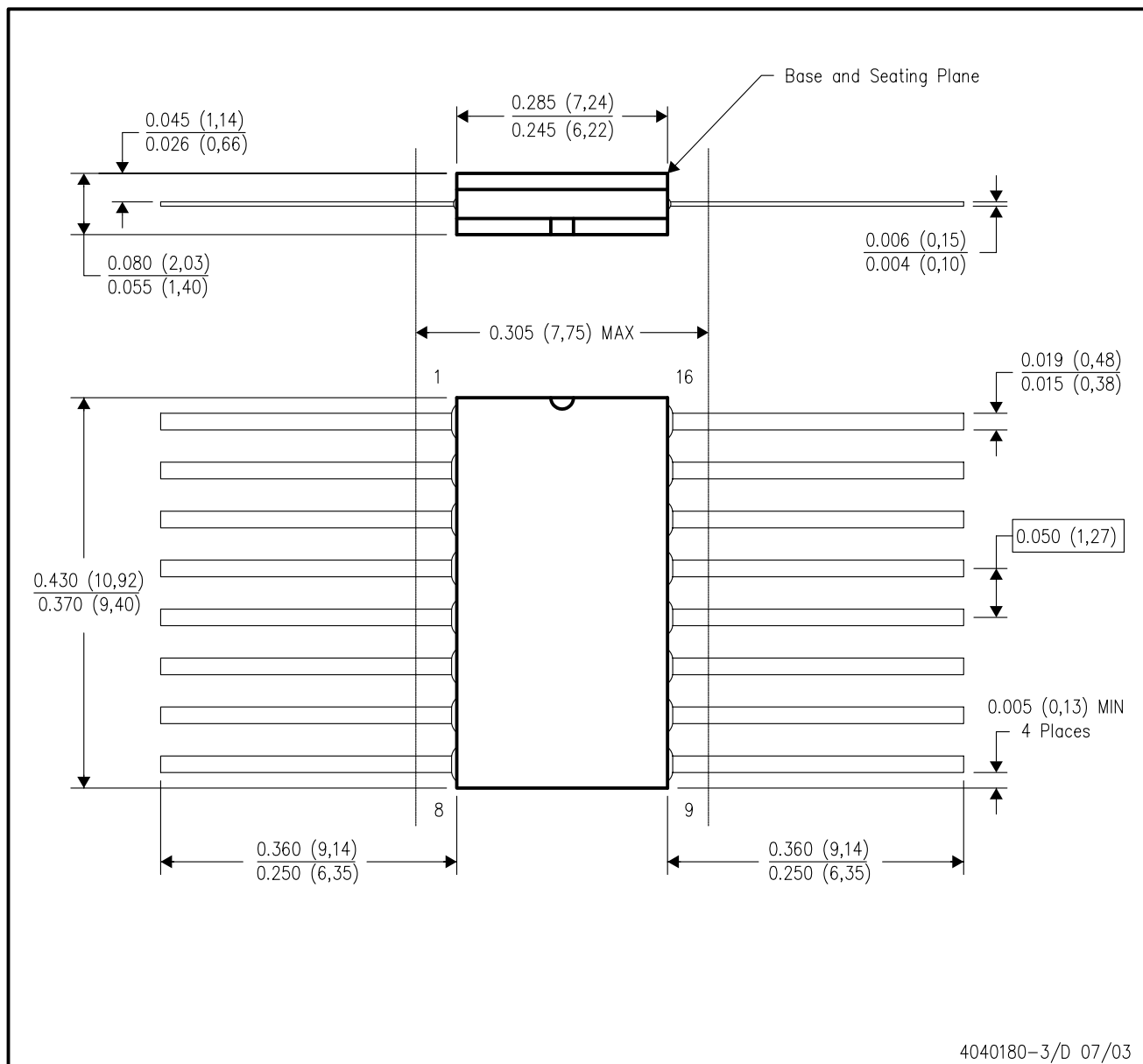


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

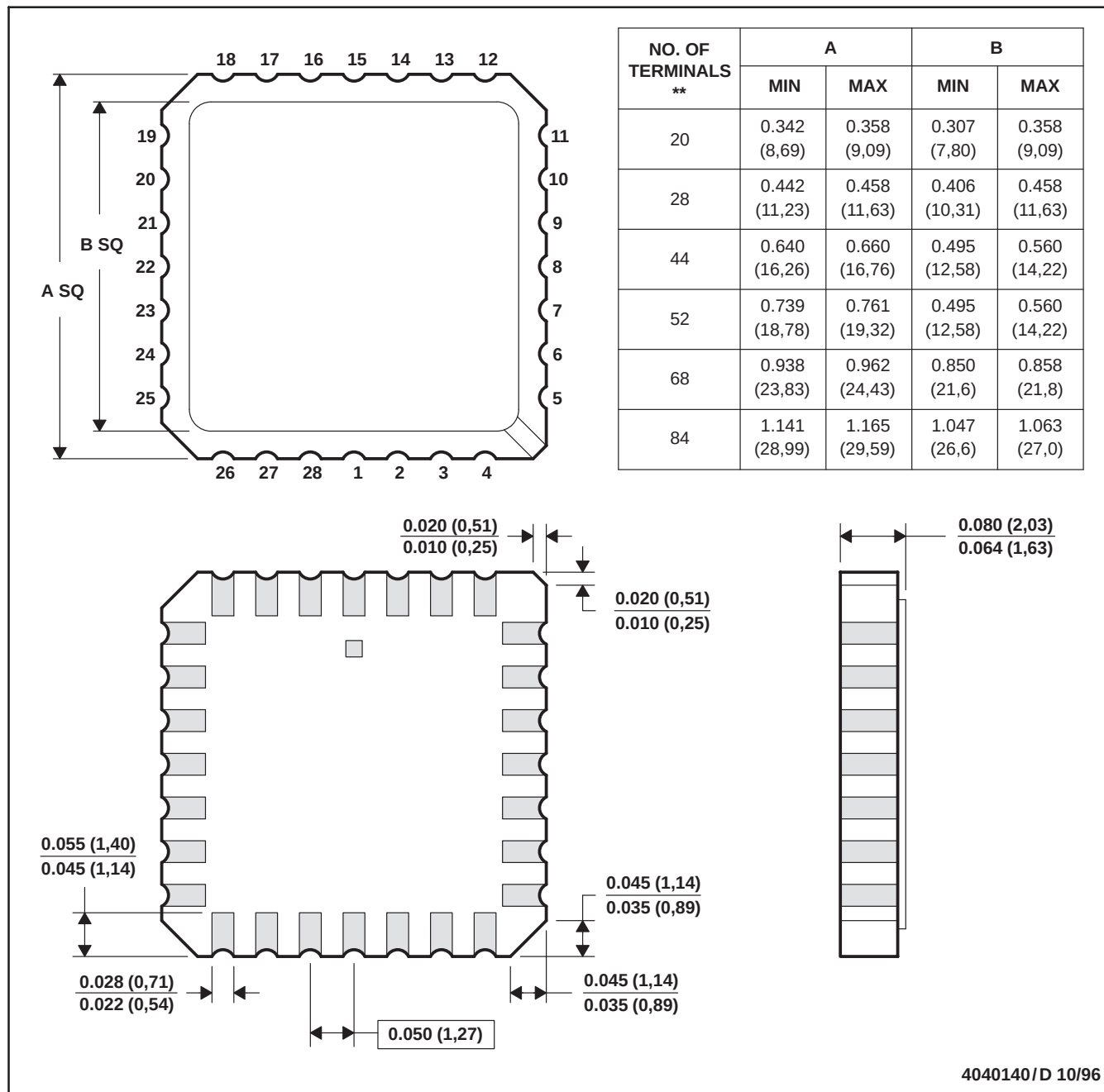


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

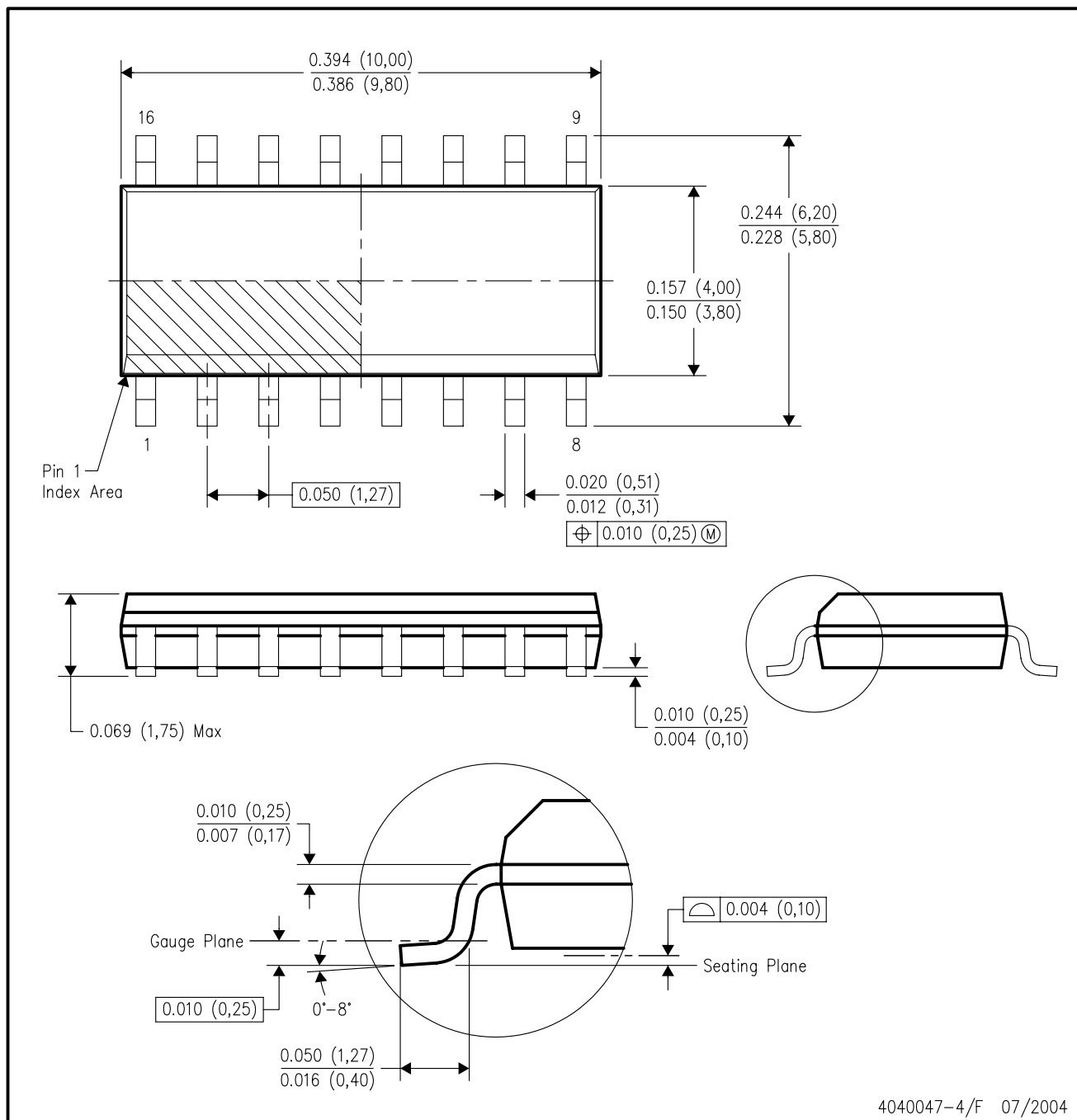
28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

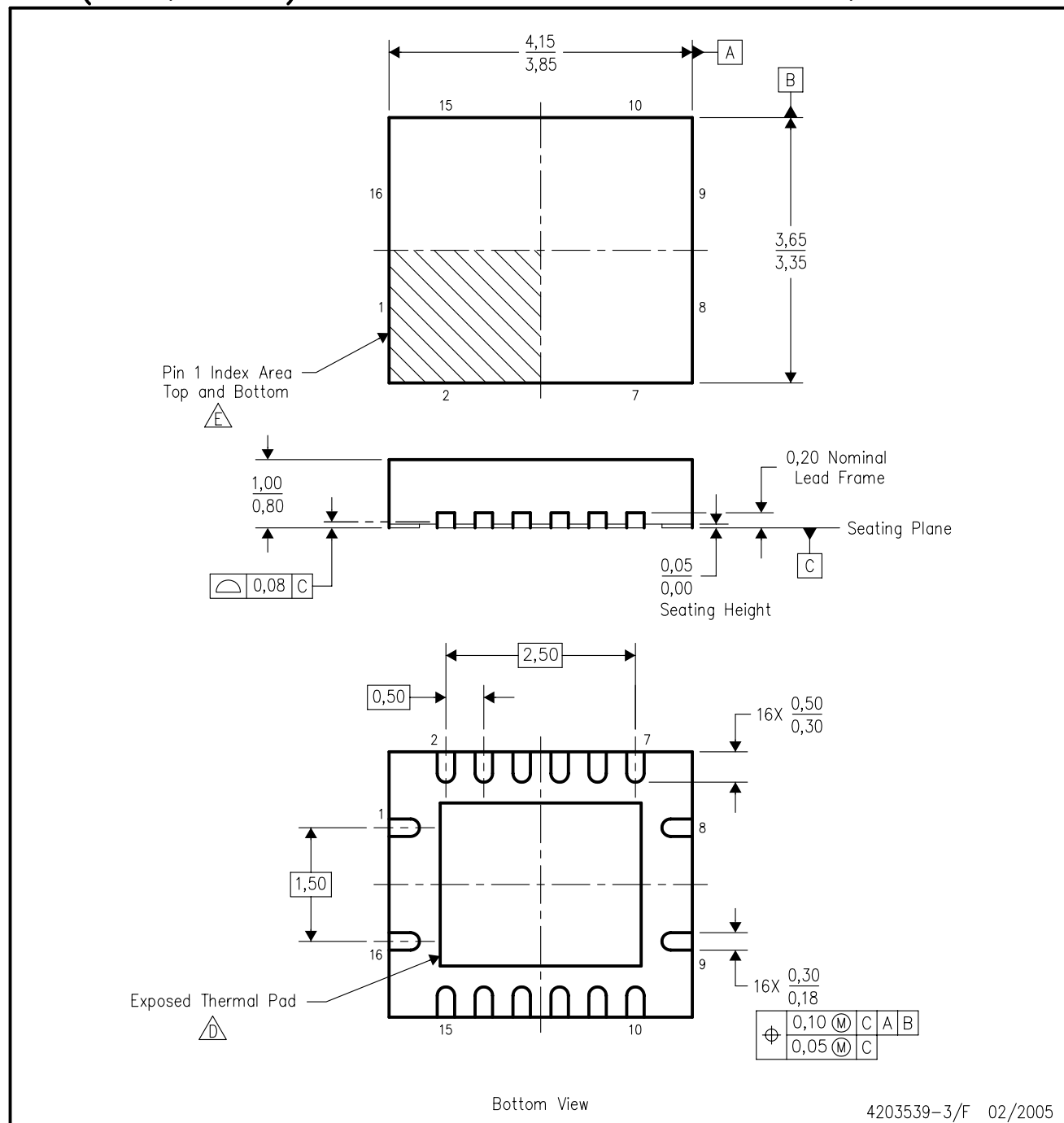
PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

RGY (R-PQFP-N16)

PLASTIC QUAD FLATPACK



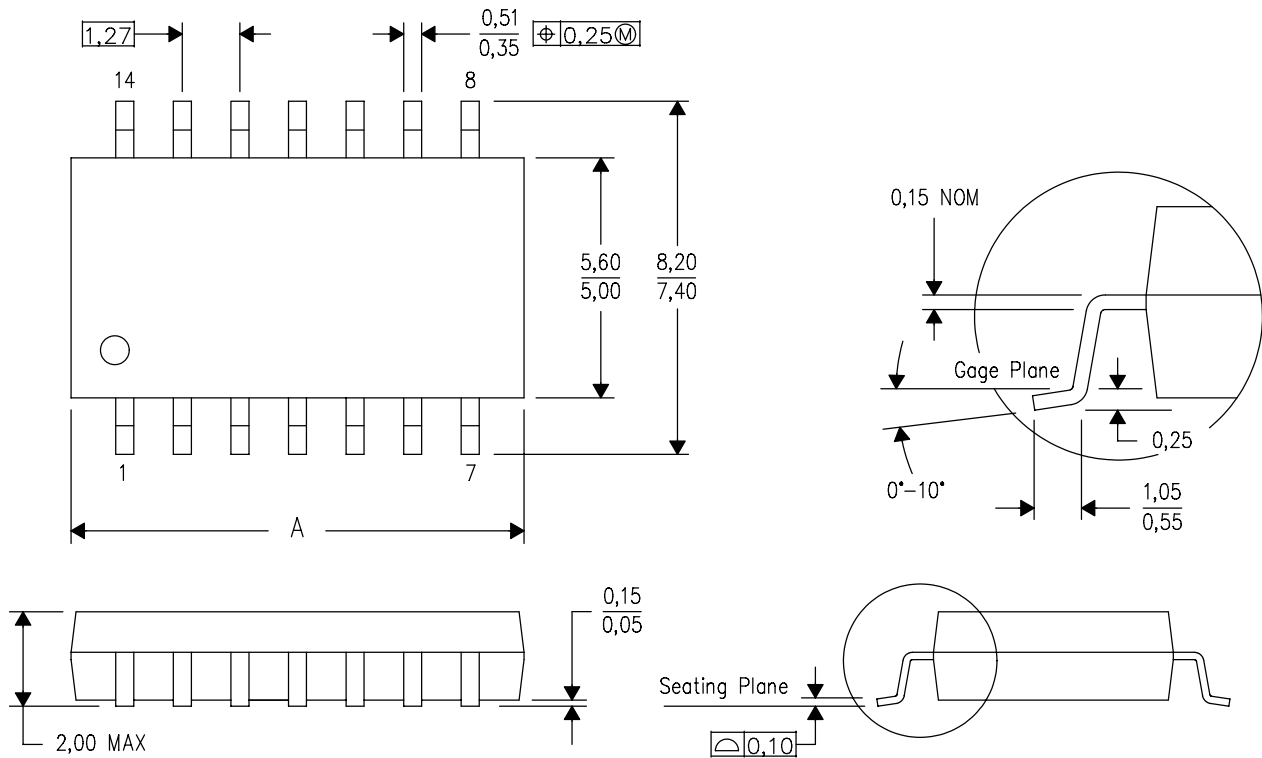
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

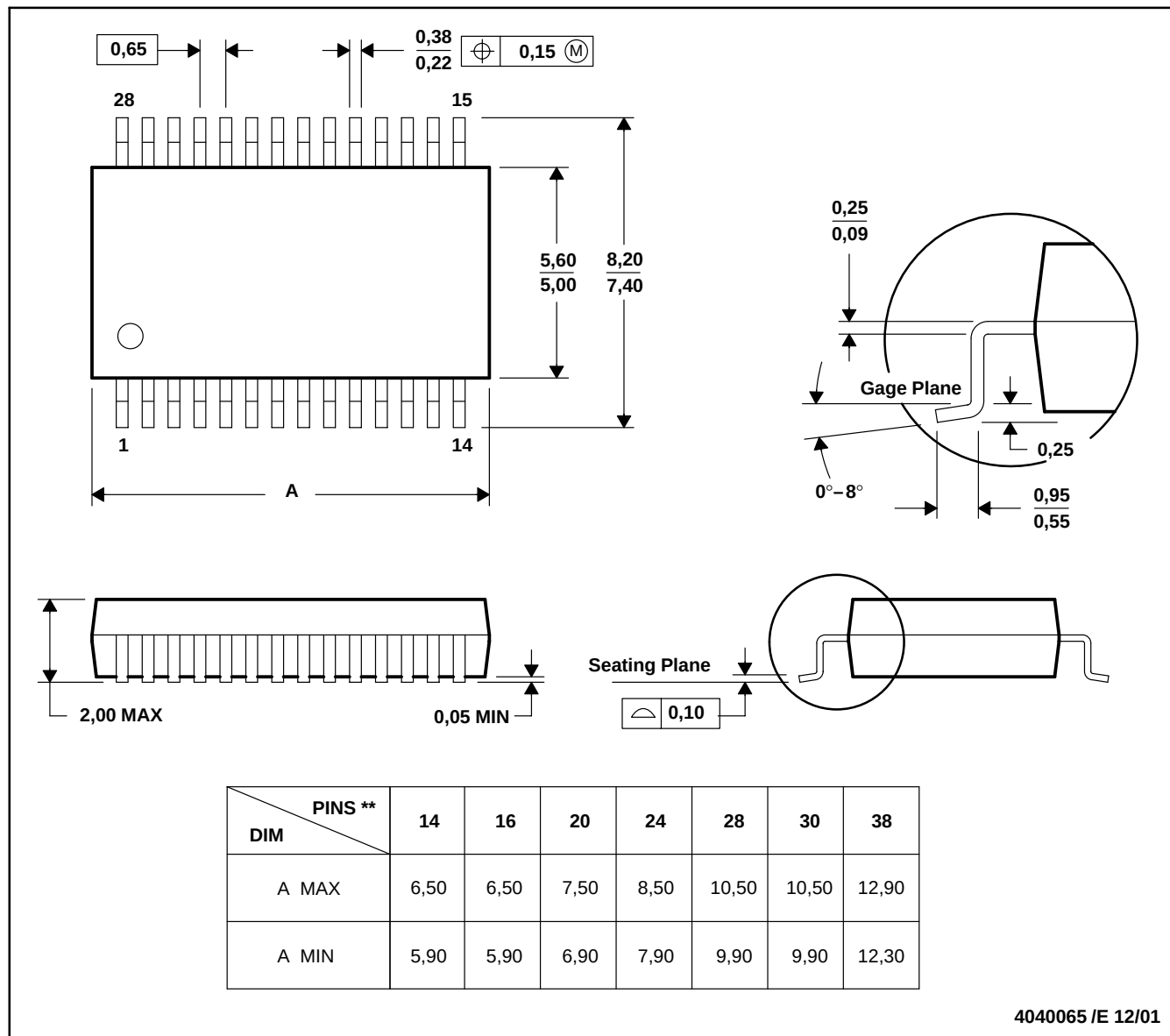
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

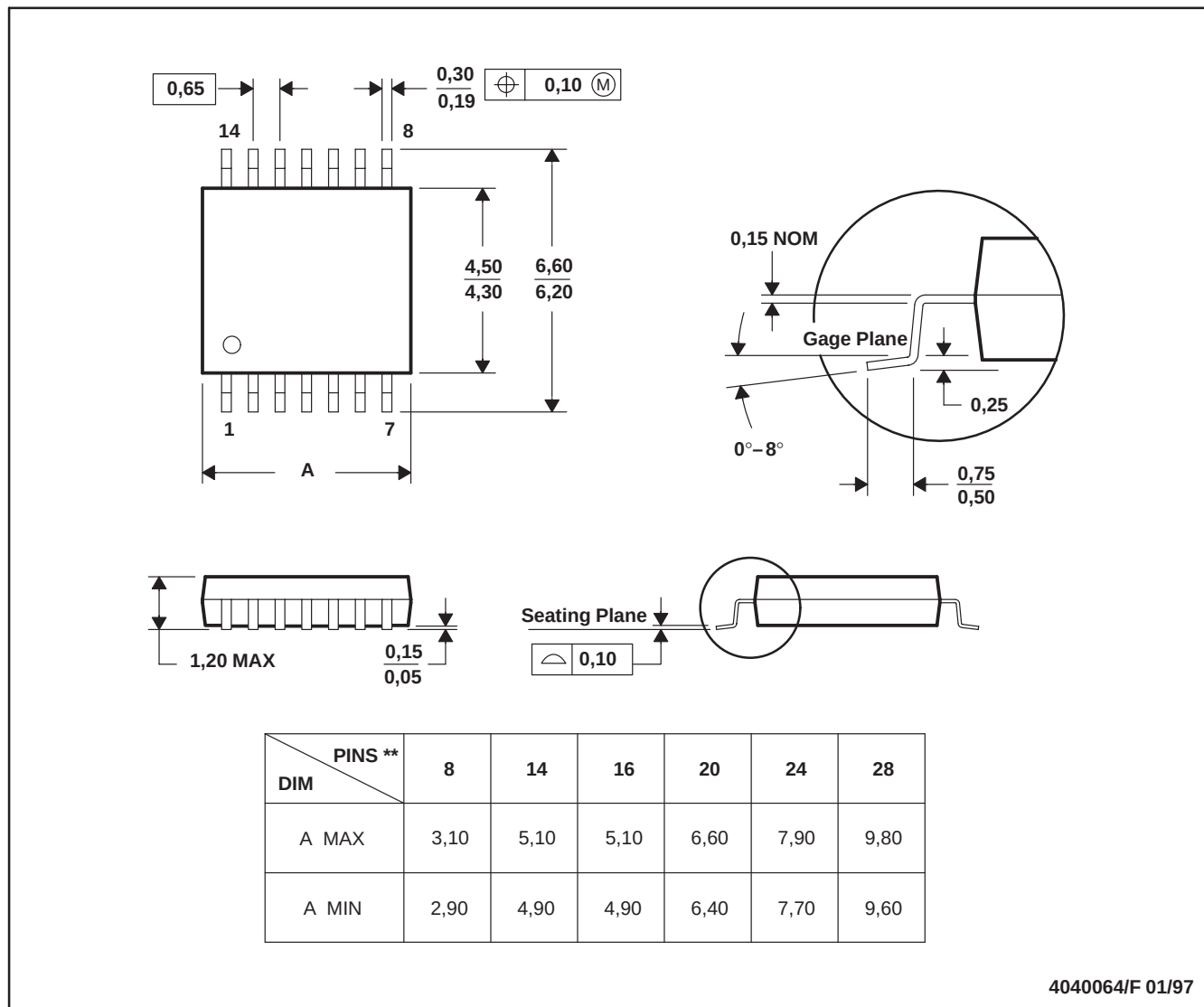


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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