PCF85363A

Tiny Real-Time Clock/calendar with 64 byte RAM, alarm function, battery switch-over time stamp input, and I²C-bus

Rev. 2 — 15 January 2015 Product data sheet

1. General description

The PCF85363A is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low power consumption and with automatic switching to battery on main power loss. The RTC can also be configured as a stop-watch (elapsed time counter). Three time log registers triggered from battery switch-over as well as input driven events. Featuring clock output and two independent interrupt signals, two alarms, I²C interface and quartz crystal calibration, 64 byte battery backed-up RAM.

For a selection of NXP Real-Time Clocks, see Table 72 on page 86.

2. Features and benefits

- UL Recognized Component (PCF85363ATL)
- Provides year, month, day, weekday, hours, minutes, seconds and 100th seconds based on a 32.768 kHz quartz crystal
- Stop-watch mode for elapsed time counting. From 100th seconds to 999999 hours
- Two independent alarms
- Battery back-up circuit
- WatchDog timer
- Three timestamp registers
- Two independent interrupt generators plus predefined interrupts at every second, minute, or hour
- 64 byte battery backed-up RAM
- Frequency adjustment via programmable offset register
- Clock operating voltage: 0.9 V to 5.5 V
- Low current; typical 0.28 μA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 400 kHz two-line I²C-bus interface (at V_{DD} = 1.8 V to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 16.384 kHz, 8.192 kHz, 4.096 kHz, 2.048 kHz, 1.024 kHz, and 1 Hz)
- Configurable oscillator circuit for a wide variety of quartzes: C_L = 6 pF, C_L = 7 pF, and C_L = 12.5 pF

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 24.

3. Applications

- Elapsed time counter
- Printers and copiers
- Digital voice recorders
- Mobile equipment
- Digital cameras
- Network powered devices
- Battery backed up systems
- Data loggers
- White goods
- Accurate high duration timer

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF85363ATL	DFN2626-10	plastic thermal enhanced extremely thin small outline package; no leads; 10 terminals; body 2.6 × 2.6 × 0.5 mm	SOT1197-1
PCF85363ATT	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCF85363ATT1	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1

4.1 Ordering options

Table 2. Ordering options

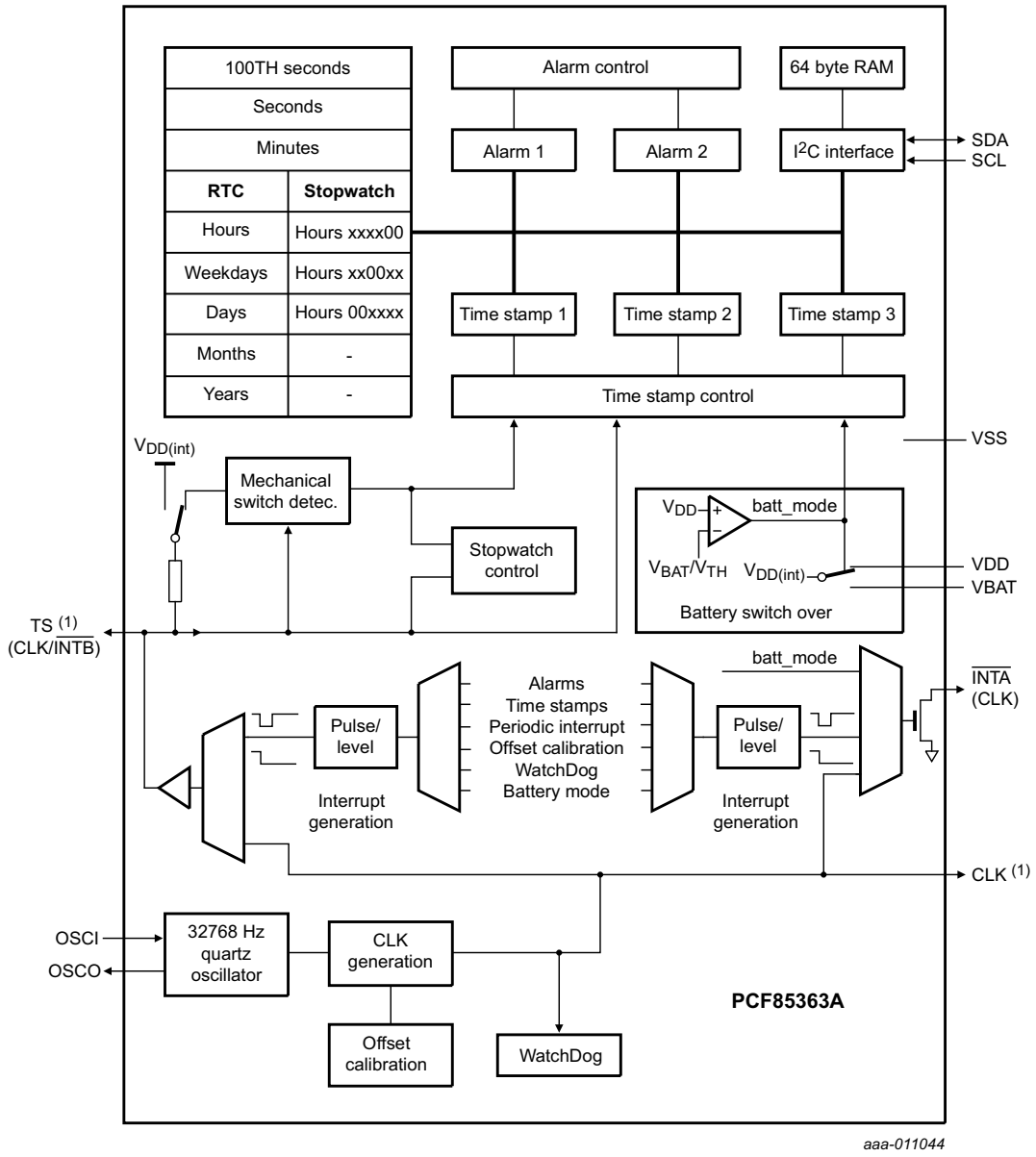
Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCF85363ATL/A	PCF85363ATL/AX	935304648115	tape and reel, 7 inch	1
PCF85363ATT/A	PCF85363ATT/AJ	935304751118	tape and reel, 13 inch	1
PCF85363ATT1/A	PCF85363ATT1/AJ	935304752118	tape and reel, 13 inch	1

5. Marking

Table 3. Marking codes

Product type number	Marking code
PCF85363ATL/A	363A
PCF85363ATT/A	363A
PCF85363ATT1/A	363A

6. Block diagram

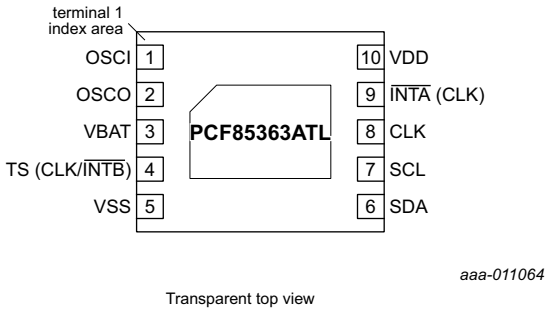


(1) Not available on all package types.

Fig 1. Block diagram of PCF85363A

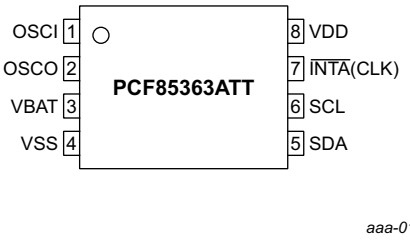
7. Pinning information

7.1 Pinning



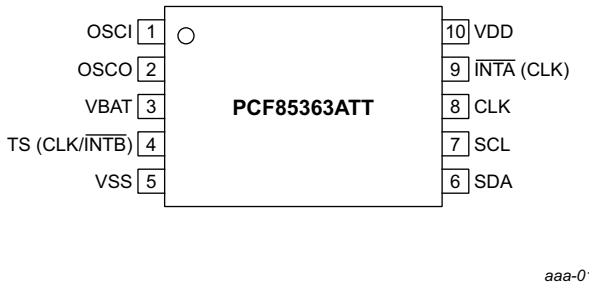
For mechanical details, see Figure 43 on page 78.

Fig 2. Pin configuration for PCF85363ATL (DFN2626-10)



For mechanical details, see Figure 44 on page 79.

Fig 3. Pin configuration for PCF85363ATT (TSSOP8)



For mechanical details, see Figure 45 on page 80.

Fig 4. Pin configuration for PCF85363ATT1 (TSSOP10)

7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol				Type	Description	
	PCF85363ATL (DFN2626-10)	PCF85363ATT (TSSOP8)	PCF85363ATT1 (TSSOP10)		Primary use	Secondary use
OSCI	1	1	1	input	oscillator input	-
OSCO	2	2	2	output	oscillator output	-
VBAT	3	3	3	supply	battery backup supply voltage[1]	-
TS (CLK/$\overline{\text{INTB}}$)	4	-	4	input/ output	can be configured with TSPM[1:0][2]	
					timestamp input	$\overline{\text{INTB}}$ and CLK output (push-pull); stop-watch control
VSS	5[3]	4	5	supply	ground supply voltage	-
SDA	6	5	6	input/ output	serial data line	-
SCL	7	6	7	input	serial clock input	-
CLK	8	-	8	output	CLK (push-pull)	-
$\overline{\text{INTA}}$ (CLK)	9	7	9	output	can be configured with INTAPM[1:0][4]	
					interrupt output (open-drain)	CLK output (open-drain)
VDD	10	8	10	supply	supply voltage	-

[1] Connect to V_{DD} if not used.

[2] See Table 7 and Table 47.

[3] The die paddle (exposed pad) is connected to V_{SS} and should be electrically isolated.

[4] See Table 7 and Table 49.

8. Functional description

The PCF85363A contains 8-bit registers for time information, for timestamp information and registers for system configuration. Included is an auto-incrementing register address, an on-chip 32.768 kHz oscillator with integrated capacitors, a frequency divider which provides the source clock for the Real-Time Clock (RTC) and calender, and an I²C-bus interface with a maximum data rate of 400 kbit/s.

The built-in address register will increment automatically after each read or write of a data byte. After register 2Fh, the auto-incrementing will wrap around to address 00h. When the RAM is accessed, the wrap around will happen after address 7Fh, (see Figure 5).

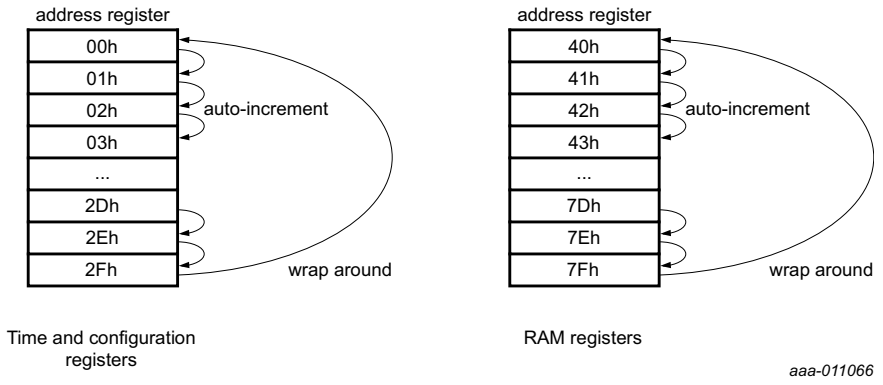


Fig 5. Address register incrementing

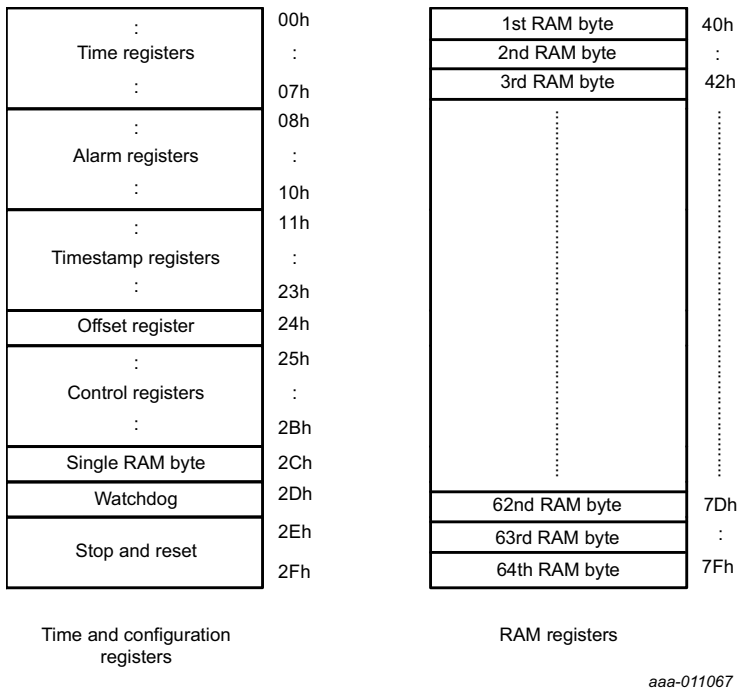


Fig 6. Register map

All registers (see Table 5 on page 8, Table 6 on page 10, and Table 7 on page 12) are designed as addressable 8-bit parallel registers although not all bits are implemented. Figure 6 gives an overview of the address map.

The 100th seconds, seconds, minutes, hours, days, months, and years as well as the corresponding alarm registers are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is read, the contents of all time counters are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented.

8.1 Registers organization overview

8.1.1 Time mode registers

The PCF85363A has two time mode register sets, one for the real-time clock mode and one for the stopwatch clock mode. The access to these registers can be switched by the RTCM bit in the Function control register (28h), see Table 7 on page 12 and Table 54 on page 54.

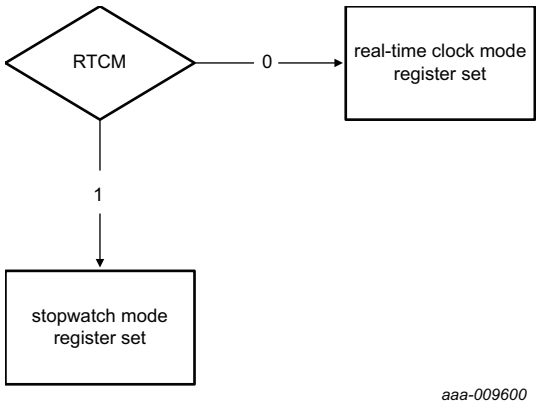


Fig 7. Time mode register set selection

8.1.1.1 RTC mode time registers overview (RTCM = 0)

Table 5. RTC mode time registers

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 58.

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
RTC time and date registers										
00h	100th_seconds	100TH_SECONDS (0 to 99)								Section 8.2
01h	Seconds	OS	SECONDS (0 to 59)							
02h	Minutes	EMON	MINUTES (0 to 59)							
03h	Hours	-	-	AMPM	HOURS (1 to 12) in 12 hour mode					
				HOURS (0 to 23) in 24 hour mode						
04h	Days	-	-	DAYS (1 to 31)						
05h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)			
06h	Months	-	-	-	MONTHS (1 to 12)					
07h	Years	YEARS (0 to 99)								
RTC alarm1										
08h	Second_alarm1	-	SEC_ALARM1 (0 to 59)							Section 8.4
09h	Minute_alarm1	-	MIN_ALARM1 (0 to 59)							
0Ah	Hour_alarm1	-	-	AMPM	HR_ALARM1 (1 to 12) in 12 hour mode					
				HR_ALARM1 (0 to 23) in 24 hour mode						
0Bh	Day_alarm1	-	-	DAY_ALARM1 (1 to 31)						
0Ch	Month_alarm1	-	-	-	MON_ALARM1 (1 to 12)					
RTC alarm2										
0Dh	Minute_alarm2	-	MIN_ALARM2 (0 to 59)							Section 8.4
0Eh	Hour_alarm2	-	-	AMPM	HR_ALARM2 (1 to 12) in 12 hour mode					
0Fh	Weekday_alarm 2	-	-	-	-	-	WDAY_ALARM2 (0 to 6)			
RTC alarm enables										
10h	Alarm_enables	WDAY_A2E	HR_A2E	MIN_A2E	MON_A1E	DAY_A1E	HR_A1E	MIN__A1E	SEC__A1E	Section 8.4

Table 5. RTC mode time registers *...continued*

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 58.

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
RTC timestamp1 (TSR1)										
11h	TSR1_seconds	-	TSR1_SECONDS (0 to 59)							Section 8.7
12h	TSR1_minutes	-	TSR1_MINUTES (0 to 59)							
13h	TSR1_hours	-	-	AMPM	TSR1_HOURS (1 to 12) in 12 hour mode					
				TSR1_HOURS (0 to 23) in 24 hour mode						
14h	TSR1_days	-	-	TSR1_DAYS (1 to 31)						
15h	TSR1_months	-	-	-	TSR1_MONTHS (1 to 12)					
16h	TSR1_years	TSR1_YEARS (0 to 99)								
RTC timestamp2 (TSR2)										
17h	TSR2_seconds	-	TSR2_SECONDS (0 to 59)							Section 8.7
18h	TSR2_minutes	-	TSR2_MINUTES (0 to 59)							
19h	TSR2_hours	-	-	AMPM	TSR2_HOURS (1 to 12) in 12 hour mode					
				TSR2_HOURS (0 to 23) in 24 hour mode						
1Ah	TSR2_days	-	-	TSR2_DAYS (1 to 31)						
1Bh	TSR2_months	-	-	-	TSR2_MONTHS (1 to 12)					
1Ch	TSR2_years	TSR2_YEARS (0 to 99)								
RTC timestamp3 (TSR3)										
1Dh	TSR3_seconds	-	TSR3_SECONDS (0 to 59)							Section 8.7
1Eh	TSR3_minutes	-	TSR3_MINUTES (0 to 59)							
1Fh	TSR3_hours	-	-	AMPM	TSR3_HOURS (1 to 12) in 12 hour mode					
				TSR3_HOURS (0 to 23) in 24 hour mode						
20h	TSR3_days	-	-	TSR3_DAYS (1 to 31)						
21h	TSR3_months	-	-	-	TSR3_MONTHS (1 to 12)					
22h	TSR3_years	TSR3_YEARS (0 to 99)								
RTC timestamp mode control										
23h	TSR_mode	TSR3M[1:0]		-	TSR2M[2:0]			TSR1M[1:0]		Section 8.7

8.1.1.2 Stop-watch mode time registers (RTCM = 1)

Table 6. Stop-watch mode time registers

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 58.

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
Stop-watch time registers										
00h	100th_seconds	100TH_SECONDS (0 to 99)								Section 8.3
01h	Seconds	OS	SECONDS (0 to 59)							
02h	Minutes	EMON	MINUTES (0 to 59)							
03h	Hours_xx_xx_00	HR_XX_XX_00 (0 to 99)								
04h	Hours_xx_00_xx	HR_XX_00_XX (0 to 99)								
05h	Hours_00_xx_xx	HR_00_XX_XX (0 to 99)								
06h	not used	-	-	-	-	-	-	-	-	
07h	not used	-	-	-	-	-	-	-	-	
Stop-watch alarm1										
08h	Second_alm1	-	SEC_ALM1 (0 to 59)							Section 8.4
09h	Minute_alm1	-	MIN_ALM1 (0 to 59)							
0Ah	Hr_xx_xx_00_alm1	HR_XX_XX_00_ALM1 (0 to 99)								
0Bh	Hr_xx_00_xx_alm1	HR_XX_00_XX_ALM1 (0 to 99)								
0Ch	Hr_00_xx_xx_alm1	HR_00_XX_XX_ALM1 (0 to 99)								
Stop-watch alarm2										
0Dh	Minute_alm2	-	MIN_ALM2 (0 to 59)							Section 8.4
0Eh	Hr_xx_00_alm2	HR_XX_00_ALM2 (0 to 99)								
0Fh	Hr_00_xx_alm2	HR_00_XX_ALM2 (0 to 99)								
Stop-watch alarm enables										
10h	Alarm_enables	HR_00_XX_A2E	HR_XX_00_A2E	MIN_A2E	HR_00_XX_XX_A1E	HR_XX_00_XX_A1E	HR_XX_XX_00_A1E	MIN_A1E	SEC_A1E	Section 8.4

Table 6. Stop-watch mode time registers *…continued*

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 58. …continued

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
Stop-watch timestamp1 (TSR1)										
11h	TSR1_seconds	-	TSR1_SECONDS (0 to 59)							Section 8.7
12h	TSR1_minutes	-	TSR1_MINUTES (0 to 59)							
13h	TSR1_hr_xx_xx_00	TSR1_HR_XX_XX_00 (0 to 99)								
14h	TSR1_hr_xx_00_xx	TSR1_HR_XX_00_XX (0 to 99)								
15h	TSR1_hr_00_xx_xx	TSR1_HR_00_XX_XX (0 to 99)								
16h	not used	-	-	-	-	-	-	-	-	
Stop-watch timestamp2 (TSR2)										
17h	TSR2_seconds	-	TSR2_SECONDS (0 to 59)							Section 8.7
18h	TSR2_minutes	-	TSR2_MINUTES (0 to 59)							
19h	TSR2_hr_xx_xx_00	TSR2_HR_XX_XX_00 (0 to 99)								
1Ah	TSR2_hr_xx_00_xx	TSR2_HR_XX_00_XX (0 to 99)								
1Bh	TSR2_hr_00_xx_xx	TSR2_HR_00_XX_XX (0 to 99)								
1Ch	not used	-	-	-	-	-	-	-	-	
Stop-watch timestamp3 (TSR3)										
1Dh	TSR3_seconds	-	TSR3_SECONDS (0 to 59)							Section 8.7
1Eh	TSR3_minutes	-	TSR3_MINUTES (0 to 59)							
1Fh	TSR3_hr_xx_xx_00	TSR3_HR_XX_XX_00 (0 to 99)								
20h	TSR3_hr_xx_00_xx	TSR3_HR_XX_00_XX (0 to 99)								
21h	TSR3_hr_00_xx_xx	TSR3_HR_00_XX_XX (0 to 99)								
22h	not used	-	-	-	-	-	-	-	-	
Stop-watch timestamp mode control										
23h	TSR_mode	TSR3M[1:0]		-	TSR2M[2:0]			TSR1M[1:0]		Section 8.7

8.1.2 Control registers overview

Table 7. Control and function registers overview

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 58.

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
Offset register										
24h	Offset	OFFSET[7:0]								Section 8.8
Control registers										
25h	Oscillator	CLKIV	OFFM	12_24	LOWJ	OSCD[1:0]		CL[1:0]		Section 8.10
26h	Battery_switch	-	-	-	BSOFF	BSRR	BSM[1:0]		BSTH	Section 8.11
27h	Pin_IO	CLKPM	TSPULL	TSL	TSIM	TSPM[1:0]		INTAPM[1:0]		Section 8.12
28h	Function	100TH	PI[1:0]		RTCM	STOPM	COF[2:0]			Section 8.13
29h	INTA_enable	ILPA	PIEA	OIEA	A1IEA	A2IEA	TSRIEA	BSIEA	WDIEA	Section 8.9
2Ah	INTB_enable	ILPB	PIEB	OIEB	A1IEB	A2IEB	TSRIEB	BSIEB	WDIEB	Section 8.9
2Bh	Flags	PIF	A2F	A1F	WDF	BSF	TSR3F	TSR2F	TSR1F	Section 8.14
Single RAM byte										
2Ch	RAM_byte	B[7:0]								Section 8.6
WatchDog registers										
2Dh	WatchDog	WDM	WDR[4:0]					WDS[1:0]		Section 8.5
Stop										
2Eh	Stop_enable	-	-	-	-	-	-	-	STOP	Section 8.16
Reset										
2Fh	Resets	CPR	0	1	0	SR	1	0	CTS	Section 8.15
RAM (64 byte)										
40h to 7Fh	RAM	B[7:0]								Section 8.17

8.2 RTC mode time and date registers

RTC mode is enabled by setting RTCM = 0. These registers are coded in the BCD format to simplify application use.

Default state is:

Time — 00:00:00.00

Date — 2000 01 01

Weekday — Saturday

Monitor bits — OS = 1, EMON = 0

Table 8. Time and date registers in RTC mode (RTCM = 0)

Bit positions labeled as - are not implemented and return 0 when read.

Address	Register name	Upper-digit (ten's place)				Digit (unit place)			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	100th_seconds[1]	0 to 9				0 to 9			
01h	Seconds	OS	0 to 5			0 to 9			
02h	Minutes	EMON	0 to 5			0 to 9			
03h	Hours[2]	-	-	AMPM	0 to 1	0 to 9			
				0 to 2		0 to 9			
04h	Days[3]	-	-	0 to 3		0 to 9			
05h	Weekdays	-	-	-	-	-	0 to 6		
06h	Months	-	-	-	0 to 1	0 to 9			
07h	Years	0 to 9				0 to 9			

[1] The 100th_seconds register is only available when the 100TH mode is enabled, see Section 8.13.1. When the 100TH mode is disabled, this register always returns 0.

[2] Hour mode is set by the 12_24 bit in the Oscillator register, see Section 8.10 on page 41.

[3] If the year counter contains a value, which is exactly divisible by 4, the PCF85363A compensates for leap years by adding a 29th day to February.

8.2.1 Definition of BCD

The Binary-Coded Decimal (BCD) is an encoding of numbers where each digit is represented by a separate bit field. Each bit field may only contain the values 0 to 9. In this way, decimal numbers and counting is implemented.

Example: 59 encoded as an entire number is represented by 3Bh or 111011. In BCD the 5 is represented as 5h or 0101 and the 9 as 9h or 1001 which combines to 59h.

Table 9. BCD coding

Value in decimal	Upper-digit (ten's place)				Digit (unit place)			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0	0
01	0	0	0	1	0	0	0	1
02	0	0	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:
09	1	0	0	1	1	0	0	1
10	0	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
98	1	0	0	1	1	0	0	0
99	1	0	0	1	1	0	0	1

8.2.2 OS: Oscillator stop

When the oscillator of the PCF85363A is stopped, the OS status bit is set. The oscillator can be stopped, for example, by connecting one of the oscillator pins OSCI or OSCO to ground. The oscillator is considered to be stopped during the time between power-on and stable crystal resonance. This time can be in the range of 200 ms to 2 s depending on crystal type, temperature, and supply voltage.

The status bit remains set until cleared by command (see Figure 8). If the bit cannot be cleared, then the oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

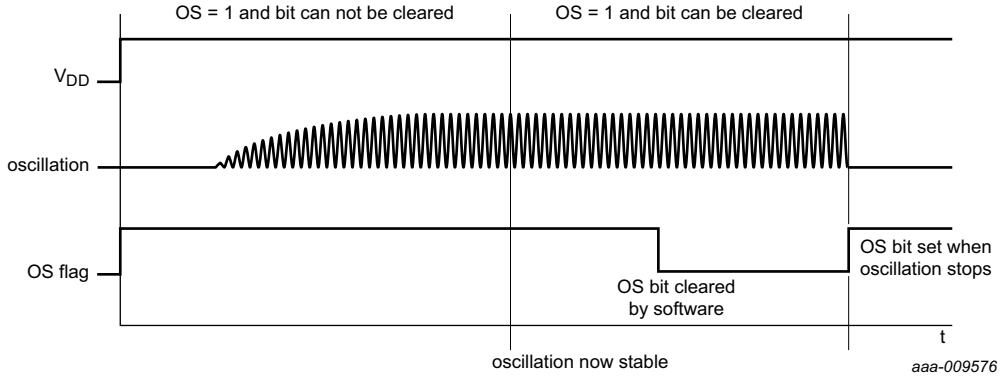


Fig 8. OS status bit

8.2.3 EMON: event monitor

The EMON can be used to monitor the status of all the flags in the Flags register, see Section 8.14 on page 56. When one or more of the flags is set, then the EMON bit returns a logic 1. The EMON bit cannot be cleared. EMON returns a logic 0 when all flags are cleared.

See Figure 21 on page 40 for a pictorial representation.

8.2.4 Definition of weekdays

Definition may be reassigned by the user.

Table 10. Weekday assignments

Day	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

8.2.5 Definition of months

Table 11. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.2.6 Setting and reading the time in RTC mode

Figure 9 shows the data flow and data dependencies starting from the 100 Hz clock tick.

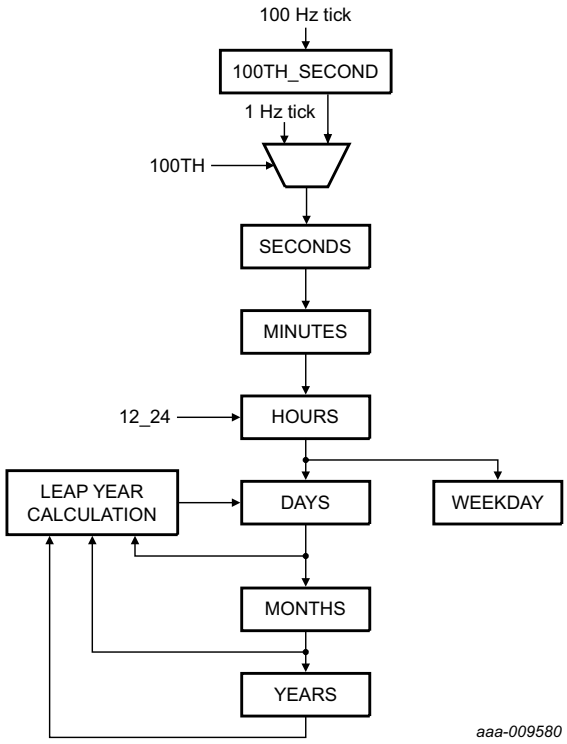


Fig 9. Data flow for the time function

During read operations, the time counting circuits (memory locations 00h through 07h) are copied into an output register. The RTC continues counting in the background.

When reading or writing the time it is very important to make a read or write access in one go, that is, setting or reading 100th seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time increments between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the minutes from one moment and the hours from the next.

Before setting the time, the STOP bit should be set and the prescalers should be cleared (see Section 8.16 “Stop_enable register” on page 59).

An example of setting the time: 14 hours, 23 minutes and 19 seconds.

- I²C START condition
- I²C slave address + write (A2h)
- register address (2Eh)
- write data (set STOP, 01h)

- write data (clear prescaler, A4h)
- write data (100th seconds, 00h)
- write data (Hours, 14h)
- write data (Minutes, 23h)
- write data (Seconds, 19h)
- I²C START condition
- I²C slave address + write (A2h)
- register address (2Eh)
- write data (clear STOP, 00h). Time starts counting from this point
- I²C STOP condition

8.3 Stop-watch mode time registers

These registers are coded in the BCD format to simplify application use.

Stop-watch mode is enabled by setting RTCM = 1. In stop-watch mode, the PCF85363A counts from 100th seconds to 999999 hours. There are no days, weekdays, months or year registers.

Default state is:

Time — 000000:00:00.00

Monitor bits — OS = 1, EMON = 0 (see Section 8.2.2 on page 14 and Section 8.2.3 on page 14)

Table 12. Time registers in stop-watch mode (RTCM = 1)

Bit positions labeled as - are not implemented and return 0 when read.

Address	Register name	Upper-digit (ten's place)				Digit (unit place)			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	100th_seconds[1]	0 to 9				0 to 9			
01h	Seconds	OS	0 to 5			0 to 9			
02h	Minutes	EMON	0 to 5			0 to 9			
03h	Hours_xx_xx_00	0 to 9				0 to 9			
04h	Hours_xx_00_xx	0 to 9				0 to 9			
05h	Hours_00_xx_xx	0 to 9				0 to 9			
06h	not used	-	-	-	-	-	-	-	-
07h	not used	-	-	-	-	-	-	-	-

[1] The 100th_seconds register is only available when the 100TH mode is enabled, see Section 8.13.1 on page 53. When the 100TH mode is disabled, this register always returns 0.

8.3.1 Setting and reading the time in stop-watch mode

Figure 10 shows the data flow and data dependencies starting from the 100 Hz clock tick.

During read operations, the time counting circuits (memory locations 00h through 07h) are copied into an output register. The RTC continues counting in the background.

When reading or writing the time it is very important to make a read or write access in one go, that is, setting or reading 100th_seconds through to HR_00_xx_xx should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the seconds value is set in one access and then in a following access the minutes value is set, it is possible that the time increments between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the seconds from one moment and the minutes from the next.

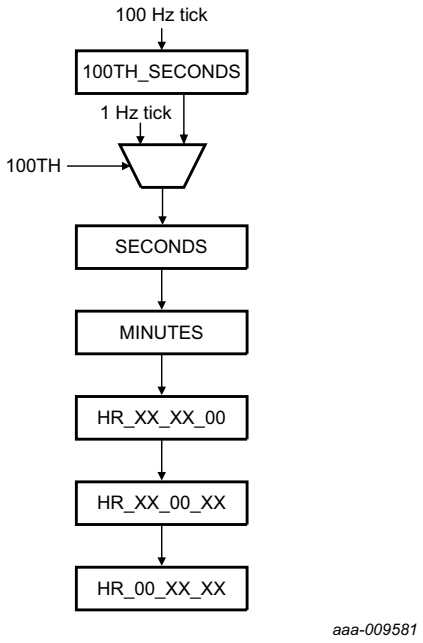


Fig 10. Data flow for the stop-watch function

8.4 Alarms

There are two independent alarms. Each is separately configured and may be used to generate an interrupt. In RTC mode, an alarm is configured for time and date. In stop-watch mode when the RTC is functioning as an elapsed time counter, an alarm is configured for time only.

8.4.1 Alarms in RTC mode

In RTC mode, Alarm 1 can be configured from seconds to months. Alarm 2 operates on minutes, hours and weekday. Each segment of the time is independently enabled. Alarms can be output on the $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ pins.

8.4.1.1 Alarm1 and alarm2 registers in RTC mode

Setting the time for alarm1: Only the information which is relevant for the alarm condition must to be programmed. The unused parts are ignored.

Table 13. Alarm1 and alarm2 registers in RTC mode coded in BCD (RTCM = 0)

Bit positions labeled as - are not implemented.

Address	Register name	Upper-digit (ten's place)				Digit (unit place)			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTC alarm1 registers									
08h	Second_alarm1	-	0 to 5			0 to 9			
09h	Minute_alarm1	-	0 to 5			0 to 9			
0Ah	Hour_alarm1	-	-	AMPM	0 to 1	0 to 9			
				0 to 2		0 to 9			
0Bh	Day_alarm1	-	-	0 to 3		0 to 9			
0Ch	Month_alarm1	-	-	-	0 to 1	0 to 9			
RTC alarm2 registers									
0Dh	Minute_alarm2	-	0 to 5			0 to 9			
0Eh	Hour_alarm2	-	-	AMPM	0 to 1	0 to 9			
				0 to 2		0 to 9			
0Fh	Weekday_alarm2	-	-	-	-	-	0 to 6		

8.4.1.2 Alarm1 and alarm2 control in RTC mode

Table 14. Alarm_enables- alarm enable control register (address 10h) bit description

Bit	Symbol	Value	Description
RTC alarm2			
7	WDAY_A2E		**weekday alarm2 enable**
		0[1]	disabled
		1	enabled
6	HR_A2E		**hour alarm2 enable**
		0[1]	disabled
		1	enabled
5	MIN_A2E		**minute alarm2 enable**
		0[1]	disabled
		1	enabled
RTC alarm1			
4	MON_A1E		**month alarm1 enable**
		0[1]	disabled
		1	enabled
3	DAY_A1E		**day alarm1 enable**
		0[1]	disabled
		1	enabled
2	HR_A1E		**hour alarm1 enable**
		0[1]	disabled
		1	enabled
1	MIN_A1E		**minute alarm1 enable**
		0[1]	disabled
		1	enabled

Table 14. Alarm_enables- alarm enable control register (address 10h) bit description

Bit	Symbol	Value	Description
0	SEC_A1E		**second alarm1 enable**
		0[1]	disabled
		1	enabled

[1] Default value.

8.4.1.3 Alarm1 and alarm2 function in RTC mode

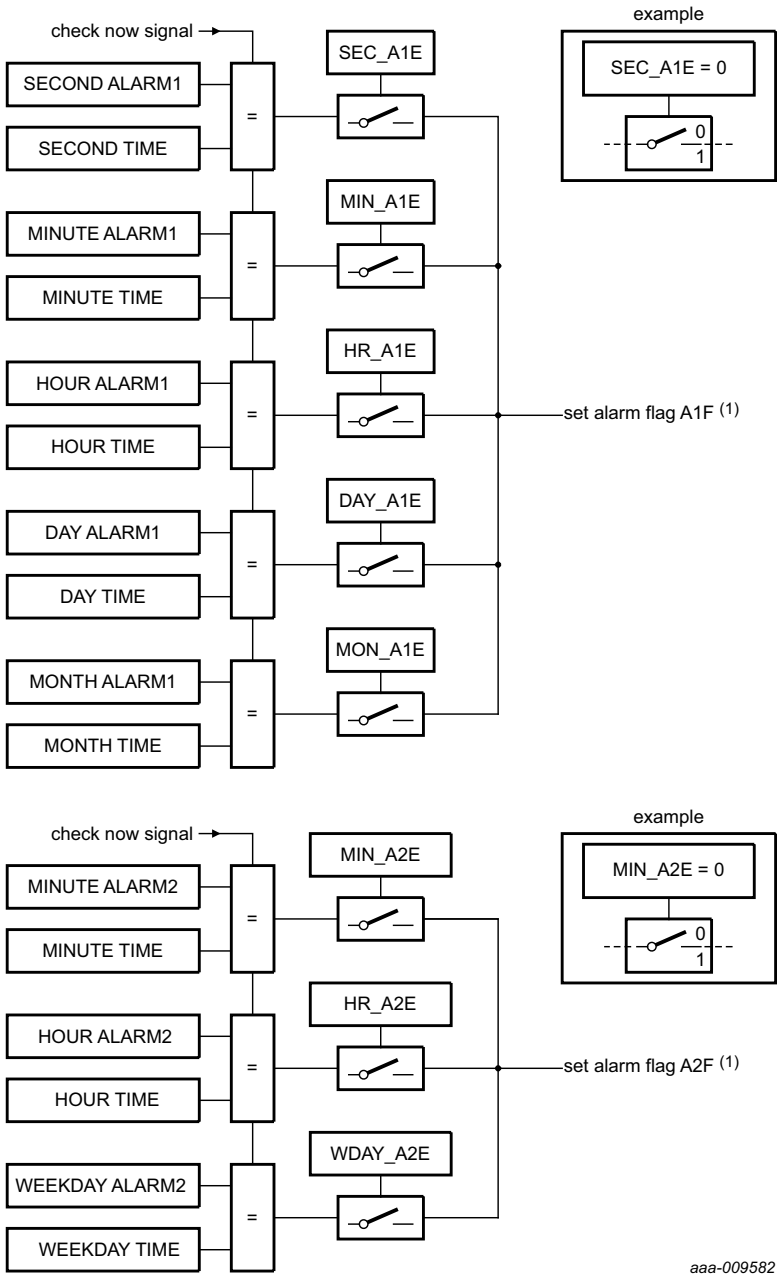
The registers at addresses 08h through 0Ch contain alarm1 information. When one or more of these registers is loaded with second, minute, hour, day, or month, and its corresponding alarm enable bit (SEC_A1E to MON_A1E) is set logic 1, then that information is compared with the current second, minute, hour, day, and month.

The registers at addresses 0Dh through 0Fh contain alarm2 information. When one or more of these registers is loaded with minute, hour or weekday, and its corresponding alarm enable bit (MIN_A2E to WDAY_A2E) is set logic 1, then that information is compared with the current minute, hour and weekday.

Alarm registers which have their alarm enable bit at logic 0 are ignored.

When the time increments to match the enabled alarms, the alarm flag in the Flags register (Section 8.14 on page 56) is set. A1F for alarm1 and A2F for alarm2. The alarm flag is cleared by command.

When the time increments to match the enabled alarms, an interrupt can be generated. See Section 8.4.3 “Alarm interrupts”.



(1) Only when all enabled alarm settings are matching.
The flag is set **only** on increment to a matched case (and not all the time it is equal).

Fig 11. Alarm1 and alarm2 function block diagram (RTC mode)

8.4.2 Alarms in stop-watch mode

In stop-watch mode, Alarm 1 can be configured from seconds to 999999 hours. Alarm 2 operates on minutes up to 9999 hours.

8.4.2.1 Alarm1 and alarm2 registers in stop-watch mode

Setting the time for alarm1 and alarm2: Only the information which is relevant for the alarm condition must to be programmed. The unused parts are ignored.

Table 15. Alarm1 and alarm2 registers in stop-watch mode coded in BCD (RTCM = 1)
Bit positions labeled as - are not implemented.

Address	Register name	Upper-digit (ten's place)				Digit (unit place)			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Stop-watch alarm1 registers									
08h	Second_alm1	-	0 to 5			0 to 9			
09h	Minute_alm1	-	0 to 5			0 to 9			
09h	Hr_xx_xx_00_alm1	0 to 9				0 to 9			
0Bh	Hr_xx_00_xx_alm1	0 to 9				0 to 9			
0Ch	Hr_00_xx_xx_alm1	0 to 9				0 to 9			
Stop-watch alarm2 registers									
0Dh	Minute_alm2	-	0 to 5			0 to 9			
0Eh	Hr_xx_00_alm2	0 to 9				0 to 9			
0Fh	Hr_00_xx_alm2	0 to 9				0 to 9			

8.4.2.2 Alarm1 and alarm2 control in stop-watch mode

Table 16. Alarm_enables- alarm enable control register (address 10h) bit description

Bit	Symbol	Value	Description
Stop-watch alarm2			
7	HR_00_XX_A2E		**thousands of hours alarm2 enable**
		0[1]	disabled
		1	enabled
6	HR_XX_00_A2E		**tens of hours alarm2 enable**
		0[1]	disabled
		1	enabled
5	MIN_A2E		**minute alarm2 enable**
		0[1]	disabled
		1	enabled
Stop-watch alarm1			
4	HR_00_XX_XX_A1E		**100 thousands of hours alarm1 enable**
		0[1]	disabled
		1	enabled
3	HR_XX_00_XX_A1E		**thousands of hours alarm1 enable**
		0[1]	disabled
		1	enabled
2	HR_XX_XX_00_A1E		**tens of hour alarm1 enable**
		0[1]	disabled
		1	enabled

Table 16. Alarm_enables- alarm enable control register (address 10h) bit description

Bit	Symbol	Value	Description
1	MIN_A1E		**minute alarm1 enable**
		0[1]	disabled
		1	enabled
0	SEC_A1E		**second alarm1 enable**
		0[1]	disabled
		1	enabled

[1] Default value.

8.4.2.3 Alarm1 and alarm2 function in stop-watch mode

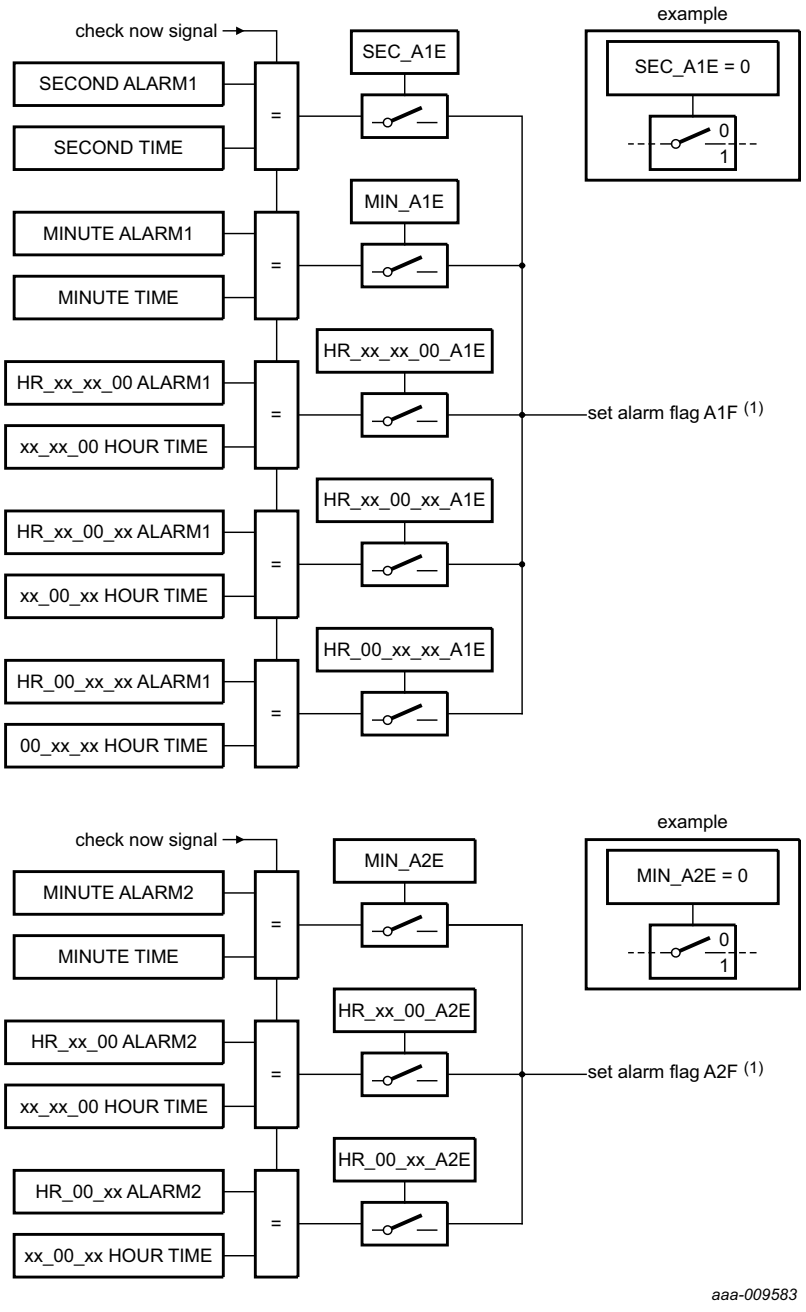
The registers at addresses 08h through 0Ch contain alarm1 information. When one or more of these registers is loaded with second, minute, and hours, and its corresponding alarm enable bit (SEC_A1E to HR_00_XX_XX_A1E) is set logic 1, then that information is compared with the current second, minute, and hours.

The registers at addresses 0Dh through 0Fh contain alarm2 information. When one or more of these registers is loaded with minute and hours, and its corresponding alarm enable bit (MIN_A2E to HR_00_XX_A2E) is set logic 1, then that information is compared with the current minute and hours.

Alarm registers which have their alarm enable bit at logic 0 are ignored.

When the time increments to match the enabled alarms, the alarm flag in the Flags register (Section 8.14 on page 56) is set. A1F for alarm1 and A2F for alarm2. The alarm flag is cleared by command.

When the time increments to match the enabled alarms, an interrupt can be generated. See Section 8.4.3 “Alarm interrupts”.



(1) Only when all enabled alarm settings are matching.
The flag is set **only** on increment to a matched case (and not all the time it is equal).

Fig 12. Alarm1 and alarm2 function block diagram (stop-watch mode)

8.4.3 Alarm interrupts

The generation of interrupts from the alarm functions is controlled via the alarm interrupt enable bits; A1IEA, A1IEB, A2IEA, A2IEB. These bits are in registers INTA_enable (address 29h) and INTB_enable (address 2Ah).

The assertion of flags A1F or A2F can be used to generate an interrupt at the pins $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$. The interrupt may be generated as a pulse signal every time the time increments to match the alarm setting or as a permanently active signal which follows the condition of bit A1F and/or A2F. See Section 8.9 on page 37 for interrupt control.

A1F and A2F remain set until cleared by command. Once an alarm flag has been cleared, it will only be set again when the time increments to match the alarm condition once more.

When an interrupt pin is configured to pulse mode and if an alarm flag is not cleared and the time increments to match the alarm condition again, then a repeated interrupt pulse will be generated.

8.5 WatchDog

Table 17. WatchDog - WatchDog control and register (address 2Dh) bit description

Bit	Symbol	Value	Description
7	WDM		**WatchDog mode**
		0[1]	single shot
		1	repeat mode
6 to 2	WDR[4:0]		**WatchDog register bits**
		0h[1] to 1Fh	Write: WatchDog counter load value
		0h to 1Fh	Read: current counter value
1 to 0	WDS[1:0]		**WatchDog step size (source clock)**
		00[1]	4 seconds (0.25 Hz)
		01	1 second (1 Hz)
		10	$\frac{1}{4}$ second (4 Hz)
		11	$\frac{1}{16}$ second (16 Hz)

[1] Default value.

8.5.1 WatchDog functions

The WatchDog has four selectable step sizes allowing for periods in the range from 62.5 ms to 124 seconds. For periods greater than 2 minutes, the alarm function can be used.

$$WatchDog\text{-}duration = WDR \times stepsize \quad (1)$$

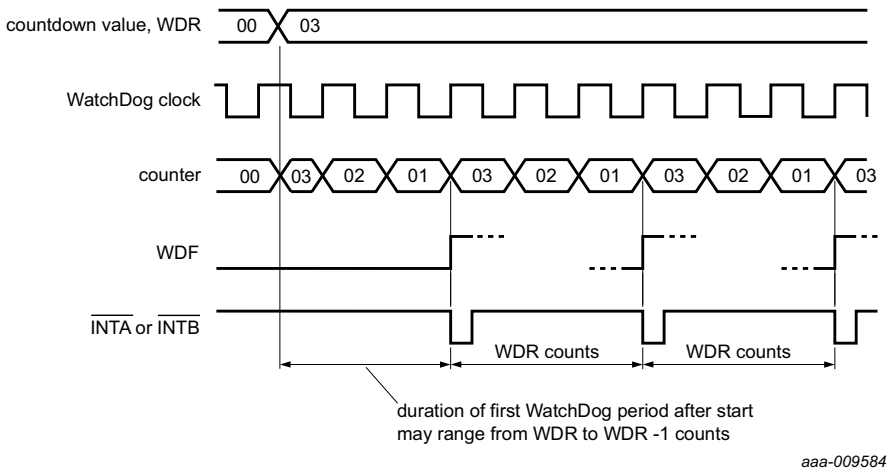
Table 18. WatchDog durations

WDS[1:0]	WatchDog step size[1]	Delay	
		Minimum WatchDog duration WDR = 1	Maximum WatchDog duration WDR = 31
00	4 s	4 s	124 s
01	1 s	1 s	31 s
10	$\frac{1}{4}$ s	0.25 s	7.75 s
11	$\frac{1}{16}$ s	0.0625 s	1.9375 s

[1] Time periods can be affected by correction pulses.

Remark: Note that all timings are generated from the 32.768 kHz oscillator and are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency results in deviation in timings. This is not applicable to interface timing.

The WatchDog counts down from a software-loaded 5-bit binary value, WDR[4:0], in register WatchDog. Loading the counter with 0 stops the WatchDog. Loading the counter with a non-0 value starts the counter. Values from 1 to 31 are allowed.



In this example, it is assumed that the WatchDog flag (WDF) is cleared before the next WatchDog period expires and that the interrupt output is set to pulsed mode.

Fig 13. WatchDog repeat mode

If a new value of WDR[4:0] is written before the end of the current WatchDog period, then this value takes immediate effect.

When starting the timer for the first time or when reloading WDR[4:0] before the end of the current period, the first period has an uncertainty of maximum one count. The uncertainty is a result of loading the WDR[4:0] from the interface clock which is asynchronous from the WatchDog source clock. Subsequent WatchDog periods do not have such variation.

Reading the WatchDog register returns the current value of the WatchDog counter (see Figure 13) and **not** the initial value WDR[4:0]. Since it is not possible to freeze the WatchDog counter during read back, it is recommended to read the register twice and check for consistent results.

8.5.1.1 WatchDog repeat mode

In repeat mode, at the end of every WatchDog period, the WatchDog flag (bit WDF in the Flags register, Section 8.14 on page 56) is set and the counter automatically reloads and starts the next WatchDog period. An example is given in Figure 13. The asserted bit WDF can be used to generate an interrupt. Bit WDF can only be cleared by command.

8.5.1.2 WatchDog single shot mode

In single shot mode, at the end of the countdown period, the WatchDog flag (bit WDF in the Flags register, Section 8.14 on page 56) is set and the counter stops with the value 0. The WatchDog register must be reloaded to start another WatchDog period.

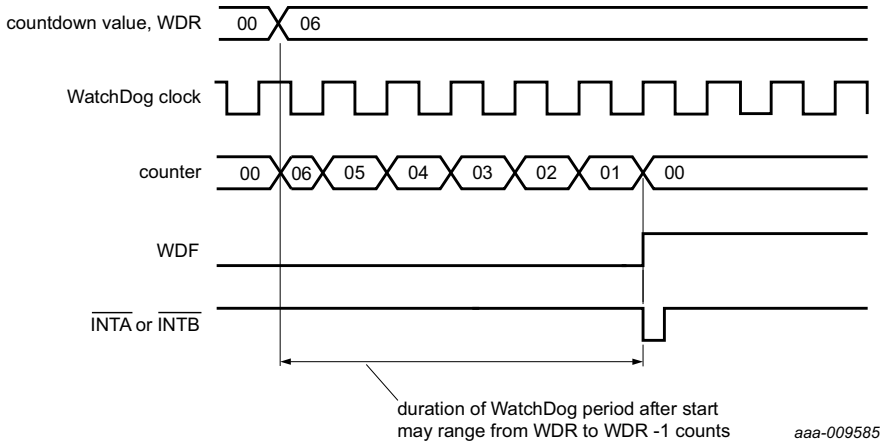


Fig 14. WatchDog single shot mode

8.5.1.3 WatchDog interrupts

The generation of interrupts from the WatchDog functions is controlled via the WatchDog interrupt enable bits; WDIEA and WDIEB. These bits are in registers INTA_enable (address 29h) and INTB_enable (address 2Ah).

The assertion of the flag WDF can be used to generate an interrupt at pins $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$. The interrupt may be generated as a pulsed signal every time the WatchDog counter reaches the end of the countdown period. Alternatively as a permanently active signal which follows the condition of bit WDF. WDF remains set until cleared by command.

When enabled, interrupts are triggered every time the WatchDog counter reaches the end of the countdown period and even if the WDF is not cleared, an interrupt pulse can be generated.

See Section 8.9 on page 37 for interrupt control.

8.6 Single RAM byte

Table 19. RAM_byte - 8-bit RAM register (address 2Ch) bit description

Bit	Symbol	Value	Description
7 to 0	B[7:0]	00000000[1] to 11111111	**single RAM byte content**

[1] Default value.

The PCF85363A provides a free single RAM byte, which can be used for any purpose, for example, status bits of the system.

8.7 Timestamps

There are three timestamp registers which can be independently configured to record the time for battery switch-over events and/or transitions on the TS pin.

Each timestamp register has an associated flag. It is also possible to generate an interrupt signal for every timestamp register update.

Timestamps work in both RTC and stop-watch mode. During battery operation, the mechanical switch detector may also be used to trigger the timestamp.

The timestamp registers are read only and cannot be written. It is possible to set all three registers to 0 with the CTS instruction in the Resets register (Section 8.15 on page 57).

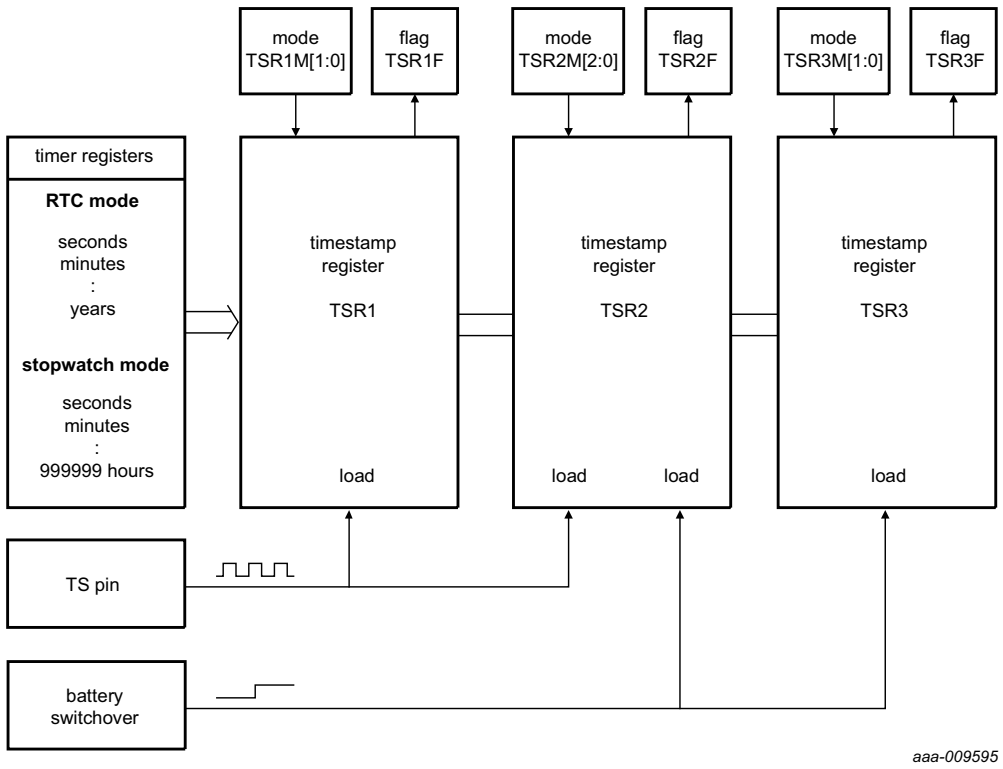


Fig 15. Timestamp

The mode for each register is controlled by the TSR_mode register.

Table 20. TSR_mode - timestamp mode control register (address 23h) bit description

Bit	Symbol	Value	Description
Timestamp3 (TSR3)			
7 to 6	TSR3M[1:0]		**timestamp register 3 mode**
		00[1]	no timestamp
		01	FB, record **F**irst time switch to **B**attery event
		10	LB, record **L**ast time switch to **B**attery event
		11	LV, record **L**ast time switch to V_{DD} event
5	-	0	not used
Timestamp2 (TSR2)			
4 to 2	TSR2M[2:0]		**timestamp register 2 mode**
		000[1]	no timestamp
		001	FB, record **F**irst time switch to **B**attery event
		010	LB, record **L**ast time switch to **B**attery event
		011	LV, record **L**ast time switch to V_{DD} event
		100	FE, record **F**irst TS pin **E**vent
		101	LE, record **L**ast TS pin **E**vent
		110 to 111	no timestamp
Timestamp1 (TSR1)			
1 to 0	TSR1M[1:0]		**timestamp register 1 mode**
		00[1]	no timestamp
		01	FE, record **F**irst TS pin **E**vent
		10	LE, record **L**ast TS pin **E**vent
		11	no timestamp

[1] Default value.

First event means that the time is only stored on the first event and not recorded for subsequent events. When the first event occurs, the associated timestamp flag is set. When the flag is cleared, then a new ‘first’ event is recorded. See Figure 16 and Figure 17.

Last event means that the time is stored on every event. When an event occurs, the associated timestamp flag is set. It is not necessary to clear the flag before a new event is recorded.

Interrupts can be generated in $\overline{\text{INTA}}$ pin and/or $\overline{\text{INTB}}$ pin. Interrupts are generated every time a timestamp register is updated. Interrupt generation is not conditional on the state of the timestamp flags. See Section 8.7.1.

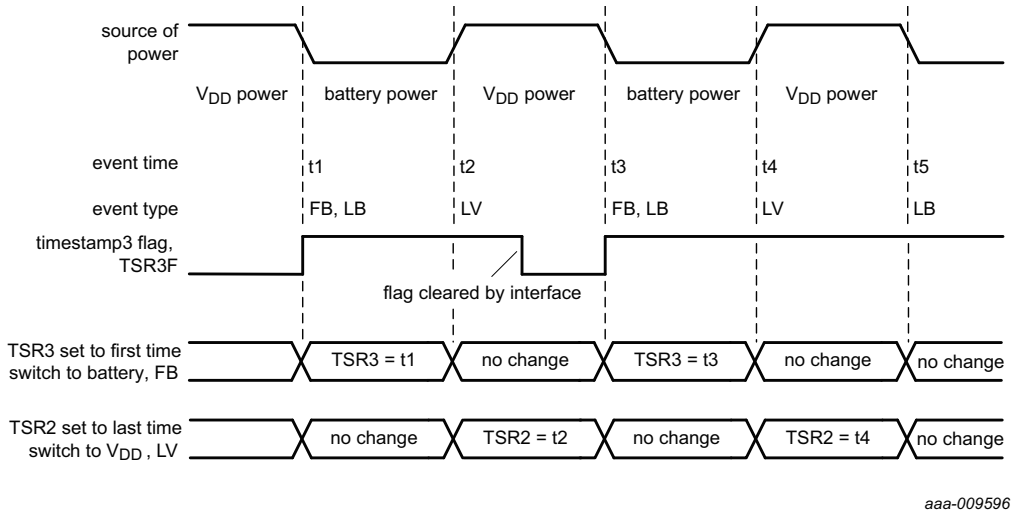
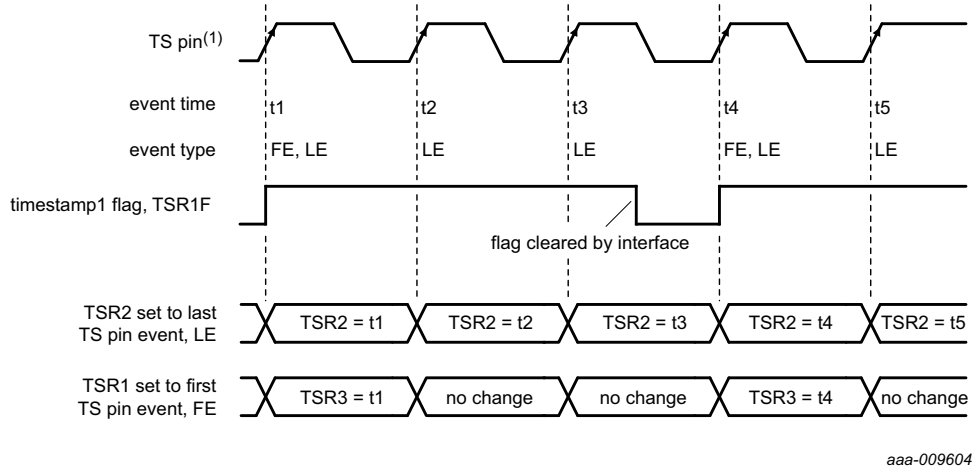


Fig 16. Example battery switch-over timestamp



(1) TS pin set to active HIGH (TSL = 0), see register Pin_IO (address 27h), Section 8.12.

Fig 17. Example TS pin driven timestamp

The recorded time is stored in the associated timestamp register. The time format depends on the RTC mode. The timestamp registers follows the time format of the time registers.

Table 21. Timestamp registers in RTC mode (RTCM = 0)

Bit positions labeled as - are not implemented and return 0 when read.

Address	Register name	Upper-digit (ten's place)				Digit (unit place)			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTC timestamp1 (TSR1)									
11h	TSR1_seconds	-	0 to 5			0 to 9			
12h	TSR1_minutes	-	0 to 5			0 to 9			
13h	TSR1_hours	-	-	AMPM	0 to 1	0 to 9			
				0 to 2		0 to 9			
14h	TSR1_days	-	-	0 to 3		0 to 9			
15h	TSR1_months	-	-	-	0 to 1	0 to 9			
16h	TSR1_years	0 to 9				0 to 9			
RTC timestamp2 (TSR2)									
17h	TSR2_seconds	-	0 to 5			0 to 9			
18h	TSR2_minutes	-	0 to 5			0 to 9			
19h	TSR2_hours	-	-	AMPM	0 to 1	0 to 9			
				0 to 2		0 to 9			
1Ah	TSR2_days	-	-	0 to 3		0 to 9			
1Bh	TSR2_months	-	-	-	0 to 1	0 to 9			
1Ch	TSR2_years	0 to 9				0 to 9			
RTC timestamp3 (TSR3)									
1Dh	TSR3_seconds	-	0 to 5			0 to 9			
1Eh	TSR3_minutes	-	0 to 5			0 to 9			
1Fh	TSR3_hours	-	-	AMPM	0 to 1	0 to 9			
				0 to 2		0 to 9			
20h	TSR3_days	-	-	0 to 3		0 to 9			
21h	TSR3_months	-	-	-	0 to 1	0 to 9			
22h	TSR3_years	0 to 9				0 to 9			

Table 22. timestamp registers in stop-watch mode (RTCM = 1)

Bit positions labeled as - are not implemented and return 0 when read.

Address	Register name	Upper-digit (ten's place)				Digit (unit place)			
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Stop-watch timestamp1 (TSR1)									
11h	TSR1_seconds	-	0 to 5			0 to 9			
12h	TSR1_minutes	-	0 to 5			0 to 9			
13h	TSR1_hr_xx_xx_00	0 to 9				0 to 9			
14h	TSR1_hr_xx_00_xx	0 to 9				0 to 9			
15h	TSR1_hr_00_xx_xx	0 to 9				0 to 9			
16h	not used	-	-	-	-	-	-	-	-
Stop-watch timestamp2 (TSR2)									
17h	TSR2_seconds	-	0 to 5			0 to 9			
18h	TSR2_minutes	-	0 to 5			0 to 9			
19h	TSR2_hr_xx_xx_00	0 to 9				0 to 9			
1Ah	TSR2_hr_xx_00_xx	0 to 9				0 to 9			
1Bh	TSR2_hr_00_xx_xx	0 to 9				0 to 9			
1Ch	not used	-	-	-	-	-	-	-	-
Stop-watch timestamp3 (TSR3)									
1Dh	TSR3_seconds	-	0 to 5			0 to 9			
1Eh	TSR3_minutes	-	0 to 5			0 to 9			
1Fh	TSR3_hr_xx_xx_00	0 to 9				0 to 9			
20h	TSR3_hr_xx_00_xx	0 to 9				0 to 9			
21h	TSR3_hr_00_xx_xx	0 to 9				0 to 9			
22h	not used	-	-	-	-	-	-	-	-

8.7.1 Timestamps interrupts

The generation of interrupts from the timestamp functions is controlled via the timestamp interrupt enable bits; TSRIEA and TSRIEB. These bits are in registers INTA_enable (address 29h) and INTB_enable (address 2Ah).

The loading of new information into one of the timestamp registers can be used to generate an interrupt at pins $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$. The interrupt may be generated as a pulsed signal every time a timestamp register updates or as a permanently active signal which follows the condition of timestamp flags, TSR1F to TSR3F. The timestamp flags remain set until cleared by command.

When enabled, interrupts are triggered every time a timestamp register updates and even if the associated flag is not cleared, an interrupt pulse can be generated.

See Section 8.9 on page 37 for interrupt control.

8.8 Offset register

The PCF85363A incorporates an offset register (address 24h) which can be used to implement several functions, such as:

- Accuracy tuning
- Aging adjustment
- Temperature compensation

Table 23. Offset - offset register (address 24h) bit description

Bit	Symbol	Value	Description
7 to 0	OFFSET[7:0]	see Table 25	**offset value**

There are two modes which define the correction period, normal mode and fast mode. The **normal mode** is suitable for offset trimming. The **fast mode** is suitable for dynamic offset correction e.g. implementing a temperature correction. The fast mode consumes more current. Offset mode is defined by bit OFFM in the Oscillator register (Section 8.10).

Table 24. OFFM bit - oscillator control register (address 25h)
See Section 8.10 on page 41.

Bit	Symbol	Value	Description
6	OFFM		**offset mode bit**
		0[1]	normal mode: correction is made every 4 hours; 2.170 ppm/step
		1	fast mode: correction is made once every 8 minutes;2.0345 ppm/step

[1] Default value.

For OFFM = 0, each LSB introduces an offset of 2.170 ppm. For OFFM = 1, each LSB introduces an offset of 2.0345 ppm. The offset value is coded in two's complement giving a range of +127 LSB to −128 LSB, see Table 25.

Table 25. Offset values

OFFSET[7:0]	Offset value in decimal	Offset value in ppm	
		Normal mode OFFM = 0	Fast mode OFFM = 1
01111111	+127	+275.590	+258.3815
01111110	+126	+273.420	+256.3470
:	:	:	:
00000010	+2	+4.340	+4.0690
00000001	+1	+2.170	+2.0345
00000000[1]	0	0[1]	0[1]
11111111	−1	−2.170	−2.0345
11111110	−2	−4.340	−4.0690
:	:	:	:
10000001	−127	−275.590	−258.3815
10000000	−128	−277.760	−260.416

[1] Default value.

The correction is made by adding or subtracting clock correction pulses, thereby changing the period of a single second but not by changing the oscillator frequency.

It is possible to monitor when correction pulses are applied. See Section 8.8.4.

8.8.1 Correction when OFFM = 0

The correction is triggered once every four hours and then correction pulses are applied once per minute until the programmed correction values have been implemented.

Table 26. Correction pulses for OFFM = 0

Correction value	Every n^{th} hour	Actual minute
+1 or −1	4	00
+2 or −2	4	00 and 01
+3 or −3	4	00, 01, and 02
:	:	:
+59 or −59	4	00 to 58
+60 or −60	4	00 to 59
+61 or −61	4	00 to 59
	4 + 1	00
+62 or −62	4	00 to 59
	4 + 1	00 and 01
:	:	:
+123 or −123	4	00 to 59
	4 + 1	00 to 59
	4 + 2	00, 01, and 02
−128	4	00 to 59
	4 + 1	00 to 59
	4 + 2	00 to 07

8.8.2 Correction when OFFM = 1

The correction is triggered once every eight minutes and then correction pulses are applied once per second until the programmed correction values have been implemented.

Clock correction is made more frequently in OFFM = 1; however, this can result in higher power consumption.

Table 27. Correction pulses for OFFM = 1

Correction value	Every n^{th} minute	Actual second
+1 or −1	8	00
+2 or −2	8	00 and 01
+3 or −3	8	00, 01, and 02
:	:	:
+59 or −59	8	00 to 58
+60 or −60	8	00 to 59
+61 or −61	8	00 to 59
	8 + 1	00
+62 or −62	8	00 to 59
	8 + 1	00 and 01
:	:	:
+123 or −123	8	00 to 59
	8 + 1	00 to 59
	8 + 2	00, 01, and 02
−128	8	00 to 59
	8 + 1	00 to 59
	8 + 2	00 to 07

8.8.3 Offset calibration workflow

The calibration offset has to be calculated based on the time. Figure 18 shows the workflow how the offset register values can be calculated:

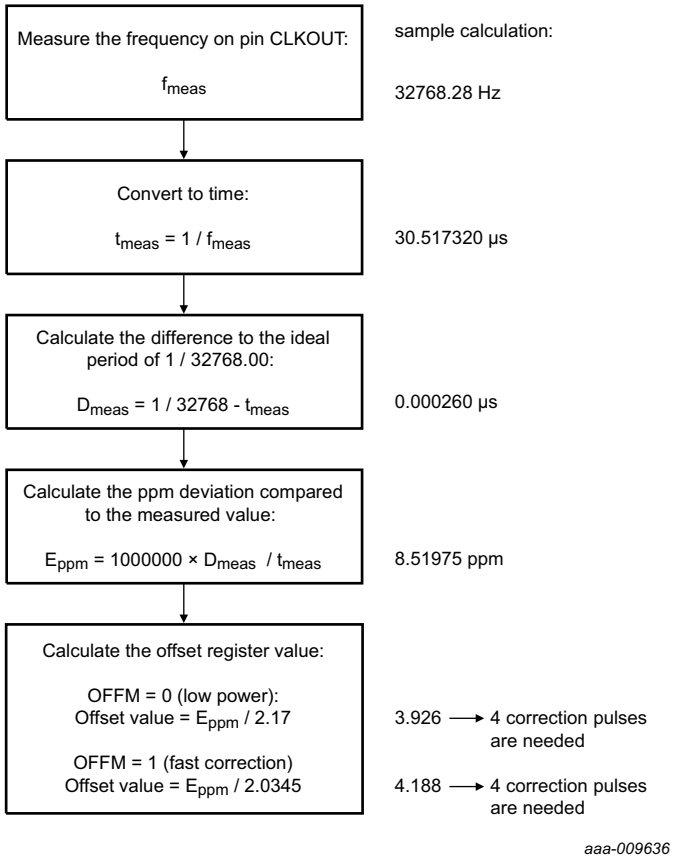
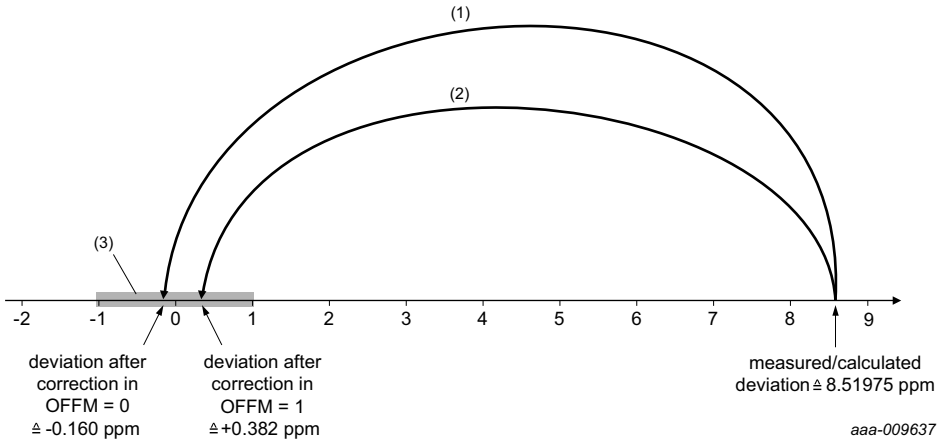


Fig 18. Offset calibration calculation workflow



With the offset calibration an accuracy of ±1 ppm (0.5 × offset per LSB) can be reached (see Table 25).

±1 ppm corresponds to a time deviation of 0.0864 seconds per day.

(1) 4 correction pulses in OFFM = 0 correspond to −8.680 ppm.

(2) 4 correction pulses in OFFM = 1 correspond to −8.138 ppm.

(3) Reachable accuracy zone.

Fig 19. Result of offset calibration

8.8.4 Offset interrupts

The generation of interrupts from the offset functions is controlled via the offset interrupt enable bits; OIEA and OIEB. These bits are in registers INTA_enable (address 29h) and INTB_enable (address 2Ah).

Every time a correction pulse is made an interrupt pulse can be generated at pins $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$. As there are is no offset calibration flag, it is only possible to generate pulse interrupts.

See Section 8.9 on page 37 for interrupt control.

8.9 Interrupts

There are two interrupt output pins, $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$. Both pins have the same possible sources and a dedicated register to control what is output. The pins can be used independently from each other.

$\overline{\text{INTA}}$ data is output on the $\overline{\text{INTA}}$ pin. $\overline{\text{INTA}}$ is an interrupt output pin with open-drain drive. $\overline{\text{INTA}}$ pin mode is controlled by INTAPM[1:0] bits in the Pin_IO register (Section 8.12 on page 49).

$\overline{\text{INTB}}$ data is output on TS pin with push-pull drive. The TS pin must first be configured as $\overline{\text{INTB}}$ output by setting TSIO[1:0] bits in the Pin_IO register (Section 8.12 on page 49).

Interrupts will only be output when the pin mode is correctly defined. Interrupts are output from the IC as active LOW signals.

The registers INTA_enable (address 29h) and INTB_enable (address 2Ah) are used to select which interrupts should be output on which pin.

Table 28. $\overline{\text{INTA}}$ and $\overline{\text{INTB}}$ interrupt control bits

Bit	7	6	5	4	3	2	1	0
INTA_enable - $\overline{\text{INTA}}$ pin enable control (address 29h)								
Symbol	ILPA	PIEA	OIEA	A1IEA	A2IEA	TSRIEA	BSIEA	WDIEA
INTB_enable - $\overline{\text{INTB}}$ pin enable control (address 2Ah)								
Symbol	ILPB	PIEB	OIEB	A1IEB	A2IEB	TSRIEB	BSIEB	WDIEB

Table 29. Definition of interrupt control bits

Bit	Symbol		Value	Description
	$\overline{\text{INTA}}$	**$\overline{\text{INTB}}$**		
7	ILPA	ILPB		**level or pulse mode**
			0[1]	interrupt generates a pulse
			1	interrupt follows flags (permanent signal)
6	PIEA	PIEB		**periodic interrupt enable**
			0[1]	no periodic interrupt generated
			1	periodic interrupt generated
5	OIEA	OIEB		**offset correction interrupt enable**
			0[1]	no correction interrupt generated
			1	interrupt generated from correction
4	A1IEA	A1IEB		**alarm1 interrupt enable**
			0[1]	no alarm interrupt generated
			1	alarm interrupt generated
3	A2IEA	A2IEB		**alarm2 interrupt enable**
			0[1]	no alarm interrupt generated
			1	alarm interrupt generated
2	TSRIEA	TSRIEB		**timestamp register interrupt enable**
			0[1]	no timestamp register interrupt generated
			1	timestamp register interrupt generated
1	BSIEA	BSIEB		**battery switch interrupt enable**
			0[1]	no battery switch interrupt generated
			1	battery switch interrupt generated
0	WDIEA	WDIEB		**WatchDog interrupt enable**
			0[1]	no WatchDog interrupt generated
			1	WatchDog interrupt generated

[1] Default value.

8.9.1 ILPA/ILPB: interrupt level or pulse mode

Interrupts can be configured to generate a pulse or to send a continuous level (permanent signal) which follows the state of the flag.

In pulse mode, an interrupt pulse is generated every time that the selected source triggers.

Triggered means

- for periodic interrupts, every time a period has elapsed
- for offset correction, every time a correction pulse is initiated
- for alarms, every time the time increments to match the alarm time
- for timestamps, every time a register updates
- for battery switch, every time the IC switches to or from battery
- for WatchDog, every time the counter reaches the end of its count

The interrupt signal goes active coincident with the triggering event. The signal is cleared by an internal 128 Hz clock. The internal clock is asynchronous to the triggering event and so the pulse duration has a minimum period of one 128 Hz cycle and a maximum of two 128 Hz cycles. Interrupt pulses may be shortened by clearing the flag before the end of the pulse period.

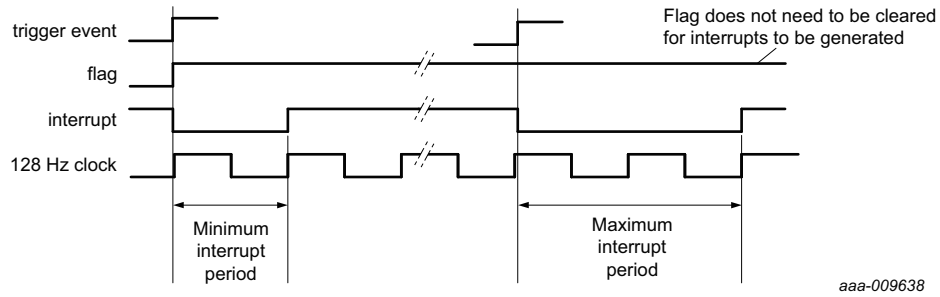


Fig 20. Interrupt pulse width

In level mode, the interrupt signal follows the state of the flag. Only interrupts which are enabled will affect the pin state. All enabled flags must be cleared for the interrupt signal to be cleared.

The EMON is used only for monitoring **all** flags and can be read back in the minutes register. See Section 8.2.3 on page 14.

8.9.2 Interrupt enable bits

The remainder of the bits in register INTA_enable (address 29h) and register INTB_enable (address 2Ah) are used to select which interrupt data goes where. See Figure 21 “Interrupt selection”

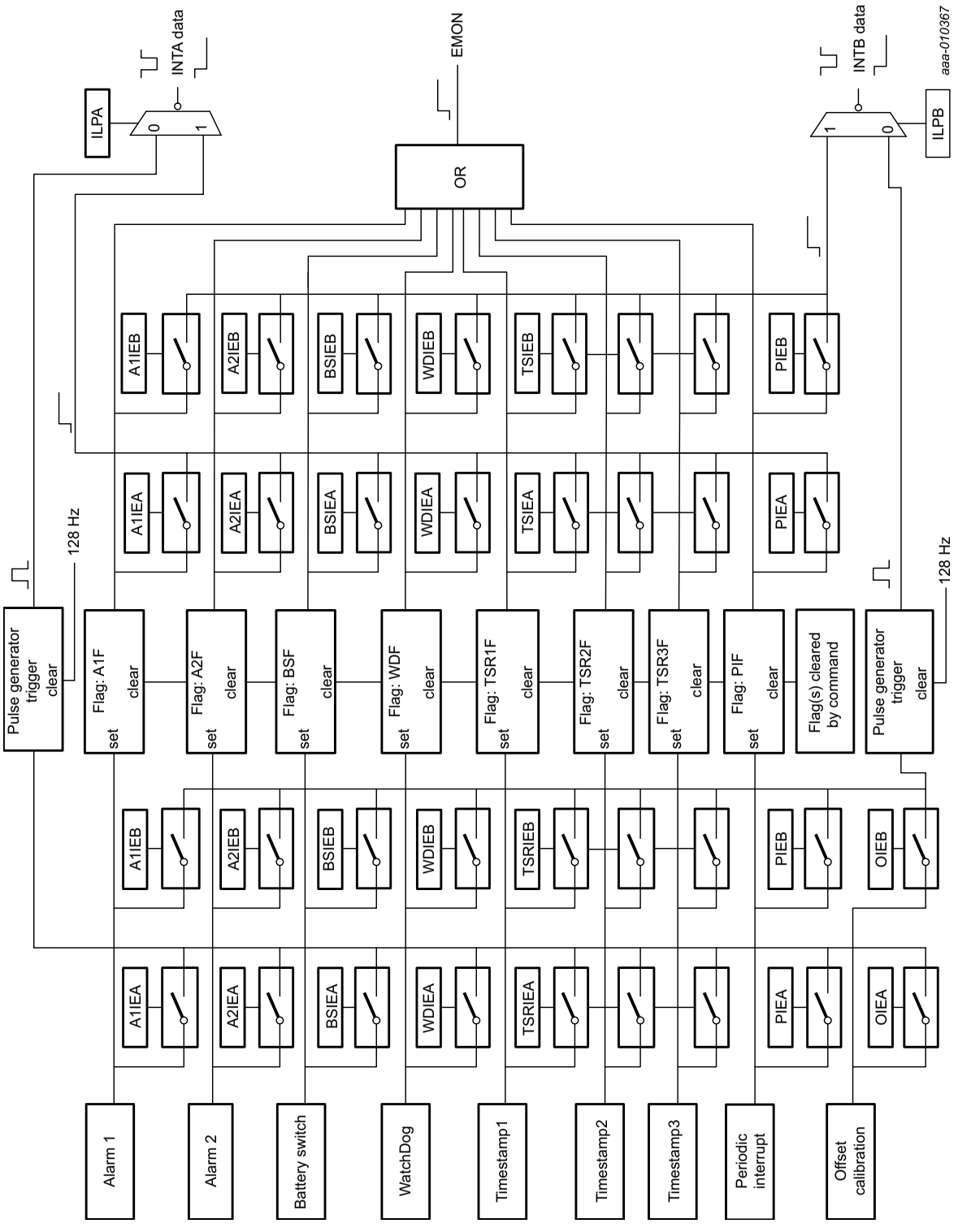


Fig 21. Interrupt selection

8.10 Oscillator register

Table 30. Oscillator - oscillator control register (address 25h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	CLKIV	OFFM	12_24	LOWJ	OSCD[1:0]		CL[1:0]	
Section	Section 8.16	Section 8.8	Section 8.10.3	Section 8.10.4	Section 8.10.5		Section 8.10.6	

8.10.1 CLKIV: invert the clock output

Table 31. CLKIV bit - oscillator control register (address 25h)

Bit	Symbol	Value	Description
7	CLKIV		**output clock inversion**
		0[1]	non-inverting; LOWJ mode will affect rising edge
		1	inverted; LOWJ mode will affect falling edge

[1] Default value.

The clock selected with the COF[2:0] bits (register Function, address 28h) can be inverted. This is intended for use in conjunction with the low jitter mode, LOWJ. The low jitter mode reduces the jitter for the rising edge of the output clock. If the reduced jitter needs to be on the falling edge, for example when using an open-drain clock output, then the CLKIV bit can be used to implement this.

8.10.2 OFFM: offset calibration mode

See Section 8.8 “Offset register” on page 33 for a full description of offset calibration.

8.10.3 12_24: 12 hour or 24 hour clock

Table 32. 12_24 bit - oscillator control register (address 25h)

Bit	Symbol	Value	Description
5	12_24		**12 hour or 24 hour mode**
		0[1]	24 hour mode is selected
		1	12 hour mode is selected

[1] Default value.

In RTC mode, time counting can be configured for 24 hour clock or 12 hour clock with the AMPM flag.

This bit is ignored in stop-watch mode.

8.10.4 LOWJ: low jitter mode

Table 33. LOWJ bit - oscillator control register (address 25h)

Bit	Symbol	Value	Description
4	LOWJ		**low jitter CLK output bit**
		0[1]	normal
		1	reduced CLK output jitter; increase I_{DD}

[1] Default value.

Oscillator circuits suffer from jitter. In particular, ultra low-power oscillators like the one used in the PCF85363A are optimized for power and not jitter. By setting the LOWJ bit, the jitter performance can be improved at the cost of power consumption.

8.10.5 OSCD[1:0]: quartz oscillator drive control

Table 34. OSCD[1:0] bits - oscillator control register (address 25h)

Bit	Symbol	Value	Description
3 to 2	OSCD[1:0]		**oscillator drive bit**s
		00[1]	normal drive; $R_{S(max)}$: 100 kΩ
		01	low drive; $R_{S(max)}$: 60 kΩ; reduced I_{DD}
		10, 11	high drive; $R_{S(max)}$: 500 kΩ; increased I_{DD}

[1] Default value.

The oscillator is designed to be used with quartz with a series resistance up to 100 kΩ. This covers the typical range of 32.768 kHz quartz crystals. Series resistance is also referred to as: ESR, motional resistance, or R_S.

A low drive mode is available for low series resistance quartz. This reduces the current consumption.

For very high series resistance quartz, there is a high drive mode. Current consumption increases substantially in this mode.

8.10.6 CL[1:0]: quartz oscillator load capacitance

Table 35. CL[1:0] bits - oscillator control register (address 25h)

Bit	Symbol	Value	Description
1 to 0	CL[1:0]		**internal oscillator capacitor selection** for quartz crystals with the corresponding load capacitance of C_L:
		00[1]	7.0 pF
		01	6.0 pF
		10	12.5 pF
		11	12.5 pF

[1] Default value.

C_L refers to the load capacitance of the oscillator circuit and allows for a certain amount of package and PCB parasitic capacitance. When the oscillator circuit matches the C_L parameter of the quartz, then the frequency offset is zero.

The PCF85363A is designed to operate with quartz with C_L values of 6.0 pF, 7.0 pF and 12.5 pF.

12.5 pF are generally the cheapest and most widely available, but also require the most power to drive. The circuit also operates with 9.0 pF quartz, however the offset calibration would be needed to compensate. If a 9.0 pF quartz is used, then it is recommended to set C_L to 7.0 pF.

8.11 Battery switch register

This register configures the battery switch-over mode.

Associated with the battery switch-over is the battery switch flag (BSF) in the Flags register (Section 8.14 on page 56). Whenever the IC switches to battery operation, the flag is set. The flag can only be read when operating from V_{DD} power, however an interrupt pulse or static LOW signal can be generated whenever switching to battery. An interrupt pulse can also be generated when switching back to V_{DD} power. Examples are given in Figure 23 and Figure 24.

When switched to battery, the V_{DD} power domain is disabled. This means that I²C pins are ignored, CLK output is disabled and Hi-Z, TS pin output mode is disabled and Hi-Z, TS digital input is ignored and may be left floating. TS pin mechanical switch detector is active. $\overline{INTA}$ output is still active for interrupt output and battery switch indication, but disabled for clock output.

Table 36. IO pin behavior in battery mode

IO pin (mode)	V_{DD} operation	V_{BAT} operation
SCL	active input	disabled; may be left floating
SDA	active input/output	disabled; may be left floating
CLK	active output	disabled; Hi-Z
TS (output mode)	active output	disabled; Hi-Z
TS (digital input)	active input	disabled; may be left floating
TS (mechanical switch input)	active input	active input
$\overline{INTA}$	active output	active interrupt output

Table 37. Battery_switch - battery switch control (address 26h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	BSOFF	BSRR	BSM[1:0]		BSTH
Section	-	-	-	Section 8.11.1	Section 8.11.2	Section 8.11.3		Section 8.11.4

8.11.1 BSOFF: battery switch on/off control

Table 38. BSOFF bit - battery switch control (address 26h) bit description

Bit	Symbol	Value	Description
4	BSOFF		**battery switch on/off**
		0[1]	enable battery switch feature
		1	disable battery switch feature

[1] Default value.

The battery switch circuit may be disabled when not used. This disables all the circuit and save power consumption. When disabled connect V_{BAT} and V_{DD} together.

8.11.2 BSRR: battery switch internal refresh rate

Table 39. BSRR bit - battery switch control (address 26h) bit description

Bit	Symbol	Value	Description
3	BSRR		**battery switch refresh rate**
		0[1]	low
		1	high

[1] Default value.

Non-user bit. Recommended to leave set at default.

8.11.3 BSM[1:0]: battery switch mode

Table 40. BSM[1:0] bits - battery switch control (address 26h) bit description

Bit	Symbol	Value	Description
2 to 1	BSM[1:0]		**battery switch mode bits**
		00[1]	switching at the V_{th} level
		01	switching at the V_{BAT} level
		10	switching at the higher level of V_{th} or V_{BAT}
		11	switching at the lower level of V_{th} or V_{BAT}

[1] Default value.

Switching is automatic and controlled by the voltages on the VBAT and VDD pins. There are three modes:

- Compare V_{DD} with an internal reference (V_{th})
- Compare V_{DD} with V_{BAT}
- Compare V_{DD} with an internal reference (V_{th}) and V_{BAT}

The last mode is useful when a rechargeable battery is employed.

Table 41. Battery switch-over modes

BSM[1:0]	Condition	Internal power
00	$V_{DD} > V_{th}$	V_{DD}
	$V_{DD} < V_{th}$	V_{BAT}
01	$V_{DD} > V_{BAT}$	V_{DD}
	$V_{DD} < V_{BAT}$	V_{BAT}
10	V_{DD} > the higher of V_{th} or V_{BAT}	V_{DD}
	V_{DD} < the higher of V_{th} or V_{BAT}	V_{BAT}
11	V_{DD} > the lower of V_{th} or V_{BAT}	V_{DD}
	V_{DD} < the lower of V_{th} or V_{BAT}	V_{BAT}

Due to the nature of the power switch circuit there is a switching hysteresis (see Figure 22 and Table 68).

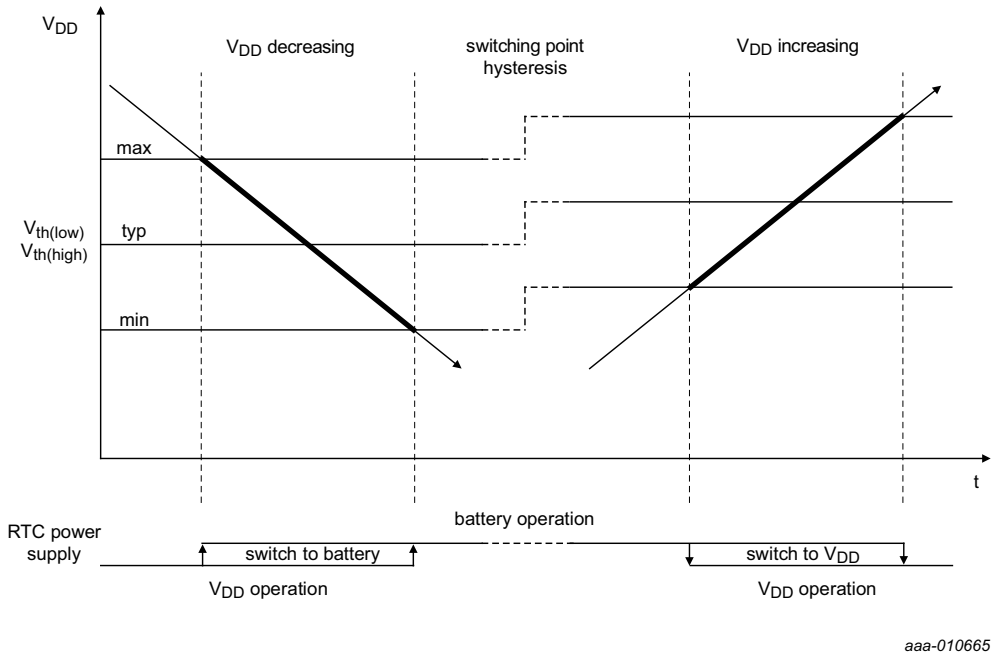


Fig 22. Threshold voltage switching hysteresis

8.11.3.1 Switching at the V_{th} level, BSM[1:0] = 00

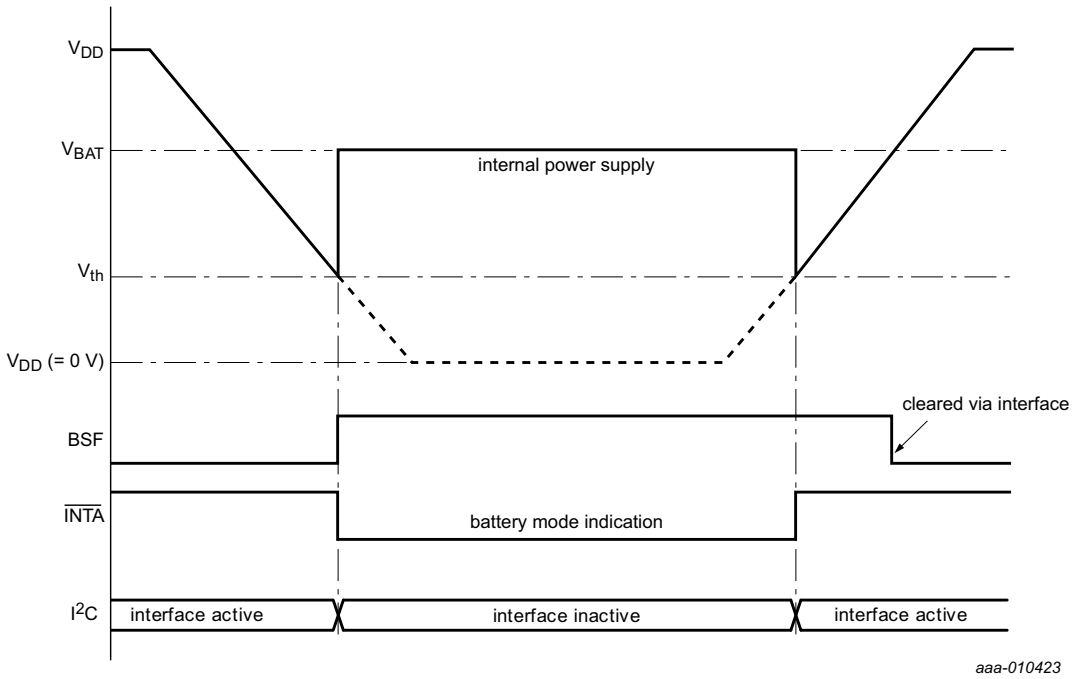


Fig 23. Switching at V_{th}

8.11.3.2 Switching at the V_{BAT} level, BSM[1:0] = 01

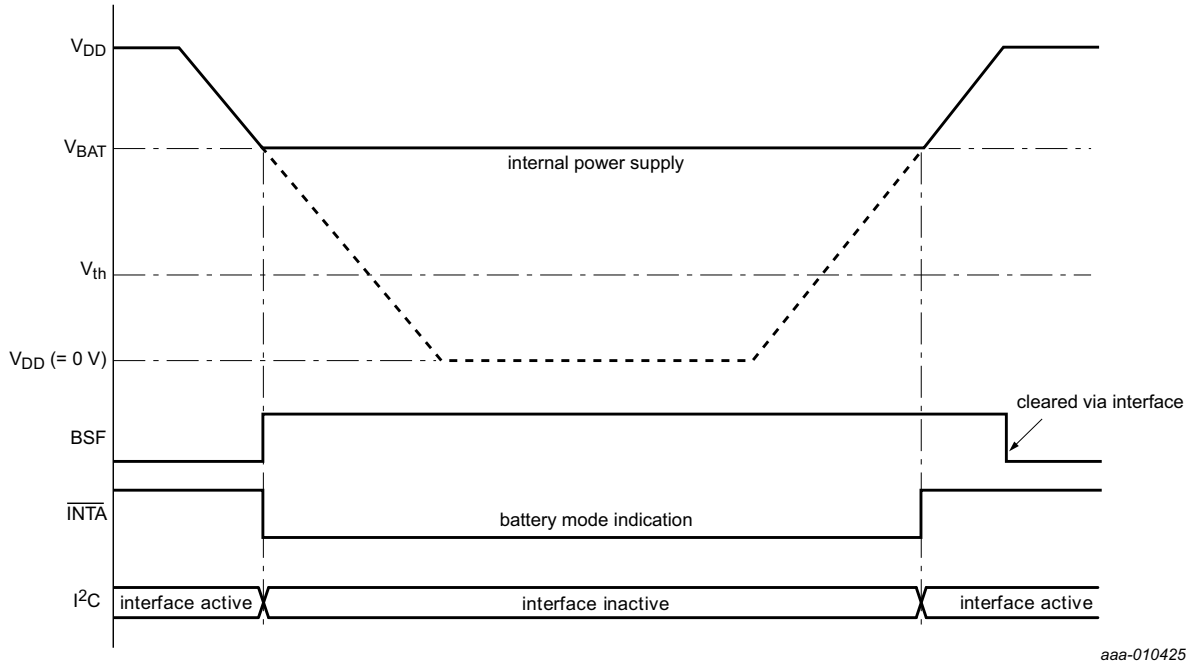


Fig 24. Switching at V_{BAT}

8.11.3.3 Switching at the higher of V_{BAT} or V_{th} level, BSM[1:0] = 10

With this mode switching takes place when V_{DD} falls below the higher of V_{th} or V_{BAT}. In Figure 25, an example is given where the threshold is set to 1.5 V and a single cell battery is connected to VBAT. In this example, switching to the battery voltage takes place when V_{DD} falls below V_{th}.

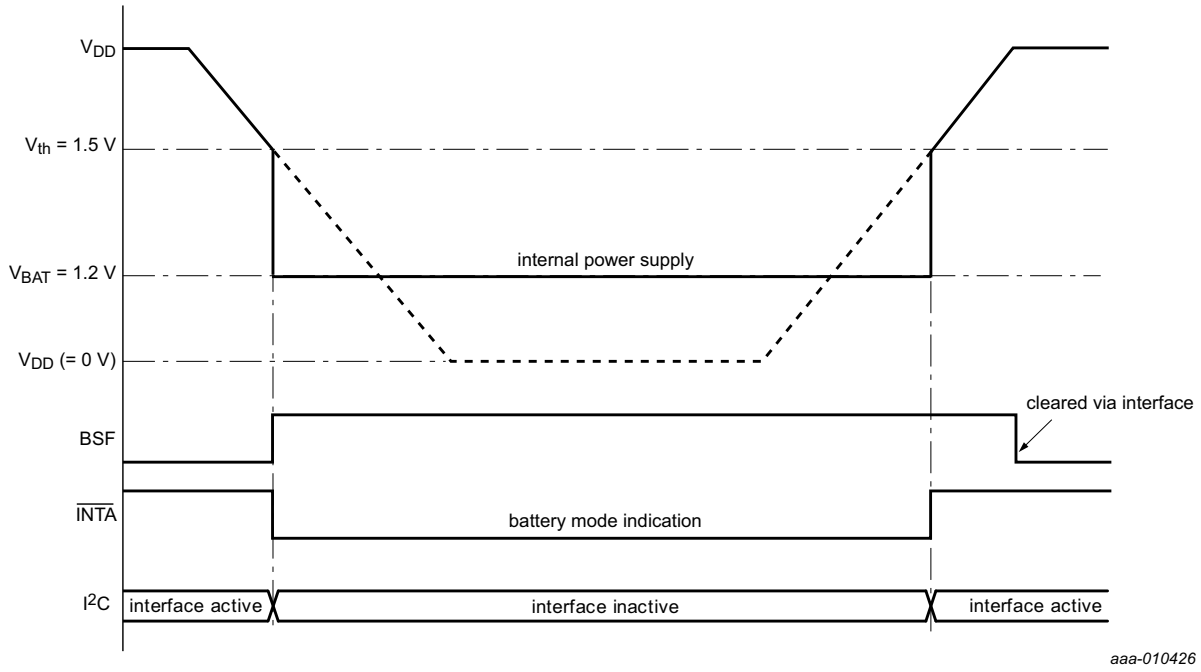


Fig 25. Switching at the higher of V_{BAT} or V_{th}

8.11.3.4 Switching at the lower of V_{BAT} and V_{th} level, BSM[1:0] = 11

With this mode switching takes place when V_{DD} falls below the lower of V_{th} or V_{BAT}. In Figure 26, an example is given where the threshold is set to 1.5 V and a single cell battery is connected to VBAT. In this example, switching to the battery voltage takes place when V_{DD} falls below V_{BAT}.

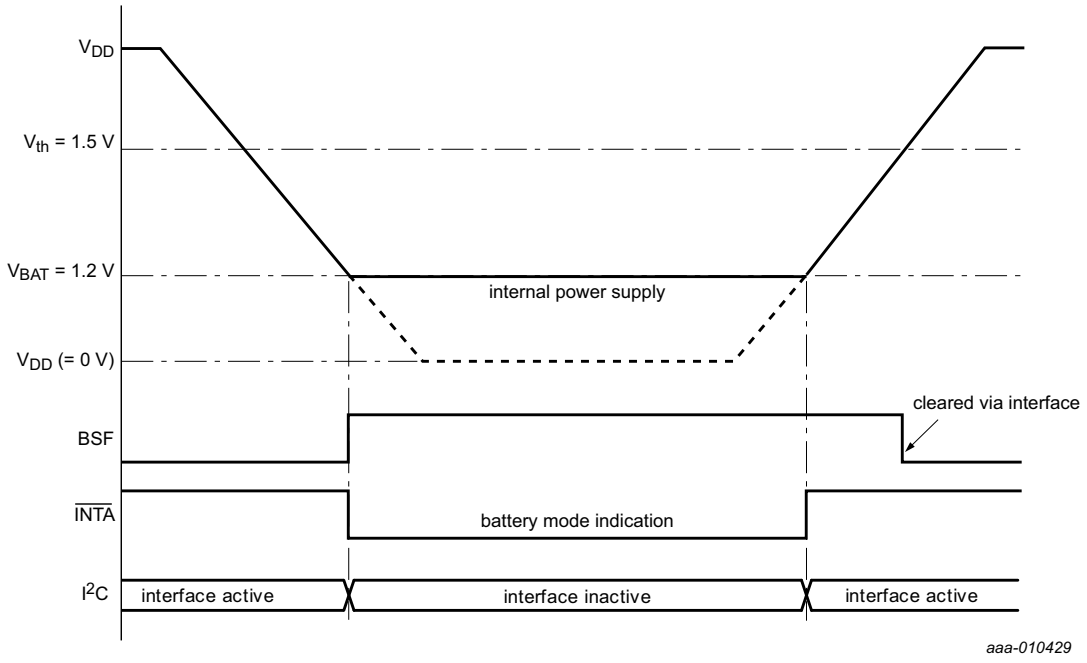


Fig 26. Switching at the lower of V_{BAT} or V_{th}

8.11.4 BSTH: threshold voltage control

Table 42. BSTH - battery switch control (address 26h) bit description

Bit	Symbol	Value	Description
0	BSTH		**battery switch threshold voltage, V_{th}**
		0[1]	V_{th} = 1.5 V
		1	V_{th} = 2.8 V

[1] Default value.

The threshold for battery switch-over is selectable between two voltages, 1.5 V and 2.8 V.

8.11.5 Battery switch interrupts

The generation of interrupts from the battery switch function is controlled via the battery switch interrupt enable bits; BSIEA and BSIEB. These bits are in registers INTA_enable (address 29h) and INTB_enable (address 2Ah).

The assertion of the flag BSF (register Flags, address 2Bh) can be used to generate an interrupt at pins $\overline{INTA}$ and $\overline{INTB}$. The interrupt may be generated as a pulsed signal or alternatively as a permanently active signal which follows the condition of bit BSF. BSF remains set until cleared by command.

When enabled, interrupts are triggered every time the battery switch circuit switches to either battery or to V_{DD} and even if the BSF is not cleared, an interrupt pulse can be generated.

In addition, the $\overline{INTA}$ pin can be configured as a battery mode indicator (INTAPM[1:0] = 00). See Section 8.12.6 on page 51. This mode differs from a general interrupt signal in that it is only controlled by the current battery switch status.

See Section 8.9 on page 37 for interrupt control.

Remark: $\overline{INTB}$ pin is only active when the IC is operating from V_{DD}.

8.12 Pin_IO register

Table 43. Pin_IO- pin input output control register (address 27h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	CLKPM	TSPULL	TSL	TSIM	TSPM[1:0]		INTAPM[1:0]	
Section	Section 8.12.1	Section 8.12.2	Section 8.12.3	Section 8.12.5	Section 8.12.4		Section 8.12.6	

This register is used to define the input and output modes of the IC.

8.12.1 CLKPM: CLK pin mode control

Table 44. CLKPM bit - Pin_IO control register (address 27h)

Bit	Symbol	Value	Description
7	CLKPM[1]		**CLK pin mode**
		0[2]	enable CLK pin
		1	disable CLK pin

[1] CLK pin is not available on all package types.

[2] Default value.

Setting the CLKPM bit disables the CLK output and force the pin to drive out a logic 0. Clearing this bit enables the pad to output the selected clock frequency (see bits COF[2:0] in the Function register, see Table 51 on page 53).

8.12.2 TSPULL: TS pin pull-up resistor value

Table 45. TSPULL bit - Pin_IO control register (address 27h)

Bit	Symbol	Value	Description
6	TSPULL		**TS pin pull-up resistor value**
		0[1]	80 kΩ
		1	40 kΩ

[1] Default value.

Controls the pull-up resistor value used in the mechanical switch detector. For applications where there is a large capacitance on the TS pin e.g. from a long connecting cable to the mechanical switch, the pull-up resistor value can be halved to improve switch detection.

Using the low-resistance value increases current consumption when the switch is closed i.e. shorting to V_{SS}.

8.12.3 TSL: TS pin level sense

Table 46. TSL bit - Pin_IO control register (address 27h)

Bit	Symbol	Value	Description
5	TSL		**TS pin input sense**
		0[1]	active HIGH
		1	active LOW

[1] Default value.

The active state of the TS pin can be defined for use as a timestamp trigger and/or as stop control for the time counting. Active HIGH implies a transition from logic 0 to logic 1 is active. Active LOW implies a transition from logic 1 to logic 0 is active.

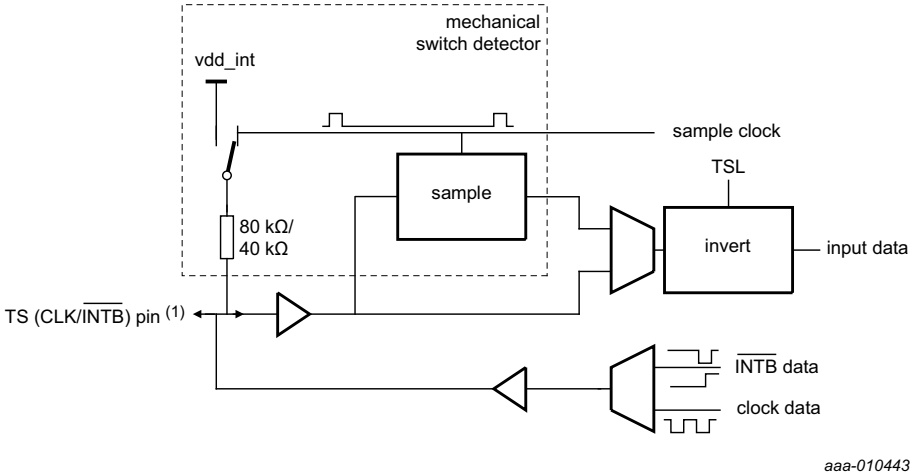
8.12.4 TSPM[1:0]: TS pin I/O control

Table 47. TSPM[1:0] bits - Pin_IO control register (address 27h)

Bit	Symbol	Value	Description
3 to 2	TSPM[1:0]		**TS pin IO mode**
		00[1]	disabled; input can be left floating
		01	$\overline{\text{INTB}}$ output; push-pull
		10	CLK output; push-pull
		11	input mode

[1] Default value.

These bits control the operation of the TS pin.



(1) Not available on all package types.

Fig 27. TS pin

TSIM is only considered when the TS pin is in input mode.

8.12.4.1 TS pin output mode; $\overline{\text{INTB}}$

It is possible to output $\overline{\text{INTB}}$ data on the TS pin. The output is push-pull. No output is available when on V_{BAT}. When on V_{BAT} the output is Hi-Z.

8.12.4.2 TS pin output mode; CLK

It is possible to output a clock frequency on the TS pin. Clock frequency is selected with the COF[2:0] bits in the Function register (Section 8.13 on page 53). The output is push-pull. No output is available when on V_{BAT}. When on V_{BAT} the output is Hi-Z.

8.12.4.3 TS pin disabled

When disabled the pin is Hi-Z and can be left floating.

8.12.5 TSIM: TS pin input type control

Table 48. TSIM bit - Pin_IO control register (address 27h)

Bit	Symbol	Value	Description
4	TSIM		**TS pin input mode**
		0[1]	CMOS input; reference to V_{DD}; disabled when on V_{BAT}
		1	mechanical switch mode; active pull-up sampled at 16 Hz; operates on V_{DD} and V_{BAT}

[1] Default value.

In CMOS input mode (TSIM = 0), input is taken directly from the TS pin. The input is conditioned by the setting of TSL. When operating on the battery voltage (V_{BAT}), the input is disabled and is allowed to float.

In mechanical switch detector mode (TSIM = 1), the TS pin is sampled at a rate of 16 Hz for a period of 30.5 μs. At the same time as the sample a pull-up resistor is activated to detect an open pin or a pin shorted to V_{SS}. The input is referenced to the internal power supply. This mode operates when on V_{DD} or V_{BAT}. The pull-up resistor value can be controlled by TSPULL bit in the Pin_IO register (see Section 8.12 on page 49).

8.12.5.1 TS pin input mode

There are two input types which are controlled by the TSIM bit. The TS input can be used to generate a timestamp event by configuring the timestamp mode bits; TSR2M[2:0] and TSR1M[1:0] bits in TSR_mode register (see Table 20 on page 29).

Also it is possible to use the TS pin to control counting of time. This is typically for use with the stop-watch mode where an elapsed time counter function can be implemented. Using the STOPM bit in the Function register (see Table 51 on page 53) it is possible to control the STOP bit by the TS pin.

8.12.6 INTAPM[1:0]: $\overline{\text{INTA}}$ pin mode control

Table 49. INTAPM[1:0] bits - Pin_IO control register (address 27h)

Bit	Symbol	Value	Description
1 to 0	INTAPM[1:0]		**$\overline{\text{INTA}}$ pin mode**
		00[1]	CLK output mode
		01	battery mode indication
		10	$\overline{\text{INTA}}$ output
		11	Hi-Z

[1] Default value.

The $\overline{\text{INTA}}$ pin can be used to output three different signals.

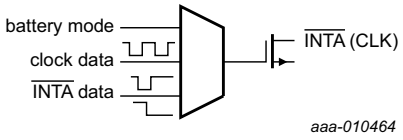


Fig 28. $\overline{\text{INTA}}$ pin

8.12.6.1 INTAPM[1:0]: $\overline{\text{INTA}}$

The primary function of the $\overline{\text{INTA}}$ pin is to output $\overline{\text{INTA}}$ data. $\overline{\text{INTA}}$ data is controlled by the bits of the INTA_enable register (see Table 29 on page 38).

The output is active LOW with an open-drain output. The output is available during V_{DD} and V_{BAT} operation.

8.12.6.2 INTAPM[1:0]: clock data

It is possible to output a clock frequency on the $\overline{\text{INTA}}$ pin. Clock frequency is selected with the COF[2:0] bits in the Function register (Section 8.13 on page 53). The output is active LOW with an open-drain output. The output is available only during V_{DD} operation. The output is Hi-Z when operating from V_{BAT}.

Remark: Clock output is the default state. To save power, it is recommended to disable the clock when not being used. If no clock is required, then set COF[2:0] in the Function register (Section 8.13 on page 53) to CLK disabled. If clock output is only required on the CLK pin, then set the $\overline{\text{INTA}}$ pin to either $\overline{\text{INTA}}$ data or battery mode.

8.12.6.3 INTAPM[1:0]: battery mode indication

It is possible to output the state of the power switch on the $\overline{\text{INTA}}$ pin. The output has an open-drain output. The output is available during V_{DD} and V_{BAT} operation.

Table 50. $\overline{\text{INTA}}$ battery mode

Power supply	$\overline{\text{INTA}}$ pin state
V_{DD}	$\overline{\text{INTA}}$ = Hi-Z
V_{BAT}	$\overline{\text{INTA}}$ = logic 0

8.13 Function register

Table 51. Function - chip function control register (address 28h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	100TH	PI[1:0]		RTCM	STOPM	COF[2:0]		
Section	Section 8.13.1	Section 8.13.2		Section 8.13.3	Section 8.13.4	Section 8.13.5		

8.13.1 100TH: 100th seconds mode

Table 52. 100TH bit - Function control register (address 28h)

Bit	Symbol	Value	Description
7	100TH		**100th second mode**
		0[1]	100th second disabled
		1	100th second enabled

[1] Default value.

The PCF85363A can be configured to count at a resolution of 1 second or 0.01 seconds. In 100th mode, the 100th_seconds register becomes available and the RTC counts at a resolution of 0.01 seconds.

The 256 Hz clock signal is divided by 3 for fourteen 100 Hz periods and then by 2 for eleven 100 Hz periods. This produces an effective division ratio of 2.56 with a maximum jitter of 3.91 ms. Over twenty-five 100 Hz cycles the jitter is 0 ns.

8.13.2 PI[1:0]: Periodic interrupt

Table 53. PI[1:0] bits - Function control register (address 28h)

Bit	Symbol	Value	Description
6 to 5	PI[1:0]		**periodic interrupt**
		00[1]	no periodic interrupt
		01	once per second
		10	once per minute
		11	once per hour

[1] Default value.

The periodic interrupt mode can be used to enable pre-defined timers for generating pulses on the interrupt pin. Interrupts once per second, once per minute or once per hour can be generated.

When disabled, the timers are reset. When enabled, the time to the first pulse is between the chosen period and the chosen period minus 1 seconds.

The timers are not affected by STOP.

When the periodic interrupt triggers, the PIF (PI flag) in the Flags register (Section 8.14 on page 56) is set.

The flag does not have to be cleared to allow another $\overline{\text{INTA}}$ or $\overline{\text{INTB}}$ pulse.

The duration of the periodic interrupt is unaffected by offset calibration.

See Section 8.9 “Interrupts” for a description of interrupt pulse control and output pins.

8.13.3 RTCM: RTC mode

Table 54. RTCM bit - Function control register (address 28h)

Bit	Symbol	Value	Description
4	RTCM		**RTC mode**
		0[1]	real-time clock mode
		1	stop-watch mode

[1] Default value.

The RTC mode is used to control how the time is counted. When configured as a classic RTC, then time is counted from 100th seconds to years. In stop-watch mode, time is counted from 100th seconds to 999999 hours.

Table 55. RTC time counting modes

RTCM	Mode	Time counting
0	RTC	100th seconds[1], seconds, minutes, hours, days, weekdays, months, years
1	stop-watch	100th seconds[1], seconds, minutes, hours (0 hours to 999999 hours)

[1] Enabled with 100TH bit in the Function register (Section 8.13 on page 53).

8.13.4 STOPM: STOP mode control

Table 56. STOPM bit - Function control register (address 28h)

Bit	Symbol	Value	Description
3	STOPM		**STOP mode**
		0[1]	RTC stop is controlled by STOP bit only
		1	RTC stop is controlled by STOP bit or TS pin

[1] Default value.

The STOP register bit in the Oscillator register (Section 8.10 on page 41) is used to stop the counting of time in both RTC mode and stop-watch mode. Stopping of the oscillator can also be controlled from the TS pin. The TS pin must first be configured as an input by the TSPM[1:0] bits, then selected for active HIGH or active LOW by the TSL bits.

Table 57. Oscillator stop control when STOPM = 1

STOP bit[1]	TSL	TS pin[2]	Oscillator state	Description
0	0	0	running	TS pin active HIGH
		1	stopped	
	1	0	stopped	TS pin active LOW
		1	running	
1	-	-	stopped	TS pin ignored

[1] In the Oscillator register (Section 8.10 on page 41).

[2] TSPM[1:0] = 11.

8.13.5 COF[2:0]: Clock output frequency

Table 58. COF[2:0] bits - Function control register (address 28h)

Bit	Symbol	Value	Frequency selection (Hz)		
			CLK pin	TS pin	$\overline{\text{INTA}}$ pin
2 to 0	COF[2:0]	000[1]	32768	32768	32768
		001	16384	16384	16384
		010	8192	8192	8192
		011	4096	4096	4096
		100	2048	2048	2048
		101	1024	1024	1024
		110	1	1	1
		111	static LOW	static LOW	Hi-Z

[1] Default value.

A programmable square wave is available at pin CLK. Operation is controlled by the COF[2:0] bits. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLK is a push-pull output and enabled at power-on. Pin CLK can be disabled by setting CLKPM = 1 in the Pin_IO register (Section 8.12 on page 49). When disabled, the CLK pin is LOW.

The selected clock frequency may also be output on the TS pin and the $\overline{\text{INTA}}$ pin. The CLKIV bit may be used to invert the clock output. CLKIV does not invert for the setting COF[2:0] = 111.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all clock frequencies except 32.768 kHz have a duty cycle of 50 : 50.

Table 59. Clock duty cycles

COF[2:0]	Frequency (Hz)	Typical duty cycle[1]
000[2]	32768	60 : 40 to 40 : 60
001	16384	50 : 50
010	8192	50 : 50
011	4096	50 : 50
100	2048	50 : 50
101	1024	50 : 50
110	1[3]	50 : 50
111	static	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] Default value.

[3] 1 Hz clock pulses are not affected by offset correction pulses.

8.14 Flags register

Table 60. Flags - Flag status register (address 2Bh) bit description

Bit	Symbol	Flag name	Value	Description
7	PIF	Periodic Interrupt Flag Section 8.13.2 on page 53	0[1]	read: periodic interrupt flag inactive
				write: periodic interrupt flag is cleared
			1	read: periodic interrupt flag active
				write: periodic interrupt flag remains unchanged
6	A2F	Alarm2 Flag Section 8.4 on page 18	0[1]	read: alarm2 flag inactive
				write: alarm2 flag is cleared
			1	read: alarm2 flag active
				write: alarm2 flag remains unchanged
5	A1F	Alarm1 Flag Section 8.4 on page 18	0[1]	read: alarm1 flag inactive
				write: alarm1 flag is cleared
			1	read: alarm1 flag active
				write: alarm1 flag remains unchanged
4	WDF	WatchDog Flag Section 8.5 on page 25	0[1]	read: WatchDog flag inactive
				write: WatchDog flag is cleared
			1	read: WatchDog flag active
				write: WatchDog flag remains unchanged
3	BSF	Battery Switch Flag Section 8.11 on page 43	0[1]	read: battery switch flag inactive
				write: battery switch flag is cleared
			1	read: battery switch flag active
				write: battery switch flag remains unchanged
2	TSR3F	Timestamp Register 3 event Flag Section 8.7 on page 27	0[1]	read: timestamp register 3 flag inactive
				write: timestamp register 3 flag is cleared
			1	read: timestamp register 3 flag active
				write: timestamp register 3 flag remains unchanged
1	TSR2F	Timestamp Register 2 event Flag Section 8.7 on page 27	0[1]	read: timestamp register 2 flag inactive
				write: timestamp register 2 flag is cleared
			1	read: timestamp register 2 flag active
				write: timestamp register 2 flag remains unchanged
0	TSR1F	Timestamp Register 1 event Flag Section 8.7 on page 27	0[1]	read: timestamp register 1 flag inactive
				write: timestamp register 1 flag is cleared
			1	read: timestamp register 1 flag active
				write: timestamp register 1 flag remains unchanged

[1] Default value.

The flags are set by their respective function. A full description can be found there. All flags behave the same way. They are set by some function of the IC and remain set until overwritten by command. It is possible to clear flags individually. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access. All flags are combined to generate an event monitoring signal called EMON. EMON is described in Section 8.2.3 on page 14 and can be read as the MSB of minutes register.

8.15 Reset register

Table 61. Reset - software reset control (address 2Fh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	CPR	0	1	0	SR	1	0	CTS
Section	Section 8.15.2				Section 8.15.1			Section 8.15.3

For a

- software reset (SR), 00101100 (2Ch) must be sent to register Reset (address 2Fh). A software reset also triggers CPR and CTS
- clear prescaler (CPR), 10100100 (A4h) must be sent to register Reset (address 2Fh)
- clear timestamp (CTS),00100101 (25h) must be sent to register Reset (address 2Fh)

It is possible to combine CPR and CTS by sending 10100101 (A5h).

Remark: Any other value sent to this register is ignored.

8.15.1 SR - Software reset

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command.

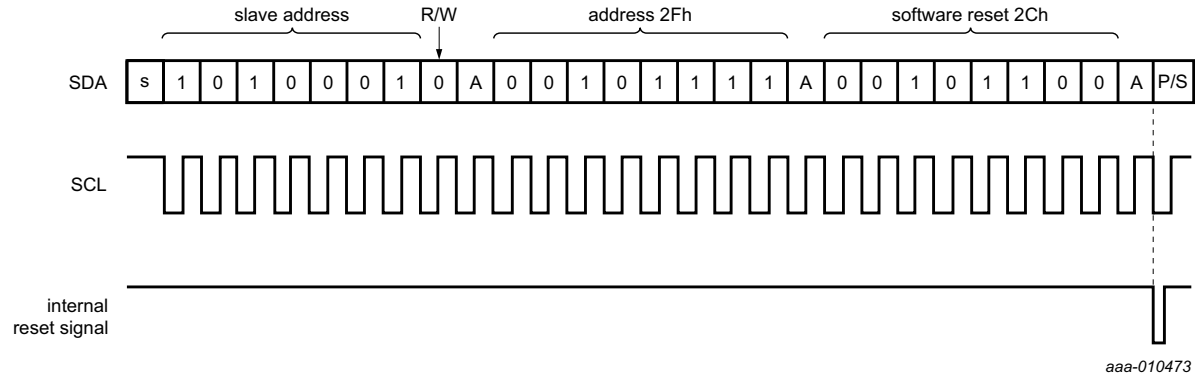


Fig 29. Software reset command

The PCF85363A resets to:

Mode — real-time clock, 100th second off

Time — 00:00:00.00

Date — 2000.01.01

Weekday — Saturday

Battery switch — on, switching on the lower threshold voltage

Oscillator — C_L = 7 pF

Pins — $\overline{\text{INTA}}$ = 32 kHz output, CLK = 32 kHz output, TS = disabled

In the reset state, all registers are set according to Table 62.

Table 62. Registers reset values

Registers labeled as - remain unchanged.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	100TH_seconds	0	0	0	0	0	0	0	0
01h	Seconds	1	0	0	0	0	0	0	0
02h	Minutes	0	0	0	0	0	0	0	0
03h	Hours	0	0	0	0	0	0	0	0
04h	Days	0	0	0	0	0	0	0	1
05h	Weekdays	0	0	0	0	0	1	1	0
06h	Months	0	0	0	0	0	0	0	1
07h	Years	0	0	0	0	0	0	0	0
08h	Second_alarm1	-	-	-	-	-	-	-	-
	Second_alm1								
09h	Minute_alarm1	-	-	-	-	-	-	-	-
	Minute_alm1								
0Ah	Hour_alarm1	-	-	-	-	-	-	-	-
	Hr_xx_xx_00_alm1								
0Bh	Day_alarm1	-	-	-	-	-	-	-	-
	Hr_xx_00_xx_alm1								
0Ch	Month_alarm1	-	-	-	-	-	-	-	-
	Hr_00_xx_xx_alm1								
0Dh	Minute_alarm2	-	-	-	-	-	-	-	-
	Minute_alm2								
0Eh	Hour_alarm2	-	-	-	-	-	-	-	-
	Hr_xx_00_alm2								
0Fh	Weekday_alarm2	-	-	-	-	-	-	-	-
	Hr_00_xx_alm2								
10h	Alarm enables	0	0	0	0	0	0	0	0
11h to 16h	Timestamp 1	0	0	0	0	0	0	0	0
17h to 1Ch	Timestamp 2	0	0	0	0	0	0	0	0
1Dh to 22h	Timestamp 3	0	0	0	0	0	0	0	0
23h	Timestamp_mode	0	0	0	0	0	0	0	0
24h	Offset	0	0	0	0	0	0	0	0
25h	Oscillator	0	0	0	0	0	0	0	0
26h	Battery_switch	0	0	0	0	0	0	0	0
27h	Pin_IO	0	0	0	0	0	0	0	0
28h	Function	0	0	0	0	0	0	0	0
29h	INTA_enable	0	0	0	0	0	0	0	0
2Ah	INTB_enable	0	0	0	0	0	0	0	0
2Bh	Flags	0	0	0	0	0	0	0	0

Table 62. Registers reset values *...continued*

Registers labeled as - remain unchanged.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
2Ch	RAM_byte	0	0	0	0	0	0	0	0
2Dh	WatchDog	0	0	0	0	0	0	0	0
2Fh	Reset	0	0	0	0	0	0	0	0

8.15.2 CPR: clear prescaler

To set the time for RTC mode accurately or to clear the time in stop-watch mode, the clear prescaler instruction is needed.

Before sending this instruction, it is recommended to first set *stop* either by the STOP bit or by the TS pin (see STOPM bit).

See STOP definition for an explanation on using this instruction.

8.15.3 CTS: clear timestamp

The timestamp registers (address 11h to 22h) can be set to all 0 with this instruction.

8.16 Stop_enable register

Table 63. Stop_enable - control of STOP bit (address 2Eh)

Bit	Symbol	Value	Description
7 to 1	-	0000000	not used
0	STOP		**STOP bit**
		0[1]	RTC clock runs
		1	RTC clock is stopped

[1] Default value.

The STOP bit stops the time from counting in both RTC mode and stop-watch mode. For RTC mode STOP is useful to set the time accurately. For stop-watch mode it is the start/stop control for the watch.

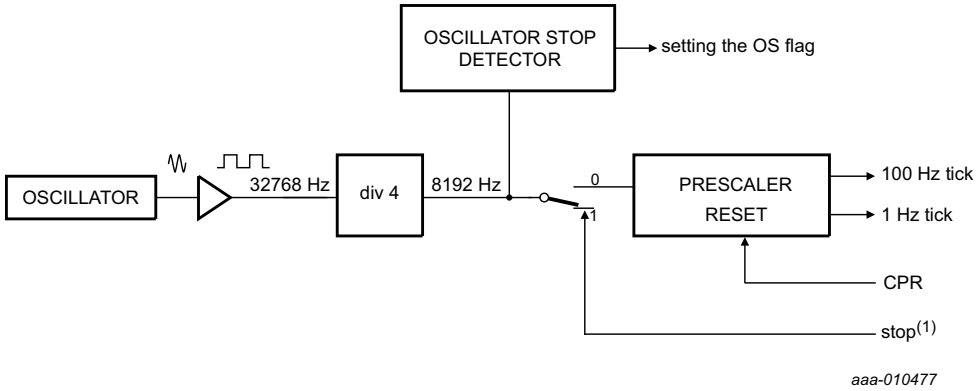
The counter can also be controlled from the TS pin by configuring STOPM in the Function register (Section 8.13 on page 53). The internal *stop* signal is a combination of STOP and the TS pin state.

Table 64. Counter stop signal

STOP bit	TS pin[1][2]	*stop* signal	Counter
1	-	1	stopped
-	1	1	stopped
0	0	0	running

[1] Requires STOPM and TSPM[1:0] to be configured.

[2] TSL = 0 (active HIGH) (Pin_IO register, address 27h).



(1) *stop* is a combination of STOP register bit and the TS pin when programmed for stop control.

Fig 30. CPR and STOP bit functional diagram

The *stop* signal blocks the 8.192 kHz clock from generating system clocks and freezes the time. In this state, the prescaler can be cleared with the CPR command in the Resets register (Section 8.15 on page 57).

Remark: The output of clock frequencies is not affected.

The time circuits can then be set and do not increment until the STOP bit is released.

The *stop* acts on the 8.192 kHz signal. And because the I²C-bus or TS pin input is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between zero and one 8.192 kHz cycle (see Figure 31).

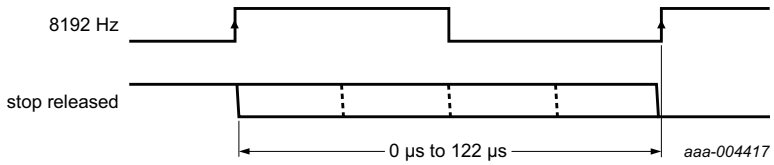


Fig 31. STOP release timing

The first increment of the time circuits is between 0 s and 122 µs after STOP is released.

The flow for accurately setting the time in RTC mode is:

- start an I²C access at register 2Eh
- set STOP bit
- send CPR instruction
- address counter rolls over to address 00h
- set time (100th seconds, seconds to years)
- end I²C access
- wait for external time reference to indicate that time counting should start
- start an I²C access at register 2Eh
- clear STOP bit (time starts counting from now)

- end I²C access

The flow for resetting time in stop-watch mode is:

- start an I²C access at register 2Eh
- set STOP bit
- send CPR instruction
- address counter will roll over to address 00h
- set time to 000000:00:00.00
- end I²C access

8.17 64 byte RAM

In addition to the single RAM byte, there is a 64 byte RAM available from address 40h to 7Fh. The RAM can be written and read when the device is powered from V_{DD}. The RAM content is backed-up when the device is powered from V_{BAT}, but cannot be accessed as the interface is disabled.

The address pointer is set during interface initiation and will auto increment after each byte access. The pointer will wrap around from address 7Fh to 40h after the last byte is accessed, (see Figure 5).

9. I²C-bus interface

The I²C-bus is for bidirectional, two-line communication between different ICs. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy. Both data and clock lines remain HIGH when the bus is not busy. The PCF85363A acts as a slave receiver when being written to and as a slave transmitter when being read from.

Remark: When on V_{BAT} power, the interface is not accessible.

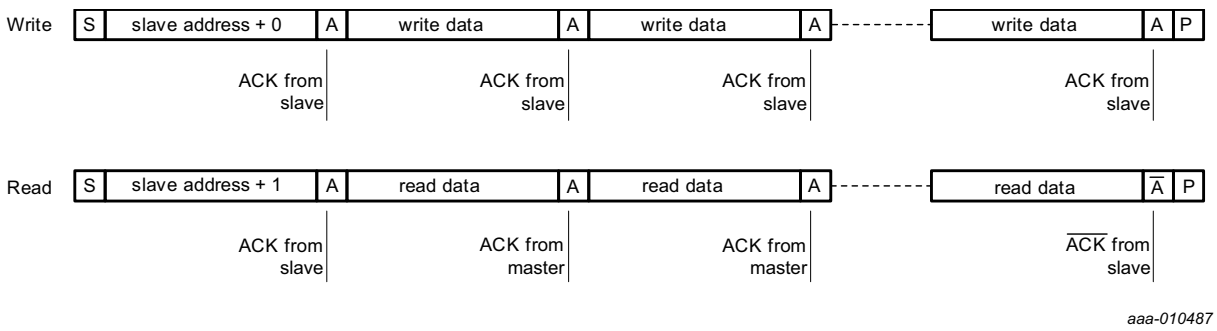


Fig 32. I²C read and write protocol

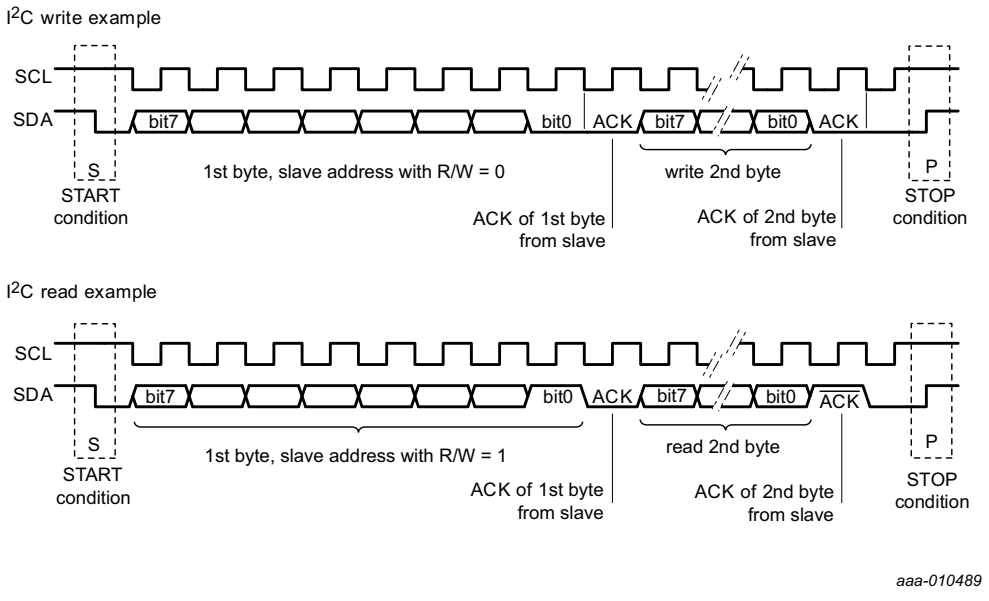


Fig 33. I²C read and write signaling

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time are interpreted as STOP or START conditions.

9.2 START and STOP conditions

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P (see Figure 33).

9.3 Acknowledge

Each byte of 8 bits is followed by an acknowledge cycle. An acknowledge is defined as logic 0. A not-acknowledge is defined as logic 1.

When written to, the slave will generate an acknowledge after the reception of each byte. After the acknowledge, another byte may be transmitted. It is also possible to send a STOP or START condition.

When read from, the master receiver must generate an acknowledge after the reception of each byte. When the master receiver no longer requires bytes to be transmitter, it must generate a not-acknowledge. After the not-acknowledge, either a STOP or START condition must be sent.

A detailed description of the I²C-bus specification is given in Ref. 10 “UM10204”.

10. Interface protocol

The PCF85363A uses the I²C interface for data transfer. Interpretation of the data is determined by the interface protocol.

10.1 Write protocol

After the I²C slave address is transmitted, the PCF85363A requires that the register address pointer is defined. It can take the value 00h to 2Fh. Values outside of that range will result in the transfer being ignored, however the slave will still respond with acknowledge pulses.

After the register address is transmitted, write data is transmitted. The minimum number of data write bytes is 0 and the maximum number is unlimited. After each write, the address pointer increments by one. After address 2Fh, the address pointer will roll over to 00h.

- I²C START condition
- I²C slave address + write
- register address
- write data
- write data
- :
- write data
- I²C STOP condition; an I²C RE-START condition is also possible.

10.2 Read protocol

When reading the PCF85363A, reading starts at the current position of the address pointer. The address pointer for read data should first be defined by a write sequence.

- I²C START condition
- I²C slave address + write
- register address
- I²C STOP condition; an I²C RE-START condition is also possible.

After setting the address pointer, a read can be executed. After the I²C slave address is transmitted, the PCF85363A will immediately output read data. After each read, the address pointer increments by one. After address 2Fh, the address pointer will roll over to 00h.

- I²C START condition
- I²C slave address + read
- read data (master sends acknowledge bit)
- read data (master sends acknowledge bit)
- :
- read data (master sends **not**-acknowledge bit)
- I²C STOP condition. An I²C RE-START condition is also possible.

The master must indicate that the last byte has been read by generating a not-acknowledge after the last read byte.

10.3 Slave addressing

10.3.1 Slave address

One I²C-bus slave address (1010 001) is reserved for the PCF85363A. The entire I²C-bus slave address byte is shown in Table 65.

Table 65. I²C slave address byte

	Slave address							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	MSB							**LSB**
	1	0	1	0	0	0	1	R/$\overline{W}$

After a START condition, the I²C slave address has to be sent to the PCF85363A device.

Slave address can also be written in a hexadecimal format:

- A2h - Write slave address
- A3h - Read slave address

11. Application design-in information

In this application, stop-watch mode is used to implement an elapsed time counter. The TS pin is used with a mechanical switch to start and stop the time. Each time the time is stopped, timestamp2 is loaded with the current time and an interrupt is generated on the $\overline{\text{INTA}}$ pin.

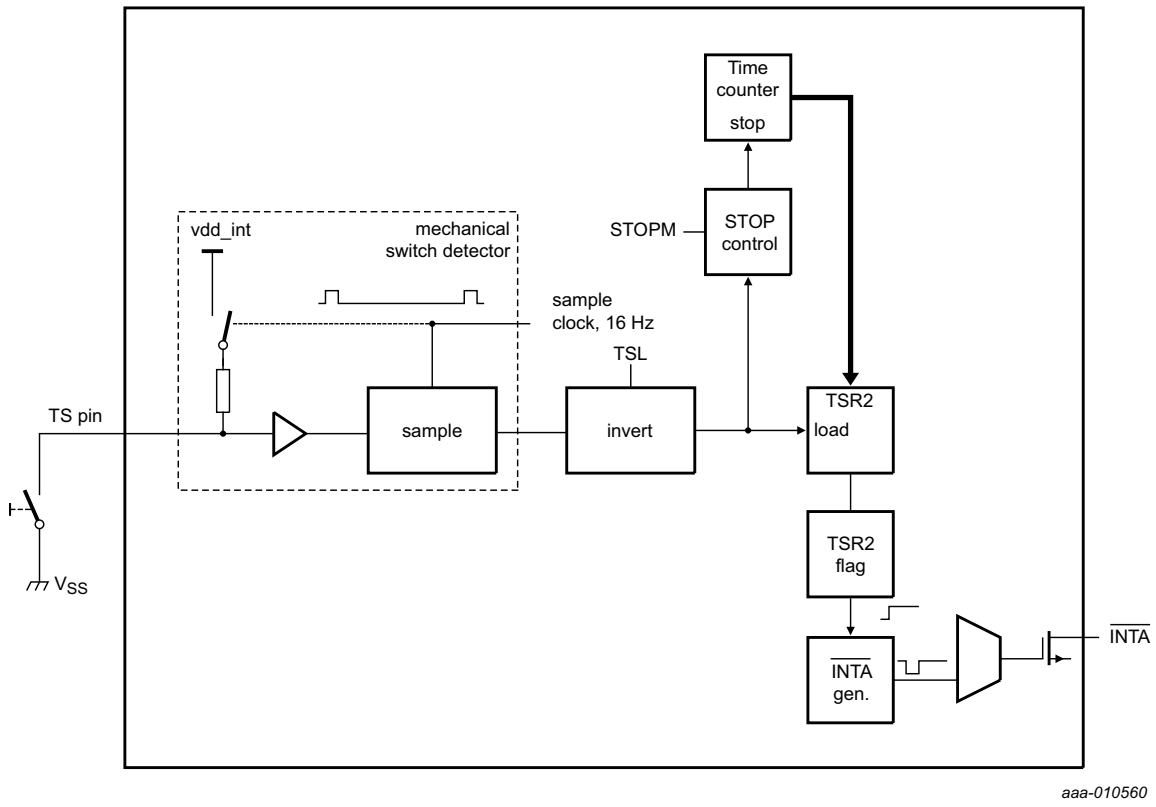


Fig 34. Application example

The RTC must be configured correctly for this mode of operation. Outlined in Table 66 are the settings needed for this mode.

In addition, the time must be set and any other configurations like battery switch-over, quartz oscillator driving mode, etc., which are dependent on the application.

The sampler circuit shown in Figure 34 will hold invalid data until the mechanical switch detector mode is enabled. It then requires a minimum of one sample period to initialize to the current TS pin level. It is recommended to enable the mechanical detector mode on the TS pin at least 62.5 ms before enabling the TS event mode. Failure to do so can result in a false first event.

Table 66. Application configuration

Register	Section	Bit(s)	State	Comment
Pin_IO	Section 8.12	TSPM[1:0]	11	TS pin in input mode
Pin_IO	Section 8.12	TSIM	1	select mechanical switch mode
Pin_IO	Section 8.12	TSL	1	TS pin input is active LOW
Function	Section 8.13	STOPM	1	allow TS pin to control STOP
		TSRIEA	1	allow timestamps to create interrupts
		ILPA	0	generate interrupt pulses
TSR_mode	Section 8.12	TSR2M[2:0]	101	last event mode for timestamp2
Pin_IO	Section 8.12	INTAPM[1:0]	10	output interrupt on $\overline{\text{INTA}}$

Figure 35 shows the waveforms that can be expected. *sample clock*, *vdd_int* and *stop* are internal nodes. *vdd_int* is supply which operates the IC and will be either V_{DD} or V_{BAT}, depending on the state of the battery switch-over.

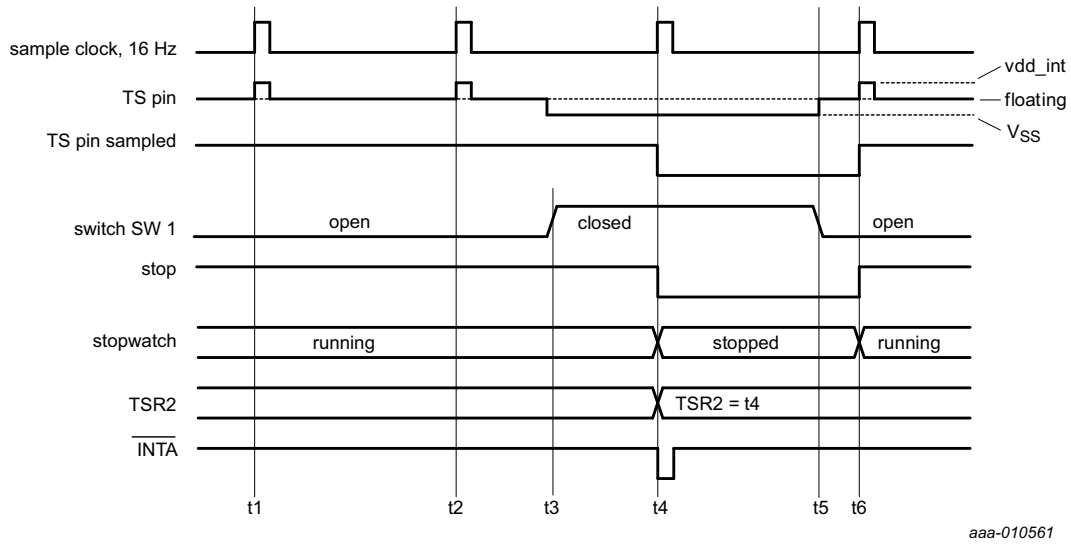


Fig 35. Application example timing

- At and before t1, SW1 is open (TS pin floating). The TS pin is sampled and the internal pull-up resistor will pull the pin HIGH to *vdd_int*. No actions are taken by the IC.
- At t2, SW1 is still open. No action is taken by the IC.
- At t3, SW1 closes. The TS pin is now shorted to V_{SS}. The TS pin has not been sampled yet, so no action is taken by the IC.
- At t4, SW1 is closed. The internal pull-up resistor is enabled, but TS pin remains LOW. The pin is then sampled and the LOW level detected. As the TSL bit was set for active LOW detection, the HIGH-LOW transition of TS pin sampled triggers an event.

  STOPM mode was configured to allow the TS pin to stop the time counting. As the TSL bit was set for active LOW, time counting stops when the TS pin is LOW.

  Timestamp register 2 was configured to take a copy of the time on an event of the TS pin, hence TSR2 loads the time t4. TSR2F is also set.

$\overline{\text{INTA}}$ was configured to generate an interrupt when TSR2 loads a new time, hence an interrupt pulse is seen on $\overline{\text{INTA}}$.

- At t5, SW1 is opened. No action is taken by the IC.
- At t6, SW1 is open. The internal pull-up is active and the TS pin raises to *vdd_int* level. The HIGH level is sampled and causes the *stop* signal to be released and time starts counting again.

12. Internal circuitry

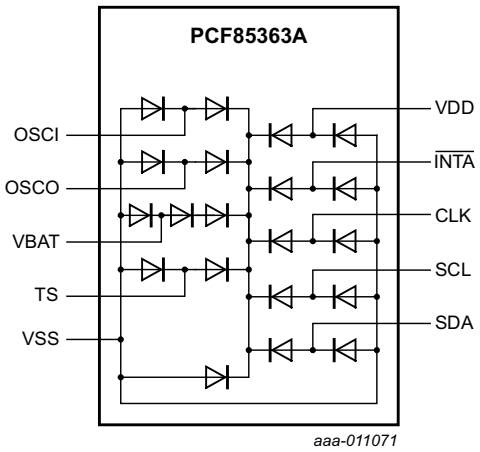


Fig 36. Device diode protection diagram of PCF85363A

13. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

14. Limiting values

Table 67. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.5	V
I_{DD}	supply current		–50	+50	mA
V_{BAT}	battery supply voltage		–0.5	+6.5	V
I_{BAT}	battery supply current		–50	+50	mA
V_I	input voltage	on pins SCL, SDA, OSCI, TS	–0.5	+6.5	V
V_O	output voltage		–0.5	+6.5	V
I_I	input current	at any input	–10	+10	mA
I_O	output current	at any output	–10	+10	mA
P_{tot}	total power dissipation		-	300	mW
V_{ESD}	electrostatic discharge voltage	HBM [1]	-	±3500	V
		CDM [2]			
		PCF85363ATL	-	±1750	V
		PCF85363ATT	-	±1000	V
		PCF85363ATT1	-	±2000	V
I_{lu}	latch-up current	[3]	-	200	mA
T_{stg}	storage temperature	[4]	–65	+150	°C
T_{amb}	ambient temperature	operating device	–40	+85	°C

[1] Pass level; Human Body Model (HBM) according to Ref. 6 “JESD22-A114”.

[2] Pass level; Charged-Device Model (CDM), according to Ref. 7 “JESD22-C101”.

[3] Pass level; latch-up testing, according to Ref. 8 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see Ref. 11 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

15. Characteristics

Table 68. Static characteristics

V_{DD} = 0.9 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 7 pF; all registers in reset state; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage	interface inactive; f_{SCL} = 0 Hz [1]	0.9	-	5.5	V
		interface active; f_{SCL} = 400 kHz [1]	1.8	-	5.5	V
V_{BAT}	battery supply voltage	[1]	0.9	-	5.5	V
I_{DD}	supply current	CLKOUT disabled; V_{DD} = 3.3 V; interface inactive; f_{SCL} = 0 Hz [2]				
		battery switch enabled				
		T_{amb} = 25 °C	-	320	480	nA
		T_{amb} = 50 °C	-	370	550	nA
		T_{amb} = 85 °C	-	590	885	nA
		battery switch disabled [3]				
		T_{amb} = 25 °C	-	280	420	nA
		T_{amb} = 50 °C	-	330	500	nA
		T_{amb} = 85 °C	-	550	825	nA
		CLKOUT disabled; V_{DD} = 3.3 V; interface active; f_{SCL} = 400 kHz	-	10	-	µA
Reference voltage						
V_{th}	threshold voltage	HIGH falling V_{DD}	2.4	2.6	2.8	V
		HIGH rising V_{DD}	2.5	2.7	2.95	V
		LOW falling V_{DD}	1.3	1.4	1.5	V
		LOW rising V_{DD}	1.37	1.47	1.6	V
		reference voltage hysteresis	-	±50	-	mV
Inputs [4]						
V_I	input voltage		V_{SS}	-	5.5	V
V_{IL}	LOW-level input voltage		V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	V_{DD}	V
I_{LI}	input leakage current	V_I = V_{SS} or V_{DD}	-	0	-	µA
		post ESD event	−0.5	-	+0.5	µA
C_i	input capacitance	[5]	-	-	7	pF
$R_{PU(TS)}$	pull-up resistance on pin TS	80 kΩ mode	68	80	92	kΩ
		40 kΩ mode	36	40	64	kΩ

Table 68. Static characteristics *…continued*

V_{DD} = 0.9 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 7 pF; all registers in reset state; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Outputs						
V_{OH}	HIGH-level output voltage	on pin CLK, TS	$0.8V_{DD}$	-	V_{DD}	V
V_{OL}	LOW-level output voltage	on pins SDA, $\overline{INTA}$, CLK, TS	V_{SS}	-	$0.2V_{DD}$	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 2.9 V; V_{DD} = 3.3 V; on pin CLK, TS	1	3	-	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 3.3 V				
		on pin SDA	3	8.5	-	mA
		on pin $\overline{INTA}$	2	6	-	mA
		on pin CLK	1	3	-	mA
		on pin TS	1	3	-	mA
Oscillator						
$\Delta f_{osc}/f_{osc}$	relative oscillator frequency variation	ΔV_{DD} = 200 mV; T_{amb} = 25 °C	-	0.075	-	ppm
t_{jit}	jitter time	LOWJ = 0	-	50	-	ns
		LOWJ = 1	-	25	-	ns
$C_{L(itg)}$	integrated load capacitance	on pins OSCO, OSCI; V_{DD} = 3.3 V [6]				
		C_L = 6 pF	4.8	6	7.2	pF
		C_L = 7 pF	5.6	7	8.4	pF
		C_L = 12.5 pF	10	12.5	15	pF
R_S	series resistance	normal mode	-	-	100	kΩ

[1] For reliable oscillator start-up at power-on: $V_{DD(po)min} = V_{DD(min)} + 0.3$ V.

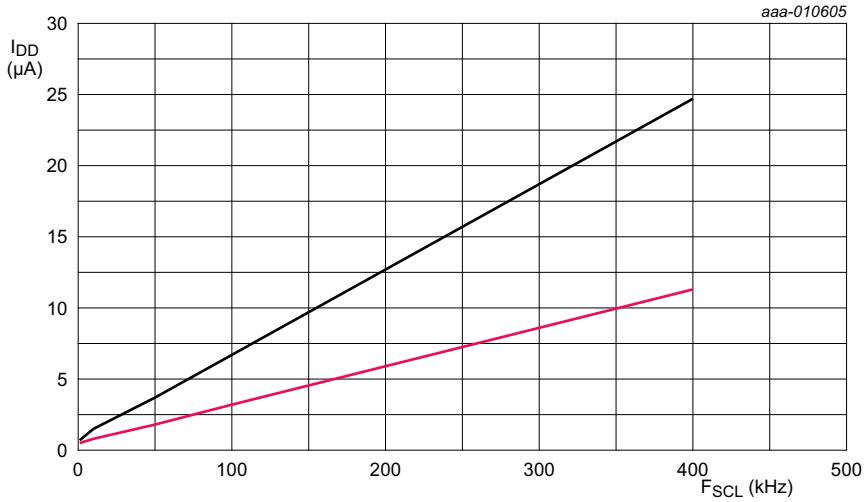
[2] Measured after reset and CLK disabled, level of inputs is V_{DD} or V_{SS}.

[3] Measured after reset, CLK disabled, battery switch disabled and level of inputs is V_{DD} or V_{SS}.

[4] The I²C-bus interface of PCF85363A is 5 V tolerant.

[5] Implicit by design.

[6] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series: $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$.

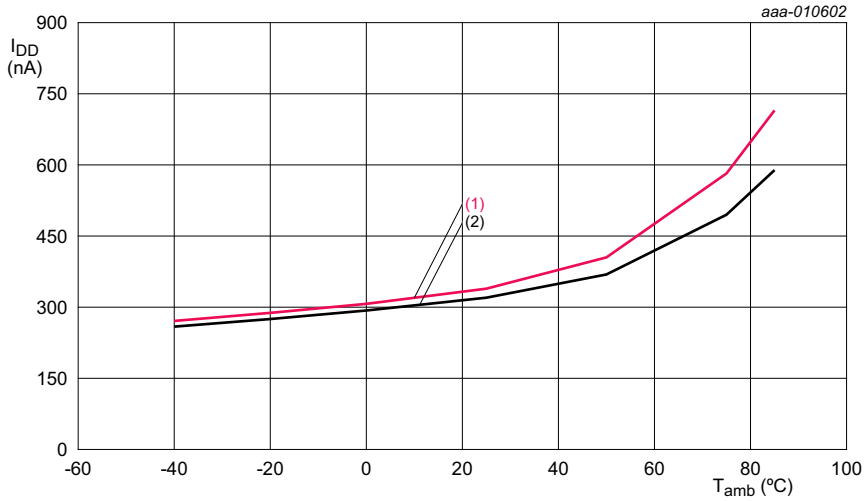


T_{amb} = 25 °C; CLKOUT disabled.

(1) V_{DD} = 5.0 V.

(2) V_{DD} = 3.3 V.

Fig 37. Typical I_{DD} with respect to f_{SCL}

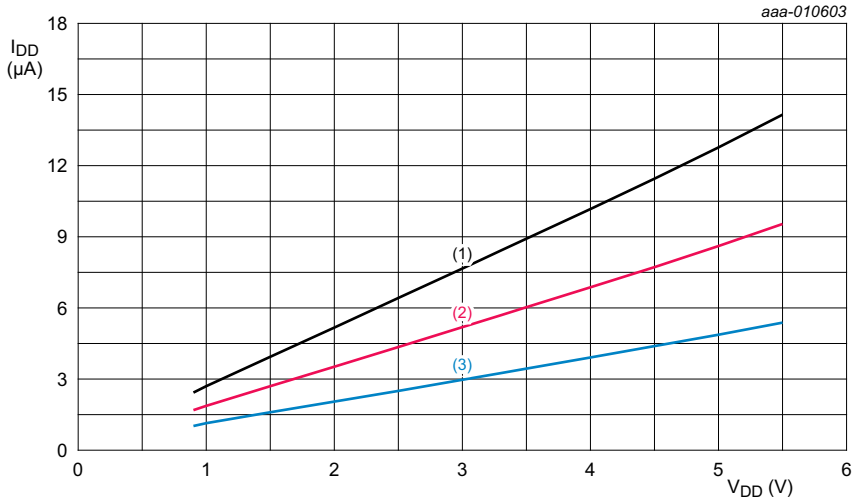


$C_{L(itg)}$ = 7 pF; CLKOUT disabled; battery switched on.

(1) V_{DD} = 5 V.

(2) V_{DD} = 3.3 V.

Fig 38. Typical I_{DD} as a function of temperature

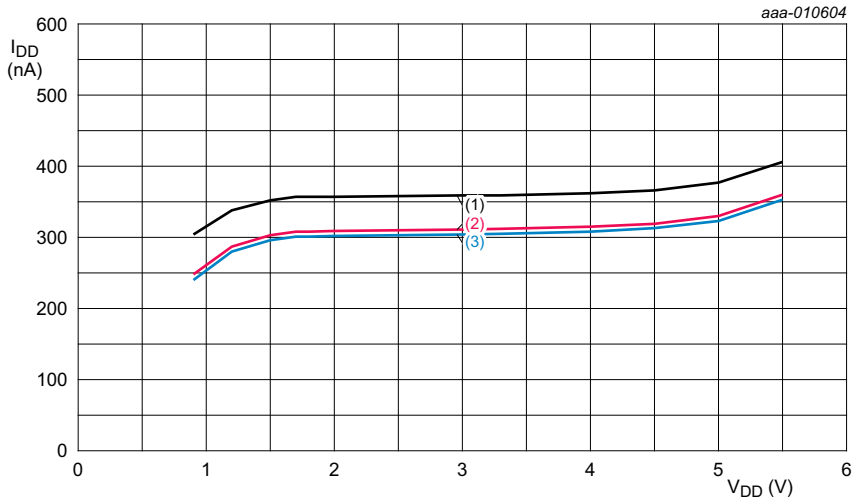


T_{amb} = 25 °C; f_{CLKOUT} = 32768 Hz.

(1) 47 pF CLKOUT load.

(2) 22 pF CLKOUT load.

(3) 0 pF CLKOUT load.



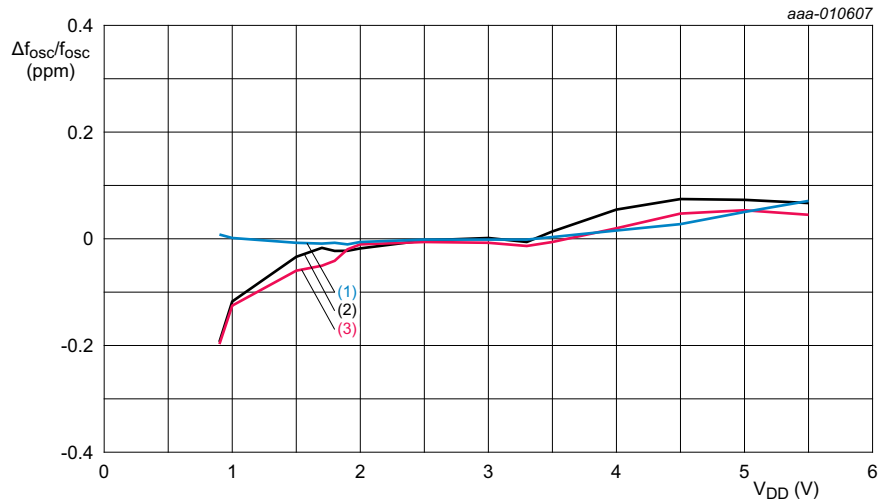
T_{amb} = 25 °C; CLKOUT disabled.

(1) $C_{L(itg)}$ = 12.5 pF.

(2) $C_{L(itg)}$ = 7 pF.

(3) $C_{L(itg)}$ = 6 pF.

Fig 39. Typical I_{DD} with respect to V_{DD}



T_{amb} = 25 °C.

(1) $C_{L(itg)}$ = 12.5 pF.

(2) $C_{L(itg)}$ = 6 pF.

(3) $C_{L(itg)}$ = 7 pF.

Fig 40. Oscillator frequency variation with respect to V_{DD}

Table 69. I²C-bus characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 7 pF; unless otherwise specified. All timing values are valid within the operating supply voltage and temperature range and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}[1].

Symbol	Parameter	Conditions	Min	Max	Unit
C_b	capacitive load for each bus line		-	400	pF
f_{SCL}	SCL clock frequency	[2]	0	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	µs
t_{LOW}	LOW period of the SCL clock		1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	µs
t_r	rise time of both SDA and SCL signals		20	300	ns
t_f	fall time of both SDA and SCL signals	[3][4]	20 × (V_{DD} / 5.5 V)	300	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	µs
$t_{SU;DAT}$	data set-up time		100	-	ns
$t_{HD;DAT}$	data hold time		0	-	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	µs
$t_{VD;DAT}$	data valid time		0	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time		0	0.9	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	50	ns

[1] A detailed description of the I²C-bus specification is given in Ref. 10 “UM10204”.

[2] I²C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

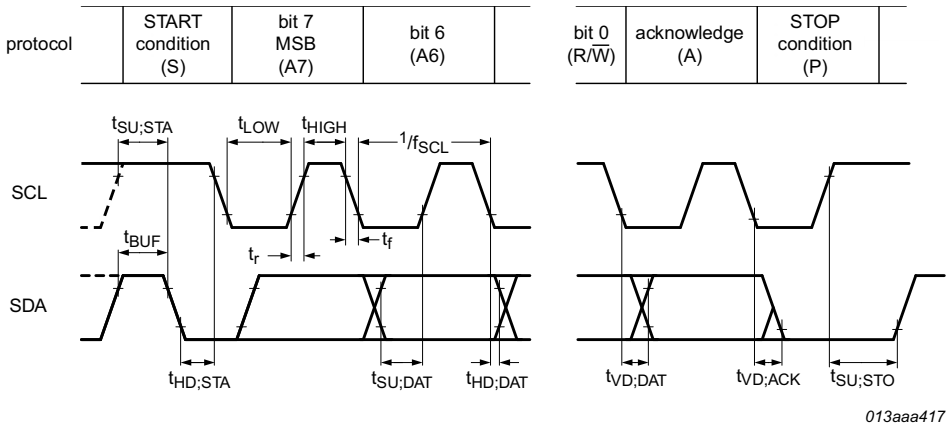


Fig 41. I²C-bus timing diagram; rise and fall times refer to 30 % and 70 %

16. Application information

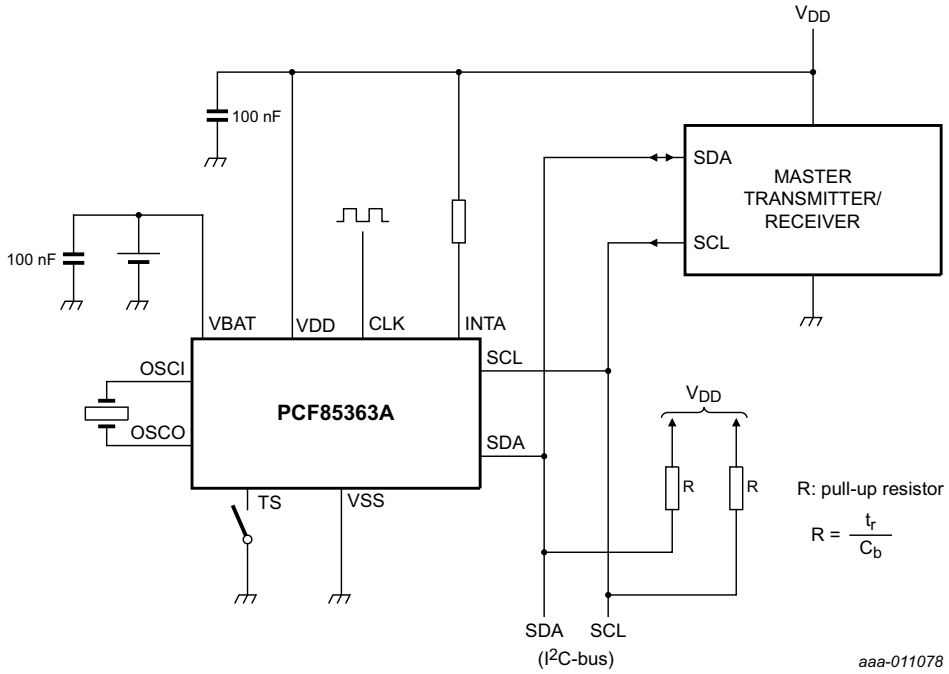


Fig 42. Application diagram for PCF85363A

17. Test information

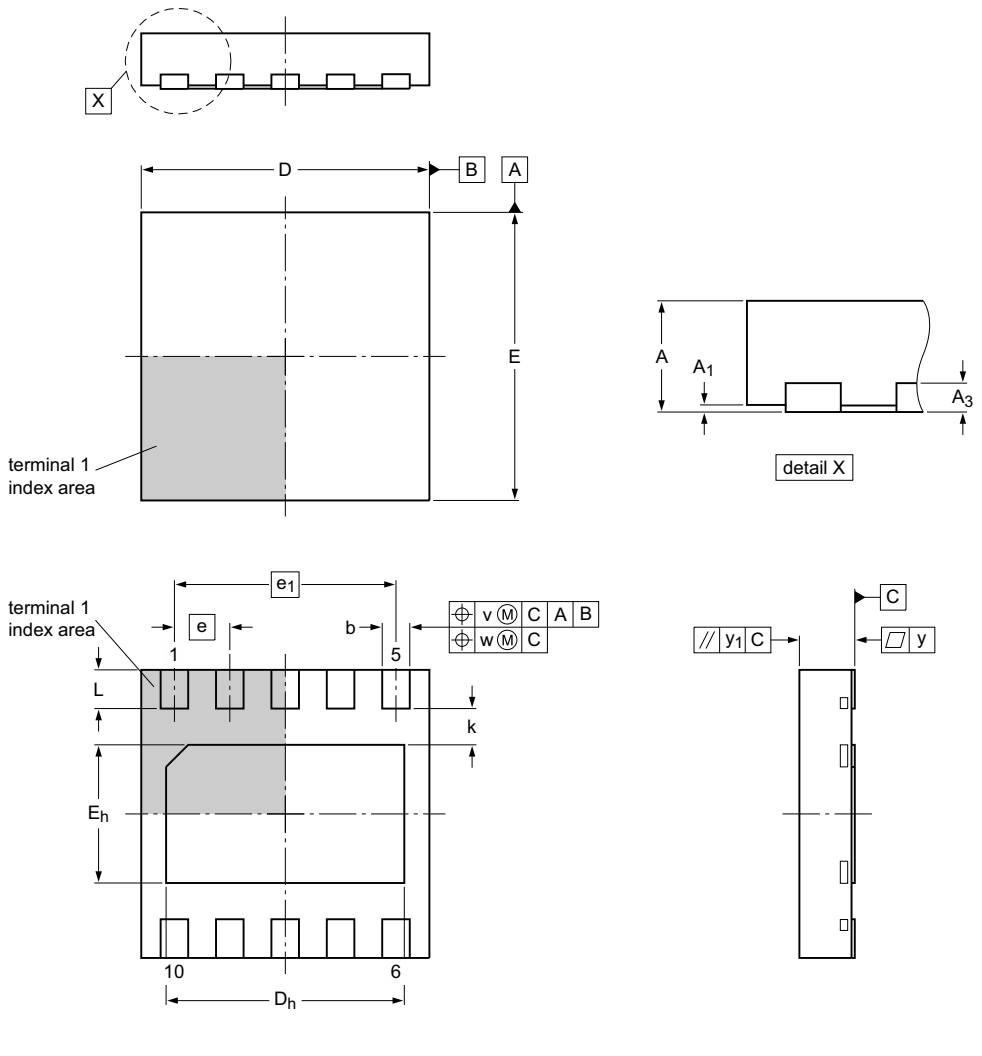
17.1 Quality information

UL Component Recognition

This (component or material) is Recognized by UL. Representative samples of this component have been evaluated by UL and meet applicable UL requirements.

18. Package outline

DFN2626-10: plastic thermal enhanced extremely thin small outline package; no leads; 10 terminals; body 2.6 x 2.6 x 0.5 mm **SOT1197-1**



Dimensions

Unit[1]		A	A_1	A_3	b	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	0.5	0.05		0.30	2.7	2.20	2.7	1.30				0.40				
	nom			0.127	0.25	2.6	2.15	2.6	1.25	0.5	2		0.35	0.1	0.05	0.05	0.05
	min		0.00		0.20	2.5	2.10	2.5	1.20			0.2	0.30				

Note

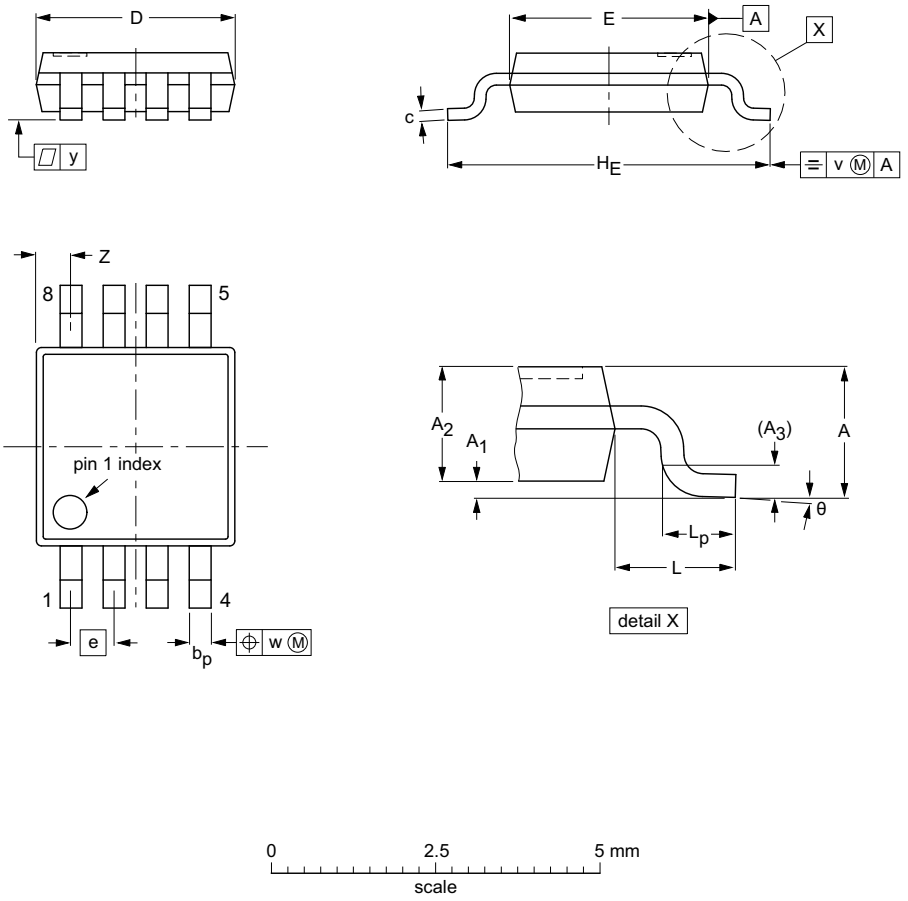
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1197-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1197-1	- - -	- - -	- - -			~~11-01-20~~ 12-09-16

Fig 43. Package outline SOT1197-1 (DFN2626-10), PCF85363ATL

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

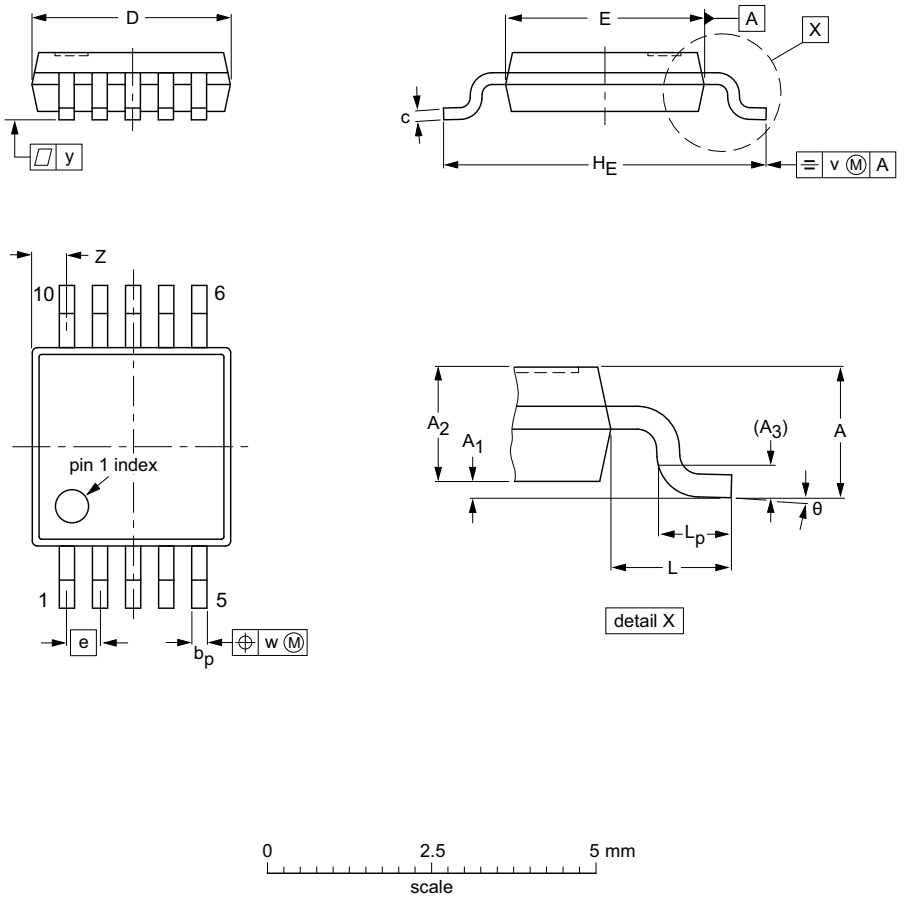
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 44. Package outline SOT505-1 (TSSOP8), PCF85363ATT

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm **SOT552-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.15	0.23 0.15	3.1 2.9	3.1 2.9	0.5	5.0 4.8	0.95	0.7 0.4	0.1	0.1	0.1	0.67 0.34	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT552-1						~~99-07-29~~ 03-02-18

Fig 45. Package outline SOT552-1 (TSSOP10), PCF85363ATT1

19. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

20. Packing information

For tape and reel packing information, please see

- Ref. 12 “SOT505-1_118” on page 88
- Ref. 13 “SOT552-1_118” on page 88
- Ref. 14 “SOT1197-1_115” on page 88

21. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

21.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

21.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias

- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

21.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

21.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 46) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 70 and 71

Table 70. SnPb eutectic process (from J-STD-020D)

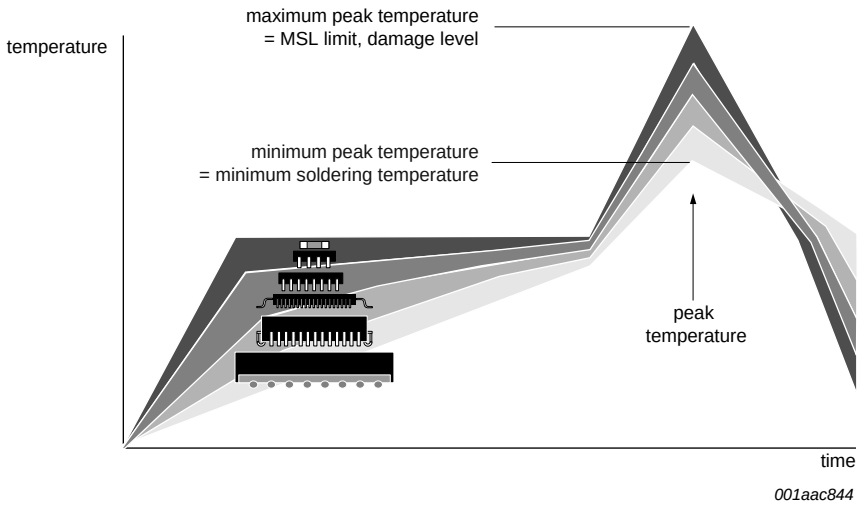
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 71. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 46.



MSL: Moisture Sensitivity Level

Fig 46. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

22. Footprint information

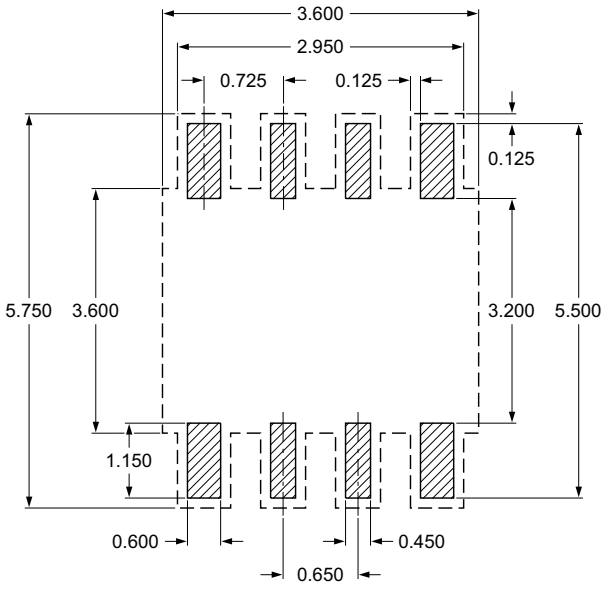
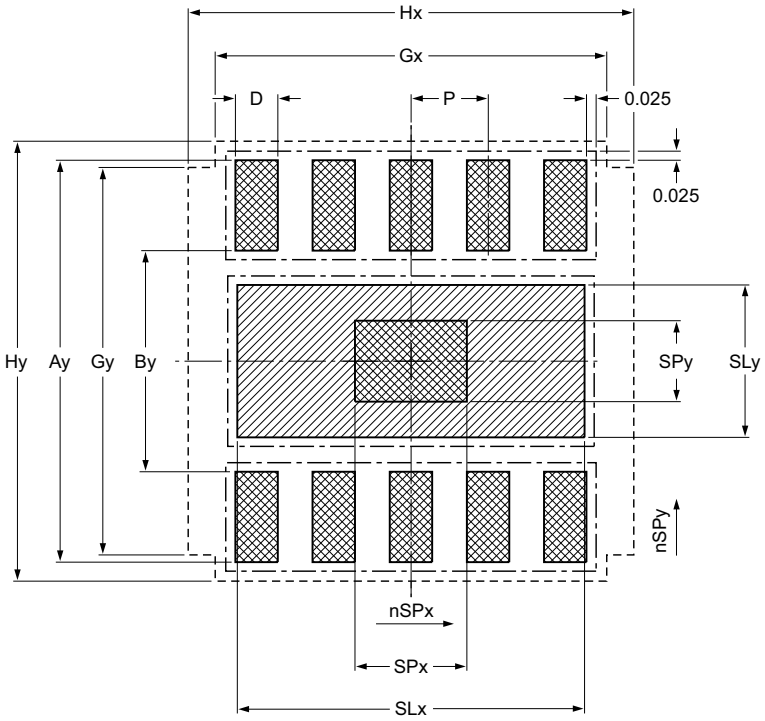


Fig 47. Footprint information for reflow soldering of SOT505-1 (TSSOP8), PCF85363ATT

Footprint information for reflow soldering of DFN2626-10 package **SOT1197-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

solder resist

DIMENSIONS in mm

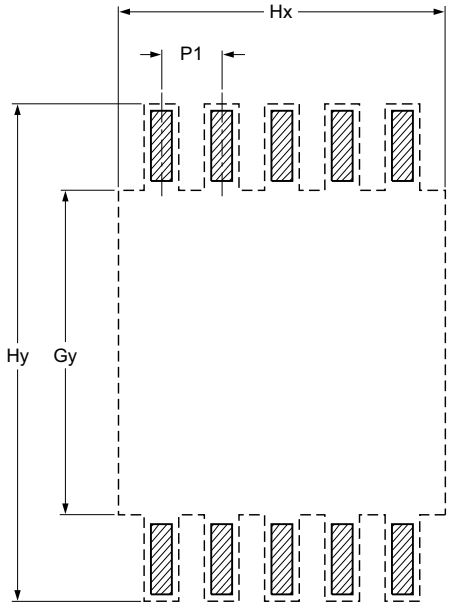
P	Ay	By	D	SLx	SLy	SPx	SPy	Gx	Gy	Hx	Hy
0.5	3.05	1.9	0.25	2.2	1.3	0.8	0.4	2.5	2.85	2.85	3.3

Issue date ~~11-07-27~~ 12-09-16

sot1197-1_fr

Fig 48. Footprint information for reflow soldering of SOT1197-1 (DFN2626-10),PCF85363ATL

Footprint information for reflow soldering of TSSOP10 package **SOT552 -1**



solder land

occupied area

Dimensions in mm

Gy	Hy	Hx	P1
3.1	5.0	3.1	0.5

Issue date ~~11-04-19~~ 13-05-02

sot552-1_fr

Fig 49. Footprint information for reflow soldering of SOT552-1 (TSSOP10), PCF85363ATT1

23. Appendix

23.1 Real-Time Clock selection

Table 72. Selection of Real-Time Clocks

Type name	Alarm, Timer, Watchdog	Interrupt output	Interface	I_{DD}, typical (nA)	Battery backup	Timestamp, tamper input	AEC-Q100 compliant	Special features	Packages
PCF8563	X	1	I²C	250	-	-	-	-	SO8, TSSOP8, HVSON10
PCF8564A	X	1	I²C	250	-	-	-	integrated oscillator caps	WLCSP
PCA8565	X	1	I²C	600	-	-	grade 1	high robustness, T_{amb}= −40 °C to 125 °C	TSSOP8, HVSON10
PCA8565A	X	1	I²C	600	-	-	-	integrated oscillator caps, T_{amb}= −40 °C to 125 °C	WLCSP
PCF85063	-	1	I²C	220	-	-	-	basic functions only, no alarm	HXSON8
PCF85063A	X	1	I²C	220	-	-	-	tiny package	SO8, DFN2626-10
PCF85063B	X	1	SPI	220	-	-	-	tiny package	DFN2626-10
PCF85263A	X	2	I²C	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$ s	SO8, TSSOP10, TSSOP8, DFN2626-10
PCF85263B	X	2	SPI	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$s	TSSOP10, DFN2626-10
PCF85363A	X	2	I²C	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$s, 64 Byte RAM	TSSOP10, DFN2626-10
PCF85363B	X	2	SPI	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$s, 64 Byte RAM	TSSOP10, DFN2626-10
PCF8523	X	2	I²C	150	X	-	-	lowest power 150 nA in operation, FM+ 1 MHz	SO8, HVSON8, TSSOP14, WLCSP
PCF2123	X	1	SPI	100	-	-	-	lowest power 100 nA in operation	TSSOP14, HVQFN16
PCF2127	X	1	I²C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated, 512 Byte RAM	SO16

Table 72. Selection of Real-Time Clocks *...continued*

Type name	Alarm, Timer, Watchdog	Interrupt output	Interface	I_{DD}, typical (nA)	Battery backup	Timestamp, tamper input	AEC-Q100 compliant	Special features	Packages
PCF2127A	X	1	I²C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated, 512 Byte RAM	SO20
PCF2129	X	1	I²C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated	SO16
PCF2129A	X	1	I²C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated	SO20
PCA2129	X	1	I²C and SPI	500	X	X	grade 3	temperature compensated, quartz built in, calibrated	SO16
PCA21125	X	1	SPI	820	-	-	grade 1	high robustness, T_{amb}= −40 °C to 125 °C	TSSOP14

24. Abbreviations

Table 73. Abbreviations

Acronym	Description
BCD	Binary Coded Decimal
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LSB	Least Significant Bit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
POR	Power-On Reset
RTC	Real-Time Clock
SCL	Serial CLock line
SDA	Serial DAta line
SMD	Surface Mount Device

25. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10366 —** HVQFN application information

[3] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[4] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[5] **IPC/JEDEC J-STD-020 —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[6] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **UM10204 —** I^2C-bus specification and user manual

[11] **UM10569 —** Store and transport requirements

[12] **SOT505-1_118 —** TSSOP8; Reel pack; SMD, 13", packing information

[13] **SOT552-1_118 —** TSSOP10; Reel pack; SMD, 13", packing information

[14] **SOT1197-1_115 —** DFN2626-10; Reel pack; SMD, 7", packing information

26. Revision history

Table 74. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF85363A v.2	20150115	Product data sheet	-	PCF85363A v.1
Modifications:	• Corrected Figure 34 • Corrected V_{th} values in Table 68			
PCF85363A v.1	20140710	Product data sheet	-	-

27. Legal information

27.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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