SPECIFICATIONS

P/N: N2P2FF35

Product Name: Camera Module

Date: 2017-02-15

New Concept			
Department	R&D	Quality	Sales
Sign			

Customer			
REMARK			
Date			

Revise History

Rev	Date	Description	Author
V1.0	2017.2.15	Original Version	Johnson

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1. Product Specification

1.1 Specification

This approval sheet contains the general information of N2P2FF35 CMOS camera module. It includes sensor and lens. It contains the key features of the module as well as the information for the reliability test purposes.

1.2 Features

- Pixel Size : 1.75um X 1.75um
- Effective Pixel Array Size : 2,856um X 2,149um
- Resolution : 1,632(H) X 1228(V)
- Chip Size : 3,975um x 3,450um
- Optical Format : 1/5inch
- Frame Rate : 30fps@1632x1228, 60fps@816 x614
- Power Supply : 2.8V for analog, 2.8V or 1.8V for IO, 1.8V for digital core.
- Power Consumption : 132mW
- ADC : 10bit
- PLL : On Chip
- Operation Temperature : -20 ~ 60°C
- Master Clock : 48MHz(max)
- Host Interface : Two-wire serial bus interface
- Output Format : Raw8/10bit
- MIPI : Single lane @ 720Mbps
- Windowing & Crop : Programmable
- Image Flip : X/Y FLIP
- Black Level calibration
- Built-in Test Pattern Generator

1.3 Applications

mobile phone camera
digital still camera products.

2. General Description

2.1 Camera Module Basic Specification

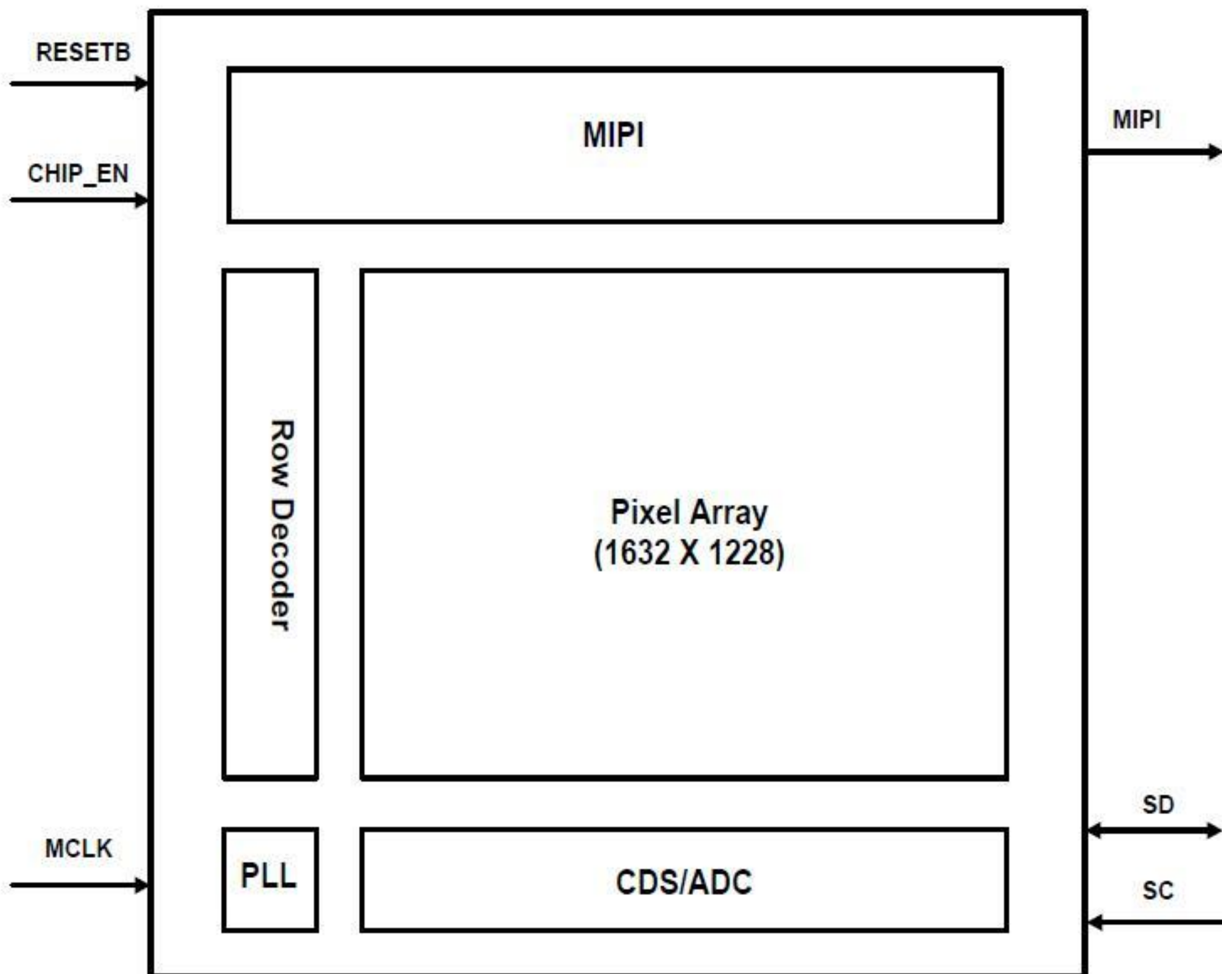
NO	ITEM	SPECIFICATION	Remark
1	Type	Camera Module	
2	Model Name	N2P2FF35	
3	Resolution	1600H×1200V Pixels	2-megapixel
4	Sensor	1/5″ CMOS Sensor	Hi-259
5	Unit Pixel Size	1.75um×1.75um	
6	Output format	RAW 10-bit RGB	
7	Max frame rate	UXGA:30fps@672Mbps；720P：30fps@480Mbps	
8	Supply voltage	AVDD:2.7~3.0V;DVDD:1.7~1.9V;DOVDD1.7~3.0V	
9	Number of output	MIPI	1-lanes
10	Lens Type	FF	XY-2006AG
11	View angle	68°	
12	Temperature Range	Operating -20°C to 70°C；Stable image 0°C to 50°C	
17	Module head size	6.5(W)mmx6.5(L)mmx3.75(H)mm	
18	Connection mode	金手指25pin	FH26-25S-0.3SHW
19	Focal Length	2.6mm	
20	Resolution	Central area≥800LW/PH； Oblique 45 degree angle≥700LW/PH	

2.2 Camera Lens Specification

NO	ITEM	SPECIFICATION	Remark
1	Lens size	1/5inch	
2	Lens Construction	3P+IR FILTER	
3	Focal Length	2.187mm	
4	F/NO.	2.8±5%	
5	Field of View Angle (Diagonal)	78.4°	
6	TV Distortion	＜1.5%	

2.3 Camera Module Sensor Electrical Specification

2.3.1 Block Diagram



2.3.2 Absolute Maximum Ratings

Item	Symbol	Min	Max	Note
Digital Core & PLL	$V_{DD:PLL}$ & $V_{DD:D}$	-0.3V	2.1V	5, 6
Analog Power	$V_{DD:A}$	-0.3V	3.3V	5
Digital I/O Power	$V_{DD:I}$	-0.3V	3.3V	5
Input Pin Voltage	V_{IN}	-0.2V	$V_{DD:I}$ + 0.2V	5
Output Pin Voltage	V_{OUT}	-0.2V	$V_{DD:I}$ + 0.2V	5

Note5) Exposure to absolute maximum rating conditions for extended periods may affect reliability.
Note6) $V_{DD:PLL}$ should be supplied by $V_{DD:D}$ power

2.3.3 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Note
Digital Core Circuit and PLL Power Supply Voltage	$V_{DD:D}$, $V_{DD:PLL}$	1.7	1.8	1.9	V	
Analog Circuit Power Supply Voltage	$V_{DD:A}$	2.7	2.8	3.0	V	
Digital I/O Circuit Power Supply Voltage	$V_{DD:I}$	1.7	1.8 / 2.8	3.0	V	
H level Input Voltage	V_{IH}	0.7 * $V_{DD:I}$			V	
L level Input Voltage	V_{IL}			0.3 * $V_{DD:I}$	V	
MCLK Rising & falling time			6.5	7.15	nS	1
MCLK jitter		23.52	24	24.48	Mhz	

Note1) Based on 24Mhz(20~80%)

2.3.4 AC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Note
MCLK	Frequency	6		48	MHz	
MCLK	Duty Cycle	45	50	55	%	
SC	Frequency			400	KHz	

2.3.5 Power Consumption for MIPI

Item	Condition	Min	Typ	Max	Unit	Note
1632x1228 @ 30fps	$V_{DD:A}$ = 2.8V		18	27	mA	2
	$V_{DD:I}$ = 1.8V		0.1	0.15	mA	3
	$V_{DD:PLL}$ & $V_{DD:D}$ = 1.8V		45	68	mA	
Stand by Current				300	uA	4

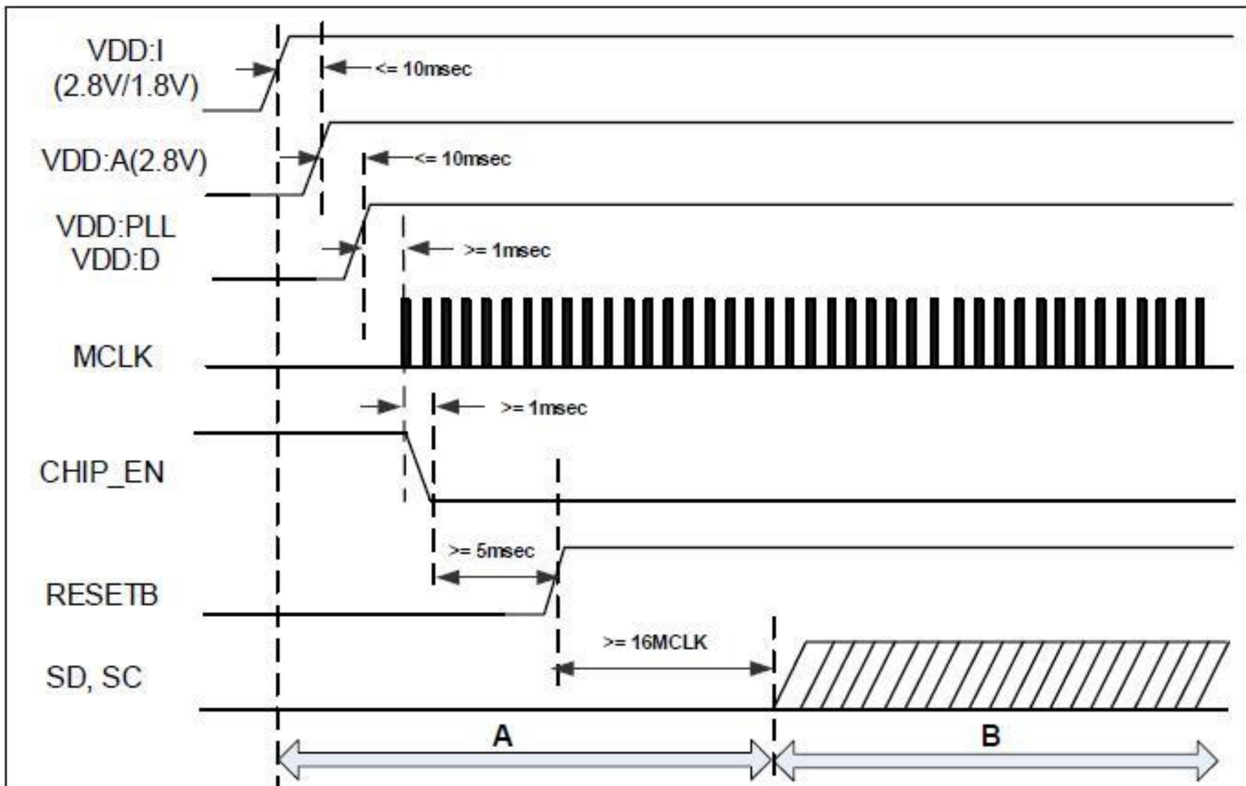
Note2) Because current of analog circuit depends on the registers' values, it is measured at specific register's value.
Note3) Because power consumption of $V_{DD:I}$ depends on the output load and system environment, user should supply enough current to sensor for stable operation. It is measured when output load is floated.
Note4) Stand by current is measured at CHIP_EN = HIGH(CEN_OPT=LO) and MCLK = LO.

We recommend that power should be turned off, when low standby power consumption is required.

2.3.6 Power on sequence
(Chip Enable Active Low)

VDD:A(ON) → VDD:D(ON) → MCLK(ON) → CHIP_EN(OFF) → RESETB(ON) → Set Software reset register (Toggle bit[1] of PWRCTL[0x01:P0] : Low → Hi → Low) → Set registers for normal operation → Normal Operation

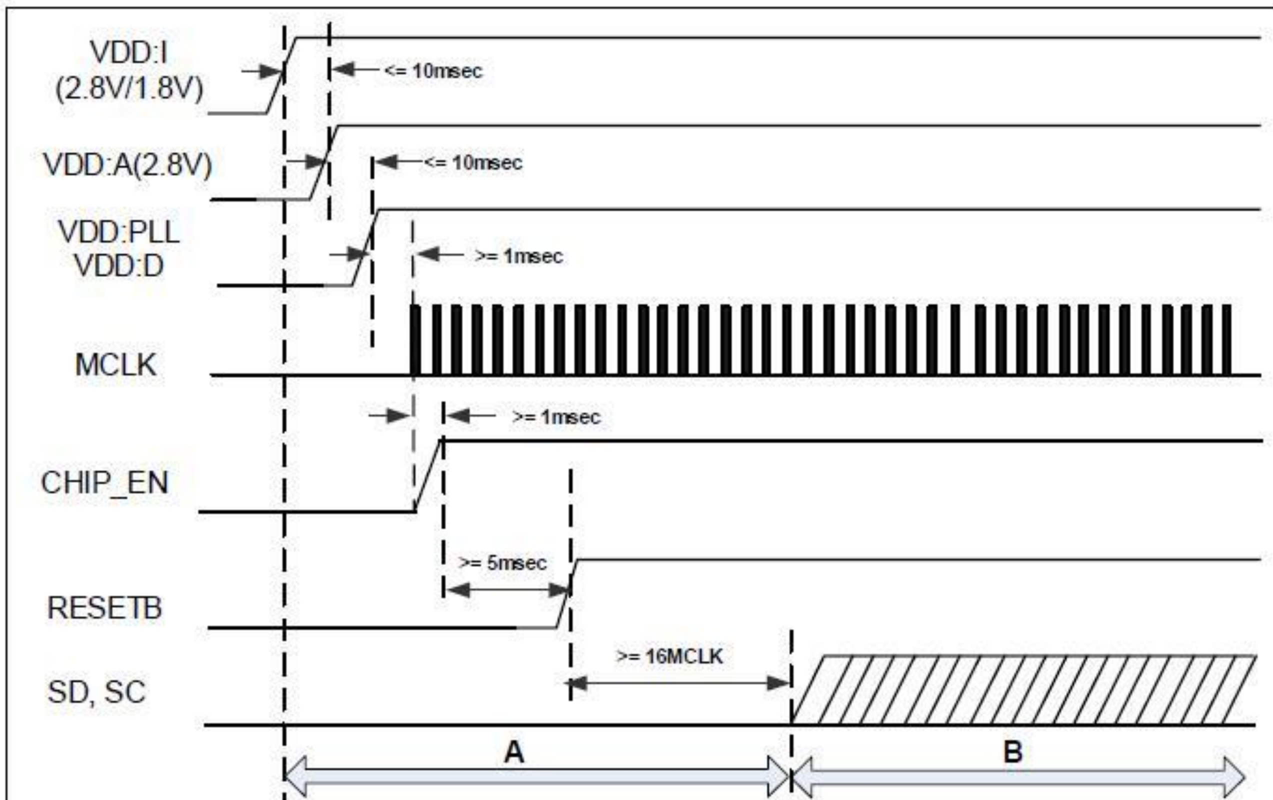
If possible, we recommend that $V_{DD:A}$ and $V_{DD:D}$ are supplied at same time.
If the power sequence of $V_{DD:I}$ and $V_{DD:A}$ are separated, $V_{DD:I}$ should be supplied firstly.



(Chip Enable Active High)

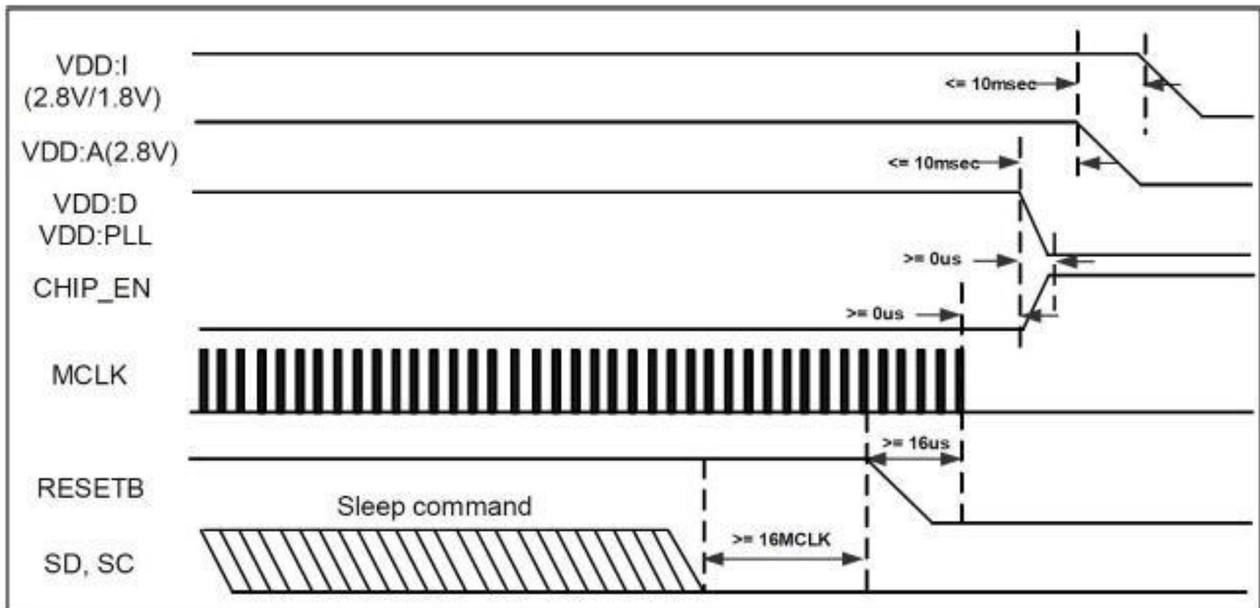
VDD:A(ON) → VDD:D(ON) → MCLK(ON) → CHIP_EN(ON) → RESETB(ON) → Set Software reset register (Toggle bit[1] of PWRCTL[0x01:P0] : Low → Hi → Low) → Set registers for normal operation → Normal Operation

If possible, we recommend that $V_{DD:A}$ and $V_{DD:D}$ are supplied at same time.
If the power sequence of $V_{DD:I}$ and $V_{DD:A}$ are separated, $V_{DD:I}$ should be supplied firstly.



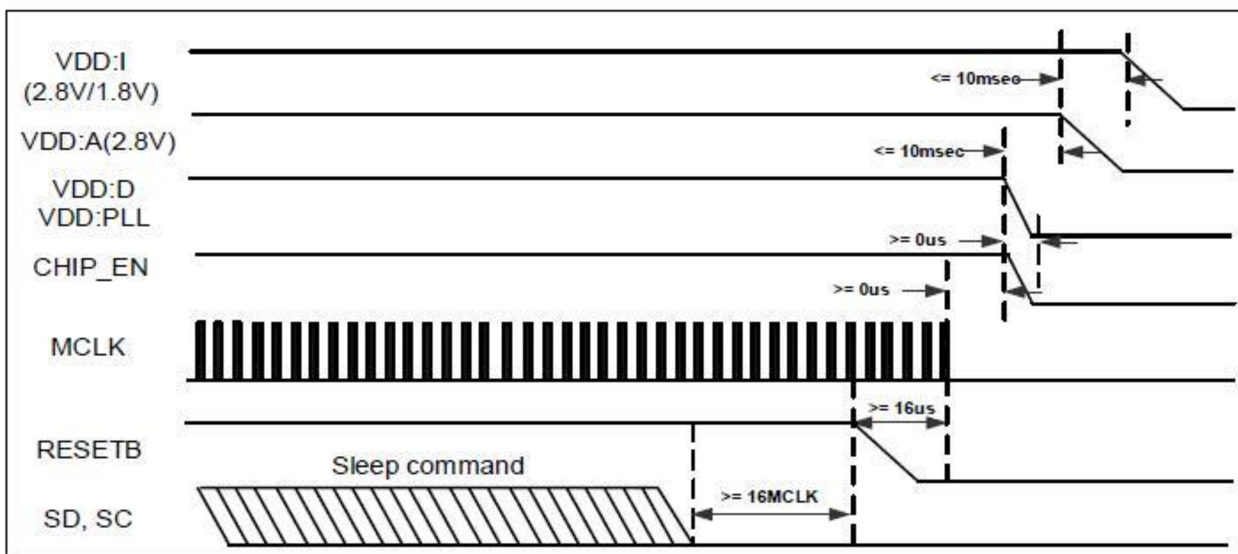
2.3.7 Power off sequence
(Chip Enable Active Low)

Normal Operation → Power Sleep command and disable PLL → SC, SD (OFF) → RESETB(OFF) → MCLK (OFF) → CHIP_EN(ON) → VDD:D (OFF) → VDD:A (OFF) → VDD:I (OFF)



(Chip Enable Active High)

Normal Operation → Power Sleep command and disable PLL → SC, SD (OFF) → RESETB(OFF) → MCLK (OFF) → CHIP_EN(OFF) → VDD:D (OFF) → VDD:A (OFF) → VDD:I (OFF)

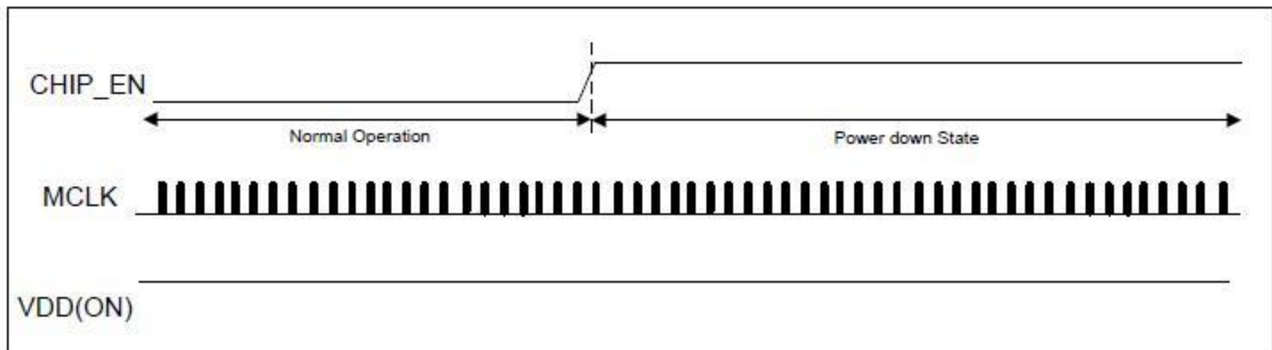


2.3.8 standby sequence
(Chip Enable Active Low)

From Normal Operation State to Stand-by(Power down) State

Before CHIP_EN is disabled(Low state), following registers should be set.

Step 1) Set the software reset register (PWRCTL[0x01:P0] : 0x01 → 0x03 → 0x01)
Step 2) Set PLLCTL1[0x07:P0] to 0x00
Step 3) Set PWCTL1[0x3D:P2] to 0x00



From Stand-by(Power down) State to Normal Operation State

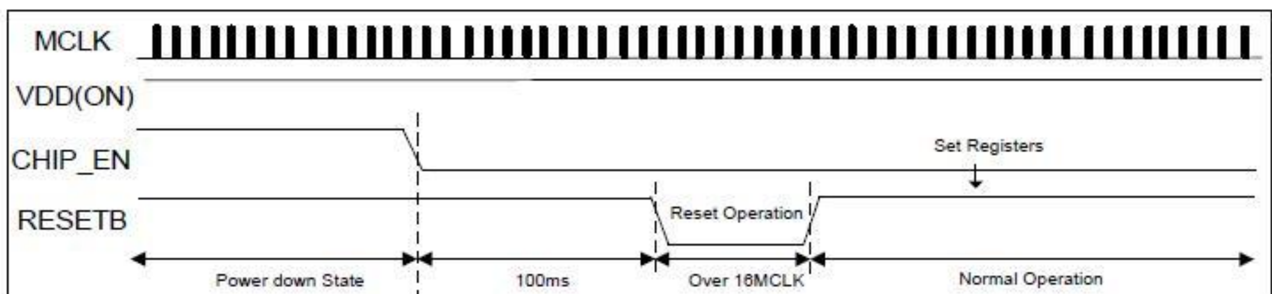
Step 1) Set CHIP_EN to Low

Step 2) Wait 100ms

Step 3) Toggle RESETB Hi → Low → Hi

Step 4) Set the software reset register(Toggle PWRCTL[0x01:P0]'s B[1] : Low → Hi → Low)

Step 5) Set the registers for normal operation

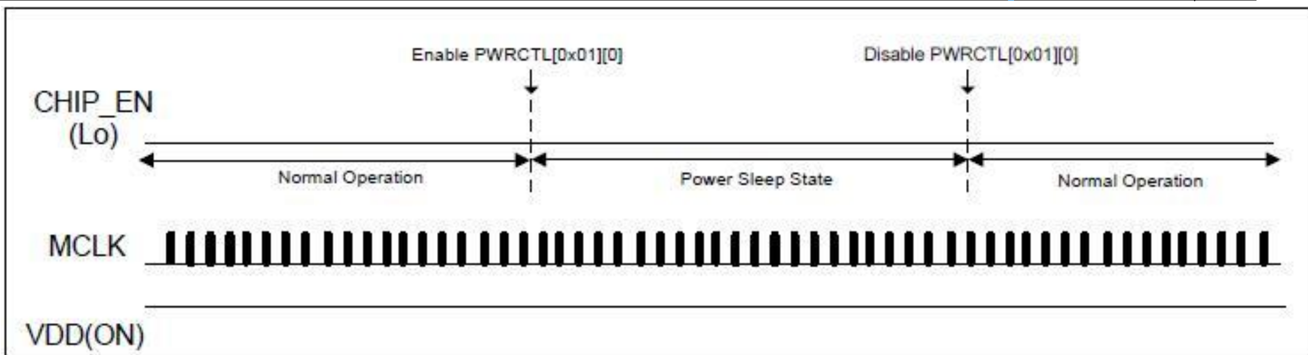


From Normal Operation State to Power Sleep State

Set PWLCTL[0x01:P0]'s B[0] to high and disable PLL

From Power Sleep State to Normal Operation State

Set PWLCTL[0x01:P0]'s B[0] to low

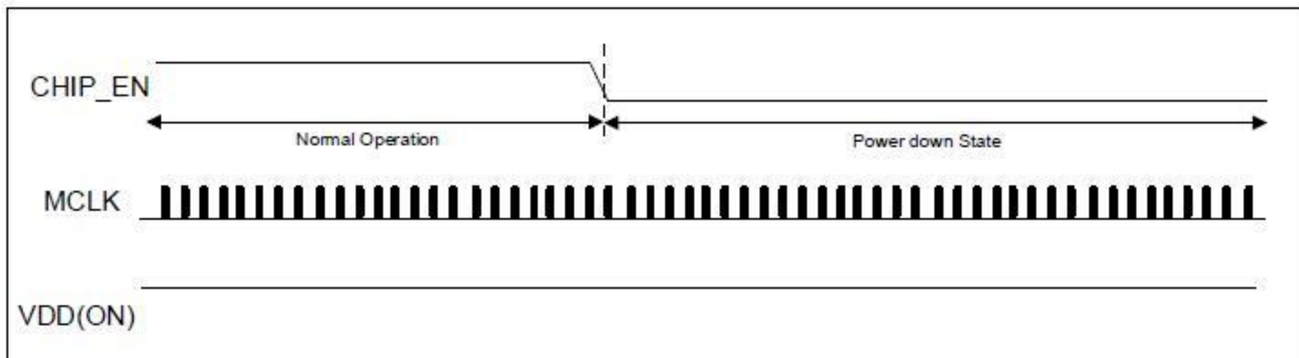


(Chip Enable Active High)

From Normal Operation State to Stand-by(Power down) State

Before CHIP_EN is disabled(Hi state), following registers should be set.

Step 1) Set the software reset register (PWRCTL[0x01:P0] : 0x01 → 0x03 → 0x01)
Step 2) Set PLLCTL1[0x07:P0] to 0x00
Step 3) Set PWCTL1[0x3D:P2] to 0x00



From Stand-by(Power down) State to Normal Operation State

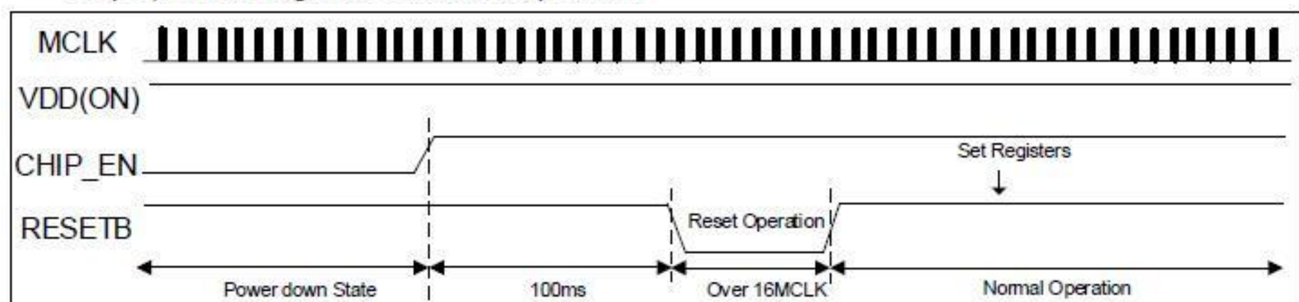
Step 1) Set CHIP_EN to Hi

Step 2) Wait 100ms

Step 3) Toggle RESETB Hi → Low → Hi

Step 4) Set the software reset register(Toggle PWRCTL[0x01:P0]'s B[1] : Low → Hi → Low)

Step 5) Set the registers for normal operation

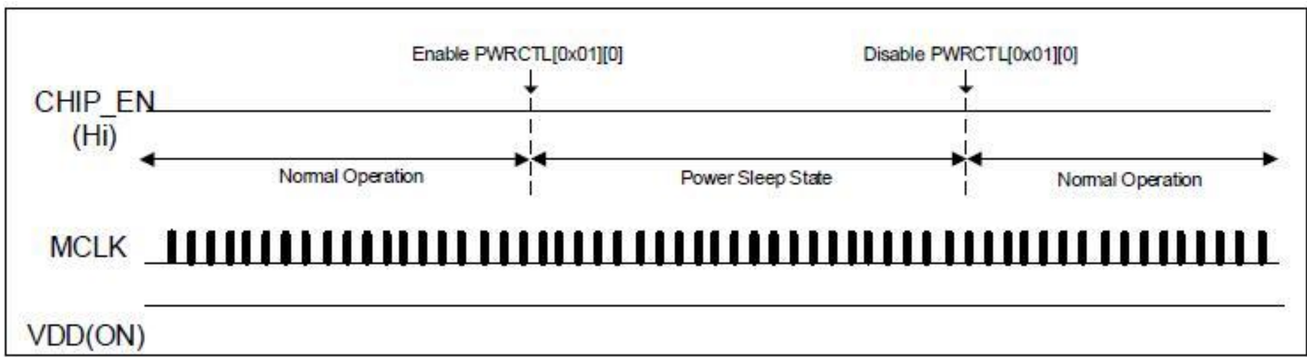


From Normal Operation State to Power Sleep State

Set PWLCTL[0x01:P0]'s B[0] to high and disable PLL

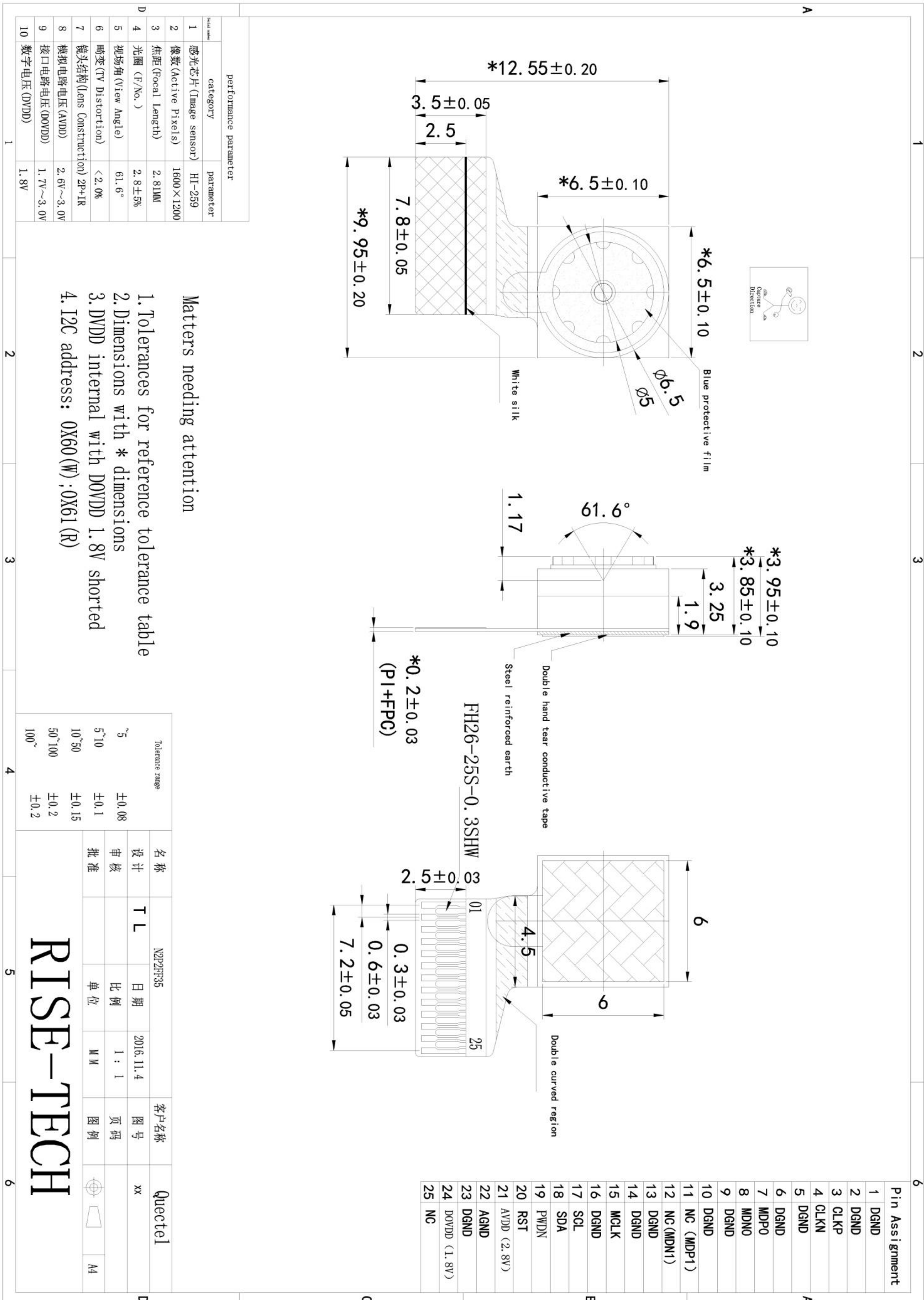
From Power Sleep State to Normal Operation State

Set PWLCTL[0x01:P0]'s B[0] to low


Enable PWRCTL[0x01][0]
Disable PWRCTL[0x01][0]
CHIP_EN
(Hi)
Normal Operation
Power Sleep State
Normal Operation
MCLK
VDD(ON)

3. Module Mechanical Drawing

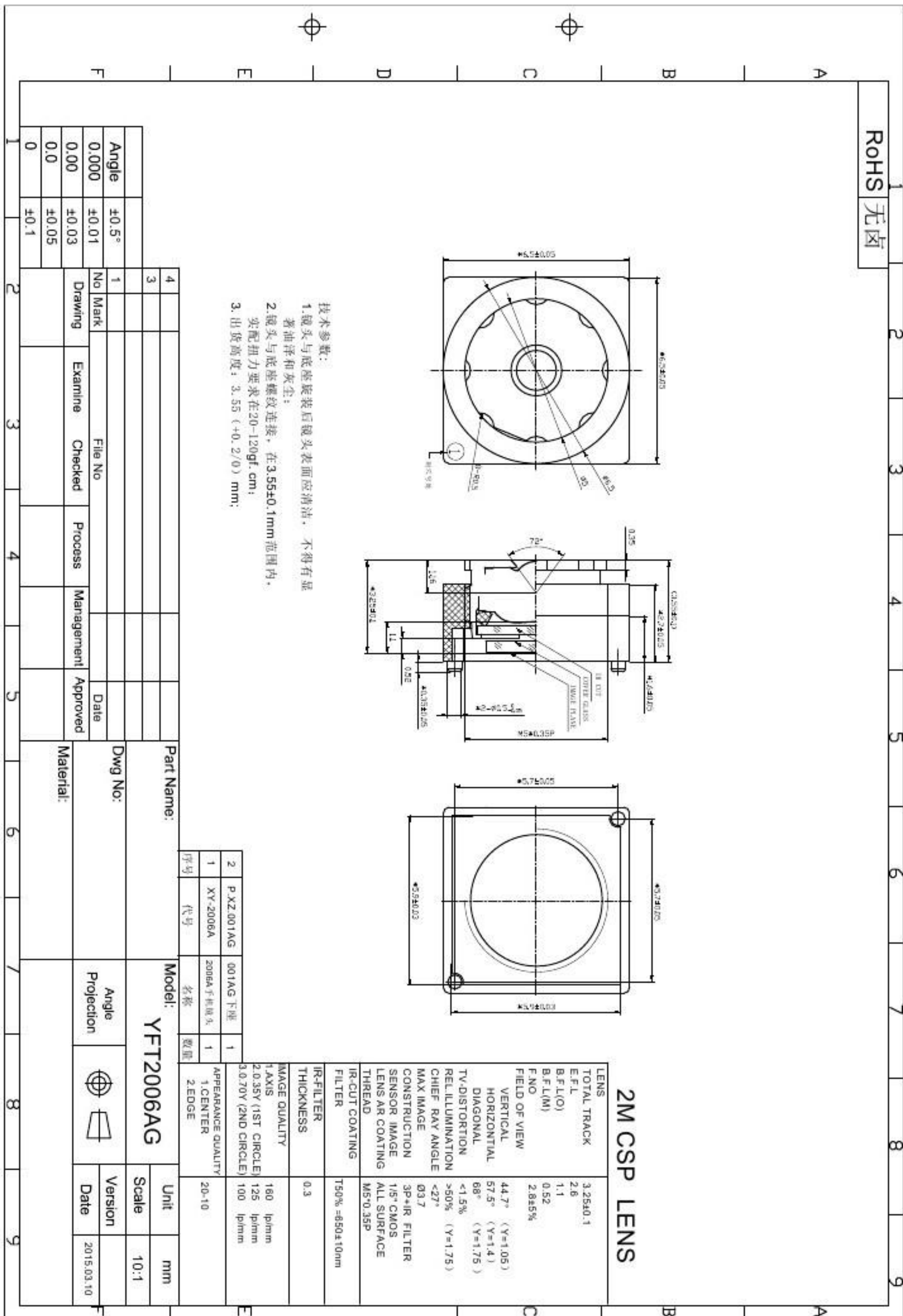
3.1 Module Picture



3.2 Pin Definition

Pin Number	Name	Pin Type	Function/ Description
1	DGND	Ground	Digital ground
2	DGND	Ground	Digital ground
3	MCP	Output	MIPI TX clock lane positive output
4	MCN	Output	MIPI TX clock lane negative output
5	DGND	Ground	Digital ground
6	DGND	Ground	Digital ground
7	MDP0	Output	MIPI TX first data lane positive output
8	MDN0	Output	MIPI TX first data lane negative output
9	DGND	Ground	Digital ground
10	DGND	Ground	Digital ground
11	NC		
12	NC		
13	DGND	Ground	Digital ground
14	DGND	Ground	Digital ground
15	MCLK	Input	Sensor Master Clock
16	DGND	Ground	Digital ground
17	SLC	Input	SCCB serial interface clock input
18	SDA	I/O	SCCB serial interface data I/O
19	PWDN	Input	XSHUTDOWN Signal
20	RESET	Input	RESETB initializes sensor. Active Low
21	AVDD2.8V	Power	Analog power supply(VDD =2.8V)
22	AGND	Ground	Analog ground
23	DGND	Ground	Digital ground
24	DOVDD1.8V	Power	Digital power supply (VDD-IO= 1.8 V) for I/O
25	NC		

3.3 Lens drawing



4. Reliability Test Items and Criteria

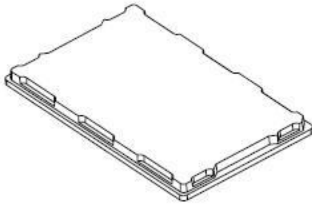
NO	Test item	Test condition	Test Qty'	Judgment standard
1	Low temperature storage test	Temperature: -40℃ Duration: 96hrs	5	Module normal work / image test standard
2	High Temperature Storage Test	Temperature: 80℃ Duration: 96hrs	5	Module normal work / image test standard
3	High Temperature / Humidity Storage Test	Temperature: 60℃ Humidity: 95%RH Duration: 96hrs	5	Module normal work / image test standard
4	High Temperature / Humidity operation Test	Temperature: 60℃ Humidity: 90%RH Duration: 48hrs operation	5	Module normal work / image test standard
5	Thermal Shock Test	Temperature:-40°C± 3 ℃ (45min)~85°C ± 3 ℃(45min) Chang time≦15sec; Totally 24cycles	5	Module normal work / image test standard
6	High temp operation	Temperature: 70℃ Duration: 48hrs operation	5	Module normal work / image test standard
7	Low temp operation	Temperature: -20℃ Duration: 48hrs Max Work Voltage	5	Module normal work / image test standard
8	28Days humidity &high temp Test（By Phone）	Temp：50±2℃，Humidity：95%(+2%/-3%)，Time：28Days，check it per 2days	5	Module normal work / image test standard
9	28Days temp cycle Tes	1.25±2℃ last 6Hr 2.Follow this cycle 3times and per cycle 6Hr： - From +25±2℃ to +55±2℃ in 30 minutes, then last 2Hr at +55±2℃; - From +55±2℃ to -20±3℃ in 1Hr, then last 2Hr at -20±3℃; - From -20±3℃ to +25±2℃ in 30minutes;	5	Module normal work / image test standard
10	Module Vibration test	Frequency Range:10-55-10Hz;Amplitude:2mm;TestAxies(X,Y,Z);Duration:30min for Each Axis	5	Module normal work / image test standard
11	ESD test	6KV Contact Discharge;10KV Air Discharge;10 time,1time/Second Or Follow supplier spec	5	Module normal work / image test standard
12	Drop Test	a.150cm high drop, 4 corners, 6 planes; 2 cycles;(performed with 100g weight jig, free drop), Marble ground b.150cm high drop, 4 corners, 6 planes; 2 cycles, Marble ground	5	Module normal work / image test standard

13	Pressure Test	Surface pressure: FF 5kgf,AF 8kgf; Point Pressure: 2kgf; Pressure Head speed: 10mm/min; Pressure Head size: surface Jig > Camera surface, point Jig=Φ1mm; Pressure Positon: Jig center and camera aline;	5	Module normal work / image test standard
14	FPC Bending Test	Place the 1mm metal rod in the bending position up and down, bending FPC +/-90 degrees or +/-180 Degree, 50 times. (The bending position is defined according to the project design and material)	5	Module normal work / image test standard
15	FPC/BTB Conn	20 times	5	Module normal work /
16	Packaging drop test	Follow supplier spec	5	Module normal work / image test standard
17	Packaging vibration test	Follow supplier spec	5	Module normal work / image test standard

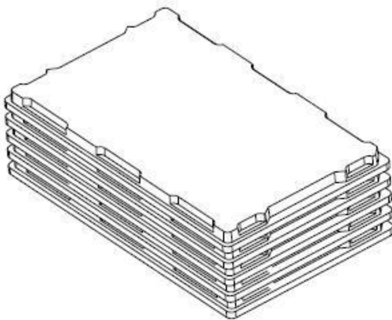
5. Packaging Information

1. Every module is placed into a tray until all empty slots of a tray are filled.
2. Each tray use an anti-static bag to prevent the module from moisture by partially socking out the air from the stack.
3. A stack have 10 trays.
4. Insert a stack into a inner box.
5. Insert two inner boxes into a outside box. Then attach the label onto the outside box.

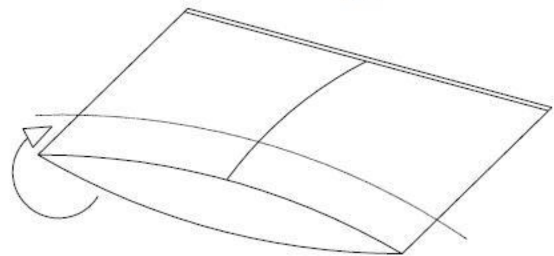
Put the product into the tray



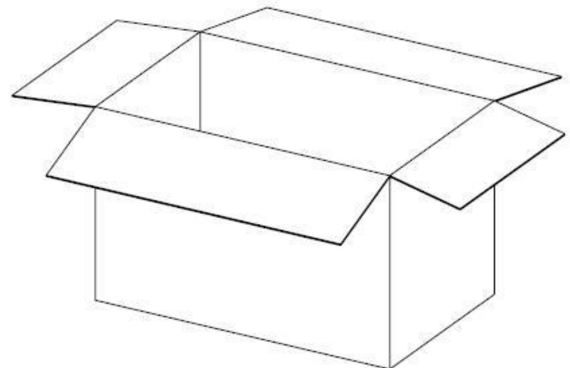
Pallet stack, top cover



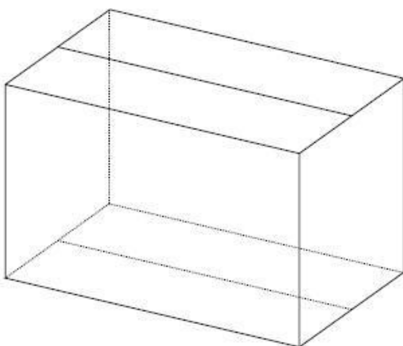
Vacuum anti-static bag (GP standard)



Packing



Pack and label



6. Storage and Operating Conditions

To keep the product and packaging material in good condition, care must be taken to control temperature and humidity in the storage area.

Recommended conditions:

Ambient temperature: 0～+40℃

Humidity: 30～70%RH

No rapid change on temperature and humidity.
The products listed in this catalog are not designed for use under the following conditions.
Storage and/or usage under following conditions is prohibited.
1). Exposure to corrosive gas such as chlorine, hydrogen sulfide, ammonia, sulfur dioxide,nitrogen oxide, etc.
2). Exposure to direct sunlight.
3). Exposure to dust.
4). Exposure to excessive moisture or wet locations.
5). Exposure to salt water or sea breezes.
6). Exposure to strong static electricity or electromagnetic waves.

7. Transportation and Handling

1). Minimize any mechanical vibration or shock and avoid dropping of the product during transportation or dropping the product that contains the substrate.
2). Since the application of static electricity or over voltage may cause defect in the product or deterioration of its reliability, caution must be taken against exposure to any static electricity generated by electrified items such as workbenches, soldering irons, tools,carrying containers, etc.
3). Caution shall be taken to avoid overstress to the product.