FUJITSU SEMICONDUCTOR
DATA SHEET

DS702-00010-3v0-E

*8-bit Microcontrollers*

# New 8FX MB95560H/570H/580H Series

## MB95F562H/F562K/F563H/F563K/F564H/F564K
## MB95F572H/F572K/F573H/F573K/F574H/F574K
## MB95F582H/F582K/F583H/F583K/F584H/F584K

## ■ DESCRIPTION

The MB95560H/570H/580H Series are three series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of these series contain a variety of peripheral resources.

## ■ FEATURES

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instructions
  - Bit manipulation instructions, etc.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

- Clock (The main oscillation clock and the suboscillation clock are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.)
  - Selectable main clock source
    Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
    External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
    Main CR clock (4 MHz ± 2%)
    The main CR clock frequency becomes 8 MHz when the PLL multiplier is 2.
    The main CR clock frequency becomes 10 MHz when the PLL multiplier is 2.5.
    The main CR clock frequency becomes 12 MHz when the PLL multiplier is 3.
    The main CR clock frequency becomes 16 MHz when the PLL multiplier is 4.
  - Selectable subclock source
    Suboscillation clock (32.768 kHz)
    External clock (32.768 kHz)
    Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)
- Timer
  - 8/16-bit composite timer × 2 channels (only one channel on MB95F572H/F572K/F573H/F573K/F574H/F574K)
  - Time-base timer × 1 channel
  - Watch prescaler × 1 channel

*(Continued)*

For the information for microcontroller supports, see the following website.

http://edevice.fujitsu.com/micom/en-support/


2011.12

FUJITSU

*(Continued)*

- LIN-UART (only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K)
  - Full duplex double buffer
  - Capable of clock-synchronized serial data transfer and clock-asynchronized serial data transfer
- External interrupt
  - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
  - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter
  - 8-bit or 10-bit resolution can be selected.
- Low power consumption (standby) modes

  There are four standby modes as follows:
  - Stop mode
  - Sleep mode
  - Watch mode
  - Time-base timer mode

  In standby mode, the device can be made to enter either normal standby mode or deep standby mode.
- I/O port
  - MB95F562H/F563H/F564H (maximum no. of I/O ports: 16)
    General-purpose I/O ports (N-ch open drain) : 1
    General-purpose I/O ports (CMOS I/O) : 15
  - MB95F562K/F563K/F564K (maximum no. of I/O ports: 17)
    General-purpose I/O ports (N-ch open drain) : 2
    General-purpose I/O ports (CMOS I/O) : 15
  - MB95F572H/F573H/F574H (maximum no. of I/O ports: 4)
    General-purpose I/O ports (N-ch open drain) : 1
    General-purpose I/O ports (CMOS I/O) : 3
  - MB95F572K/F573K/F574K (maximum no. of I/O ports: 5)
    General-purpose I/O ports (N-ch open drain) : 2
    General-purpose I/O ports (CMOS I/O) : 3
  - MB95F582H/F583H/F584H (maximum no. of I/O ports: 12)
    General-purpose I/O ports (N-ch open drain) : 1
    General-purpose I/O ports (CMOS I/O) : 11
  - MB95F582K/F583K/F584K (maximum no. of I/O ports: 13)
    General-purpose I/O ports (N-ch open drain) : 2
    General-purpose I/O ports (CMOS I/O) : 11
- On-chip debug
  - 1-wire serial control
  - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
  - Built-in hardware watchdog timer
  - Built-in software watchdog timer
- Power-on reset
  - A power-on reset is generated when the power is switched on.
- Low-voltage detection reset circuit (only available on MB95F562K/F563K/F564K/F572K/F573K/F574K/F582K/F583K/F584K)
  - Built-in low-voltage detector
- Clock supervisor counter
  - Built-in clock supervisor counter function
- Dual operation Flash memory
  - The program/erase operation and the read operat.ion can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
  - Protects the content of the Flash memory.

## ■ PRODUCT LINE-UP

- MB95560H Series

| Parameter \ Part number | MB95F562H | MB95F563H | MB95F564H | MB95F562K | MB95F563K | MB95F564K |
|---|---|---|---|---|---|---|
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 8 Kbyte | 12 Kbyte | 20 Kbyte | 8 Kbyte | 12 Kbyte | 20 Kbyte |
| RAM capacity | 240 bytes | 496 bytes | 496 bytes | 240 bytes | 496 bytes | 496 bytes |
| Power-on reset | Yes | | | | | |
| Low-voltage detection reset | No | | | Yes | | |
| Reset input | Dedicated | | | Selected through software | | |
| CPU functions | • Number of basic instructions : 136<br>• Instruction bit length : 8 bits<br>• Instruction length : 1 to 3 bytes<br>• Data bit length : 1, 8 and 16 bits<br>• Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz)<br>• Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | • I/O ports (Max) : 16<br>• CMOS I/O : 15<br>• N-ch open drain: 1 | | | • I/O ports (Max) : 17<br>• CMOS I/O : 15<br>• N-ch open drain: 2 | | |
| Time-base timer | Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz) | | | | | |
| Hardware/ software watchdog timer | • Reset generation cycle<br>Main oscillation clock at 10 MHz: 105 ms (Min)<br>• The sub-CR clock can be used as the source clock of the hardware watchdog timer. | | | | | |
| Wild register | It can be used to replace 3 bytes of data. | | | | | |
| LIN-UART | • A wide range of communication speed can be selected by a dedicated reload timer.<br>• It has a full duplex double buffer.<br>• Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled.<br>• The LIN function can be used as a LIN master or a LIN slave. | | | | | |
| 8/10-bit A/D converter | 6 channels | | | | | |
| | 8-bit or 10-bit resolution can be selected. | | | | | |
| 8/16-bit composite timer | 2 channels | | | | | |
| | • The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel".<br>• It has the following functions: interval timer function, PWC function, PWM function and input capture function.<br>• Count clock: it can be selected from internal clocks (seven types) and external clocks.<br>• It can output square wave. | | | | | |
| External interrupt | 6 channels | | | | | |
| | • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.)<br>• It can be used to wake up the device from the standby mode. | | | | | |
| On-chip debug | • 1-wire serial control<br>• It supports serial writing (asynchronous mode). | | | | | |

*(Continued)*

*(Continued)*

<table>
<tr><th>Part number<br>Parameter</th><th>MB95F562H</th><th>MB95F563H</th><th>MB95F564H</th><th>MB95F562K</th><th>MB95F563K</th><th>MB95F564K</th></tr>
<tr><td>Watch prescaler</td><td colspan="6">Eight different time intervals can be selected.</td></tr>
<tr><td>Flash memory</td><td colspan="6">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.<br>• It has a flag indicating the completion of the operation of Embedded Algorithm.<br>• Flash security feature for protecting the content of the Flash memory<br><table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table></td></tr>
<tr><td>Standby mode</td><td colspan="6">Sleep mode, stop mode, watch mode, time-base timer mode</td></tr>
<tr><td>Package</td><td colspan="6">LCC-32P-M19<br>FPT-20P-M09<br>FPT-20P-M10</td></tr>
</table>

- MB95570H Series

| Parameter \ Part number | MB95F572H | MB95F573H | MB95F574H | MB95F572K | MB95F573K | MB95F574K |
|---|---|---|---|---|---|---|
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 8 Kbyte | 12 Kbyte | 20 Kbyte | 8 Kbyte | 12 Kbyte | 20 Kbyte |
| RAM capacity | 240 bytes | 496 bytes | 496 bytes | 240 bytes | 496 bytes | 496 bytes |
| Power-on reset | Yes | | | | | |
| Low-voltage detection reset | No | | | Yes | | |
| Reset input | Dedicated | | | Selected through software | | |
| CPU functions | • Number of basic instructions : 136<br>• Instruction bit length : 8 bits<br>• Instruction length : 1 to 3 bytes<br>• Data bit length : 1, 8 and 16 bits<br>• Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz)<br>• Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | • I/O ports (Max) : 4<br>• CMOS I/O : 3<br>• N-ch open drain: 1 | | | • I/O ports (Max) : 5<br>• CMOS I/O : 3<br>• N-ch open drain: 2 | | |
| Time-base timer | Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz) | | | | | |
| Hardware/ software watchdog timer | • Reset generation cycle<br>Main oscillation clock at 10 MHz: 105 ms (Min)<br>• The sub-CR clock can be used as the source clock of the hardware watchdog timer. | | | | | |
| Wild register | It can be used to replace 3 bytes of data. | | | | | |
| LIN-UART | No LIN-UART | | | | | |
| 8/10-bit A/D converter | 2 channels<br>8-bit or 10-bit resolution can be selected. | | | | | |
| 8/16-bit composite timer | 1 channel<br>• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel".<br>• It has the following functions: interval timer function, PWC function, PWM function and input capture function.<br>• Count clock: it can be selected from internal clocks (seven types) and external clocks.<br>• It can output square wave. | | | | | |
| External interrupt | 2 channels<br>• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.)<br>• It can be used to wake up the device from standby modes. | | | | | |
| On-chip debug | • 1-wire serial control<br>• It supports serial writing (asynchronous mode). | | | | | |
| Watch prescaler | Eight different time intervals can be selected. | | | | | |
| Flash memory | • It supports automatic programming (Embedded Algorithm) and program/erase/erase-suspend/erase-resume commands.<br>• It has a flag indicating the completion of the operation of Embedded Algorithm.<br>• Flash security feature for protecting the content of the Flash memory | | | | | |
| Standby mode | Sleep mode, stop mode, watch mode, time-base timer mode | | | | | |
| Package | DIP-8P-M03<br>FPT-8P-M08 | | | | | |

| Number of program/erase cycles | 1000 | 10000 | 100000 |
|---|---|---|---|
| Data retention time | 20 years | 10 years | 5 years |

- MB95580H Series

| Parameter \ Part number | MB95F582H | MB95F583H | MB95F584H | MB95F582K | MB95F583K | MB95F584K |
|---|---|---|---|---|---|---|
| Type | Flash memory product | | | | | |
| Clock supervisor counter | It supervises the main clock oscillation. | | | | | |
| Flash memory capacity | 8 Kbyte | 12 Kbyte | 20 Kbyte | 8 Kbyte | 12 Kbyte | 20 Kbyte |
| RAM capacity | 240 bytes | 496 bytes | 496 bytes | 240 bytes | 496 bytes | 496 bytes |
| Power-on reset | Yes | | | | | |
| Low-voltage detection reset | No | | | Yes | | |
| Reset input | Dedicated | | | Selected through software | | |
| CPU functions | • Number of basic instructions : 136<br>• Instruction bit length : 8 bits<br>• Instruction length : 1 to 3 bytes<br>• Data bit length : 1, 8 and 16 bits<br>• Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz)<br>• Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz) | | | | | |
| General-purpose I/O | • I/O ports (Max) : 12<br>• CMOS I/O : 11<br>• N-ch open drain: 1 | | | • I/O ports (Max) : 13<br>• CMOS I/O : 11<br>• N-ch open drain: 2 | | |
| Time-base timer | Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz) | | | | | |
| Hardware/ software watchdog timer | • Reset generation cycle<br>Main oscillation clock at 10 MHz: 105 ms (Min)<br>• The sub-CR clock can be used as the source clock of the hardware watchdog timer. | | | | | |
| Wild register | It can be used to replace 3 bytes of data. | | | | | |
| LIN-UART | • A wide range of communication speed can be selected by a dedicated reload timer.<br>• It has a full duplex double buffer.<br>• Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled.<br>• The LIN function can be used as a LIN master or a LIN slave. | | | | | |
| 8/10-bit A/D converter | 5 channels | | | | | |
| | 8-bit or 10-bit resolution can be selected. | | | | | |
| 8/16-bit composite timer | 1 channel | | | | | |
| | • The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel".<br>• It has the following functions: interval timer function, PWC function, PWM function and input capture function.<br>• Count clock: it can be selected from internal clocks (seven types) and external clocks.<br>• It can output square wave. | | | | | |
| External interrupt | 6 channels | | | | | |
| | • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.)<br>• It can be used to wake up the device from standby modes. | | | | | |
| On-chip debug | • 1-wire serial control<br>• It supports serial writing (asynchronous mode). | | | | | |

*(Continued)*

*(Continued)*

<table>
<tr><th>Part number<br>Parameter</th><th>MB95F582H</th><th>MB95F583H</th><th>MB95F584H</th><th>MB95F582K</th><th>MB95F583K</th><th>MB95F584K</th></tr>
<tr><td>Watch prescaler</td><td colspan="6">Eight different time intervals can be selected.</td></tr>
<tr><td>Flash memory</td><td colspan="6">• It supports automatic programming (Embedded Algorithm) and program/erase/erase-suspend/erase-resume commands.<br>• It has a flag indicating the completion of the operation of Embedded Algorithm.<br>• Flash security feature for protecting the content of the Flash memory<br><table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table></td></tr>
<tr><td>Standby mode</td><td colspan="6">Sleep mode, stop mode, watch mode, time-base timer mode</td></tr>
<tr><td>Package</td><td colspan="6">LCC-32P-M19<br>FPT-16P-M08<br>FPT-16P-M23</td></tr>
</table>

## ■ PACKAGES AND CORRESPONDING PRODUCTS

• MB95560H Series

| Part number / Package | MB95F562H | MB95F562K | MB95F563H | MB95F563K | MB95F564H | MB95F564K |
|---|---|---|---|---|---|---|
| LCC-32P-M19 | O | O | O | O | O | O |
| FPT-20P-M09 | O | O | O | O | O | O |
| FPT-20P-M10 | O | O | O | O | O | O |
| FPT-16P-M08 | X | X | X | X | X | X |
| FPT-16P-M23 | X | X | X | X | X | X |
| DIP-8P-M03 | X | X | X | X | X | X |
| FPT-8P-M08 | X | X | X | X | X | X |

• MB95570H Series

| Part number / Package | MB95F572H | MB95F572K | MB95F573H | MB95F573K | MB95F574H | MB95F574K |
|---|---|---|---|---|---|---|
| LCC-32P-M19 | X | X | X | X | X | X |
| FPT-20P-M09 | X | X | X | X | X | X |
| FPT-20P-M10 | X | X | X | X | X | X |
| FPT-16P-M08 | X | X | X | X | X | X |
| FPT-16P-M23 | X | X | X | X | X | X |
| DIP-8P-M03 | O | O | O | O | O | O |
| FPT-8P-M08 | O | O | O | O | O | O |

• MB95580H Series

| Part number / Package | MB95F582H | MB95F582K | MB95F583H | MB95F583K | MB95F584H | MB95F584K |
|---|---|---|---|---|---|---|
| LCC-32P-M19 | O | O | O | O | O | O |
| FPT-20P-M09 | X | X | X | X | X | X |
| FPT-20P-M10 | X | X | X | X | X | X |
| FPT-16P-M08 | O | O | O | O | O | O |
| FPT-16P-M23 | O | O | O | O | O | O |
| DIP-8P-M03 | X | X | X | X | X | X |
| FPT-8P-M08 | X | X | X | X | X | X |

O: Available
X: Unavailable

## ■ DIFFERENCES AMONG PRODUCTS AND NOTES ON PRODUCT SELECTION

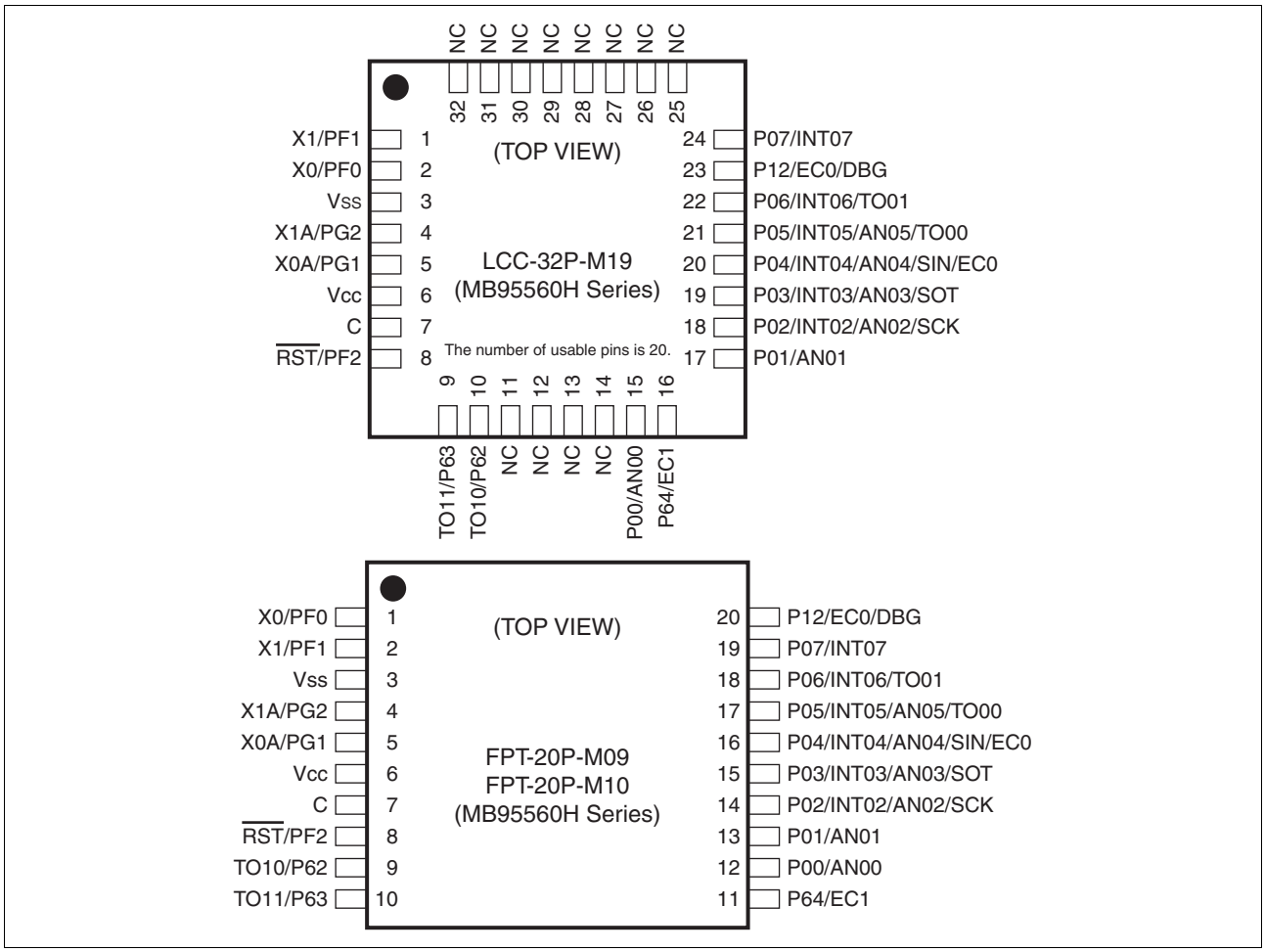
- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash program/erase.
  For details of current consumption, see "■ ELECTRICAL CHARACTERISTICS".

- Package
  For details of information on each package, see "■ PACKAGES AND CORRESPONDING PRODUCTS" and "■ PACKAGE DIMENSION".

- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of the operating voltage, see "■ ELECTRICAL CHARACTERISTICS".

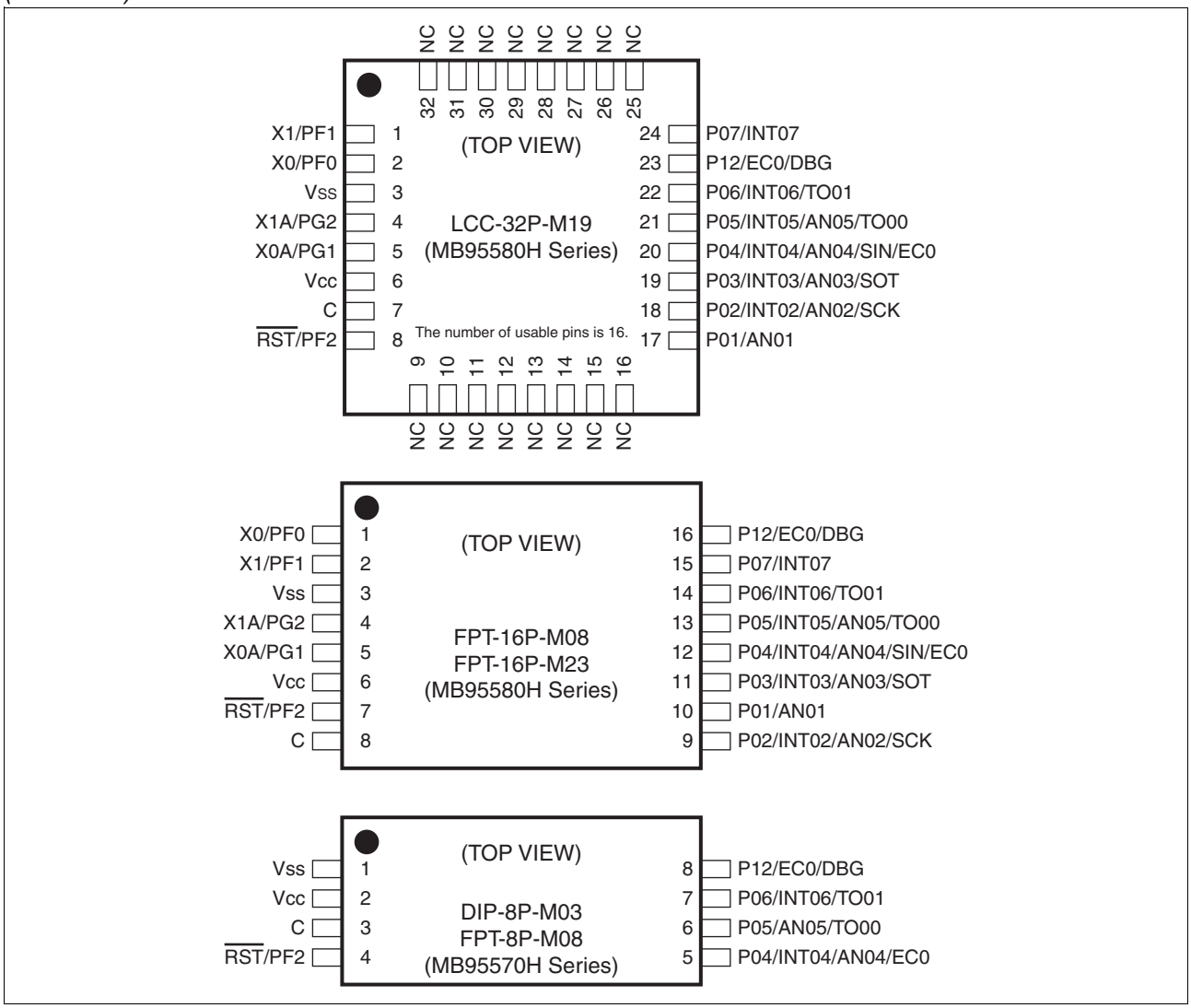
- On-chip debug function
  The on-chip debug function requires that $V_{CC}$, $V_{SS}$ and one serial wire be connected to an evaluation tool. For details of the connection method, refer to "CHAPTER 21 EXAMPLE OF SERIAL PROGRAMMING CONNECTION" in the hardware manual of the MB95560H/570H/580H Series.

## ■ PIN ASSIGNMENT




*(Continued)*

*(Continued)*


NC NC NC NC NC NC NC NC
32 31 30 29 28 27 26 25
X1/PF1 1
X0/PF0 2
Vss 3
X1A/PG2 4
X0A/PG1 5
Vcc 6
C 7
RST/PF2 8
(TOP VIEW)
LCC-32P-M19
(MB95580H Series)
The number of usable pins is 16.
24 P07/INT07
23 P12/EC0/DBG
22 P06/INT06/TO01
21 P05/INT05/AN05/TO00
20 P04/INT04/AN04/SIN/EC0
19 P03/INT03/AN03/SOT
18 P02/INT02/AN02/SCK
17 P01/AN01
9 10 11 12 13 14 15 16
NC NC NC NC NC NC NC NC
X0/PF0 1
X1/PF1 2
Vss 3
X1A/PG2 4
X0A/PG1 5
Vcc 6
RST/PF2 7
C 8
(TOP VIEW)
FPT-16P-M08
FPT-16P-M23
(MB95580H Series)
16 P12/EC0/DBG
15 P07/INT07
14 P06/INT06/TO01
13 P05/INT05/AN05/TO00
12 P04/INT04/AN04/SIN/EC0
11 P03/INT03/AN03/SOT
10 P01/AN01
9 P02/INT02/AN02/SCK
Vss 1
Vcc 2
C 3
RST/PF2 4
(TOP VIEW)
DIP-8P-M03
FPT-8P-M08
(MB95570H Series)
8 P12/EC0/DBG
7 P06/INT06/TO01
6 P05/AN05/TO00
5 P04/INT04/AN04/EC0

## ■ PIN FUNCTIONS (MB95560H Series, 32 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 1 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 2 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 3 | $V_{SS}$ | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | $V_{CC}$ | — | Power supply pin |
| 7 | C | — | Decoupling capacitor connection pin |
| 8 | PF2 | A | General-purpose I/O port |
| | $\overline{RST}$ | | Reset pin<br>Dedicated reset pin on MB95F562H/F563H/F564H |
| 9 | P63 | E | General-purpose I/O port<br>High-current pin |
| | TO11 | | 8/16-bit composite timer ch. 1 output pin |
| 10 | P62 | E | General-purpose I/O port<br>High-current pin |
| | TO10 | | 8/16-bit composite timer ch. 1 output pin |
| 11 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 12 | | | |
| 13 | | | |
| 14 | | | |
| 15 | P00 | D | General-purpose I/O port<br>High-current pin |
| | AN00 | | A/D converter analog input pin |
| 16 | P64 | E | General-purpose I/O port<br>High-current pin |
| | EC1 | | 8/16-bit composite timer ch. 1 clock input pin |
| 17 | P01 | D | General-purpose I/O port<br>High-current pin |
| | AN01 | | A/D converter analog input pin |
| 18 | P02 | D | General-purpose I/O port<br>High-current pin |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |

*(Continued)*

*(Continued)*

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 19 | P03 | D | General-purpose I/O port<br>High-current pin |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |
| 20 | P04 | D | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 21 | P05 | D | General-purpose I/O port<br>High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 22 | P06 | E | General-purpose I/O port<br>High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 23 | P12 | F | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |
| 24 | P07 | E | General-purpose I/O port<br>High-current pin |
| | INT07 | | External interrupt input pin |
| 25 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 26 | | | |
| 27 | | | |
| 28 | | | |
| 29 | | | |
| 30 | | | |
| 31 | | | |
| 32 | | | |

*: For the I/O circuit types, see "■ I/O CIRCUIT TYPE".

## ■ PIN FUNCTIONS (MB95560H Series, 20 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 1 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 2 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 3 | $V_{SS}$ | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | $V_{CC}$ | — | Power supply pin |
| 7 | C | — | Decoupling capacitor connection pin |
| 8 | PF2 | A | General-purpose I/O port |
| | $\overline{RST}$ | | Reset pin<br>Dedicated reset pin on MB95F562H/F563H/F564H |
| 9 | P62 | E | General-purpose I/O port<br>High-current pin |
| | TO10 | | 8/16-bit composite timer ch. 1 output pin |
| 10 | P63 | E | General-purpose I/O port<br>High-current pin |
| | TO11 | | 8/16-bit composite timer ch. 1 output pin |
| 11 | P64 | E | General-purpose I/O port<br>High-current pin |
| | EC1 | | 8/16-bit composite timer ch. 1 clock input pin |
| 12 | P00 | D | General-purpose I/O port<br>High-current pin |
| | AN00 | | A/D converter analog input pin |
| 13 | P01 | D | General-purpose I/O port<br>High-current pin |
| | AN01 | | A/D converter analog input pin |
| 14 | P02 | D | General-purpose I/O port<br>High-current pin |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |
| 15 | P03 | D | General-purpose I/O port<br>High-current pin |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |

*(Continued)*

*(Continued)*

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 16 | P04 | D | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 17 | P05 | D | General-purpose I/O port<br>High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 18 | P06 | E | General-purpose I/O port<br>High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 19 | P07 | E | General-purpose I/O port<br>High-current pin |
| | INT07 | | External interrupt input pin |
| 20 | P12 | F | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |

*: For the I/O circuit types, see "■ I/O CIRCUIT TYPE".

## ■ PIN FUNCTIONS (MB95570H Series, 8 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 1 | $V_{SS}$ | — | Power supply pin (GND) |
| 2 | $V_{CC}$ | — | Power supply pin |
| 3 | C | — | Decoupling capacitor connection pin |
| 4 | PF2 | A | General-purpose I/O port |
| | $\overline{RST}$ | | Reset pin<br>Dedicated reset pin on MB95F572H/F573H/F574H |
| 5 | P04 | D | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 6 | P05 | D | General-purpose I/O port<br>High-current pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 7 | P06 | E | General-purpose I/O port<br>High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 8 | P12 | F | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |

*: For the I/O circuit types, see "■ I/O CIRCUIT TYPE".

## ■ PIN FUNCTIONS (MB95580H Series, 32 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 1 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 2 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 3 | $V_{SS}$ | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | $V_{CC}$ | — | Power supply pin |
| 7 | C | — | Decoupling capacitor connection pin |
| 8 | PF2 | A | General-purpose I/O port |
| | $\overline{RST}$ | | Reset pin<br>Dedicated reset pin on MB95F582H/F583H/F584H |
| 9 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 10 | | | |
| 11 | | | |
| 12 | | | |
| 13 | | | |
| 14 | | | |
| 15 | | | |
| 16 | | | |
| 17 | P01 | D | General-purpose I/O port<br>High-current pin |
| | AN01 | | A/D converter analog input pin |
| 18 | P02 | D | General-purpose I/O port<br>High-current pin |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |
| 19 | P03 | D | General-purpose I/O port<br>High-current pin |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |

*(Continued)*

*(Continued)*

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 20 | P04 | D | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| 21 | P05 | D | General-purpose I/O port<br>High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 22 | P06 | E | General-purpose I/O port<br>High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 23 | P12 | F | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |
| 24 | P07 | E | General-purpose I/O port<br>High-current pin |
| | INT07 | | External interrupt input pin |
| 25 | NC | — | It is an internally connected pin. Always leave it unconnected. |
| 26 | | | |
| 27 | | | |
| 28 | | | |
| 29 | | | |
| 30 | | | |
| 31 | | | |
| 32 | | | |

*: For the I/O circuit types, see "■ I/O CIRCUIT TYPE".

## ■ PIN FUNCTIONS (MB95580H Series, 16 pins)

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 1 | PF0 | B | General-purpose I/O port |
| | X0 | | Main clock input oscillation pin |
| 2 | PF1 | B | General-purpose I/O port |
| | X1 | | Main clock I/O oscillation pin |
| 3 | $V_{SS}$ | — | Power supply pin (GND) |
| 4 | PG2 | C | General-purpose I/O port |
| | X1A | | Subclock I/O oscillation pin |
| 5 | PG1 | C | General-purpose I/O port |
| | X0A | | Subclock input oscillation pin |
| 6 | $V_{CC}$ | — | Power supply pin |
| 7 | PF2 | A | General-purpose I/O port |
| | $\overline{RST}$ | | Reset pin<br>Dedicated reset pin on MB95F582H/F583H/F584H |
| 8 | C | — | Decoupling capacitor connection pin |
| 9 | P02 | D | General-purpose I/O port<br>High-current pin |
| | INT02 | | External interrupt input pin |
| | AN02 | | A/D converter analog input pin |
| | SCK | | LIN-UART clock I/O pin |
| 10 | P01 | D | General-purpose I/O port<br>High-current pin |
| | AN01 | | A/D converter analog input pin |
| 11 | P03 | D | General-purpose I/O port<br>High-current pin |
| | INT03 | | External interrupt input pin |
| | AN03 | | A/D converter analog input pin |
| | SOT | | LIN-UART data output pin |
| 12 | P04 | D | General-purpose I/O port |
| | INT04 | | External interrupt input pin |
| | AN04 | | A/D converter analog input pin |
| | SIN | | LIN-UART data input pin |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |

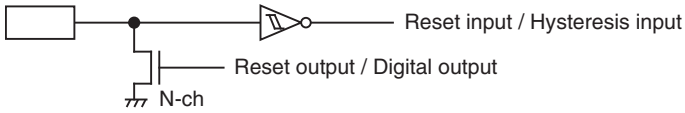
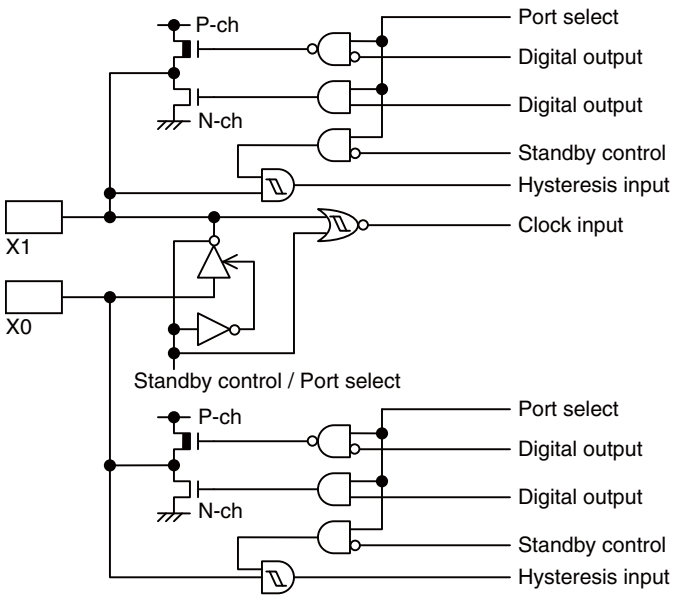
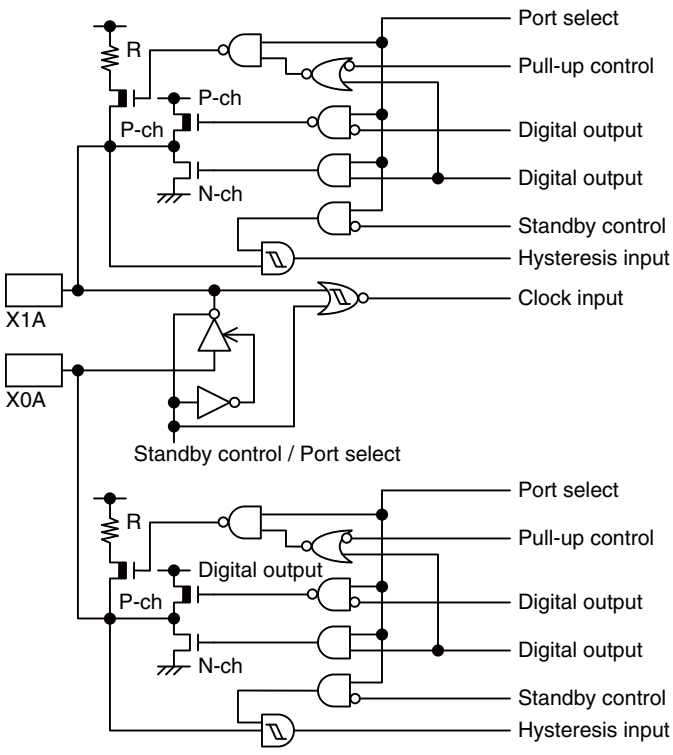
*(Continued)*

*(Continued)*

| Pin no. | Pin name | I/O circuit type* | Function |
|---|---|---|---|
| 13 | P05 | D | General-purpose I/O port<br>High-current pin |
| | INT05 | | External interrupt input pin |
| | AN05 | | A/D converter analog input pin |
| | TO00 | | 8/16-bit composite timer ch. 0 output pin |
| 14 | P06 | E | General-purpose I/O port<br>High-current pin |
| | INT06 | | External interrupt input pin |
| | TO01 | | 8/16-bit composite timer ch. 0 output pin |
| 15 | P07 | E | General-purpose I/O port<br>High-current pin |
| | INT07 | | External interrupt input pin |
| 16 | P12 | F | General-purpose I/O port |
| | EC0 | | 8/16-bit composite timer ch. 0 clock input pin |
| | DBG | | DBG input pin |

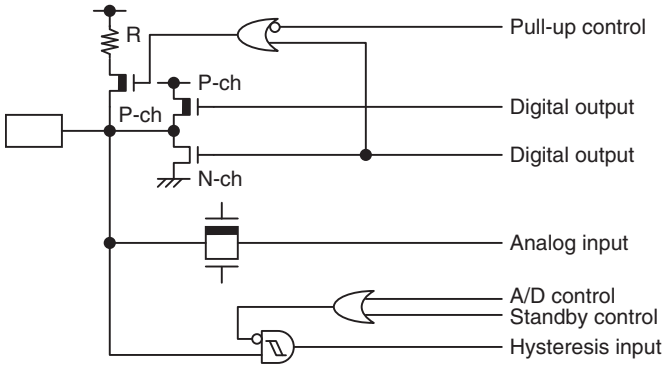
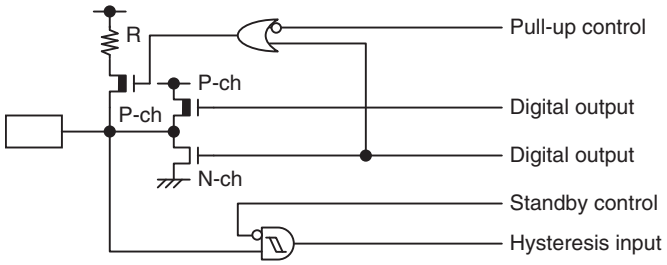
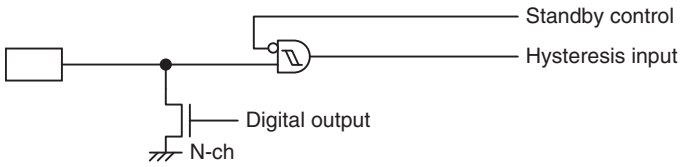
*: For the I/O circuit types, see "■ I/O CIRCUIT TYPE".

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | • N-ch open drain output<br>• Hysteresis input<br>• Reset output |
| B |  | • Oscillation circuit<br>• High-speed side<br>Feedback resistance:<br>approx. 1 MΩ<br><br>• CMOS output<br>• Hysteresis input |
| C |  | • Oscillation circuit<br>• Low-speed side<br>Feedback resistance:<br>approx.10 MΩ<br><br>• CMOS output<br>• Hysteresis input<br>• Pull-up control available |

*(Continued)*

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| D |  | • CMOS output<br>• Hysteresis input<br>• Pull-up control available<br>• Analog input |
| E |  | • CMOS output<br>• Hysteresis input<br>• Pull-up control available |
| F |  | • N-ch open drain output<br>• Hysteresis input |

## ■ NOTES ON DEVICE HANDLING

- Preventing latch-ups
  When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
  In a CMOS IC, if a voltage higher than $V_{CC}$ or a voltage lower than $V_{SS}$ is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "1. Absolute Maximum Ratings" of "■ ELECTRICAL CHARACTERISTICS" is applied to the $V_{CC}$ pin or the $V_{SS}$ pin, a latch-up may occur.
  When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

- Stabilizing supply voltage
  Supply voltage must be stabilized.
  A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the $V_{CC}$ power supply voltage.
  As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in $V_{CC}$ ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard $V_{CC}$ value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock
  When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

## ■ PIN CONNECTION

- Treatment of unused pins
  If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Power supply pins
  To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the $V_{CC}$ pin and the $V_{SS}$ pin to the power supply and ground outside the device. In addition, connect the current supply source to the $V_{CC}$ pin and the $V_{SS}$ pin with low impedance.
  It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the $V_{CC}$ pin and the $V_{SS}$ pin at a location close to this device.

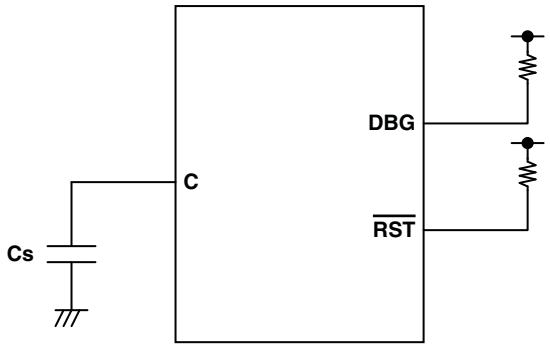
- DBG pin
  Connect the DBG pin directly to an external pull-up resistor.
  To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the $V_{CC}$ or $V_{SS}$ pin when designing the layout of the printed circuit board.
  The DBG pin should not stay at “L” level after power-on until the reset output is released.

- $\overline{\text{RST}}$ pin
  Connect the $\overline{\text{RST}}$ pin directly to an external pull-up resistor.
  To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{\text{RST}}$ pin and the $V_{CC}$ or $V_{SS}$ pin when designing the layout of the printed circuit board.
  The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

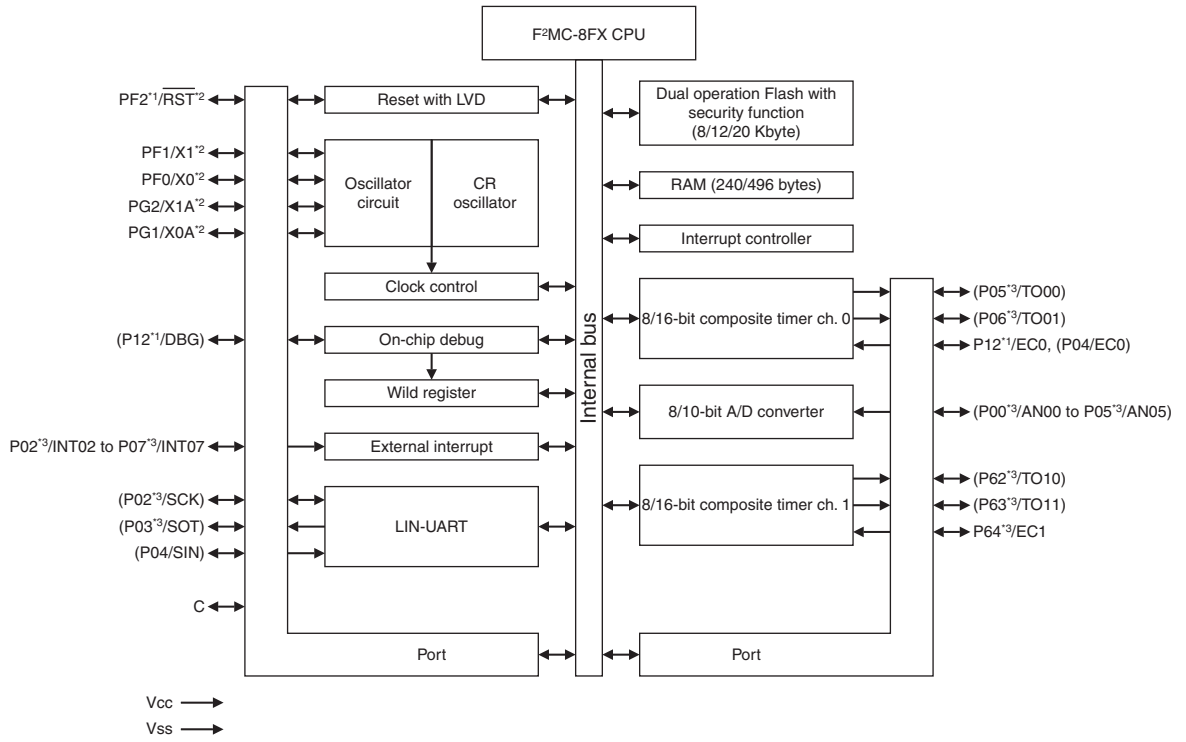
- C pin

  Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the $V_{CC}$ pin must have a capacitance larger than $C_S$. For the connection to a decoupling capacitor $C_S$, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and $C_S$ and the distance between $C_S$ and the $V_{SS}$ pin when designing the layout of a printed circuit board.

- DBG/$\overline{\text{RST}}$/C pins connection diagram



## ■ BLOCK DIAGRAM (MB95560H Series)



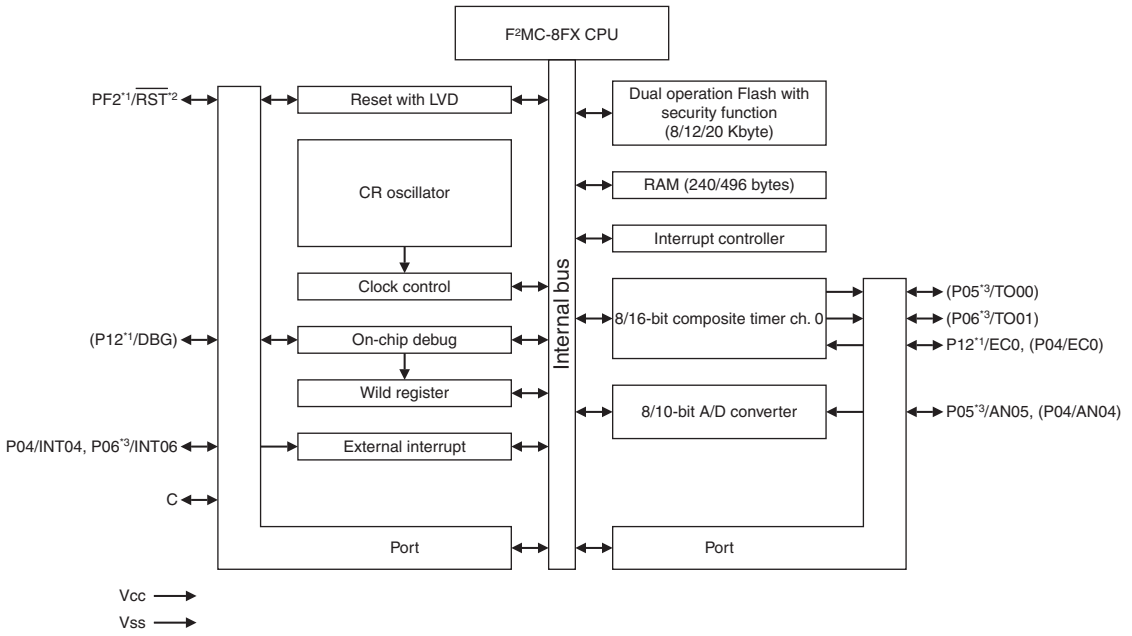

*1: PF2 and P12 are N-ch open drain pins.

*2: Software option

*3: P00 to P03, P05 to P07 and P62 to P64 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

## ■ BLOCK DIAGRAM (MB95570H Series)



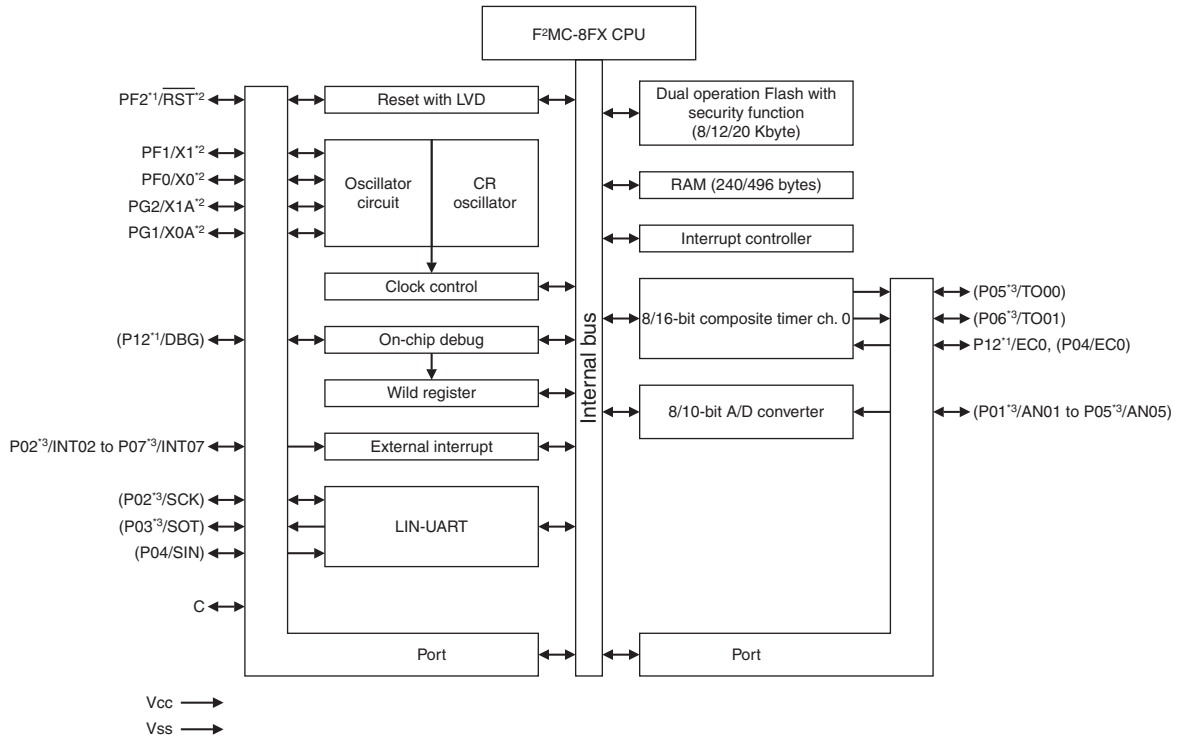

*1: PF2 and P12 are N-ch open drain pins.

*2: Software option

*3: P05 and P06 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

## ■ BLOCK DIAGRAM (MB95580H Series)




*1: PF2 and P12 are N-ch open drain pins.

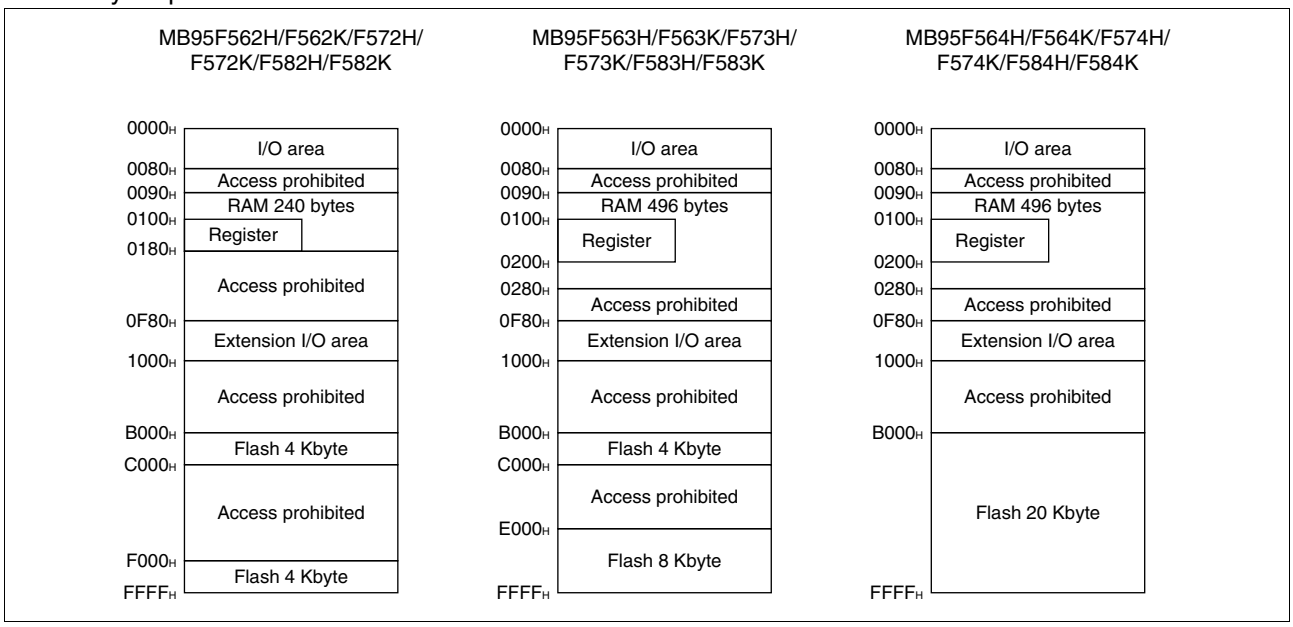
*2: Software option

*3: P01 to P03 and P05 to P07 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

## ■ CPU CORE

- Memory space
  The memory space of the MB95560H/570H/580H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95560H/570H/580H Series are shown below.
- Memory maps



## ■ I/O MAP (MB95560H Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0000H | PDR0 | Port 0 data register | R/W | 00000000B |
| 0001H | DDR0 | Port 0 direction register | R/W | 00000000B |
| 0002H | PDR1 | Port 1 data register | R/W | 00000000B |
| 0003H | DDR1 | Port 1 direction register | R/W | 00000000B |
| 0004H | — | (Disabled) | — | — |
| 0005H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111B |
| 0006H | PLLC | PLL control register | R/W | 000X0000B |
| 0007H | SYCC | System clock control register | R/W | XXX11011B |
| 0008H | STBC | Standby control register | R/W | 00000000B |
| 0009H | RSRR | Reset source register | R/W | 000XXXXXB |
| 000AH | TBTC | Time-base timer control register | R/W | 00000000B |
| 000BH | WPCR | Watch prescaler control register | R/W | 00000000B |
| 000CH | WDTC | Watchdog timer control register | R/W | 00XX0000B |
| 000DH | SYCC2 | System clock control register 2 | R/W | XXXX0011B |
| 000EH | STBC2 | Standby control register 2 | R/W | 00000000B |
| 000FH to 0015H | — | (Disabled) | — | — |
| 0016H | PDR6 | Port 6 data register | R/W | 00000000B |
| 0017H | DDR6 | Port 6 direction register | R/W | 00000000B |
| 0018H to 0027H | — | (Disabled) | — | — |
| 0028H | PDRF | Port F data register | R/W | 00000000B |
| 0029H | DDRF | Port F direction register | R/W | 00000000B |
| 002AH | PDRG | Port G data register | R/W | 00000000B |
| 002BH | DDRG | Port G direction register | R/W | 00000000B |
| 002CH | PUL0 | Port 0 pull-up register | R/W | 00000000B |
| 002DH to 0032H | — | (Disabled) | — | — |
| 0033H | PUL6 | Port 6 pull-up register | R/W | 00000000B |
| 0034H | — | (Disabled) | — | — |
| 0035H | PULG | Port G pull-up register | R/W | 00000000B |
| 0036H | T01CR1 | 8/16-bit composite timer 01 status control register 1 | R/W | 00000000B |
| 0037H | T00CR1 | 8/16-bit composite timer 00 status control register 1 | R/W | 00000000B |
| 0038H | T11CR1 | 8/16-bit composite timer 11 status control register 1 | R/W | 00000000B |
| 0039H | T10CR1 | 8/16-bit composite timer 10 status control register 1 | R/W | 00000000B |
| 003AH to 0048H | — | (Disabled) | — | — |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0049H | EIC10 | External interrupt circuit control register ch. 2/ch. 3 | R/W | 00000000B |
| 004AH | EIC20 | External interrupt circuit control register ch. 4/ch. 5 | R/W | 00000000B |
| 004BH | EIC30 | External interrupt circuit control register ch. 6/ch. 7 | R/W | 00000000B |
| 004CH, 004DH | — | (Disabled) | — | — |
| 004EH | LVDR | LVDR reset voltage selection ID register | R/W | 00000000B |
| 004FH | — | (Disabled) | — | — |
| 0050H | SCR | LIN-UART serial control register | R/W | 00000000B |
| 0051H | SMR | LIN-UART serial mode register | R/W | 00000000B |
| 0052H | SSR | LIN-UART serial status register | R/W | 00001000B |
| 0053H | RDR | LIN-UART receive data register | R/W | 00000000B |
| | TDR | LIN-UART transmit data register | R/W | 00000000B |
| 0054H | ESCR | LIN-UART extended status control register | R/W | 00000100B |
| 0055H | ECCR | LIN-UART extended communication control register | R/W | 000000XXB |
| 0056H to 006BH | — | (Disabled) | — | — |
| 006CH | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000B |
| 006DH | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000B |
| 006EH | ADDH | 8/10-bit A/D converter data register (upper) | R/W | 00000000B |
| 006FH | ADDL | 8/10-bit A/D converter data register (lower) | R/W | 00000000B |
| 0070H | — | (Disabled) | — | — |
| 0071H | FSR2 | Flash memory status register 2 | R/W | 00000000B |
| 0072H | FSR | Flash memory status register | R/W | 000X0000B |
| 0073H | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000B |
| 0074H | FSR3 | Flash memory status register 3 | R | 000XXXXXB |
| 0075H | FSR4 | Flash memory status register 4 | R/W | 00000000B |
| 0076H | WREN | Wild register address compare enable register | R/W | 00000000B |
| 0077H | WROR | Wild register data test setting register | R/W | 00000000B |
| 0078H | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0079H | ILR0 | Interrupt level setting register 0 | R/W | 11111111B |
| 007AH | ILR1 | Interrupt level setting register 1 | R/W | 11111111B |
| 007BH | ILR2 | Interrupt level setting register 2 | R/W | 11111111B |
| 007CH | ILR3 | Interrupt level setting register 3 | R/W | 11111111B |
| 007DH | ILR4 | Interrupt level setting register 4 | R/W | 11111111B |
| 007EH | ILR5 | Interrupt level setting register 5 | R/W | 11111111B |
| 007FH | — | (Disabled) | — | — |
| 0F80H | WRARH0 | Wild register address setting register (upper) ch. 0 | R/W | 00000000B |
| 0F81H | WRARL0 | Wild register address setting register (lower) ch. 0 | R/W | 00000000B |
| 0F82H | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000B |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0F83H | WRARH1 | Wild register address setting register (upper) ch. 1 | R/W | 00000000B |
| 0F84H | WRARL1 | Wild register address setting register (lower) ch. 1 | R/W | 00000000B |
| 0F85H | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000B |
| 0F86H | WRARH2 | Wild register address setting register (upper) ch. 2 | R/W | 00000000B |
| 0F87H | WRARL2 | Wild register address setting register (lower) ch. 2 | R/W | 00000000B |
| 0F88H | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000B |
| 0F89H to 0F91H | — | (Disabled) | — | — |
| 0F92H | T01CR0 | 8/16-bit composite timer 01 status control register 0 | R/W | 00000000B |
| 0F93H | T00CR0 | 8/16-bit composite timer 00 status control register 0 | R/W | 00000000B |
| 0F94H | T01DR | 8/16-bit composite timer 01 data register | R/W | 00000000B |
| 0F95H | T00DR | 8/16-bit composite timer 00 data register | R/W | 00000000B |
| 0F96H | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register | R/W | 00000000B |
| 0F97H | T11CR0 | 8/16-bit composite timer 11 status control register 0 | R/W | 00000000B |
| 0F98H | T10CR0 | 8/16-bit composite timer 10 status control register 0 | R/W | 00000000B |
| 0F99H | T11DR | 8/16-bit composite timer 11 data register | R/W | 00000000B |
| 0F9AH | T10DR | 8/16-bit composite timer 10 data register | R/W | 00000000B |
| 0F9BH | TMCR1 | 8/16-bit composite timer 10/11 timer mode control register | R/W | 00000000B |
| 0F9CH to 0FBBH | — | (Disabled) | — | — |
| 0FBCH | BGR1 | LIN-UART baud rate generator register 1 | R/W | 00000000B |
| 0FBDH | BGR0 | LIN-UART baud rate generator register 0 | R/W | 00000000B |
| 0FBEH to 0FC2H | — | (Disabled) | — | — |
| 0FC3H | AIDRL | A/D input disable register (lower) | R/W | 00000000B |
| 0FC4H to 0FE3H | — | (Disabled) | — | — |
| 0FE4H | CRTH | Main CR clock trimming register (upper) | R/W | 000XXXXXB |
| 0FE5H | CRTL | Main CR clock trimming register (lower) | R/W | 000XXXXXB |
| 0FE6H | — | (Disabled) | — | — |
| 0FE7H | CRTDA | Main CR clock temperature dependent adjustment register | R/W | 000XXXXXB |
| 0FE8H | SYSC | System configuration register | R/W | 11000011B |
| 0FE9H | CMCR | Clock monitoring control register | R/W | 00000000B |
| 0FEAH | CMDR | Clock monitoring data register | R/W | 00000000B |

*(Continued)*

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0FEB$_H$ | WDTH | Watchdog timer selection ID register (upper) | R | XXXXXXXX$_B$ |
| 0FEC$_H$ | WDTL | Watchdog timer selection ID register (lower) | R | XXXXXXXX$_B$ |
| 0FED$_H$ to 0FFF$_H$ | — | (Disabled) | — | — |

• R/W access symbols
  R/W : Readable / Writable
  R : Read only

• Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

## ■ I/O MAP (MB95570H Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0000H | PDR0 | Port 0 data register | R/W | 00000000B |
| 0001H | DDR0 | Port 0 direction register | R/W | 00000000B |
| 0002H | PDR1 | Port 1 data register | R/W | 00000000B |
| 0003H | DDR1 | Port 1 direction register | R/W | 00000000B |
| 0004H | — | (Disabled) | — | — |
| 0005H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111B |
| 0006H | PLLC | PLL control register | R/W | 000X0000B |
| 0007H | SYCC | System clock control register | R/W | XXX11011B |
| 0008H | STBC | Standby control register | R/W | 00000000B |
| 0009H | RSRR | Reset source register | R/W | 000XXXXXB |
| 000AH | TBTC | Time-base timer control register | R/W | 00000000B |
| 000BH | WPCR | Watch prescaler control register | R/W | 00000000B |
| 000CH | WDTC | Watchdog timer control register | R/W | 00XX0000B |
| 000DH | SYCC2 | System clock control register 2 | R/W | XXXX0011B |
| 000EH | STBC2 | Standby control register 2 | R/W | 00000000B |
| 000FH to 0027H | — | (Disabled) | — | — |
| 0028H | PDRF | Port F data register | R/W | 00000000B |
| 0029H | DDRF | Port F direction register | R/W | 00000000B |
| 002AH, 002BH | — | (Disabled) | — | — |
| 002CH | PUL0 | Port 0 pull-up register | R/W | 00000000B |
| 002DH to 0035H | — | (Disabled) | — | — |
| 0036H | T01CR1 | 8/16-bit composite timer 01 status control register 1 | R/W | 00000000B |
| 0037H | T00CR1 | 8/16-bit composite timer 00 status control register 1 | R/W | 00000000B |
| 0038H to 0049H | — | (Disabled) | — | — |
| 004AH | EIC20 | External interrupt circuit control register ch. 4 | R/W | 00000000B |
| 004BH | EIC30 | External interrupt circuit control register ch. 6 | R/W | 00000000B |
| 004CH, 004DH | — | (Disabled) | — | — |
| 004EH | LVDR | LVDR reset voltage selection ID register | R/W | 00000000B |
| 004FH to 006BH | — | (Disabled) | — | — |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 006C$_H$ | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000$_B$ |
| 006D$_H$ | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000$_B$ |
| 006E$_H$ | ADDH | 8/10-bit A/D converter data register (upper) | R/W | 00000000$_B$ |
| 006F$_H$ | ADDL | 8/10-bit A/D converter data register (lower) | R/W | 00000000$_B$ |
| 0070$_H$ | — | (Disabled) | — | — |
| 0071$_H$ | FSR2 | Flash memory status register 2 | R/W | 00000000$_B$ |
| 0072$_H$ | FSR | Flash memory status register | R/W | 000X0000$_B$ |
| 0073$_H$ | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000$_B$ |
| 0074$_H$ | FSR3 | Flash memory status register 3 | R | 000XXXXX$_B$ |
| 0075$_H$ | FSR4 | Flash memory status register 4 | R/W | 00000000$_B$ |
| 0076$_H$ | WREN | Wild register address compare enable register | R/W | 00000000$_B$ |
| 0077$_H$ | WROR | Wild register data test setting register | R/W | 00000000$_B$ |
| 0078$_H$ | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0079$_H$ | ILR0 | Interrupt level setting register 0 | R/W | 11111111$_B$ |
| 007A$_H$ | ILR1 | Interrupt level setting register 1 | R/W | 11111111$_B$ |
| 007B$_H$, 007C$_H$ | — | (Disabled) | — | — |
| 007D$_H$ | ILR4 | Interrupt level setting register 4 | R/W | 11111111$_B$ |
| 007E$_H$ | ILR5 | Interrupt level setting register 5 | R/W | 11111111$_B$ |
| 007F$_H$ | — | (Disabled) | — | — |
| 0F80$_H$ | WRARH0 | Wild register address setting register (upper) ch. 0 | R/W | 00000000$_B$ |
| 0F81$_H$ | WRARL0 | Wild register address setting register (lower) ch. 0 | R/W | 00000000$_B$ |
| 0F82$_H$ | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000$_B$ |
| 0F83$_H$ | WRARH1 | Wild register address setting register (upper) ch. 1 | R/W | 00000000$_B$ |
| 0F84$_H$ | WRARL1 | Wild register address setting register (lower) ch. 1 | R/W | 00000000$_B$ |
| 0F85$_H$ | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000$_B$ |
| 0F86$_H$ | WRARH2 | Wild register address setting register (upper) ch. 2 | R/W | 00000000$_B$ |
| 0F87$_H$ | WRARL2 | Wild register address setting register (lower) ch. 2 | R/W | 00000000$_B$ |
| 0F88$_H$ | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000$_B$ |
| 0F89$_H$ to 0F91$_H$ | — | (Disabled) | — | — |
| 0F92$_H$ | T01CR0 | 8/16-bit composite timer 01 status control register 0 | R/W | 00000000$_B$ |
| 0F93$_H$ | T00CR0 | 8/16-bit composite timer 00 status control register 0 | R/W | 00000000$_B$ |
| 0F94$_H$ | T01DR | 8/16-bit composite timer 01 data register | R/W | 00000000$_B$ |
| 0F95$_H$ | T00DR | 8/16-bit composite timer 00 data register | R/W | 00000000$_B$ |
| 0F96$_H$ | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register | R/W | 00000000$_B$ |
| 0F97$_H$ to 0FC2$_H$ | — | (Disabled) | — | — |

*(Continued)*

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0FC3H | AIDRL | A/D input disable register (lower) | R/W | 00000000B |
| 0FC4H to 0FE3H | — | (Disabled) | — | — |
| 0FE4H | CRTH | Main CR clock trimming register (upper) | R/W | 000XXXXXB |
| 0FE5H | CRTL | Main CR clock trimming register (lower) | R/W | 000XXXXXB |
| 0FE6H | — | (Disabled) | — | — |
| 0FE7H | CRTDA | Main CR clock temperature dependent adjustment register | R/W | 000XXXXXB |
| 0FE8H | SYSC | System configuration register | R/W | 11000011B |
| 0FE9H | CMCR | Clock monitoring control register | R/W | 00000000B |
| 0FEAH | CMDR | Clock monitoring data register | R/W | 00000000B |
| 0FEBH | WDTH | Watchdog timer selection ID register (upper) | R/W | XXXXXXXXB |
| 0FECH | WDTL | Watchdog timer selection ID register (lower) | R/W | XXXXXXXXB |
| 0FEDH to 0FFFH | — | (Disabled) | — | — |

• R/W access symbols
  R/W : Readable / Writable
  R : Read only

• Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

## ■ I/O MAP (MB95580H Series)

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0000H | PDR0 | Port 0 data register | R/W | 00000000B |
| 0001H | DDR0 | Port 0 direction register | R/W | 00000000B |
| 0002H | PDR1 | Port 1 data register | R/W | 00000000B |
| 0003H | DDR1 | Port 1 direction register | R/W | 00000000B |
| 0004H | — | (Disabled) | — | — |
| 0005H | WATR | Oscillation stabilization wait time setting register | R/W | 11111111B |
| 0006H | PLLC | PLL control register | R/W | 000X0000B |
| 0007H | SYCC | System clock control register | R/W | XXX11011B |
| 0008H | STBC | Standby control register | R/W | 00000000B |
| 0009H | RSRR | Reset source register | R/W | 000XXXXXB |
| 000AH | TBTC | Time-base timer control register | R/W | 00000000B |
| 000BH | WPCR | Watch prescaler control register | R/W | 00000000B |
| 000CH | WDTC | Watchdog timer control register | R/W | 00XX0000B |
| 000DH | SYCC2 | System clock control register 2 | R/W | XXXX0011B |
| 000EH | STBC2 | Standby control register 2 | R/W | 00000000B |
| 000FH to 0027H | — | (Disabled) | — | — |
| 0028H | PDRF | Port F data register | R/W | 00000000B |
| 0029H | DDRF | Port F direction register | R/W | 00000000B |
| 002AH | PDRG | Port G data register | R/W | 00000000B |
| 002BH | DDRG | Port G direction register | R/W | 00000000B |
| 002CH | PUL0 | Port 0 pull-up register | R/W | 00000000B |
| 002DH to 0034H | — | (Disabled) | — | — |
| 0035H | PULG | Port G pull-up register | R/W | 00000000B |
| 0036H | T01CR1 | 8/16-bit composite timer 01 status control register 1 | R/W | 00000000B |
| 0037H | T00CR1 | 8/16-bit composite timer 00 status control register 1 | R/W | 00000000B |
| 0038H to 0048H | — | (Disabled) | — | — |
| 0049H | EIC10 | External interrupt circuit control register ch. 2/ch. 3 | R/W | 00000000B |
| 004AH | EIC20 | External interrupt circuit control register ch. 4/ch. 5 | R/W | 00000000B |
| 004BH | EIC30 | External interrupt circuit control register ch. 6/ch. 7 | R/W | 00000000B |
| 004CH, 004DH | — | (Disabled) | — | — |
| 004EH | LVDR | LVDR reset voltage selection ID register | R/W | 00000000B |
| 004FH | — | (Disabled) | — | — |

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0050H | SCR | LIN-UART serial control register | R/W | 00000000B |
| 0051H | SMR | LIN-UART serial mode register | R/W | 00000000B |
| 0052H | SSR | LIN-UART serial status register | R/W | 00001000B |
| 0053H | RDR | LIN-UART receive data register | R/W | 00000000B |
| | TDR | LIN-UART transmit data register | R/W | 00000000B |
| 0054H | ESCR | LIN-UART extended status control register | R/W | 00000100B |
| 0055H | ECCR | LIN-UART extended communication control register | R/W | 000000XXB |
| 0056H to 006BH | — | (Disabled) | — | — |
| 006CH | ADC1 | 8/10-bit A/D converter control register 1 | R/W | 00000000B |
| 006DH | ADC2 | 8/10-bit A/D converter control register 2 | R/W | 00000000B |
| 006EH | ADDH | 8/10-bit A/D converter data register (upper) | R/W | 00000000B |
| 006FH | ADDL | 8/10-bit A/D converter data register (lower) | R/W | 00000000B |
| 0070H | — | (Disabled) | — | — |
| 0071H | FSR2 | Flash memory status register 2 | R/W | 00000000B |
| 0072H | FSR | Flash memory status register | R/W | 000X0000B |
| 0073H | SWRE0 | Flash memory sector write control register 0 | R/W | 00000000B |
| 0074H | FSR3 | Flash memory status register 3 | R | 000XXXXXB |
| 0075H | FSR4 | Flash memory status register 4 | R/W | 00000000B |
| 0076H | WREN | Wild register address compare enable register | R/W | 00000000B |
| 0077H | WROR | Wild register data test setting register | R/W | 00000000B |
| 0078H | — | Mirror of register bank pointer (RP) and direct bank pointer (DP) | — | — |
| 0079H | ILR0 | Interrupt level setting register 0 | R/W | 11111111B |
| 007AH | ILR1 | Interrupt level setting register 1 | R/W | 11111111B |
| 007BH | ILR2 | Interrupt level setting register 2 | R/W | 11111111B |
| 007CH | — | (Disabled) | — | — |
| 007DH | ILR4 | Interrupt level setting register 4 | R/W | 11111111B |
| 007EH | ILR5 | Interrupt level setting register 5 | R/W | 11111111B |
| 007FH | — | (Disabled) | — | — |
| 0F80H | WRARH0 | Wild register address setting register (upper) ch. 0 | R/W | 00000000B |
| 0F81H | WRARL0 | Wild register address setting register (lower) ch. 0 | R/W | 00000000B |
| 0F82H | WRDR0 | Wild register data setting register ch. 0 | R/W | 00000000B |
| 0F83H | WRARH1 | Wild register address setting register (upper) ch. 1 | R/W | 00000000B |
| 0F84H | WRARL1 | Wild register address setting register (lower) ch. 1 | R/W | 00000000B |
| 0F85H | WRDR1 | Wild register data setting register ch. 1 | R/W | 00000000B |
| 0F86H | WRARH2 | Wild register address setting register (upper) ch. 2 | R/W | 00000000B |
| 0F87H | WRARL2 | Wild register address setting register (lower) ch. 2 | R/W | 00000000B |
| 0F88H | WRDR2 | Wild register data setting register ch. 2 | R/W | 00000000B |

*(Continued)*

*(Continued)*

| Address | Register abbreviation | Register name | R/W | Initial value |
|---|---|---|---|---|
| 0F89H to 0F91H | — | (Disabled) | — | — |
| 0F92H | T01CR0 | 8/16-bit composite timer 01 status control register 0 | R/W | 00000000B |
| 0F93H | T00CR0 | 8/16-bit composite timer 00 status control register 0 | R/W | 00000000B |
| 0F94H | T01DR | 8/16-bit composite timer 01 data register | R/W | 00000000B |
| 0F95H | T00DR | 8/16-bit composite timer 00 data register | R/W | 00000000B |
| 0F96H | TMCR0 | 8/16-bit composite timer 00/01 timer mode control register | R/W | 00000000B |
| 0F97H to 0FBBH | — | (Disabled) | — | — |
| 0FBCH | BGR1 | LIN-UART baud rate generator register 1 | R/W | 00000000B |
| 0FBDH | BGR0 | LIN-UART baud rate generator register 0 | R/W | 00000000B |
| 0FBEH to 0FC2H | — | (Disabled) | — | — |
| 0FC3H | AIDRL | A/D input disable register (lower) | R/W | 00000000B |
| 0FC4H to 0FE3H | — | (Disabled) | — | — |
| 0FE4H | CRTH | Main CR clock trimming register (upper) | R/W | 000XXXXXB |
| 0FE5H | CRTL | Main CR clock trimming register (lower) | R/W | 000XXXXXB |
| 0FE6H | — | (Disabled) | — | — |
| 0FE7H | CRTDA | Main CR clock temperature dependent adjustment | R/W | 000XXXXXB |
| 0FE8H | SYSC | System configuration register | R/W | 11000011B |
| 0FE9H | CMCR | Clock monitoring control register | R/W | 00000000B |
| 0FEAH | CMDR | Clock monitoring data register | R/W | 00000000B |
| 0FEBH | WDTH | Watchdog timer selection ID register (upper) | R/W | XXXXXXXXB |
| 0FECH | WDTL | Watchdog timer selection ID register (lower) | R/W | XXXXXXXXB |
| 0FEDH to 0FFFH | — | (Disabled) | — | — |

• R/W access symbols
  R/W : Readable / Writable
  R : Read only

• Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

## ■ INTERRUPT SOURCE TABLE (MB95560H Series)

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Priority order of interrupt sources of the same level (occurring simultaneously) |
|---|---|---|---|---|---|
| | | Upper | Lower | | |
| External interrupt ch. 4 | IRQ00 | FFFA$_H$ | FFFB$_H$ | L00 [1:0] | High |
| External interrupt ch. 5 | IRQ01 | FFF8$_H$ | FFF9$_H$ | L01 [1:0] | |
| External interrupt ch. 2 | IRQ02 | FFF6$_H$ | FFF7$_H$ | L02 [1:0] | |
| External interrupt ch. 6 | | | | | |
| External interrupt ch. 3 | IRQ03 | FFF4$_H$ | FFF5$_H$ | L03 [1:0] | |
| External interrupt ch. 7 | | | | | |
| — | IRQ04 | FFF2$_H$ | FFF3$_H$ | L04 [1:0] | |
| 8/16-bit composite timer ch. 0 (lower) | IRQ05 | FFF0$_H$ | FFF1$_H$ | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (upper) | IRQ06 | FFEE$_H$ | FFEF$_H$ | L06 [1:0] | |
| LIN-UART (reception) | IRQ07 | FFEC$_H$ | FFED$_H$ | L07 [1:0] | |
| LIN-UART (transmission) | IRQ08 | FFEA$_H$ | FFEB$_H$ | L08 [1:0] | |
| — | IRQ09 | FFE8$_H$ | FFE9$_H$ | L09 [1:0] | |
| — | IRQ10 | FFE6$_H$ | FFE7$_H$ | L10 [1:0] | |
| — | IRQ11 | FFE4$_H$ | FFE5$_H$ | L11 [1:0] | |
| — | IRQ12 | FFE2$_H$ | FFE3$_H$ | L12 [1:0] | |
| — | IRQ13 | FFE0$_H$ | FFE1$_H$ | L13 [1:0] | |
| 8/16-bit composite timer ch. 1 (upper) | IRQ14 | FFDE$_H$ | FFDF$_H$ | L14 [1:0] | |
| — | IRQ15 | FFDC$_H$ | FFDD$_H$ | L15 [1:0] | |
| — | IRQ16 | FFDA$_H$ | FFDB$_H$ | L16 [1:0] | |
| — | IRQ17 | FFD8$_H$ | FFD9$_H$ | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6$_H$ | FFD7$_H$ | L18 [1:0] | |
| Time-base timer | IRQ19 | FFD4$_H$ | FFD5$_H$ | L19 [1:0] | |
| Watch prescaler | IRQ20 | FFD2$_H$ | FFD3$_H$ | L20 [1:0] | |
| — | IRQ21 | FFD0$_H$ | FFD1$_H$ | L21 [1:0] | |
| 8/16-bit composite timer ch. 1 (lower) | IRQ22 | FFCE$_H$ | FFCF$_H$ | L22 [1:0] | |
| Flash memory | IRQ23 | FFCC$_H$ | FFCD$_H$ | L23 [1:0] | Low |

## ■ INTERRUPT SOURCE TABLE (MB95570H Series)

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Priority order of interrupt sources of the same level (occurring simultaneously) |
|---|---|---|---|---|---|
| | | Upper | Lower | | |
| External interrupt ch. 4 | IRQ00 | FFFA$_H$ | FFFB$_H$ | L00 [1:0] | High |
| — | IRQ01 | FFF8$_H$ | FFF9$_H$ | L01 [1:0] | |
| — | IRQ02 | FFF6$_H$ | FFF7$_H$ | L02 [1:0] | |
| External interrupt ch. 6 | | | | | |
| — | IRQ03 | FFF4$_H$ | FFF5$_H$ | L03 [1:0] | |
| — | | | | | |
| — | IRQ04 | FFF2$_H$ | FFF3$_H$ | L04 [1:0] | |
| 8/16-bit composite timer ch. 0 (lower) | IRQ05 | FFF0$_H$ | FFF1$_H$ | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (upper) | IRQ06 | FFEE$_H$ | FFEF$_H$ | L06 [1:0] | |
| — | IRQ07 | FFEC$_H$ | FFED$_H$ | L07 [1:0] | |
| — | IRQ08 | FFEA$_H$ | FFEB$_H$ | L08 [1:0] | |
| — | IRQ09 | FFE8$_H$ | FFE9$_H$ | L09 [1:0] | |
| — | IRQ10 | FFE6$_H$ | FFE7$_H$ | L10 [1:0] | |
| — | IRQ11 | FFE4$_H$ | FFE5$_H$ | L11 [1:0] | |
| — | IRQ12 | FFE2$_H$ | FFE3$_H$ | L12 [1:0] | |
| — | IRQ13 | FFE0$_H$ | FFE1$_H$ | L13 [1:0] | |
| — | IRQ14 | FFDE$_H$ | FFDF$_H$ | L14 [1:0] | |
| — | IRQ15 | FFDC$_H$ | FFDD$_H$ | L15 [1:0] | |
| — | IRQ16 | FFDA$_H$ | FFDB$_H$ | L16 [1:0] | |
| — | IRQ17 | FFD8$_H$ | FFD9$_H$ | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6$_H$ | FFD7$_H$ | L18 [1:0] | |
| Time-base timer | IRQ19 | FFD4$_H$ | FFD5$_H$ | L19 [1:0] | |
| Watch prescaler | IRQ20 | FFD2$_H$ | FFD3$_H$ | L20 [1:0] | |
| — | IRQ21 | FFD0$_H$ | FFD1$_H$ | L21 [1:0] | |
| — | IRQ22 | FFCE$_H$ | FFCF$_H$ | L22 [1:0] | |
| Flash memory | IRQ23 | FFCC$_H$ | FFCD$_H$ | L23 [1:0] | Low |

## ■ INTERRUPT SOURCE TABLE (MB95580H Series)

| Interrupt source | Interrupt request number | Vector table address | | Bit name of interrupt level setting register | Priority order of interrupt sources of the same level (occurring simultaneously) |
|---|---|---|---|---|---|
| | | Upper | Lower | | |
| External interrupt ch. 4 | IRQ00 | FFFA$_H$ | FFFB$_H$ | L00 [1:0] | High |
| External interrupt ch. 5 | IRQ01 | FFF8$_H$ | FFF9$_H$ | L01 [1:0] | |
| External interrupt ch. 2 | IRQ02 | FFF6$_H$ | FFF7$_H$ | L02 [1:0] | |
| External interrupt ch. 6 | | | | | |
| External interrupt ch. 3 | IRQ03 | FFF4$_H$ | FFF5$_H$ | L03 [1:0] | |
| External interrupt ch. 7 | | | | | |
| — | IRQ04 | FFF2$_H$ | FFF3$_H$ | L04 [1:0] | |
| 8/16-bit composite timer ch. 0 (lower) | IRQ05 | FFF0$_H$ | FFF1$_H$ | L05 [1:0] | |
| 8/16-bit composite timer ch. 0 (upper) | IRQ06 | FFEE$_H$ | FFEF$_H$ | L06 [1:0] | |
| LIN-UART (reception) | IRQ07 | FFEC$_H$ | FFED$_H$ | L07 [1:0] | |
| LIN-UART (transmission) | IRQ08 | FFEA$_H$ | FFEB$_H$ | L08 [1:0] | |
| — | IRQ09 | FFE8$_H$ | FFE9$_H$ | L09 [1:0] | |
| — | IRQ10 | FFE6$_H$ | FFE7$_H$ | L10 [1:0] | |
| — | IRQ11 | FFE4$_H$ | FFE5$_H$ | L11 [1:0] | |
| — | IRQ12 | FFE2$_H$ | FFE3$_H$ | L12 [1:0] | |
| — | IRQ13 | FFE0$_H$ | FFE1$_H$ | L13 [1:0] | |
| — | IRQ14 | FFDE$_H$ | FFDF$_H$ | L14 [1:0] | |
| — | IRQ15 | FFDC$_H$ | FFDD$_H$ | L15 [1:0] | |
| — | IRQ16 | FFDA$_H$ | FFDB$_H$ | L16 [1:0] | |
| — | IRQ17 | FFD8$_H$ | FFD9$_H$ | L17 [1:0] | |
| 8/10-bit A/D converter | IRQ18 | FFD6$_H$ | FFD7$_H$ | L18 [1:0] | |
| Time-base timer | IRQ19 | FFD4$_H$ | FFD5$_H$ | L19 [1:0] | |
| Watch prescaler | IRQ20 | FFD2$_H$ | FFD3$_H$ | L20 [1:0] | |
| — | IRQ21 | FFD0$_H$ | FFD1$_H$ | L21 [1:0] | |
| — | IRQ22 | FFCE$_H$ | FFCF$_H$ | L22 [1:0] | |
| Flash memory | IRQ23 | FFCC$_H$ | FFCD$_H$ | L23 [1:0] | Low |

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6 | V | |
| Input voltage*1 | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6 | V | *2 |
| Output voltage*1 | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6 | V | *2 |
| Maximum clamp current | $I_{CLAMP}$ | –2 | +2 | mA | Applicable to specific pins*3 |
| Total maximum clamp current | $\Sigma\lvert I_{CLAMP}\rvert$ | — | 20 | mA | Applicable to specific pins*3 |
| "L" level maximum output current | $I_{OL}$ | — | 15 | mA | |
| "L" level average current | $I_{OLAV1}$ | — | 4 | mA | Other than P00 to P03, P05 to P07, P62 to P64*4<br>Average output current=<br>operating current × operating ratio (1 pin) |
| | $I_{OLAV2}$ | | 12 | | P00 to P03, P05 to P07, P62 to P64*4<br>Average output current=<br>operating current × operating ratio (1 pin) |
| "L" level total maximum output current | $\Sigma I_{OL}$ | — | 48 | mA | |
| "L" level total average output current | $\Sigma I_{OLAV}$ | — | 50 | mA | Total average output current=<br>operating current × operating ratio<br>(Total number of pins) |
| "H" level maximum output current | $I_{OH}$ | — | –15 | mA | |
| "H" level average current | $I_{OHAV1}$ | — | –4 | mA | Other than P00 to P03, P05 to P07, P62 to P64*4<br>Average output current=<br>operating current × operating ratio (1 pin) |
| | $I_{OHAV2}$ | | –8 | | P00 to P03, P05 to P07, P62 to P64*4<br>Average output current=<br>operating current × operating ratio (1 pin) |
| "H" level total maximum output current | $\Sigma I_{OH}$ | — | 48 | mA | |
| "H" level total average output current | $\Sigma I_{OHAV}$ | — | –50 | mA | Total average output current=<br>operating current × operating ratio<br>(Total number of pins) |
| Power consumption | $P_d$ | — | 320 | mW | |
| Operating temperature | $T_A$ | –40 | +85 | °C | |
| Storage temperature | $T_{stg}$ | –55 | +150 | °C | |

*(Continued)*

*(Continued)*

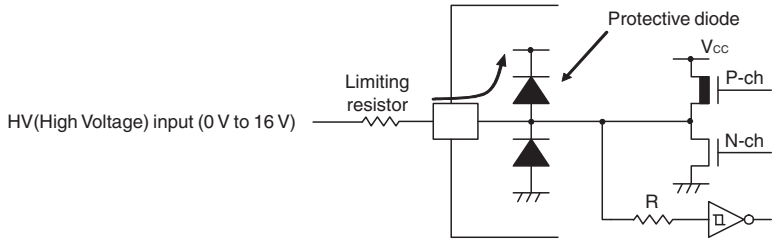
*1: These parameters are based on the condition that $V_{SS}$ is 0.0 V.

*2: $V_I$ and $V_O$ must not exceed $V_{CC}$ + 0.3 V. $V_I$ must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the $I_{CLAMP}$ rating is used instead of the $V_I$ rating.

*3: Applicable to the following pins: P00 to P07, P62 to P64, PF0, PF1, PG1, PG2 (P00, and P62 to P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K. P01, P02, P03, P07, PF0. PF1, PG1, and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.)

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the $V_{CC}$ voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the $V_{CC}$ pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

  - Input/Output equivalent circuit




*4: P62 and P63 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

($V_{SS}$ = 0.0 V)

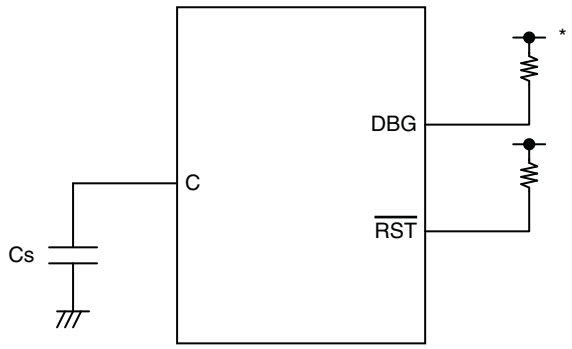
| Parameter | Symbol | Value | | Unit | Remarks | |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| Power supply voltage | $V_{CC}$ | 2.4*1*2 | 5.5*1 | V | In normal operation | Other than on-chip debug mode |
| | | 2.3 | 5.5 | | Hold condition in stop mode | |
| | | 2.9 | 5.5 | | In normal operation | On-chip debug mode |
| | | 2.3 | 5.5 | | Hold condition in stop mode | |
| Decoupling capacitor | $C_S$ | 0.022 | 1 | µF | *3 | |
| Operating temperature | $T_A$ | −40 | +85 | °C | Other than on-chip debug mode | |
| | | +5 | +35 | | On-chip debug mode | |

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the $V_{CC}$ pin must have a capacitance larger than $C_S$. For the connection to a decoupling capacitor $C_S$, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and $C_S$ and the distance between $C_S$ and the $V_{SS}$ pin when designing the layout of a printed circuit board.

- DBG / $\overline{\text{RST}}$ / C pins connection diagram




*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/EC0/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 3. DC Characteristics

($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IH}$ | P04 | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Hysteresis input |
| | $V_{IHS}$ | P00*3 to P03*4, P05 to P07*4, P12, P62 to P64*3, PF0*4, PF1*4, PG1*4, PG2*4 | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Hysteresis input |
| | $V_{IHM}$ | PF2 | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Hysteresis input |
| "L" level input voltage | $V_{IL}$ | P04 | — | $V_{SS}$ – 0.3 | — | 0.3 $V_{CC}$ | V | Hysteresis input |
| | $V_{ILS}$ | P00*3 to P03*4, P05 to P07*4, P12, P62 to P64*3, PF0*4, PF1*4, PG1*4, PG2*4 | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | Hysteresis input |
| | $V_{ILM}$ | PF2 | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | Hysteresis input |
| Open-drain output application voltage | $V_D$ | P12, PF2 | — | $V_{SS}$ – 0.3 | — | $V_{SS}$ + 5.5 | V | |
| "H" level output voltage | $V_{OH1}$ | P04, PF0*4, PF1*4, PG1*4, PG2*4 | $I_{OH}$ = –4 mA | $V_{CC}$ – 0.5 | — | — | V | |
| | $V_{OH2}$ | P00*3 to P03*4, P05 to P07*4, P62 to P64*3 | $I_{OH}$ = –8 mA | $V_{CC}$ – 0.5 | — | — | V | |
| "L" level output voltage | $V_{OL1}$ | P04, P12, PF0 to PF2*4, PG1*4, PG2*4 | $I_{OL}$ = 4 mA | — | — | 0.4 | V | |
| | $V_{OL2}$ | P00*3 to P03*4, P05 to P07*4, P62 to P64*3 | $I_{OL}$ = 12 mA | — | — | 0.4 | V | |
| Input leak current (Hi-Z output leak current) | $I_{LI}$ | All input pins | 0.0 V < $V_I$ < $V_{CC}$ | –5 | — | +5 | µA | When pull-up resistance is disabled |
| Pull-up resistance | $R_{PULL}$ | P00*3 to P07*4, P62 to P64*3, PG1*4, PG2*4 | $V_I$ = 0 V | 25 | 50 | 100 | kΩ | When pull-up resistance is enabled |
| Input capacitance | $C_{IN}$ | Other than $V_{CC}$ and $V_{SS}$ | f = 1 MHz | — | 5 | 15 | pF | |

*(Continued)*

($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ*1 | Max*2 | | |
| Power supply current*5 | $I_{CC}$ | $V_{CC}$ (External clock operation) | $F_{CH}$ = 32 MHz<br>$F_{MP}$ = 16 MHz<br>Main clock mode (divided by 2) | — | 3.5 | 4.4 | mA | Except during Flash memory programming and erasing |
| | | | | — | 7.4 | 9.8 | mA | During Flash memory programming and erasing |
| | | | | — | 5.1 | 6.4 | mA | At A/D conversion |
| | $I_{CCS}$ | | $F_{CH}$ = 32 MHz<br>$F_{MP}$ = 16 MHz<br>Main sleep mode (divided by 2) | — | 1.2 | 1.5 | mA | |
| | $I_{CCL}$ | | $F_{CL}$ = 32 kHz<br>$F_{MPL}$ = 16 kHz<br>Subclock mode (divided by 2)<br>$T_A$ = +25°C | — | 65 | 71 | µA | |
| | $I_{CCLS}$*6 | | $F_{CL}$ = 32 kHz<br>$F_{MPL}$ = 16 kHz<br>Subsleep mode (divided by 2)<br>$T_A$ = +25°C | — | 5.4 | 7 | µA | In deep standby mode |
| | $I_{CCT}$*6 | | $F_{CL}$ = 32 kHz<br>Watch mode<br>$T_A$ = +25°C | — | 4.8 | 6.9 | µA | In deep standby mode |
| | $I_{CCMCR}$ | $V_{CC}$ | $F_{CRH}$ = 4 MHz<br>$F_{MP}$ = 4 MHz<br>Main CR clock mode | — | 1.1 | 1.4 | mA | |
| | $I_{CCSCR}$ | | Sub-CR clock mode (divided by 2)<br>$T_A$ = +25°C | — | 58 | 64 | µA | |
| | $I_{CCTS}$ | $V_{CC}$ (External clock operation) | $F_{CH}$ = 32 MHz<br>Time-base timer mode<br>$T_A$ = +25°C | — | 290 | 340 | µA | In deep standby mode |
| | $I_{CCH}$ | | Main stop mode (single external clock product)/ Substop mode (dual external clock product)<br>$T_A$ = +25°C | — | 4.1 | 6.5 | µA | In deep standby mode |

*(Continued)*

*(Continued)*

($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ*1 | Max*2 | | |
| Power supply current*5 | $I_{LVD}$ | $V_{CC}$ | Current consumption for the low-voltage detection circuit | — | 3.6 | 6.6 | µA | |
| | $I_{CRH}$ | | Current consumption for the main CR oscillator | — | 220 | 280 | µA | |
| | $I_{CRL}$ | | Current consumption for the sub-CR oscillator oscillating at 100 kHz | — | 5.1 | 9.3 | µA | |
| | $I_{NSTBY}$ | | Current consumption difference between normal standby mode and deep standby mode $T_A$ = +25°C | — | 20 | 30 | µA | |

*1: $V_{CC}$ = 5.0 V, $T_A$ = + 25°C

*2: $V_{CC}$ = 5.5 V, $T_A$ = + 85°C (unless otherwise specified)

*3: P00, P62, P63 and P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

*4: P01, P02, P03, P07, PF0, PF1, PG1 and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.

*5:
- The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit ($I_{LVD}$) to one of the value from $I_{CC}$ to $I_{CCH}$. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators ($I_{CRH}$, $I_{CRL}$) and a specified value. In on-chip debug mode, the CR oscillator ($I_{CRH}$) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.
- See "4. AC Characteristics: (1) Clock Timing" for $F_{CH}$ and $F_{CL}$.
- See "4. AC Characteristics: (2) Source Clock / Machine Clock" for $F_{MP}$ and $F_{MPL}$.

*6: In sub-CR clock mode, the power supply current value is the sum of adding $I_{CRL}$ to $I_{CCLS}$ or $I_{CCT}$. In addition, when the sub-CR clock mode is selected with $F_{MPL}$ being 50 kHz, the current consumption increases accordingly.

## 4. AC Characteristics

### (1) Clock Timing

($V_{CC}$ = 2.4 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock frequency | $F_{CH}$ | X0, X1 | — | 1 | — | 16.25 | MHz | When the main oscillation circuit is used |
| | | X0 | X1: open | 1 | — | 12 | MHz | When the main external clock is used |
| | | X0, X1 | * | 1 | — | 32.5 | MHz | |
| | $F_{CRH}$ | — | — | 3.92 | 4 | 4.08 | MHz | Operating conditions<br>• The main CR clock is used.<br>• 0°C ≤ $T_A$ < +70°C |
| | | | | 3.8 | 4 | 4.2 | MHz | Operating conditions<br>• The main CR clock is used.<br>• –40°C ≤ $T_A$ < 0°C<br>• +70°C ≤ $T_A$ < +85°C |
| | $F_{MCRPLL}$ | — | — | 7.84 | 8 | 8.16 | MHz | Operating conditions<br>• PLL multiplier: 2<br>• 0°C ≤ $T_A$ < +70°C |
| | | | | 7.6 | 8 | 8.4 | MHz | Operating conditions<br>• PLL multiplier: 2<br>• –40°C ≤ $T_A$ < 0°C<br>• +70°C ≤ $T_A$ < +85°C |
| | | | | 9.8 | 10 | 10.2 | MHz | Operating conditions<br>• PLL multiplier: 2.5<br>• 0°C ≤ $T_A$ < +70°C |
| | | | | 9.5 | 10 | 10.5 | MHz | Operating conditions<br>• PLL multiplier: 2.5<br>• –40°C ≤ $T_A$ < 0°C<br>• +70°C ≤ $T_A$ < +85°C |
| | | | | 11.76 | 12 | 12.24 | MHz | Operating conditions<br>• PLL multiplier: 3<br>• 0°C ≤ $T_A$ < +70°C |
| | | | | 11.4 | 12 | 12.6 | MHz | Operating conditions<br>• PLL multiplier: 3<br>• –40°C ≤ $T_A$ < 0°C<br>• +70°C ≤ $T_A$ < +85°C |
| | | | | 15.68 | 16 | 16.32 | MHz | Operating conditions<br>• PLL multiplier: 4<br>• 0°C ≤ $T_A$ < +70°C |
| | | | | 15.2 | 16 | 16.8 | MHz | Operating conditions<br>• PLL multiplier: 4<br>• –40°C ≤ $T_A$ < 0°C<br>• +70°C ≤ $T_A$ < +85°C |
| | $F_{CL}$ | X0A, X1A | — | — | 32.768 | — | kHz | When the suboscillation circuit is used |
| | | | | — | 32.768 | — | kHz | When the sub-external clock is used |
| | $F_{CRL}$ | — | — | 50 | 100 | 150 | kHz | When the sub-CR clock is used |

*(Continued)*

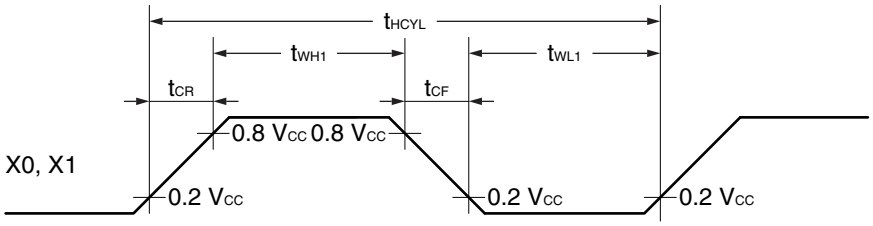
*(Continued)*

($V_{CC}$ = 2.4 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | — | 61.5 | — | 1000 | ns | When the main oscillation circuit is used |
| | | X0 | X1 : open | 83.4 | — | 1000 | ns | When an external clock is used |
| | | X0, X1 | * | 30.8 | — | 1000 | ns | |
| | $t_{LCYL}$ | X0A, X1A | — | — | 30.5 | — | µs | When the subclock is used |
| Input clock pulse width | $t_{WH1}$<br>$t_{WL1}$ | X0 | X1 : open | 33.4 | — | — | ns | When an external clock is used, the duty ratio should range between 40% and 60%. |
| | | X0, X1 | * | 12.4 | — | — | ns | |
| | $t_{WH2}$<br>$t_{WL2}$ | X0A | — | — | 15.2 | — | µs | |
| Input clock rise time and fall time | $t_{CR}$<br>$t_{CF}$ | X0 | X1 : open | — | — | 5 | ns | When an external clock is used |
| | | X0, X1 | * | — | — | 5 | ns | |
| CR oscillation start time | $t_{CRHWK}$ | — | — | — | — | 50 | µs | When the main CR clock is used |
| | $t_{CRLWK}$ | — | — | — | — | 30 | µs | When the sub-CR clock is used |

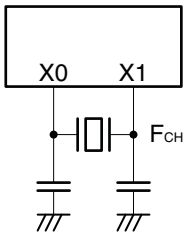
*: The external clock signal is input to X0 and the inverted external clock signal to X1.

- Input waveform generated when an external clock (main clock) is used

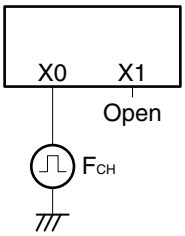



- Figure of main clock input port external connection

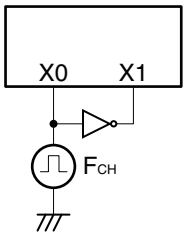
When a crystal oscillator or a ceramic oscillator is used



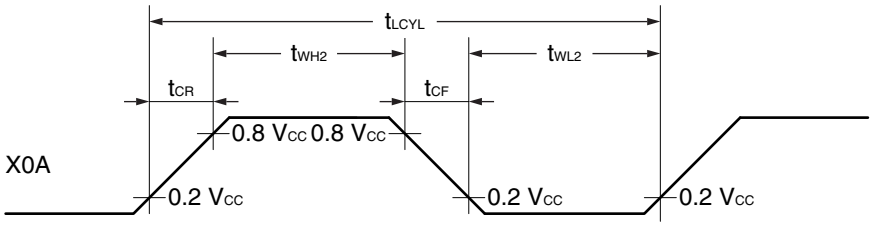

When an external clock is used (X1 is open)




When an external clock is used

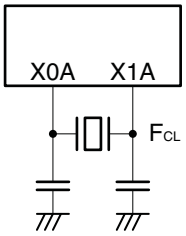



- Input waveform generated when an external clock (subclock) is used

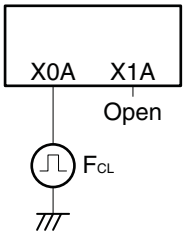



- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used




When an external clock is used



### (2) Source Clock / Machine Clock

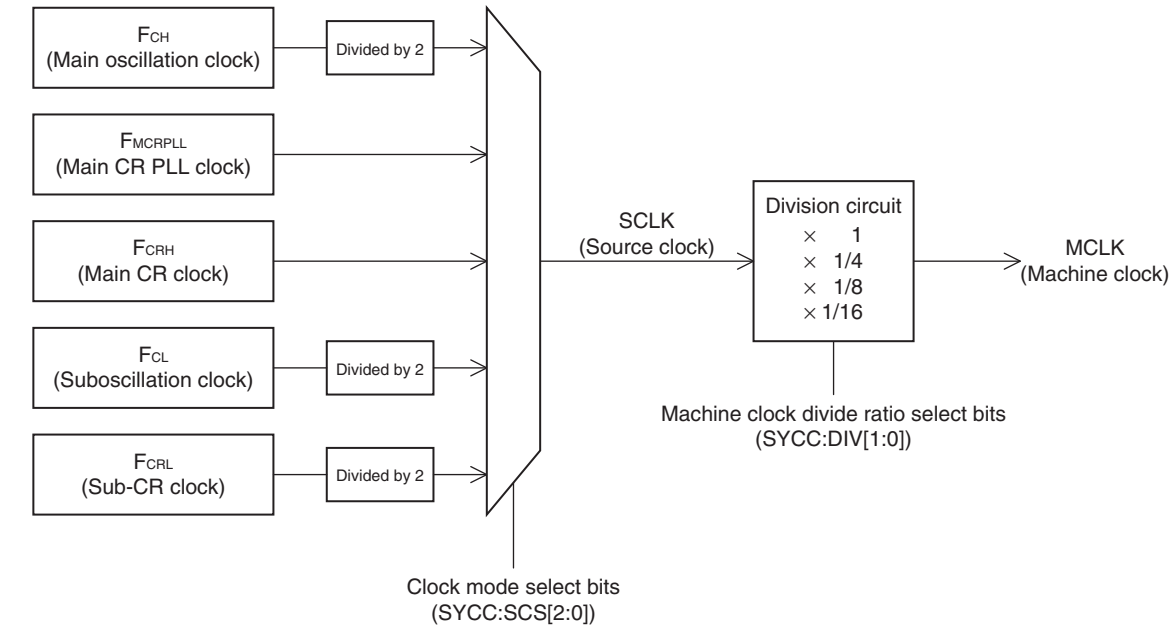
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Source clock cycle time*1 | $t_{SCLK}$ | — | 61.5 | — | 2000 | ns | When the main external clock is used<br>Min: $F_{CH}$ = 32.5 MHz, divided by 2<br>Max: $F_{CH}$ = 1 MHz, divided by 2 |
| | | | 62.5 | — | 1000 | ns | When the main CR clock is used<br>Min: $F_{CRH}$ = 4 MHz, multiplied by 4<br>Max: $F_{CRH}$ = 4 MHz, divided by 4 |
| | | | — | 61 | — | µs | When the suboscillation clock is used<br>$F_{CL}$ = 32.768 kHz, divided by 2 |
| | | | — | 20 | — | µs | When the sub-CR clock is used<br>$F_{CRL}$ = 100 kHz, divided by 2 |
| Source clock frequency | $F_{SP}$ | — | 0.5 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | — | 4 | — | MHz | When the main CR clock is used |
| | $F_{SPL}$ | | — | 16.384 | — | kHz | When the suboscillation clock is used |
| | | | — | 50 | — | kHz | When the sub-CR clock is used<br>$F_{CRL}$ = 100 kHz, divided by 2 |
| Machine clock cycle time*2 (minimum instruction execution time) | $t_{MCLK}$ | — | 61.5 | — | 32000 | ns | When the main oscillation clock is used<br>Min: $F_{SP}$ = 16.25 MHz, no division<br>Max: $F_{SP}$ = 0.5 MHz, divided by 16 |
| | | | 250 | — | 1000 | ns | When the main CR clock is used<br>Min: $F_{SP}$ = 4 MHz, no division<br>Max: $F_{SP}$ = 4 MHz, divided by 4 |
| | | | 61 | — | 976.5 | µs | When the suboscillation clock is used<br>Min: $F_{SPL}$ = 16.384 kHz, no division<br>Max: $F_{SPL}$ = 16.384 kHz, divided by 16 |
| | | | 20 | — | 320 | µs | When the sub-CR clock is used<br>Min: $F_{SPL}$ = 50 kHz, no division<br>Max: $F_{SPL}$ = 50 kHz, divided by 16 |
| Machine clock frequency | $F_{MP}$ | — | 0.031 | — | 16.25 | MHz | When the main oscillation clock is used |
| | | | 0.25 | — | 16 | MHz | When the main CR clock is used |
| | $F_{MPL}$ | | 1.024 | — | 16.384 | kHz | When the suboscillation clock is used |
| | | | 3.125 | — | 50 | kHz | When the sub-CR clock is used<br>$F_{CRL}$ = 100 kHz |

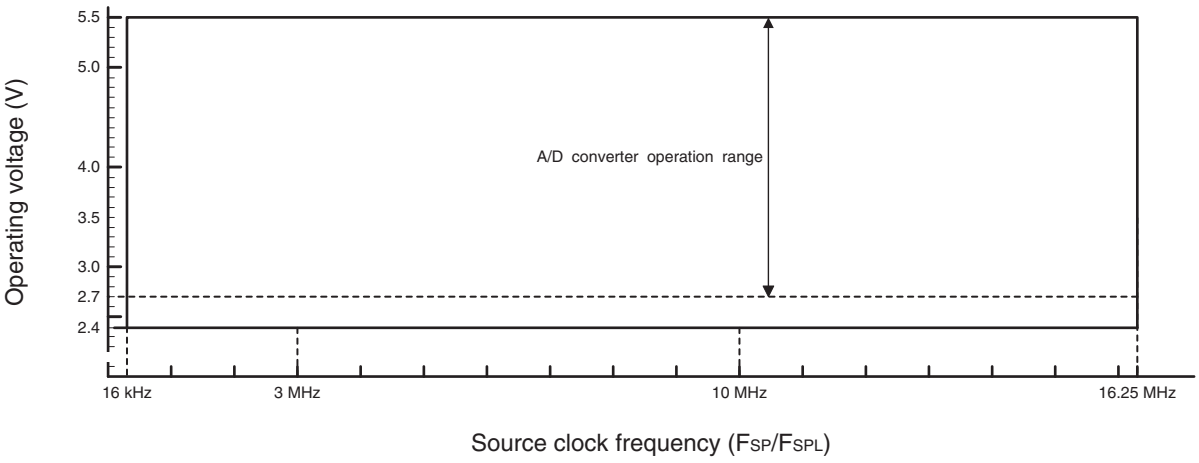
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.
- Main clock divided by 2
- PLL multiplication of main CR clock (Select a multiplier from 2, 2.5, 3 and 4.)
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

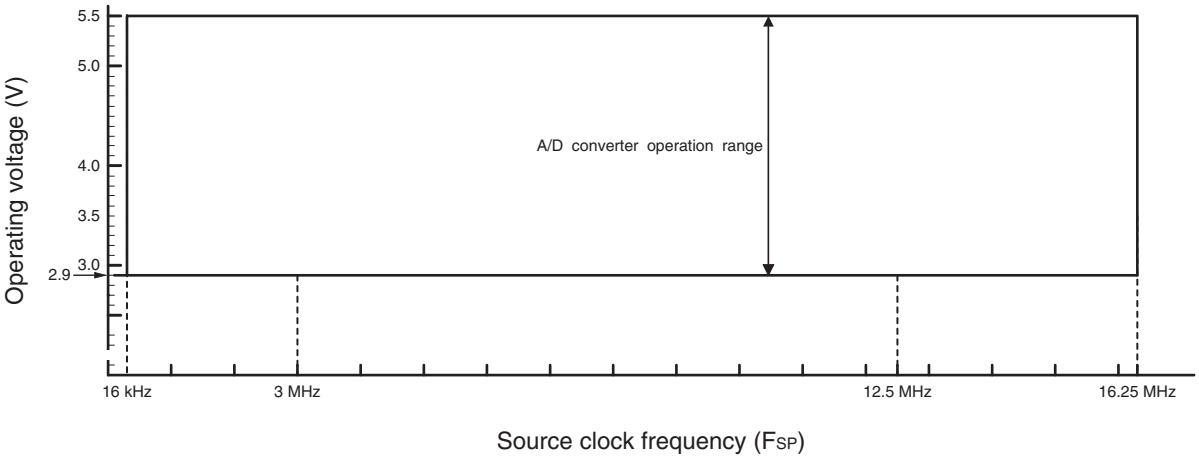
- Schematic diagram of the clock generation block




- Operating voltage - Operating frequency ($T_A$ = −40°C to +85°C)
  Without the on-chip debug function




- Operating voltage - Operating frequency ($T_A$ = −40°C to +85°C)
  With the on-chip debug function



### (3) External Reset

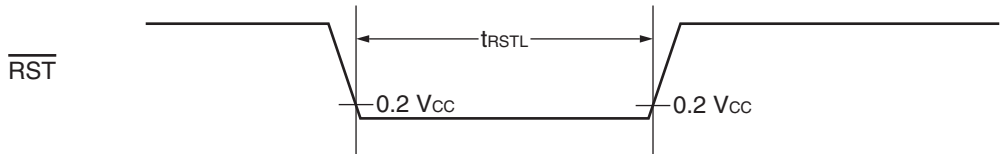
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $\overline{RST}$ "L" level pulse width | $t_{RSTL}$ | 2 $t_{MCLK}$*1 | — | ns | In normal operation |
| | | Oscillation time of the oscillator*2 + 200 | — | µs | In stop mode, subclock mode, subsleep mode, watch mode, and power-on |
| | | 200 | — | µs | In time-base timer mode |

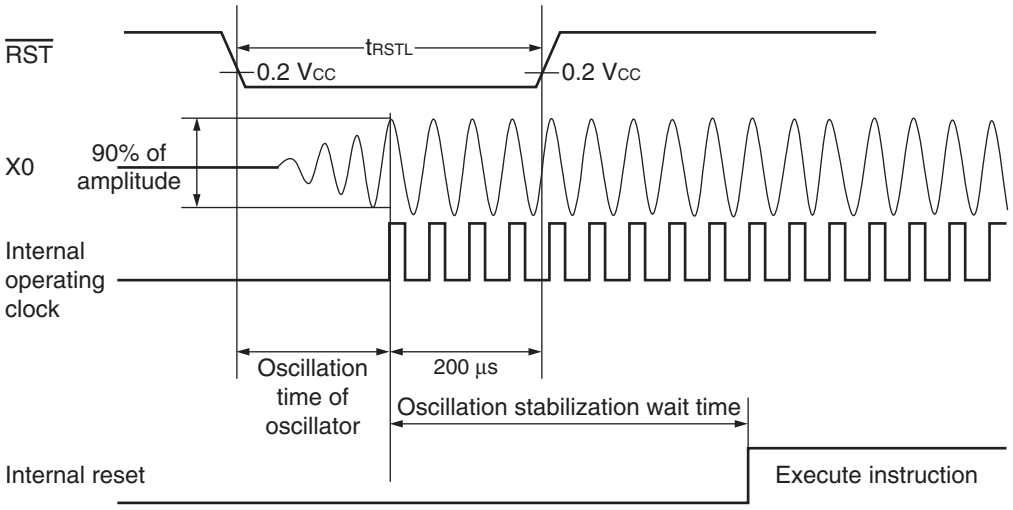
*1: See "(2) Source Clock / Machine Clock" for $t_{MCLK}$.

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator has an oscillation time of between several µs and several ms.

- In normal operation



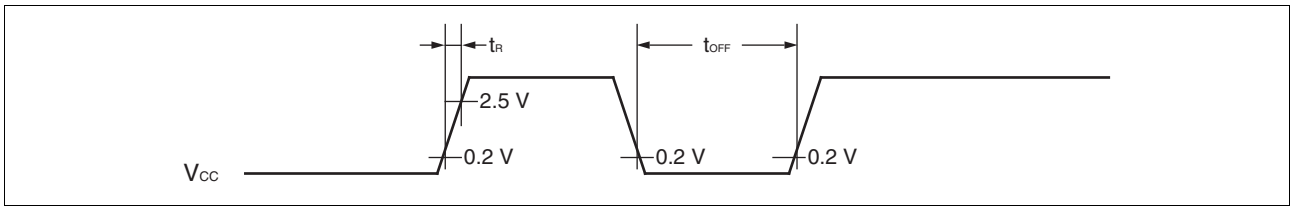

- In stop mode, subclock mode, subsleep mode, watch mode and power-on



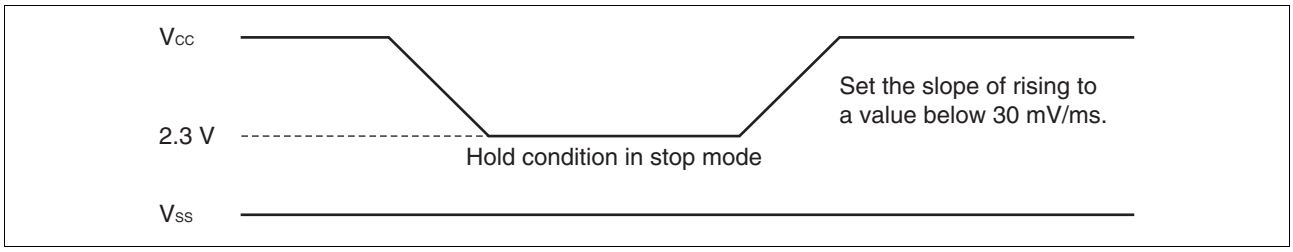
### (4) Power-on Reset

($V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Power supply rising time | $t_R$ | — | — | 50 | ms | |
| Power supply cutoff time | $t_{OFF}$ | — | 1 | — | ms | Wait time until power-on |



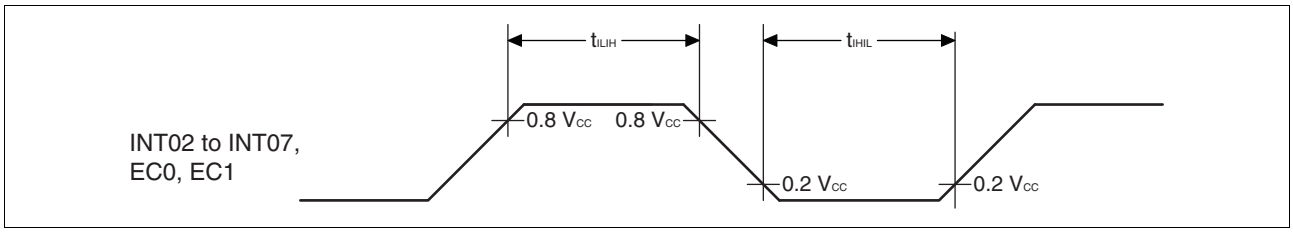

Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



### (5) Peripheral Input Timing

($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Peripheral input “H” pulse width | $t_{ILIH}$ | INT02 to INT07*1,*2, EC0*1, EC1*3 | 2 $t_{MCLK}$*4 | — | ns |
| Peripheral input “L” pulse width | $t_{IHIL}$ | | 2 $t_{MCLK}$*4 | — | ns |




*1: INT04, INT06 and EC0 are available on all products.

*2: INT02, INT03, INT05 and INT07 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.

*3: EC1 is only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

*4: See “(2) Source Clock / Machine Clock” for $t_{MCLK}$.

### (6) LIN-UART Timing (only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K)

**Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2. (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)**

($V_{CC}$ = 5.0 V ± 10%, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

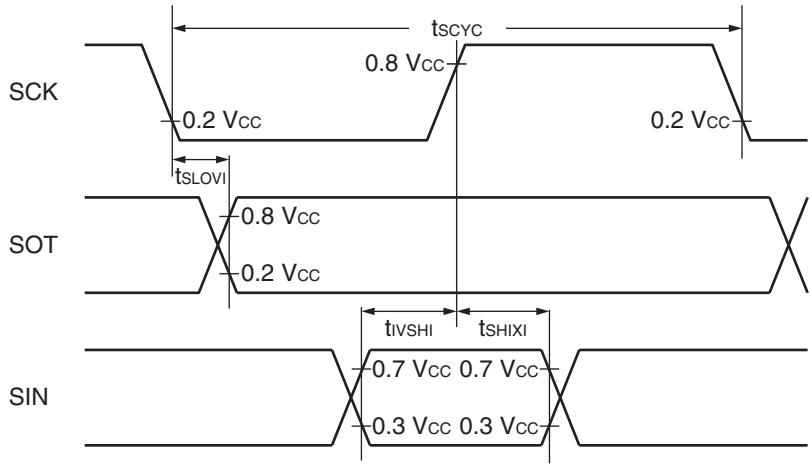
| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin: $C_L$ = 80 pF + 1 TTL | 5 $t_{MCLK}$*3 | — | ns |
| SCK ↓→ SOT delay time | $t_{SLOVI}$ | SCK, SOT | | –50 | +50 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCK, SIN | | $t_{MCLK}$*3 + 80 | — | ns |
| SCK ↑→ valid SIN hold time | $t_{SHIXI}$ | SCK, SIN | | 0 | — | ns |
| Serial clock ?L? pulse width | $t_{SLSH}$ | SCK | External clock operation output pin: $C_L$ = 80 pF + 1 TTL | 3 $t_{MCLK}$*3 – $t_R$ | — | ns |
| Serial clock ?H? pulse width | $t_{SHSL}$ | SCK | | $t_{MCLK}$*3 + 10 | — | ns |
| SCK ↓→ SOT delay time | $t_{SLOVE}$ | SCK, SOT | | — | 2 $t_{MCLK}$*3 + 60 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHE}$ | SCK, SIN | | 30 | — | ns |
| SCK ↑→ valid SIN hold time | $t_{SHIXE}$ | SCK, SIN | | $t_{MCLK}$*3 + 30 | — | ns |
| SCK fall time | $t_F$ | SCK | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK | | — | 10 | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

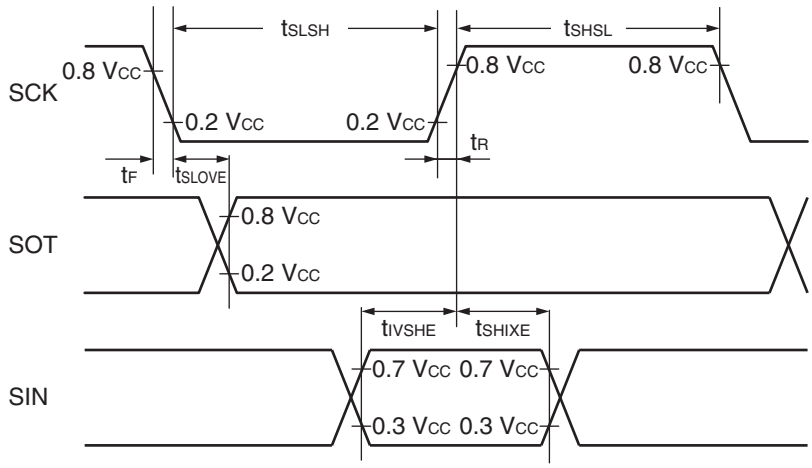
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock / Machine Clock” for $t_{MCLK}$.

- Internal shift clock mode




- External shift clock mode



**Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2. (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)**

($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

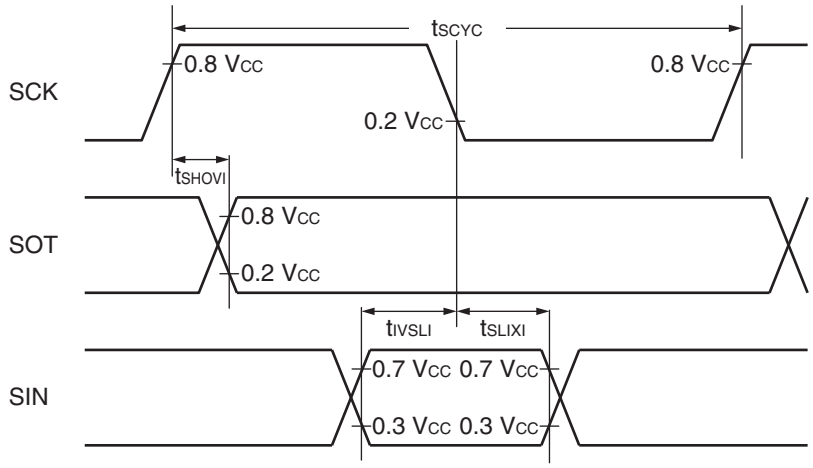
| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin: $C_L$ = 80 pF + 1 TTL | 5 $t_{MCLK}$*3 | — | ns |
| SCK ↑→ SOT delay time | $t_{SHOVI}$ | SCK, SOT | | –50 | +50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLI}$ | SCK, SIN | | $t_{MCLK}$*3 + 80 | — | ns |
| SCK ↓→ valid SIN hold time | $t_{SLIXI}$ | SCK, SIN | | 0 | — | ns |
| Serial clock ?H? pulse width | $t_{SHSL}$ | SCK | External clock operation output pin: $C_L$ = 80 pF + 1 TTL | 3 $t_{MCLK}$*3 – $t_R$ | — | ns |
| Serial clock ?L? pulse width | $t_{SLSH}$ | SCK | | $t_{MCLK}$*3 + 10 | — | ns |
| SCK ↑→ SOT delay time | $t_{SHOVE}$ | SCK, SOT | | — | 2 $t_{MCLK}$*3 + 60 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLE}$ | SCK, SIN | | 30 | — | ns |
| SCK ↓→ valid SIN hold time | $t_{SLIXE}$ | SCK, SIN | | $t_{MCLK}$*3 + 30 | — | ns |
| SCK fall time | $t_F$ | SCK | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK | | — | 10 | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

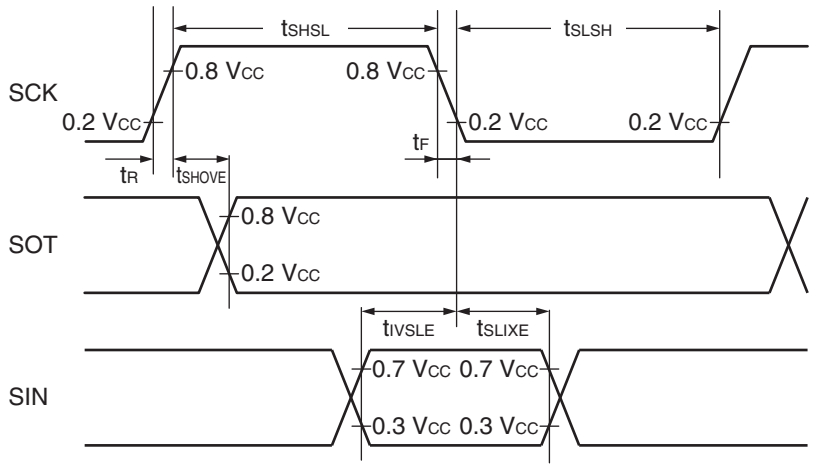
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “(2) Source Clock / Machine Clock” for $t_{MCLK}$.

- Internal shift clock mode




- External shift clock mode



**Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2. (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)**

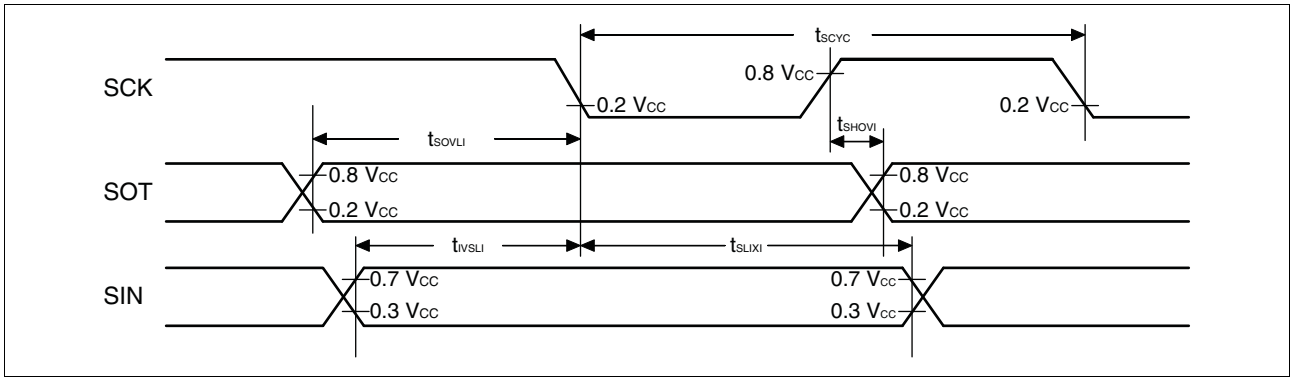
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation output pin: $C_L$ = 80 pF + 1 TTL | 5 $t_{MCLK}$*3 | — | ns |
| SCK ↑→ SOT delay time | $t_{SHOVI}$ | SCK, SOT | | –50 | +50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLI}$ | SCK, SIN | | $t_{MCLK}$*3 + 80 | — | ns |
| SCK ↓→ valid SIN hold time | $t_{SLIXI}$ | SCK, SIN | | 0 | — | ns |
| SOT → SCK ↓ delay time | $t_{SOVLI}$ | SCK, SOT | | 3 $t_{MCLK}$*3 – 70 | — | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “(2) Source Clock / Machine Clock” for $t_{MCLK}$.



**Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2. (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)**

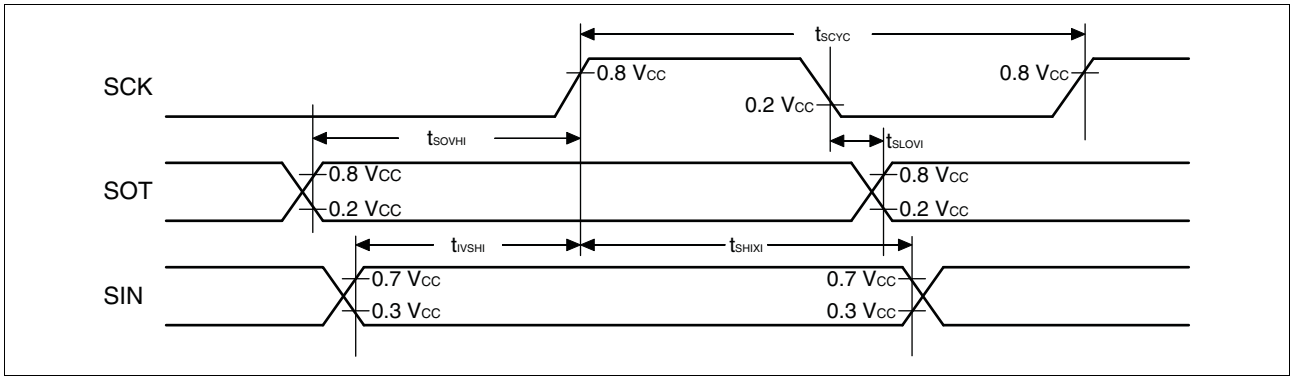
($V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operating output pin: $C_L$ = 80 pF + 1 TTL | 5 $t_{MCLK}$*3 | — | ns |
| SCK ↓→ SOT delay time | $t_{SLOVI}$ | SCK, SOT | | –50 | +50 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCK, SIN | | $t_{MCLK}$*3 + 80 | — | ns |
| SCK ↑→ valid SIN hold time | $t_{SHIXI}$ | SCK, SIN | | 0 | — | ns |
| SOT → SCK ↑ delay time | $t_{SOVHI}$ | SCK, SOT | | 3 $t_{MCLK}$*3 – 70 | — | ns |

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “(2) Source Clock / Machine Clock” for $t_{MCLK}$.

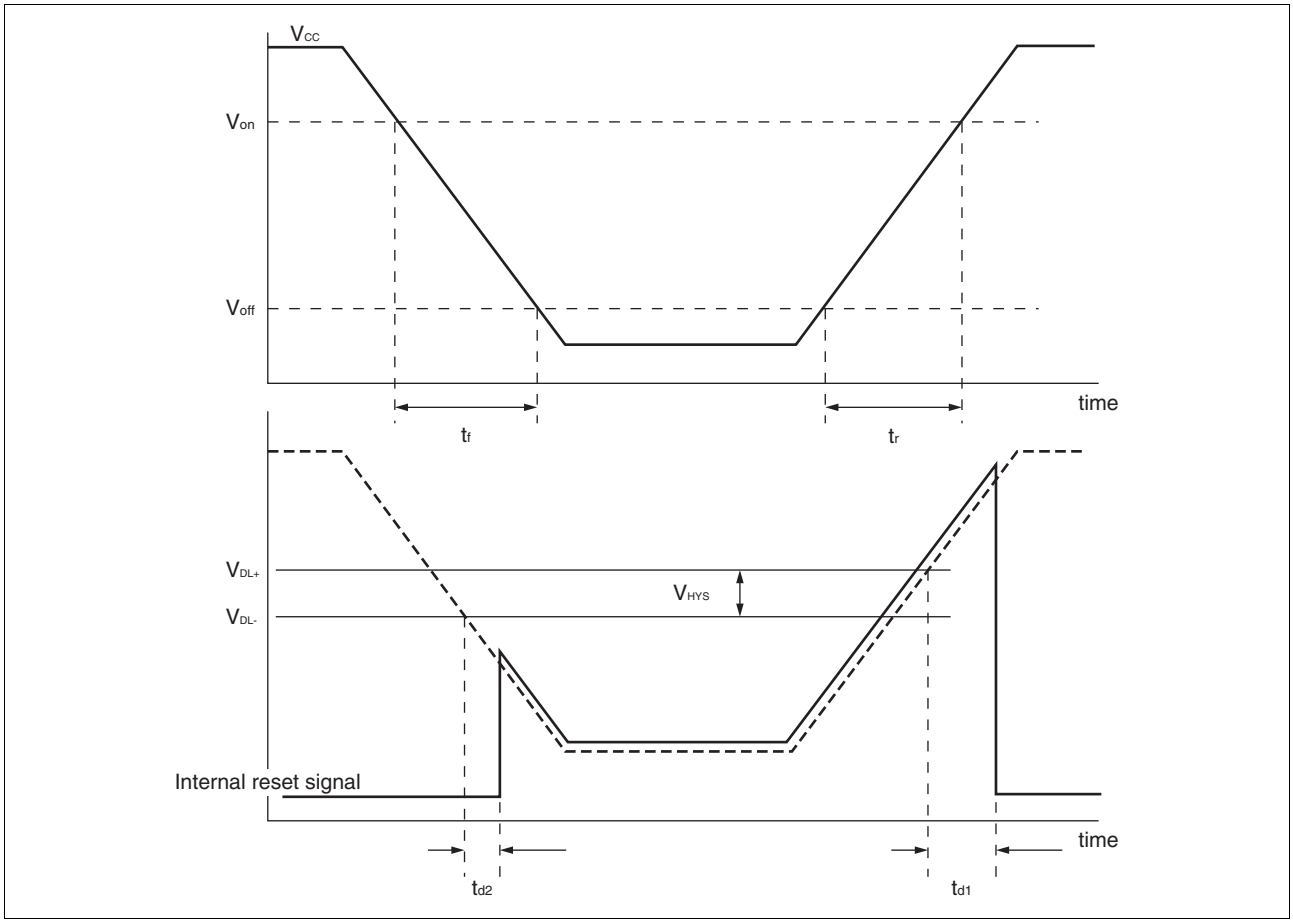


### (7) Low-voltage Detection

($V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Release voltage* | $V_{DL+}$ | 2.52 | 2.7 | 2.88 | V | At power supply rise |
| | | 2.61 | 2.8 | 2.99 | | |
| | | 2.89 | 3.1 | 3.31 | | |
| | | 3.08 | 3.3 | 3.52 | | |
| Detection voltage* | $V_{DL-}$ | 2.43 | 2.6 | 2.77 | V | At power supply fall |
| | | 2.52 | 2.7 | 2.88 | | |
| | | 2.80 | 3 | 3.20 | | |
| | | 2.99 | 3.2 | 3.41 | | |
| Hysteresis width | $V_{HYS}$ | — | 100 | — | mV | |
| Power supply start voltage | $V_{off}$ | — | — | 2.3 | V | |
| Power supply end voltage | $V_{on}$ | 4.9 | — | — | V | |
| Power supply voltage change time (at power supply rise) | $t_r$ | 650 | — | — | µs | Slope of power supply that the reset release signal generates within the rating ($V_{DL+}$) |
| Power supply voltage change time (at power supply fall) | $t_f$ | 650 | — | — | µs | Slope of power supply that the reset detection signal generates within the rating ($V_{DL-}$) |
| Reset release delay time | $t_{d1}$ | — | — | 30 | µs | |
| Reset detection delay time | $t_{d2}$ | — | — | 30 | µs | |
| LVD threshold voltage transition stabilization time | $t_{stb}$ | 10 | — | — | µs | |

*: The release voltage and the detection voltage can be selected by using the LVD reset voltage selection ID register (LVDR) in the low-voltage detection reset circuit. For details of the LVDR register, refer to “CHAPTER 18 LOW-VOLTAGE DETECTION RESET CIRCUIT” in the hardware manual of the MB95560H/570H/580H Series.


$V_{CC}$
$V_{on}$
$V_{off}$
time
$t_f$
$t_r$
$V_{DL+}$
$V_{DL-}$
$V_{HYS}$
Internal reset signal
time
$t_{d2}$
$t_{d1}$

## 5. A/D Converter

### (1) A/D Converter Electrical Characteristics

($V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0.0 V, $T_A$ = –40°C to +85°C)

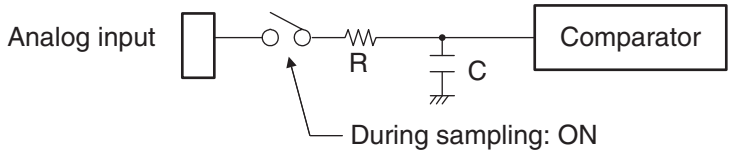
| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | bit | |
| Total error | | –3 | — | +3 | LSB | |
| Linearity error | | –2.5 | — | +2.5 | LSB | |
| Differential linearity error | | –1.9 | — | +1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | $V_{SS}$ – 1.5 LSB | $V_{SS}$ + 0.5 LSB | $V_{SS}$ + 2.5 LSB | V | |
| Full-scale transition voltage | $V_{FST}$ | $V_{CC}$ – 4.5 LSB | $V_{CC}$ – 2 LSB | $V_{CC}$ + 0.5 LSB | V | |
| Compare time | — | 1 | — | 10 | µs | 4.5 V ≤ $V_{CC}$ ≤ 5.5 V |
| | | 3 | — | 10 | µs | 2.7 V ≤ $V_{CC}$ < 4.5 V |
| Sampling time | — | 0.6 | — | ∞ | µs | 2.7 V ≤ $V_{CC}$ ≤ 5.5 V, with external impedance < 3.3 kΩ |
| Analog input current | $I_{AIN}$ | –0.3 | — | +0.3 | µA | |
| Analog input voltage | $V_{AIN}$ | $V_{SS}$ | — | $V_{CC}$ | V | |

### (2) Notes on Using A/D Converter

- External impedance of analog input and its sampling time

  The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

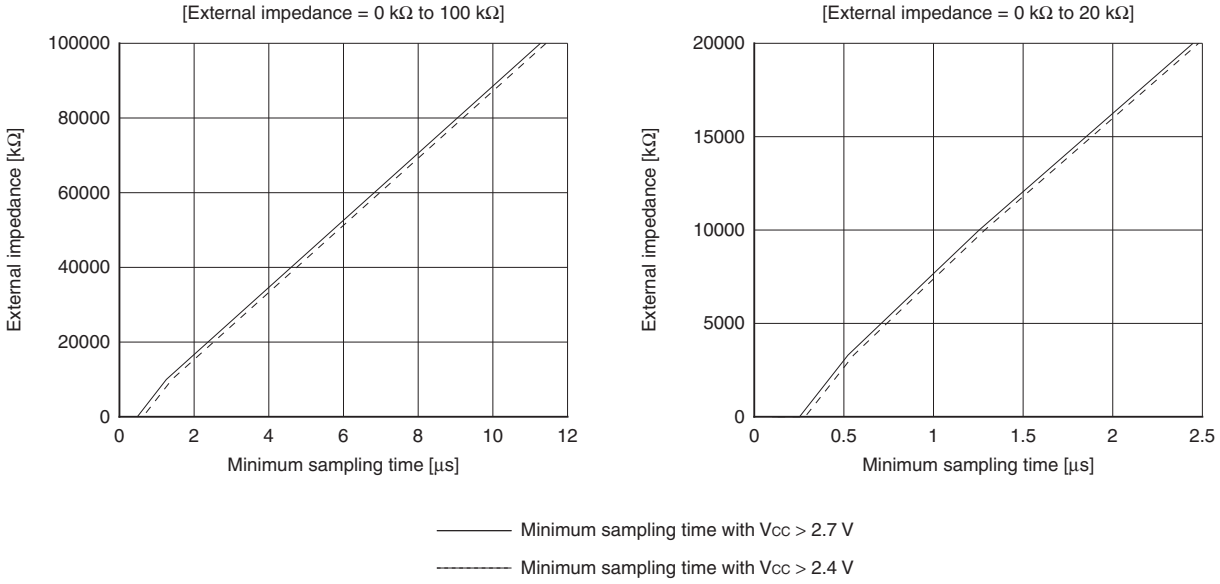
- Analog input equivalent circuit




| $V_{CC}$ | R | C |
|---|---|---|
| 4.5 V ≤ $V_{CC}$ ≤ 5.5 V | 3.3 kΩ (Max) | 14.89 pF (Max) |
| 2.7 V ≤ $V_{CC}$ < 5.5 V | 5.7 kΩ (Max) | 14.89 pF (Max) |

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time

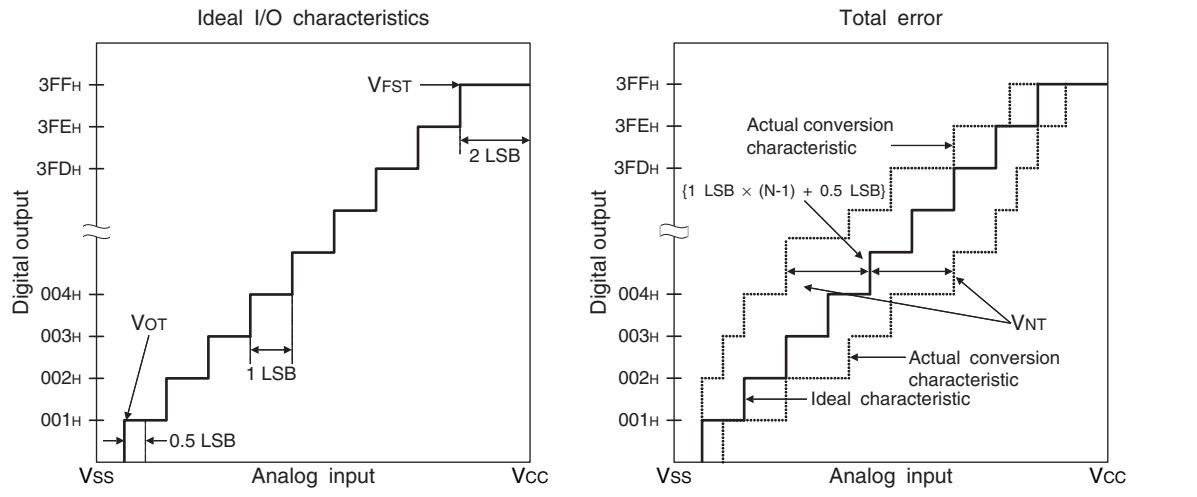



- A/D conversion error

  As |$V_{CC}$ – $V_{SS}$| decreases, the A/D conversion error increases proportionately.

### (3) Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10}$ = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“0000000000” ← → “0000000001”) of a device to the full-scale transition point (“1111111111” ← → “1111111110”) of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.




$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (\text{V})$$

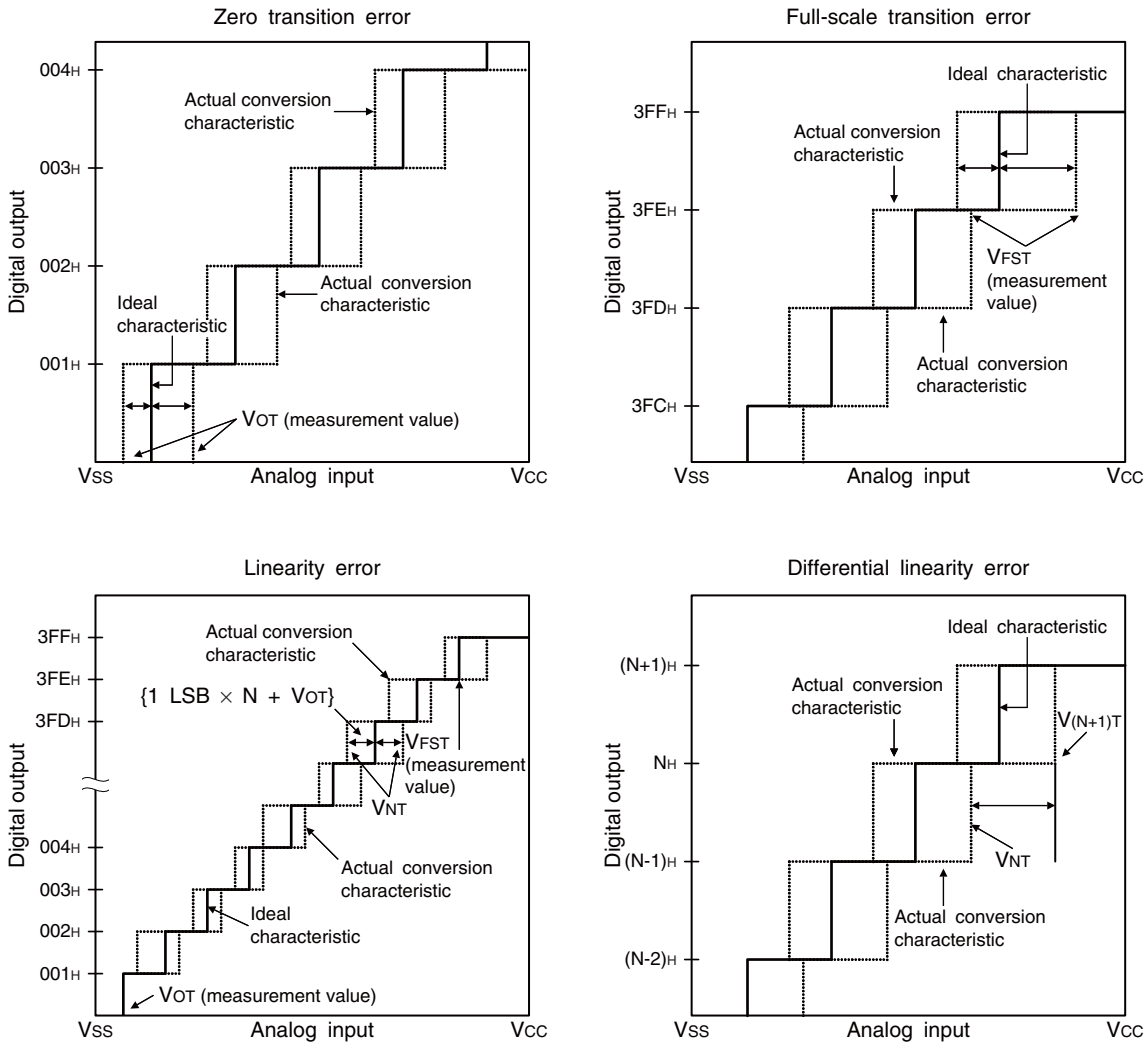
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

N : A/D converter digital output value

$V_{NT}$ : Voltage at which the digital output transits from $(N - 1)_H$ to $N_H$

*(Continued)*

*(Continued)*




$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

$V_{NT}$ : Voltage at which the digital output transits from $(N - 1)_H$ to $N_H$

$V_{OT}$ (ideal value) = $V_{SS}$ + 0.5 LSB [V]

$V_{FST}$ (ideal value) = $V_{CC}$ - 2 LSB [V]

## 6. Flash Memory Program/Erase Characteristics

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time (2 Kbyte sector) | — | 0.3*1 | 1.6*2 | s | The time of writing 00H prior to erasure is excluded. |
| Sector erase time (16 Kbyte sector) | — | 0.6*1 | 3.1*2 | s | The time of writing 00H prior to erasure is excluded. |
| Byte writing time | — | 17 | 272 | µs | System-level overhead is excluded. |
| Program/erase cycle | 100000 | — | — | cycle | |
| Power supply voltage at program/erase | 2.4 | — | 5.5 | V | |
| Flash memory data retention time | 5*3 | — | — | year | Average $T_A$ = +85°C |

*1: $V_{CC}$ = 5.5 V, $T_A$ = +25°C, 0 cycle

*2: $V_{CC}$ = 2.4 V, $T_A$ = +85°C, 100000 cycles

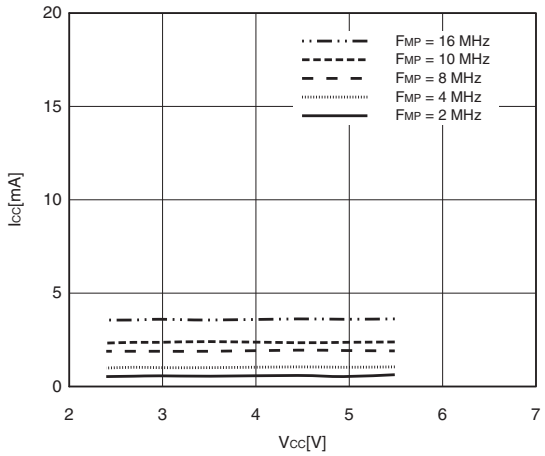
*3: This value was converted from the result of a technology reliability assessment. (The value was converted from the result of a high temperature accelerated test using the Arrhenius equation with an average temperature of +85°C).

## ■ SAMPLE CHARACTERISTICS

- Power supply current temperature characteristics

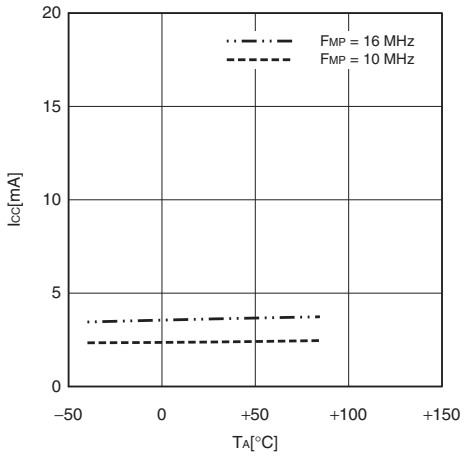
$I_{CC}$ – $V_{CC}$

$T_A$ = +25°C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



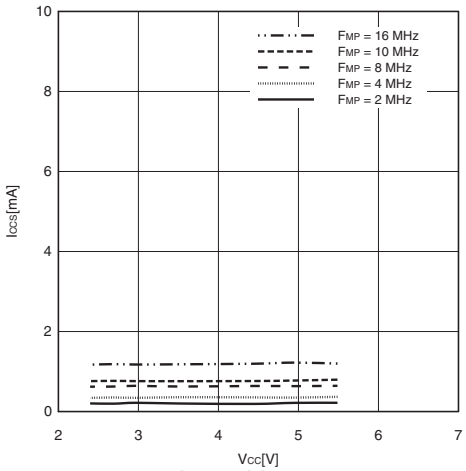

$I_{CC}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MP}$ = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



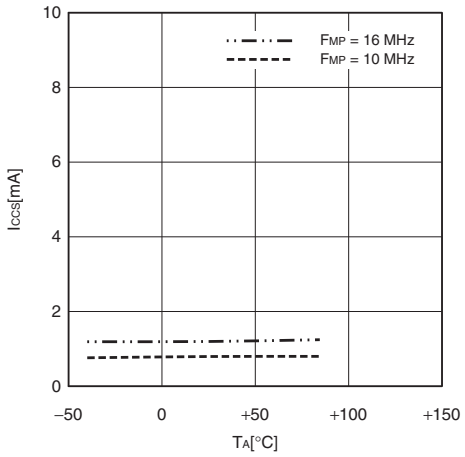

$I_{CCS}$ – $V_{CC}$

$T_A$ = +25°C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



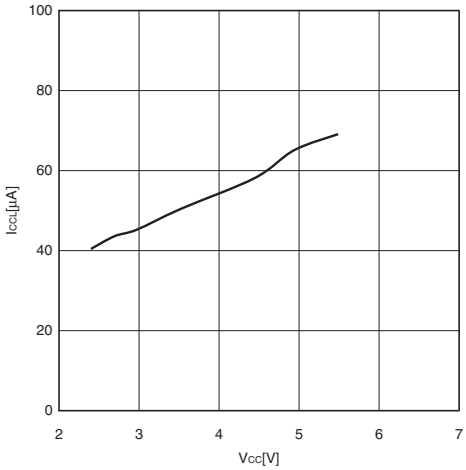

$I_{CCS}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MP}$ = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



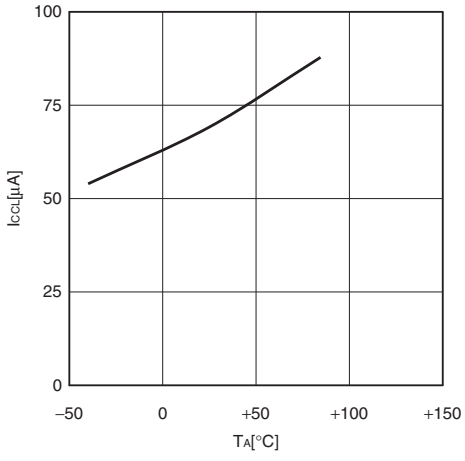

$I_{CCL}$ – $V_{CC}$

$T_A$ = +25°C, $F_{MPL}$ = 16 kHz (divided by 2)
Subclock mode with the external clock operating




$I_{CCL}$ – $T_A$

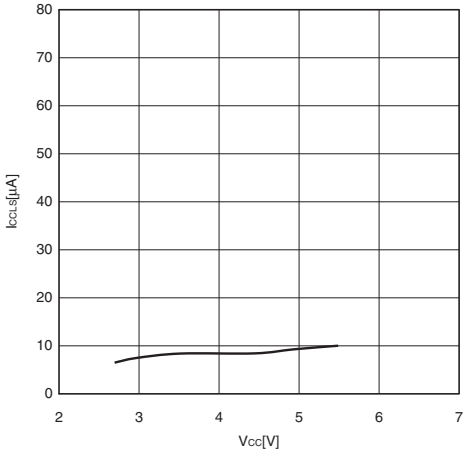
$V_{CC}$ = 5.5 V, $F_{MPL}$ = 16 kHz (divided by 2)
Subclock mode with the external clock operating




*(Continued)*

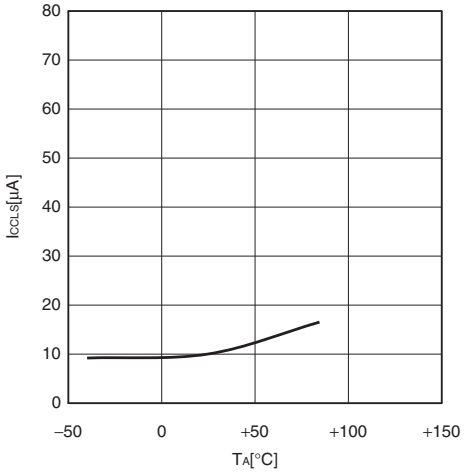
$I_{CCLS}$ – $V_{CC}$

$T_A$ = +25°C, $F_{MPL}$ = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



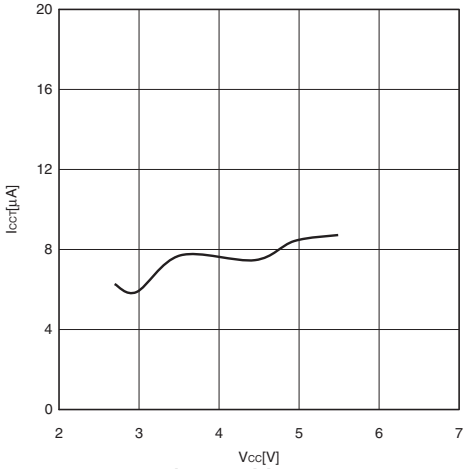

$I_{CCLS}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MPL}$ = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



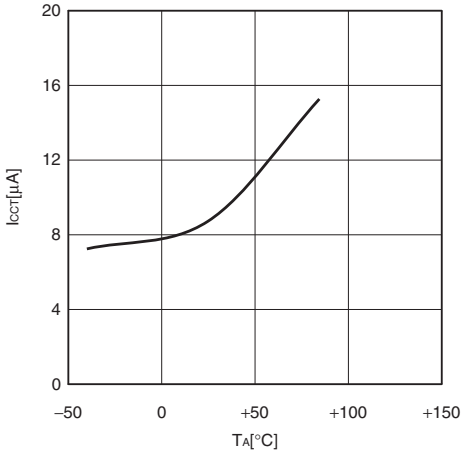

$I_{CCT}$ – $V_{CC}$

$T_A$ = +25°C, $F_{MPL}$ = 16 kHz (divided by 2)
Watch mode with the external clock operating



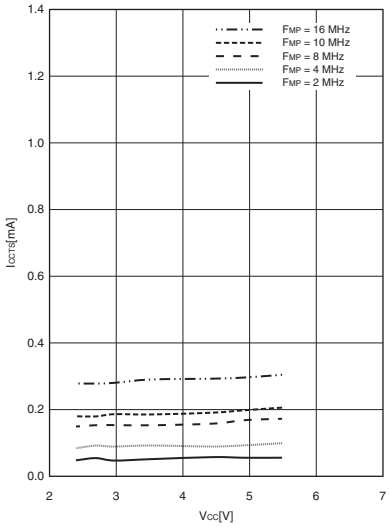

$I_{CCT}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MPL}$ = 16 kHz (divided by 2)
Watch mode with the external clock operating



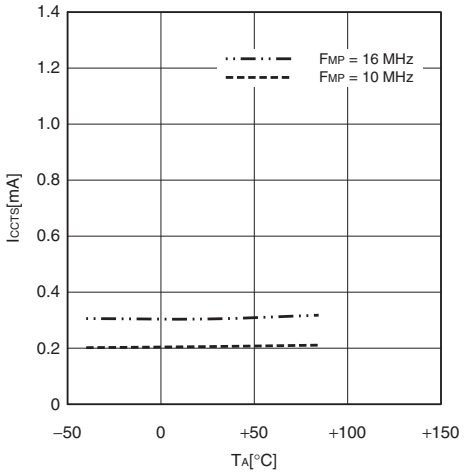

$I_{CCTS}$ – $V_{CC}$

$T_A$ = +25°C, $F_{MP}$ = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating




$I_{CCTS}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MP}$ = 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



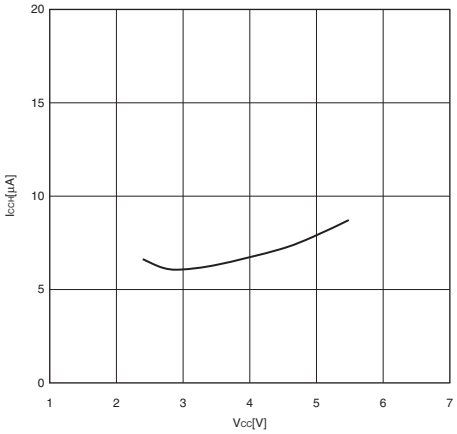

*(Continued)*

*(Continued)*

$I_{CCH}$ – $V_{CC}$

$T_A$ = +25°C, $F_{MPL}$ = (stop)

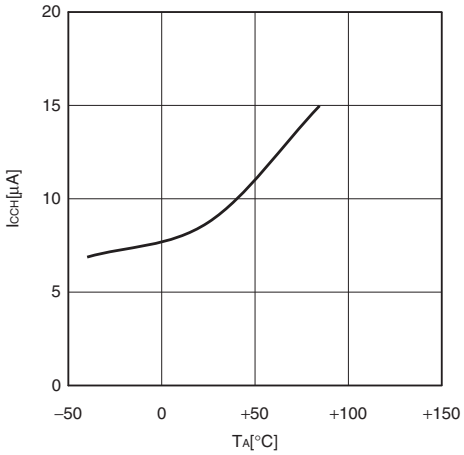
Substop mode with the external clock stopping




$I_{CCH}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MPL}$ = (stop)

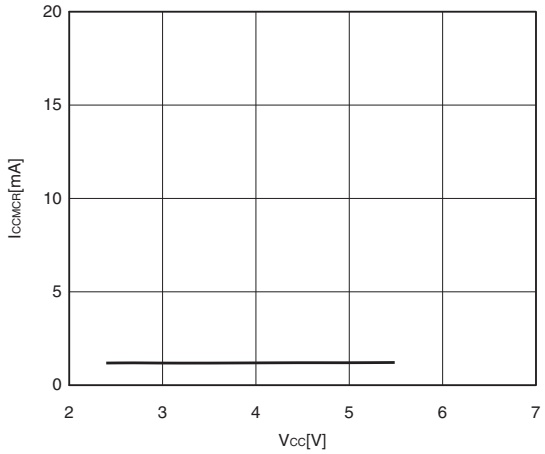
Substop mode with the external clock stopping




$I_{CCMCR}$ – $V_{CC}$

$T_A$ = +25°C, $F_{MP}$ = 4 MHz (no division)

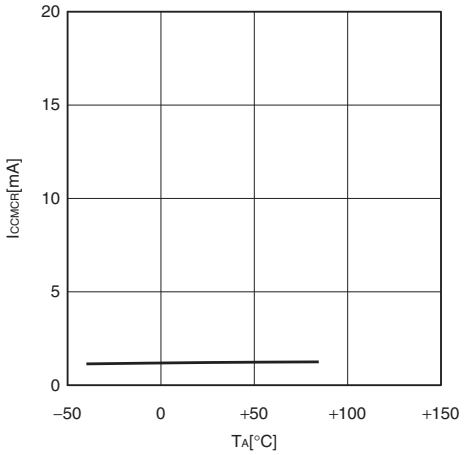
Main clock mode with the main CR clock operating




$I_{CCMCR}$ – $T_A$

$V_{CC}$ = 5.5 V, $F_{MP}$ = 4 MHz (no division)

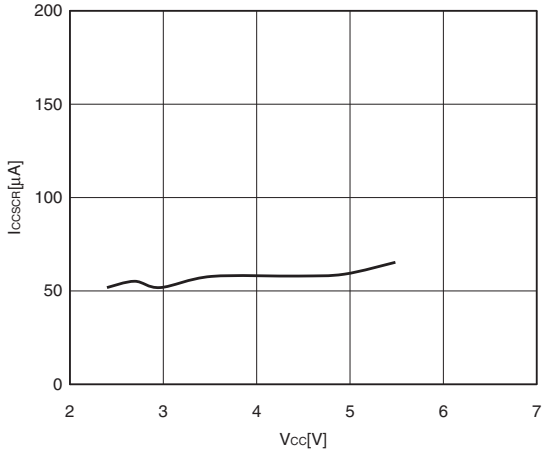
Main clock mode with the main CR clock operating




$I_{CCSCR}$ – $V_{CC}$

$T_A$ = +25°C, $F_{MPL}$ = 50 kHz (divided by 2)

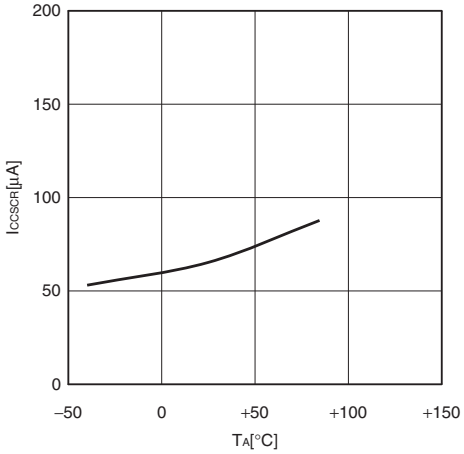
Subclock mode with the sub-CR clock operating




$I_{CCSCR}$ – $T_A$

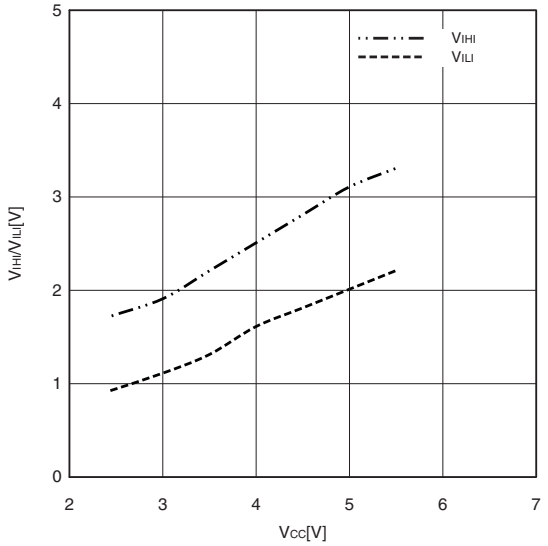
$V_{CC}$ = 5.5 V, $F_{MPL}$ = 50kHz (divided by 2)

Subclock mode with the sub-CR clock operating

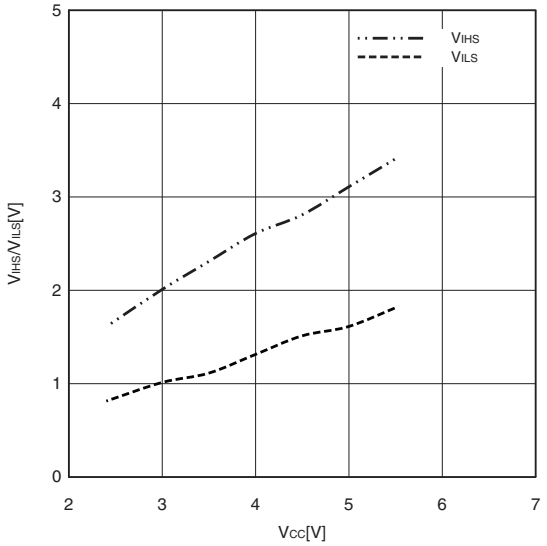


- Input voltage characteristics

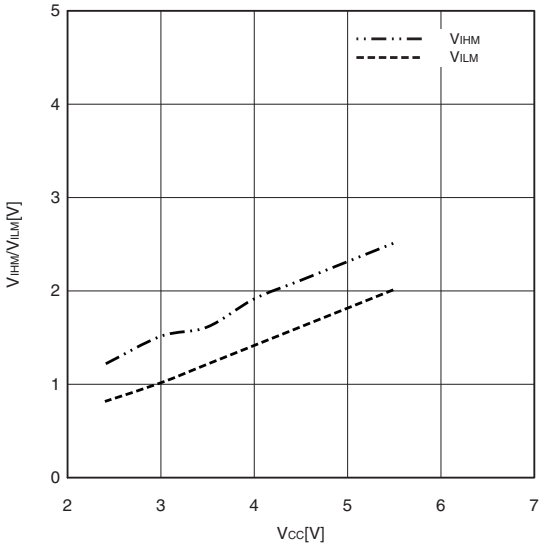
$V_{IHI}$ – $V_{CC}$ and $V_{ILI}$ – $V_{CC}$
$T_A$ = +25°C




$V_{IHS}$ – $V_{CC}$ and $V_{ILS}$ – $V_{CC}$
$T_A$ = +25°C

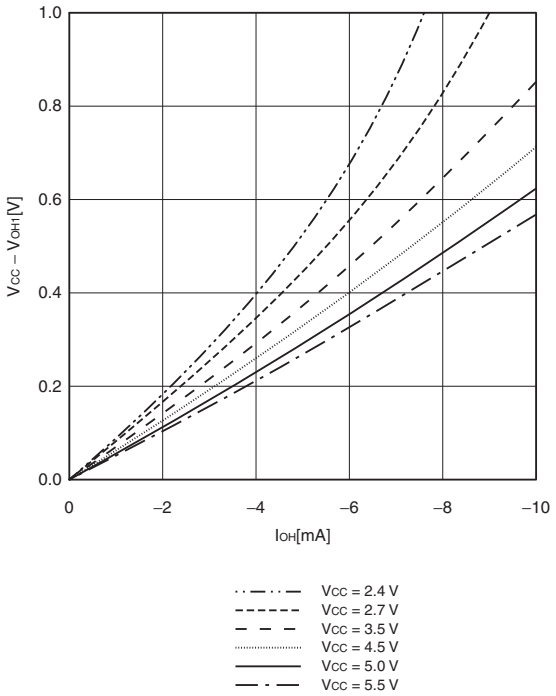



$V_{IHM}$ – $V_{CC}$ and $V_{ILM}$ – $V_{CC}$
$T_A$ = +25°C

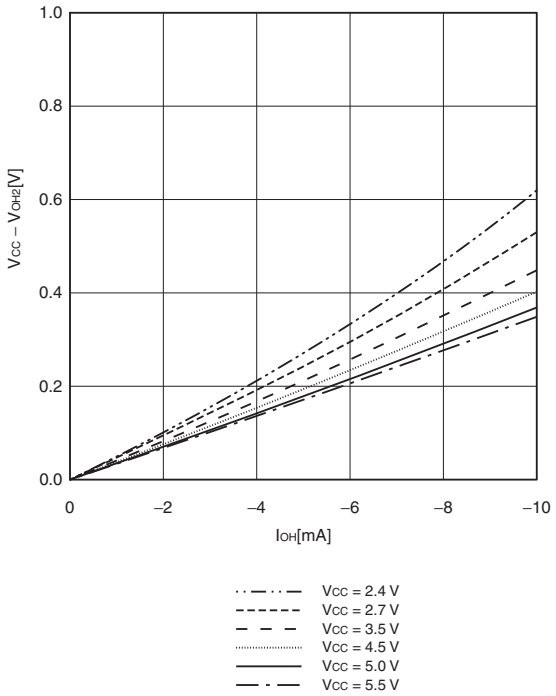


- Output voltage characteristics

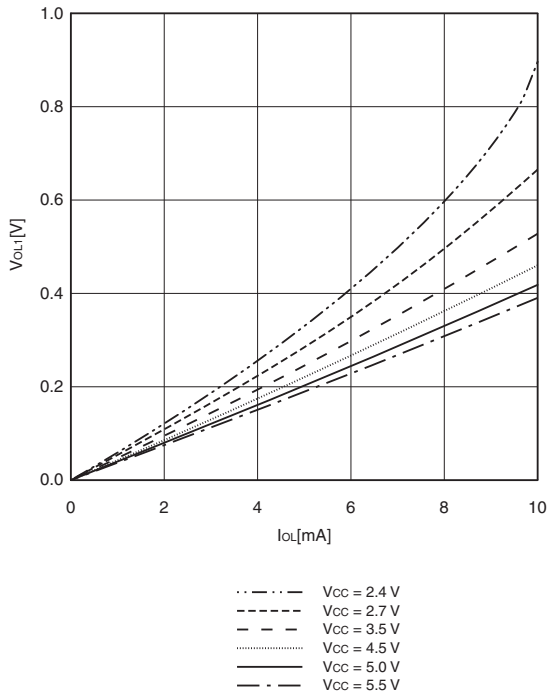
$(V_{CC} - V_{OH1}) - I_{OH}$
$T_A = +25°C$



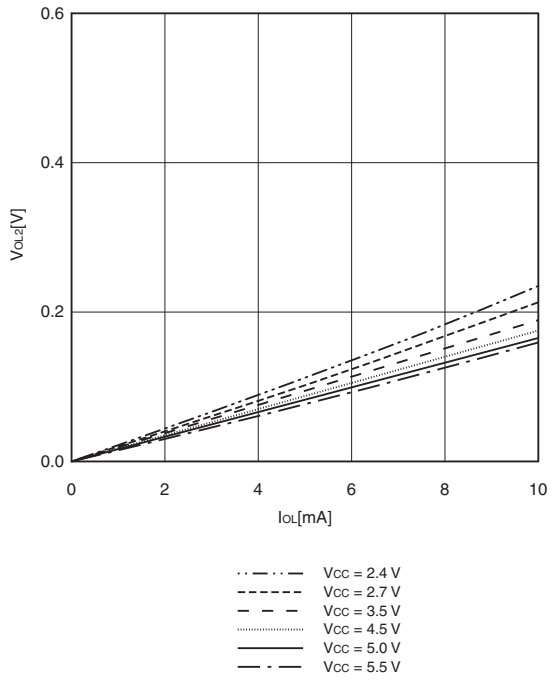

$(V_{CC} - V_{OH2}) - I_{OH}$
$T_A = +25°C$



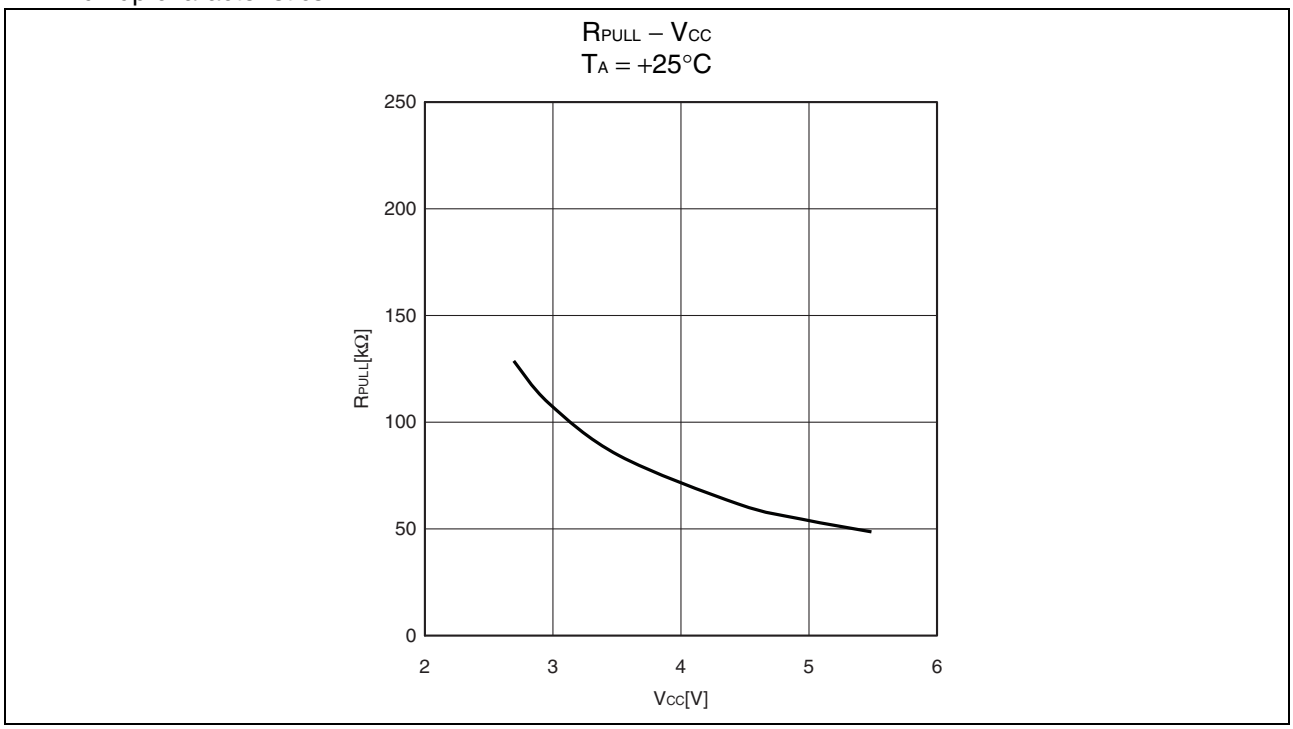

$V_{OL1} - I_{OL}$
$T_A = +25°C$




$V_{OL2} - I_{OL}$
$T_A = +25°C$



- Pull-up characteristics



## ■ MASK OPTIONS

| No. | Part Number | MB95F562H<br>MB95F563H<br>MB95F564H<br>MB95F572H<br>MB95F573H<br>MB95F574H<br>MB95F582H<br>MB95F583H<br>MB95F584H | MB95F562K<br>MB95F563K<br>MB95F564K<br>MB95F572K<br>MB95F573K<br>MB95F574K<br>MB95F582K<br>MB95F583K<br>MB95F584K |
|---|---|---|---|
| | **Selectable/Fixed** | Fixed | |
| 1 | Low-voltage detection reset | Without low-voltage detection reset | With low-voltage detection reset |
| 2 | Reset | With dedicated reset input | Without dedicated reset input |

## ■ ORDERING INFORMATION

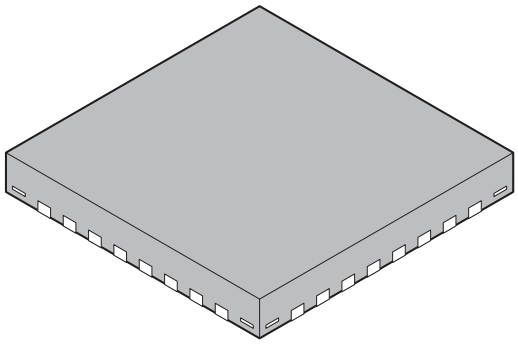
| Part number | Package |
|---|---|
| MB95F562HWQN-G-SNE1<br>MB95F562HWQN-G-SNERE1<br>MB95F562KWQN-G-SNE1<br>MB95F562KWQN-G-SNERE1<br>MB95F563HWQN-G-SNE1<br>MB95F563HWQN-G-SNERE1<br>MB95F563KWQN-G-SNE1<br>MB95F563KWQN-G-SNERE1<br>MB95F564HWQN-G-SNE1<br>MB95F564HWQN-G-SNERE1<br>MB95F564KWQN-G-SNE1<br>MB95F564KWQN-G-SNERE1 | 32-pin plastic QFN<br>(LCC-32P-M19) |
| MB95F562HPF-G-SNE2<br>MB95F562KPF-G-SNE2<br>MB95F563HPF-G-SNE2<br>MB95F563KPF-G-SNE2<br>MB95F564HPF-G-SNE2<br>MB95F564KPF-G-SNE2 | 20-pin plastic SOP<br>(FPT-20P-M09) |
| MB95F562HPFT-G-SNE2<br>MB95F562KPFT-G-SNE2<br>MB95F563HPFT-G-SNE2<br>MB95F563KPFT-G-SNE2<br>MB95F564HPFT-G-SNE2<br>MB95F564KPFT-G-SNE2 | 20-pin plastic TSSOP<br>(FPT-20P-M10) |
| MB95F582HWQN-G-SNE1<br>MB95F582HWQN-G-SNERE1<br>MB95F582KWQN-G-SNE1<br>MB95F582KWQN-G-SNERE1<br>MB95F583HWQN-G-SNE1<br>MB95F583HWQN-G-SNERE1<br>MB95F583KWQN-G-SNE1<br>MB95F583KWQN-G-SNERE1<br>MB95F584HWQN-G-SNE1<br>MB95F584HWQN-G-SNERE1<br>MB95F584KWQN-G-SNE1<br>MB95F584KWQN-G-SNERE1 | 32-pin plastic QFN<br>(LCC-32P-M19) |
| MB95F582HPFT-G-SNE2<br>MB95F582KPFT-G-SNE2<br>MB95F583HPFT-G-SNE2<br>MB95F583KPFT-G-SNE2<br>MB95F584HPFT-G-SNE2<br>MB95F584KPFT-G-SNE2 | 16-pin plastic TSSOP<br>(FPT-16P-M08) |
| MB95F582HPF-G-SNE2<br>MB95F582KPF-G-SNE2<br>MB95F583HPF-G-SNE2<br>MB95F583KPF-G-SNE2<br>MB95F584HPF-G-SNE2<br>MB95F584KPF-G-SNE2 | 16-pin plastic SOP<br>(FPT-16P-M23) |

*(Continued)*

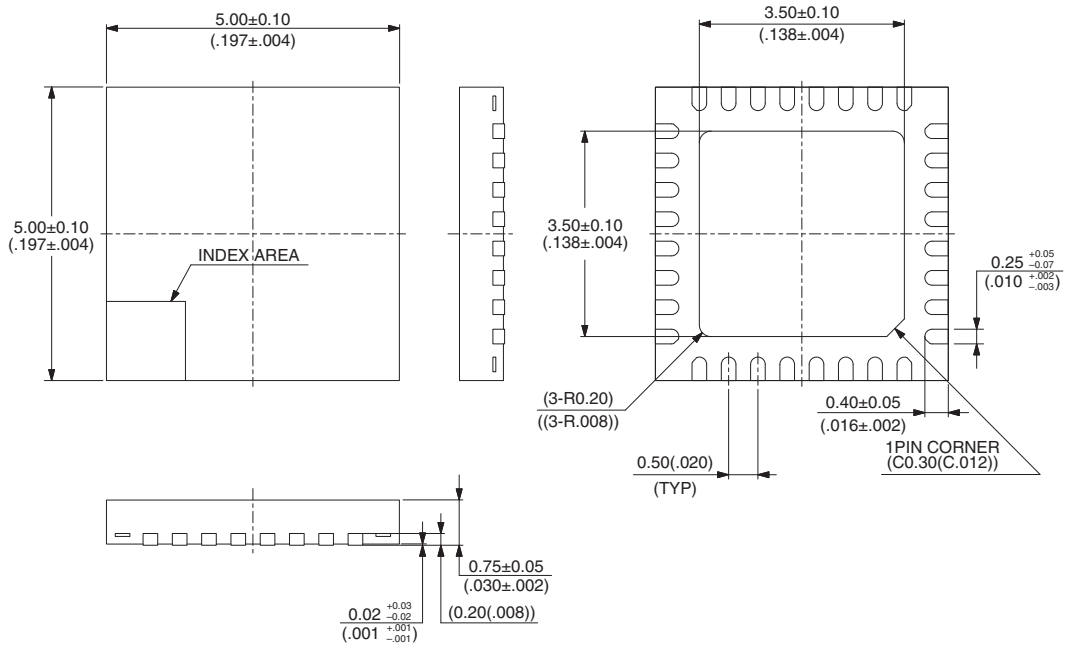
*(Continued)*

| Part number | Package |
|---|---|
| MB95F572HPH-G-SNE2<br>MB95F572KPH-G-SNE2<br>MB95F573HPH-G-SNE2<br>MB95F573KPH-G-SNE2<br>MB95F574HPH-G-SNE2<br>MB95F574KPH-G-SNE2 | 8-pin plastic DIP<br>(DIP-8P-M03) |
| MB95F572HPF-G-SNE2<br>MB95F572KPF-G-SNE2<br>MB95F573HPF-G-SNE2<br>MB95F573KPF-G-SNE2<br>MB95F574HPF-G-SNE2<br>MB95F574KPF-G-SNE2 | 8-pin plastic SOP<br>(FPT-8P-M08) |

## ■ PACKAGE DIMENSION

| 32-pin plastic QFN | | |
|---|---|---|
|  (LCC-32P-M19) | Lead pitch | 0.50 mm |
| | Package width × package length | 5.00 mm × 5.00 mm |
| | Sealing method | Plastic mold |
| | Mounting height | 0.80 mm MAX |
| | Weight | 0.06 g |
| | | |
| | | |

32-pin plastic QFN
(LCC-32P-M19)

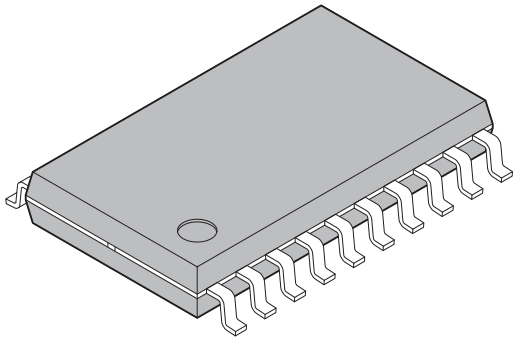





Dimensions in mm (inches).
Note: The values in parentheses are reference values.

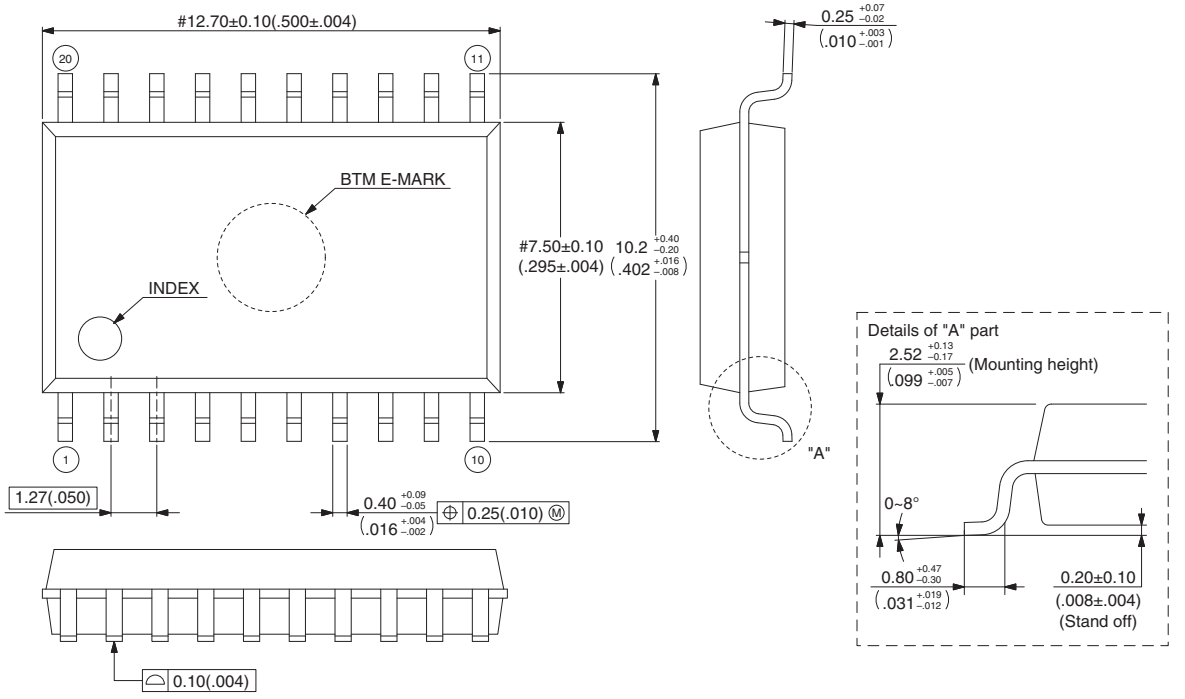
Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*

| 20-pin plastic SOP | | |
|---|---|---|
|  | Lead pitch | 1.27 mm |
| | Package width × package length | 7.50 mm × 12.70 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 2.65 mm Max |
| (FPT-20P-M09) | | |

20-pin plastic SOP
(FPT-20P-M09)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.

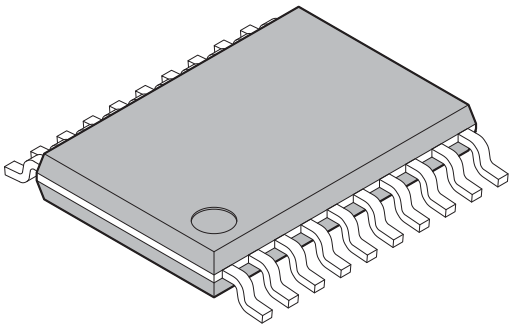





Dimensions in mm (inches).
Note: The values in parentheses are reference values.

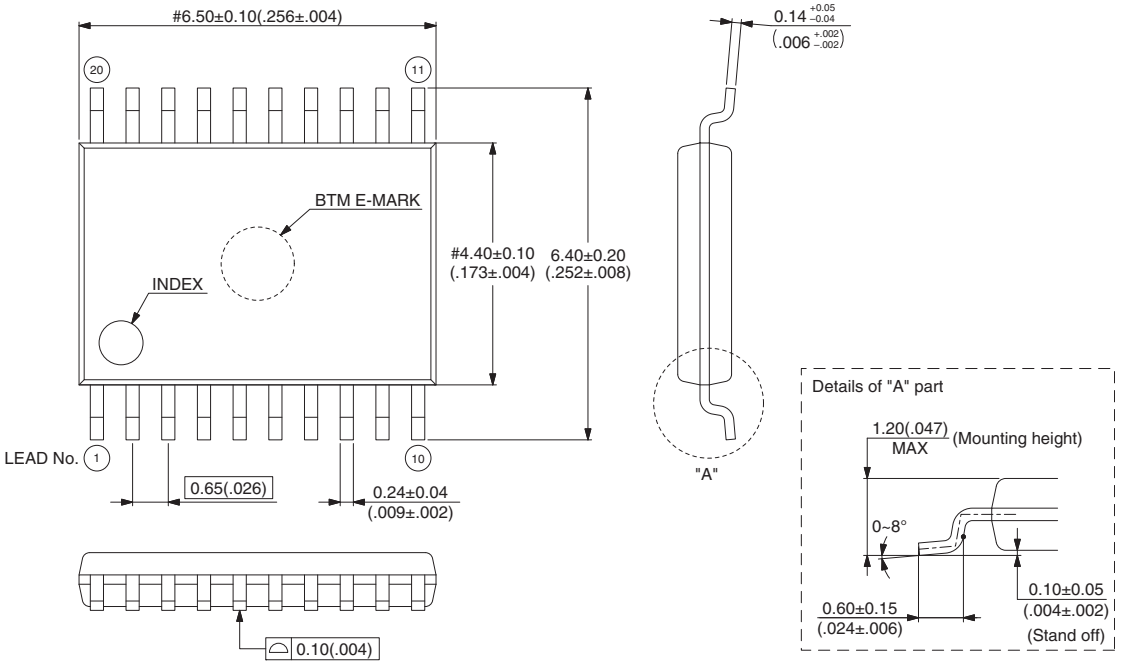
Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*

| 20-pin plastic TSSOP | | |
|---|---|---|
|  | Lead pitch | 0.65 mm |
| | Package width × package length | 4.40 mm × 6.50 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.20 mm MAX |
| | Weight | 0.08 g |
| (FPT-20P-M10) | | |

20-pin plastic TSSOP
(FPT-20P-M10)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.

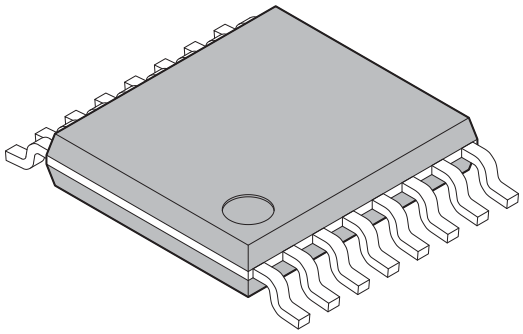





Dimensions in mm (inches).
Note: The values in parentheses are reference values.

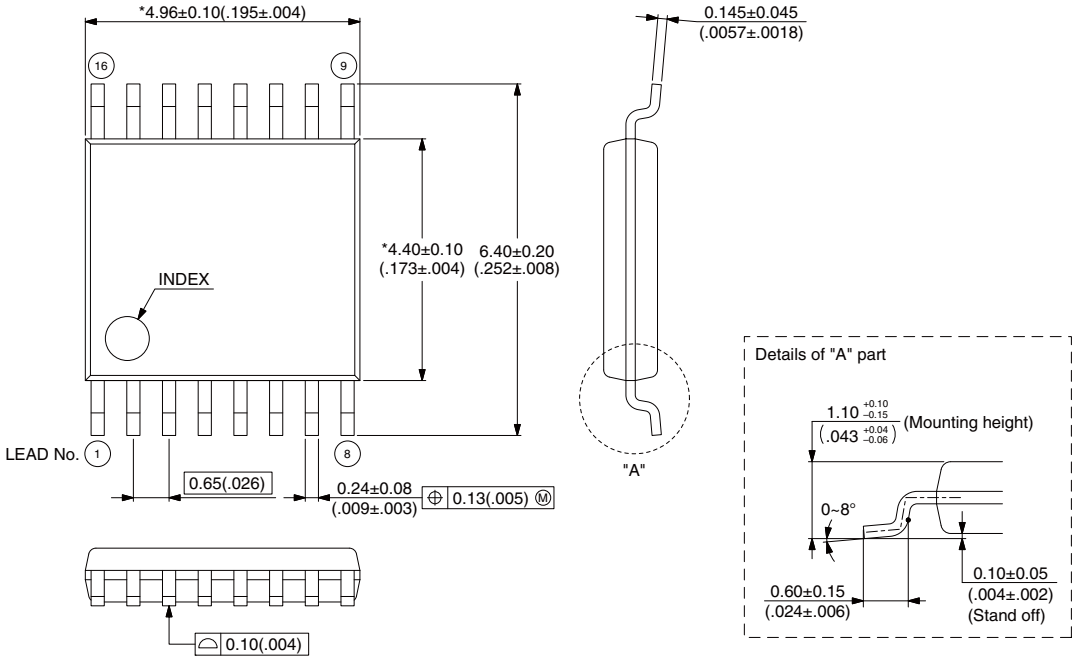
Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*

| 16-pin plastic TSSOP | | |
|---|---|---|
|  | Lead pitch | 0.65 mm |
| | Package width × package length | 4.40 mm × 4.96 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.20 mm Max |
| | Weight | 0.06 g |
| (FPT-16P-M08) | | |

16-pin plastic TSSOP
(FPT-16P-M08)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) * : These dimensions do not include resin protrusion.

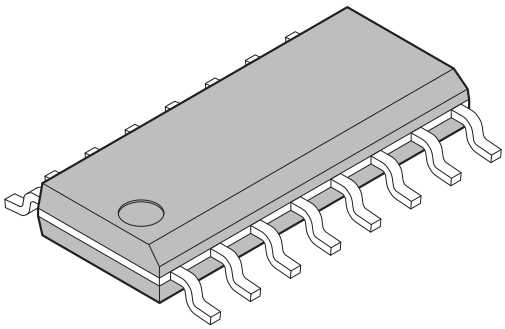





Dimensions in mm (inches).
Note: The values in parentheses are reference values.

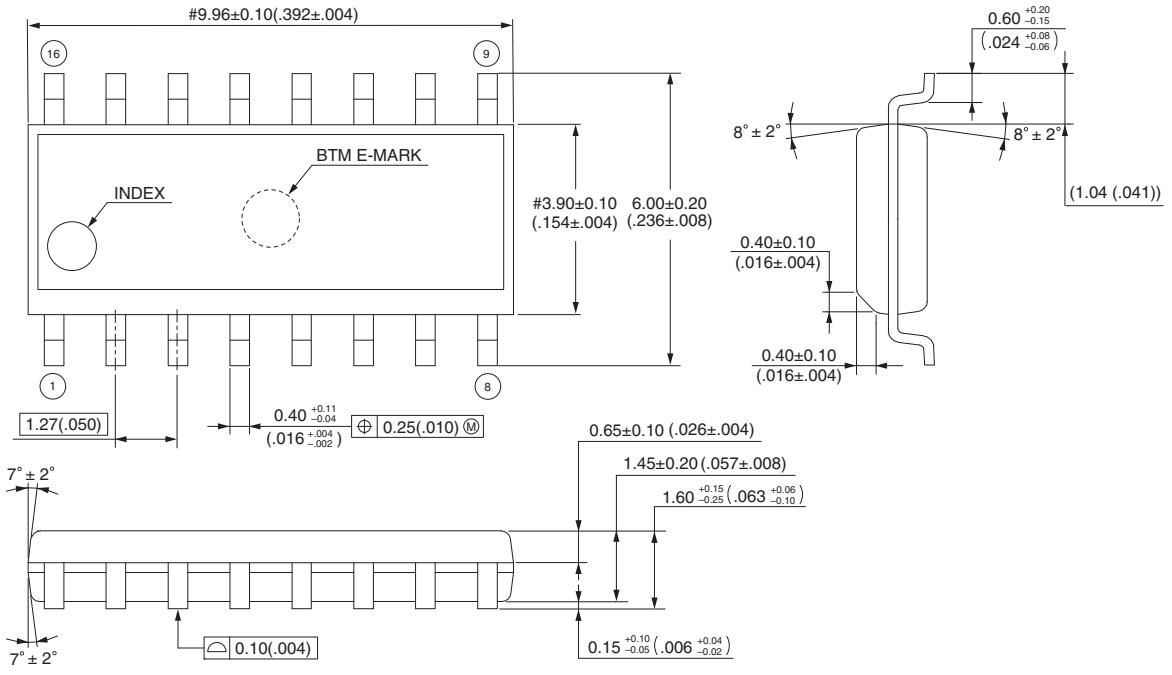
Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*

| 16-pin plastic SOP | | |
|---|---|---|
|  | Lead pitch | 1.27 mm |
| | Package width × package length | 3.90 mm × 9.96 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.75 mm MAX |
| | Weight | 0.12 g |
| (FPT-16P-M23) | | |

16-pin plastic SOP
(FPT-16P-M23)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) #: These dimensions do not include resin protrusion.

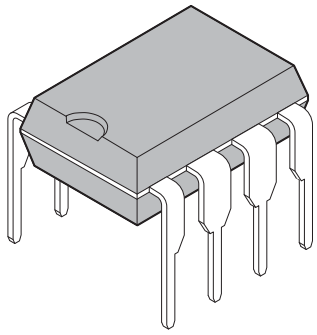




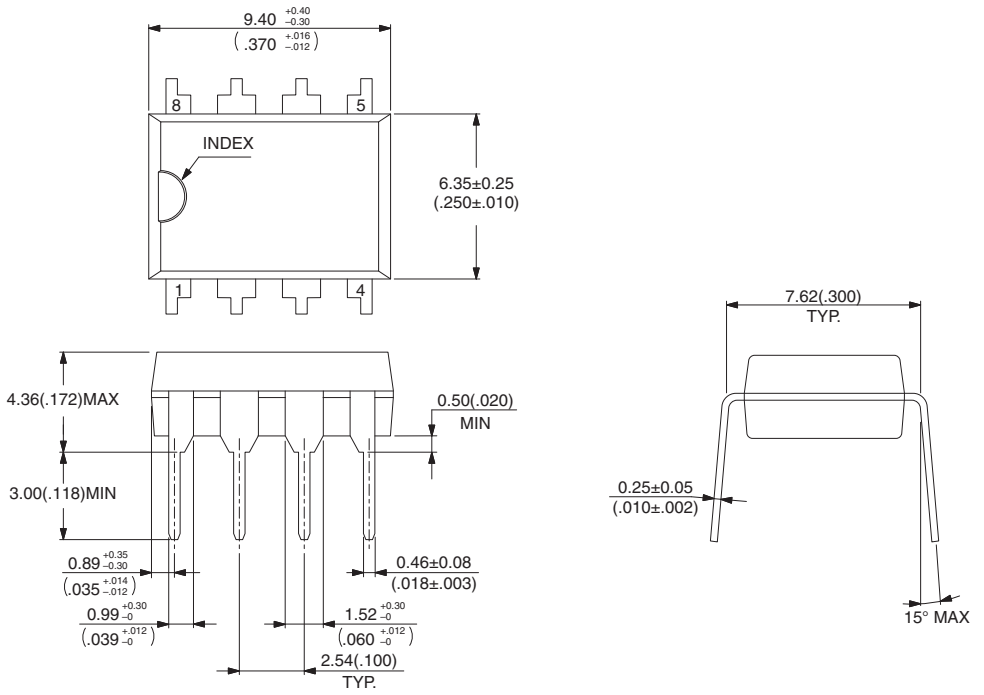

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

*(Continued)*

| 8-pin plastic DIP | Lead pitch | 2.54 mm |
|---|---|---|
|  | Sealing method | Plastic mold |
| | | |
| | | |
| | | |
| | | |
| (DIP-8P-M03) | | |

8-pin plastic DIP
(DIP-8P-M03)



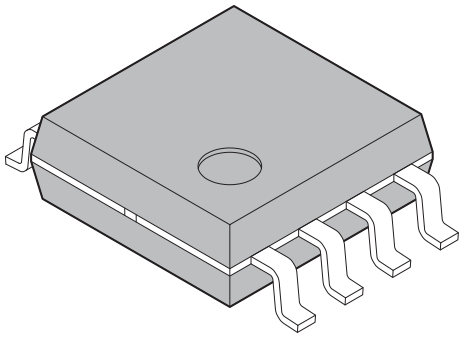



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

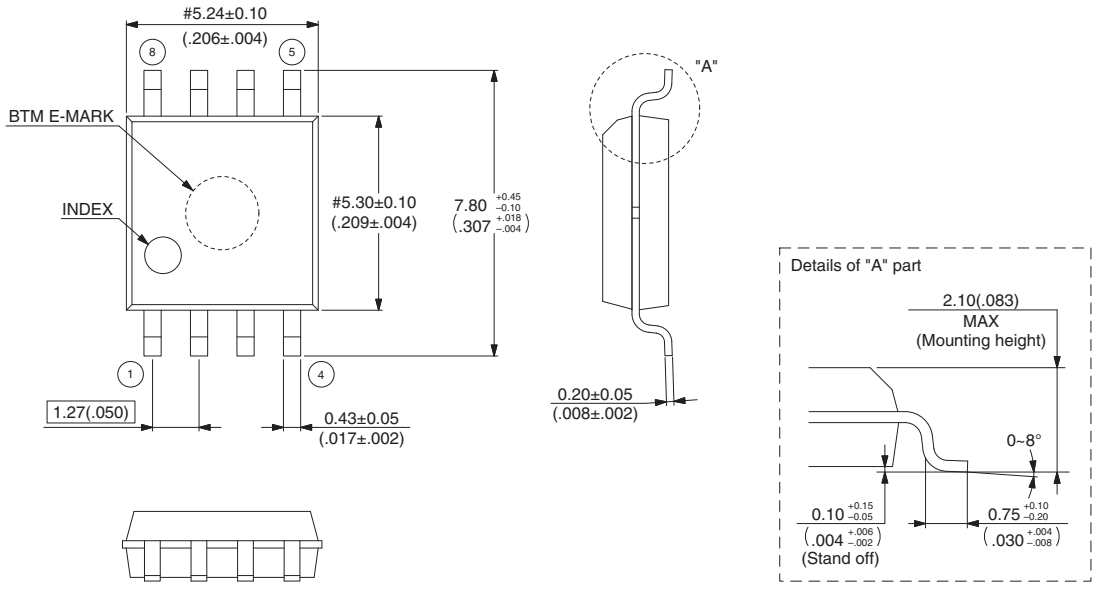
*(Continued)*

*(Continued)*

| 8-pin plastic SOP | | |
|---|---|---|
|  | Lead pitch | 1.27 mm |
| | Package width × package length | 5.30 mm × 5.24 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 2.10 mm Max |
| (FPT-8P-M08) | | |

8-pin plastic SOP
(FPT-8P-M08)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) # : These dimensions do not include resin protrusion.






Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

| Page | Section | Details |
|---|---|---|
| 5 | ■ PRODUCT LINE-UP<br>• MB95570H Series | Added the package DIP-8P-M03. |
| 8 | ■ PACKAGES AND CORRESPONDING PRODUCTS<br>• MB95560H Series | Added the package DIP-8P-M03. |
| | ■ PACKAGES AND CORRESPONDING PRODUCTS<br>• MB95570H Series | Added the package DIP-8P-M03. |
| | ■ PACKAGES AND CORRESPONDING PRODUCTS<br>• MB95580H Series | Added the package DIP-8P-M03. |
| 11 | ■ PIN ASSIGNMENT | Added the package DIP-8P-M03 to the pin assignment diagram of the MB95570H Series. |
| 12 | ■ PIN FUNCTIONS (MB95560H Series, 32 pins) | Revised the function of the C pin.<br>Capacitor connection pin<br>→<br>Decoupling capacitor connection pin |
| 14 | ■ PIN FUNCTIONS (MB95560H Series, 20 pins) | Revised the function of the C pin.<br>Capacitor connection pin<br>→<br>Decoupling capacitor connection pin |
| 16 | ■ PIN FUNCTIONS (MB95570H Series, 8 pins) | Revised the function of the C pin.<br>Capacitor connection pin<br>→<br>Decoupling capacitor connection pin |
| 17 | ■ PIN FUNCTIONS (MB95580H Series, 32 pins) | Revised the function of the C pin.<br>Capacitor connection pin<br>→<br>Decoupling capacitor connection pin |
| 19 | ■ PIN FUNCTIONS (MB95580H Series, 16 pins) | Revised the function of the C pin.<br>Capacitor connection pin<br>→<br>Decoupling capacitor connection pin |
| 24 | ■ PIN CONNECTION<br>• C pin | Revised “smoothing capacitor” to “decoupling capacitor”. |
| 29 | ■ I/O MAP (MB95560H Series) | Corrected the initial value of the PLLC register.<br>$00000000_B \rightarrow 000X0000_B$ |
| 31 | | Corrected the initial value of the CRTDA register.<br>$00011111_B \rightarrow 000XXXXX_B$ |
| 33 | ■ I/O MAP (MB95570H Series) | Corrected the initial value of the PLLC register.<br>$00000000_B \rightarrow 000X0000_B$ |
| | | Deleted all details of the PUL6 register. |
| 35 | | Corrected the initial value of the CRTDA register.<br>$00011111_B \rightarrow 000XXXXX_B$ |

*(Continued)*

| Page | Section | Details |
|---|---|---|
| 36 | ■ I/O MAP (MB95580H Series) | Corrected the initial value of the PLLC register.<br>$00000000_B \rightarrow 000X0000_B$ |
| | | Deleted all details of the PUL6 register. |
| 38 | | Corrected the initial value of the CRTDA register.<br>$00011111_B \rightarrow 000XXXXX_B$ |
| 42 | ■ ELECTRICAL CHARACTERISTICS<br>1. Absolute Maximum Ratings | Replaced $I_{OL1}$ and $I_{OL2}$ with $I_{OL}$ for the parameter ““L” level maximum output current”. |
| | | Revised the remarks of the parameter ““L” level average current”. |
| | | Replaced $I_{OH1}$ and $I_{OH2}$ with $I_{OH}$ for the parameter ““H” level maximum output current”. |
| | | Revised the remarks of the parameter ““H” level average current”. |
| 44 | 2. Recommended Operating Conditions | Revised “Smoothing capacitor” to “Decoupling capacitor” in the Parameter column and note *3. |
| 45 | 3. DC Characteristics | Deleted P12 from the pins of $V_{OL2}$ for the parameter ““L” level output voltage”. |
| 46, 47 | | Revised specifications of the parameter “Power supply current”. |
| 47 | | Added $I_{NSTBY}$ to the parameter “Power supply current”. |
| 48 | 4. AC Characteristics<br>(1) Clock Timing | Revised specifications of $F_{CRH}$ of the parameter “Clock frequency”. |
| | | Added $F_{MCRPLL}$ to the parameter “Clock frequency”. |
| 49 | | Corrected the minimum value of the parameter “Input clock pulse width” for the X0 pin and the X1 pin.<br>14.4 → 12.4 |
| 52 | 4. AC Characteristics<br>(2) Source Clock / Machine Clock<br>• Schematic diagram of the clock generation block | Corrected the symbol and the clock name in the block of the main CR PLL clock.<br>$F_{MPLL} \rightarrow F_{MCRPLL}$<br>Main CR PLL → Main CR PLL clock<br><br>Corrected the abbreviation of the clock mode select bits.<br>SYCC2:RCS1, RCS0 → SYCC:SCS[2:0] |
| 62 | 4. AC Characteristics<br>(7) Low-voltage Detection | Revised specifications of the parameter “Hysteresis width”.<br>Typ : — → 100<br>Max : 100 → — |
| 64 | 5. A/D Converter<br>(1) A/D Converter Electrical Characteristics | Revised specifications of the parameters “Zero transition voltage”, “Full-scale transition voltage” and “Compare time”.<br><br>Revised the minimum value of the parameter “Sampling time”.<br>0.517 → 0.6 |
| 65 | 5. A/D Converter<br>(2) Notes on Using A/D Converter | Corrected the resistance for “2.7 V ≤ $V_{CC}$ < 5.5 V”.<br>15.7 kΩ → 5.7 kΩ |

*(Continued)*

*(Continued)*

| Page | Section | Details |
|---|---|---|
| 68 | 6. Flash Memory Program/Erase Characteristics | Added the following note.<br>*2: $V_{CC}$ = 2.4 V, $T_A$ = +85°C, 100000 cycles |
| 69 to 74 | ■ SAMPLING CHARACTERISTICS | Revised all sampling characteristics diagrams. |
| 76, 77 | ■ ORDERING INFORMATION | Revised all part numbers. |
| 77 | | Added part numbers of the package “8-pin plastic DIP (DIP-8P-M03)”. |
| 83 | ■ PACAKGE DIMENSION | Added the package diagram of DIP-8P-M03. |

# FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
*http://jp.fujitsu.com/fsl/en/*

*For further information please contact:*

**North and South America**
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
*http://us.fujitsu.com/micro/*

**Europe**
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
*http://emea.fujitsu.com/semiconductor/*

**Korea**
FUJITSU SEMICONDUCTOR KOREA LTD.
902 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
*http://kr.fujitsu.com/fsk/*

**Asia Pacific**
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
*http://sg.fujitsu.com/semiconductor/*

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
30F, Kerry Parkside, 1155 Fang Dian Road,
Pudong District, Shanghai 201204, China
Tel : +86-21-6146-3688 Fax : +86-21-6146-3660
*http://cn.fujitsu.com/fss/*

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
*http://cn.fujitsu.com/fsp/*



Edited: Sales Promotion Department