FUJITSU SEMICONDUCTOR
MEMORY SOLUTION DATA SHEET

DS501-00027-5v0-E

Memory FeRAM

1M (128 K × 8) Bit I²C

MB85RC1MT

■ DESCRIPTION

The MB85RC1MT is an FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 131,072 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

Unlike SRAM, the MB85RC1MT is able to retain data without using a data backup battery.

The read/write endurance of the nonvolatile memory cells used for the MB85RC1MT has improved to be at least 10^{13} cycles, significantly outperforming other nonvolatile memory products in the number.

The MB85RC1MT does not need a polling sequence after writing to the memory such as the case of Flash memory or E²PROM.

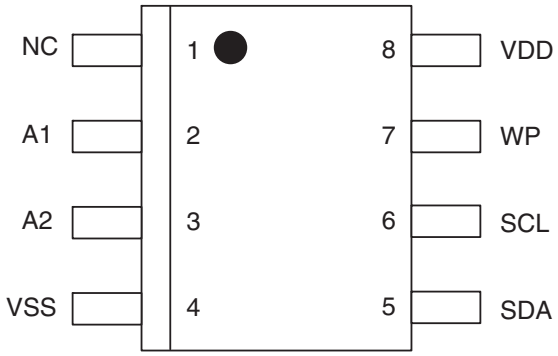
■ FEATURES

- Bit configuration : 131,072 words × 8 bits
- Two-wire serial interface : Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating frequency : 3.4 MHz (Max @HIGH SPEED MODE)
  1 MHz (Max @FAST MODE PLUS)
- Read/write endurance : 10^{13} times / byte
- Data retention : 10 years (+ 85 °C), 95 years (+ 55 °C), over 200 years (+ 35 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low-power consumption : Operating power supply current 0.71 mA (Typ @3.4 MHz)
  1.2 mA (Max @3.4 MHz)
  Standby current 15 μA (Typ)
  Sleep current 4 μA (Typ)
- Operation ambient temperature range
  : − 40 °C to + 85 °C
- Package : 8-pin plastic SOP (FPT-8P-M02)
  RoHS compliant

2022.07

■ PIN ASSIGNMENT

(TOP VIEW)

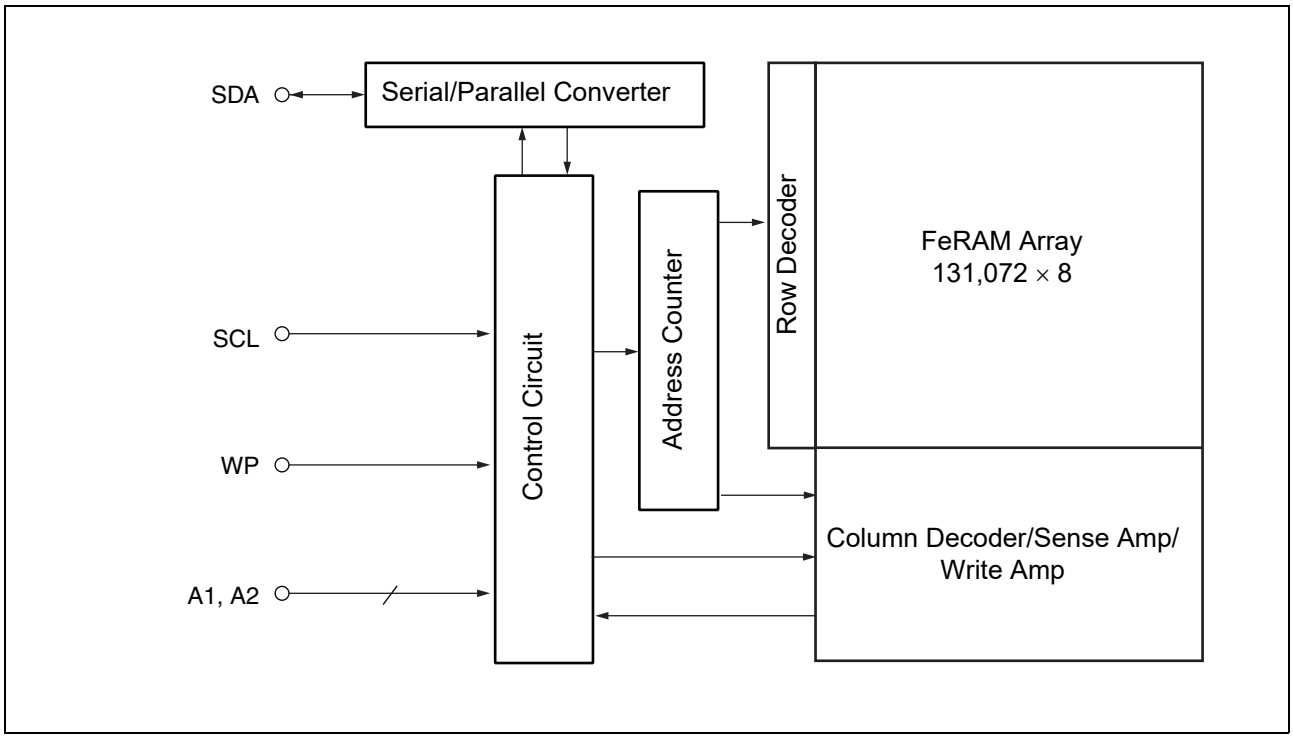


(FPT-8P-M02)

■ PIN FUNCTIONAL DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1	NC	No Connect pin Leave this pin open, or connect to VDD or VSS.
2, 3	A1, A2	Device Address pins The MB85RC1MT can be connected to the same data bus up to 4 devices. Device addresses are used in order to identify each of these devices. Connect these pins to VDD pin or VSS pin externally. Only if the combination of VDD and VSS pins matches Device Address Code inputted from the SDA pin, the device operates. In the open pin state, A1 and A2 pins are internally pulled-down and recognized as the "L" level.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin which performs bidirectional communication for both memory address and writing/reading data. It is possible to connect multiple devices. It is an open drain output, so a pull-up resistor is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When the Write Protect pin is the “H” level, the writing operation is disabled. When the Write Protect pin is the “L” level, the entire memory region can be overwritten. The reading operation is always enabled regardless of the Write Protect pin input level. The Write Protect pin is internally pulled down to VSS pin, and that is recognized as the “L” level (write enabled) when the pin is the open state.
8	VDD	Supply Voltage pin

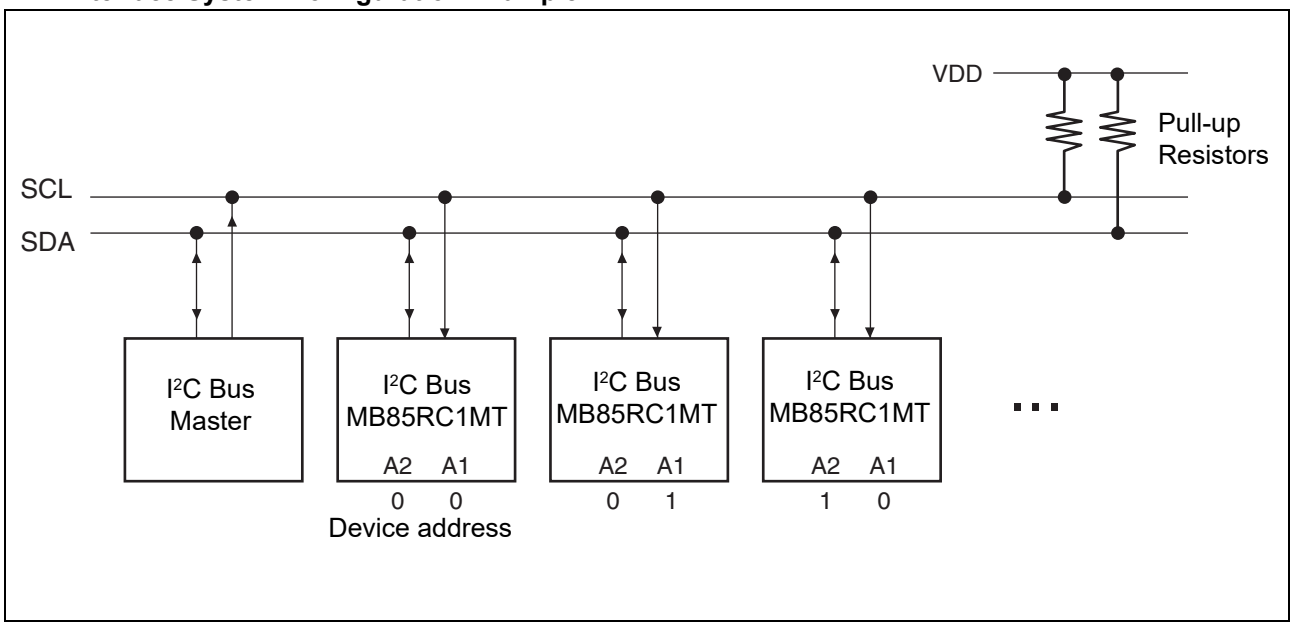
■ BLOCK DIAGRAM



■ I²C (Inter-Integrated Circuit)

The MB85RC1MT has the two-wire serial interface; the I²C bus, and operates as a slave device.
The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, the I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration. In this case, it is necessary to assign a unique device address to the slave device, the master side starts communication after specifying the slave to communicate by addresses.

- **I²C Interface System Configuration Example**



■ I²C COMMUNICATION PROTOCOL

The I²C bus is a two wire serial interface that uses a bidirectional data bus (SDA) and serial clock (SCL). A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The SDA signal should change while the SCL is the “L” level. However, as an exception, when starting and stopping communication sequence, the SDA is allowed to change while the SCL is the “H” level.

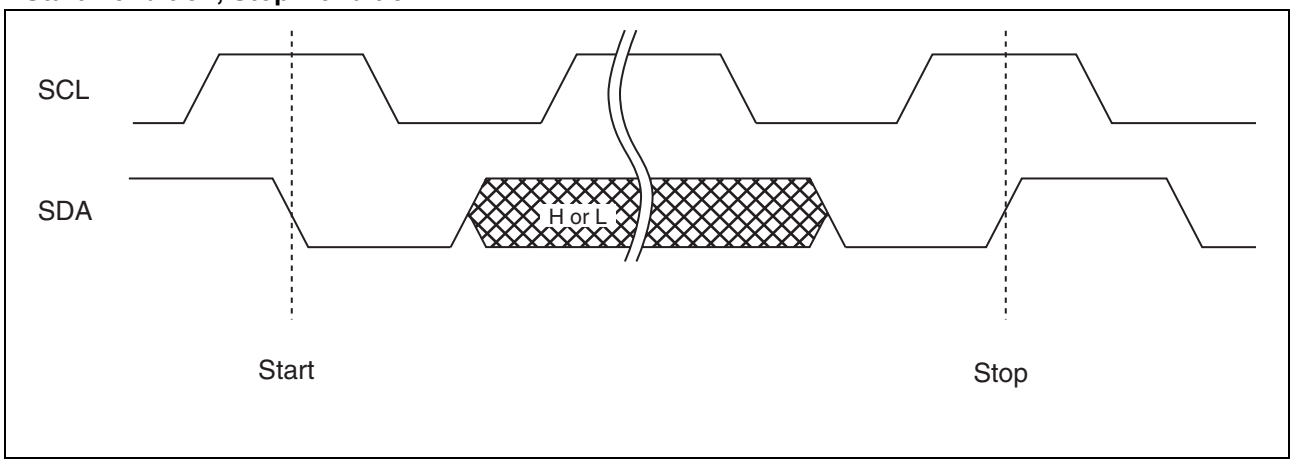
- Start Condition

To start read or write operations by the I²C bus, change the SDA input from the “H” level to the “L” level while the SCL input is in the “H” level.

- Stop Condition

To stop the I²C bus communication, change the SDA input from the “L” level to the “H” level while the SCL input is in the “H” level. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data and enters the standby state.

• Start Condition, Stop Condition



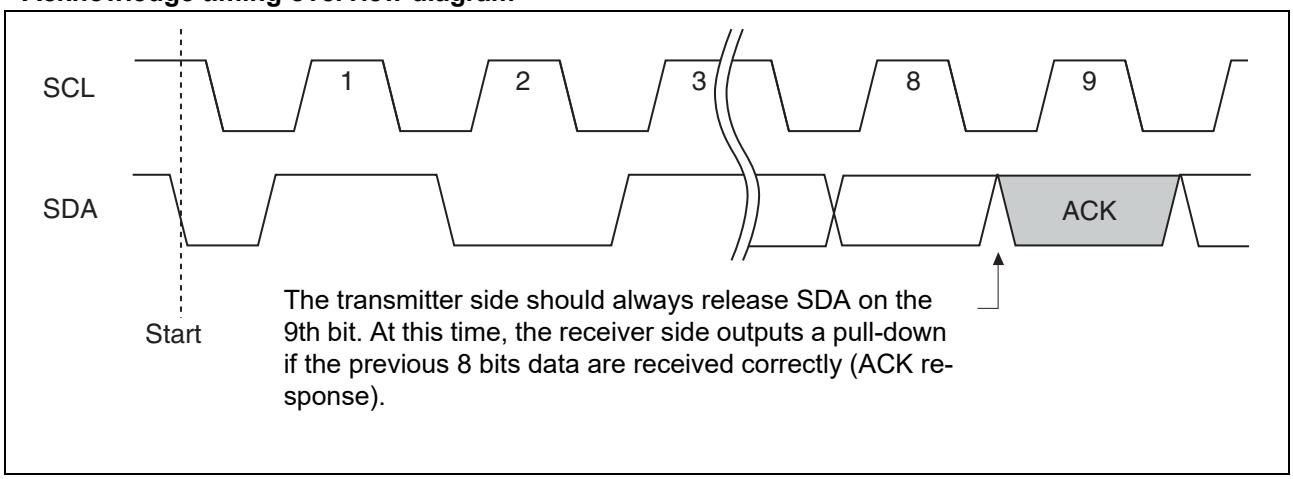
Note : At the write operation, the FeRAM device does not need the programming wait time (t_{WC}) after issuing the Stop Condition.

■ ACKNOWLEDGE (ACK)

In the I²C bus, serial data including memory address or memory information is sent and received in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the “L” level every time on the 9th SCL clock after each 8 bits are successfully transmitted and received. On the transmitter side, the bus is temporarily released to Hi-Z every time on this 9th clock to allow the acknowledge signal to be received and checked. During this Hi-Z released period, the receiver side pulls the SDA line down to indicate the “L” level that the previous 8 bits communication is successfully received.

In case the slave side receives Stop condition before sending or receiving the ACK “L” level, the slave side stops the operation and enters to the standby state. On the other hand, the slave side releases the bus state after sending or receiving the NACK “H” level. The master side generates Stop condition or Start condition in this released bus state.

• Acknowledge timing overview diagram



■ DEVICE ADDRESS WORD (Slave address)

Following the start condition, the master inputs the 8 bits device address word to start I²C communication. The device address word (8 bits) consists of a device Type code (4 bits), device address code (2 bits), most significant address (1 bit) and a read/write code (1 bit).

• Device Type Code (4 bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at “1010” for the MB85RC1MT.

• Device Address Code (2 bits)

Following the device type code, the 2 bits of the device address code are input in order of A2 and A1. The device address code identifies one device from up to four devices connected to the bus. Each MB85RC1MT is given a unique 2 bits code on the device address pin (external hardware pin A2 and A1). The slave only responds if the received device address code is equal to this unique 2 bits code.

• Most Significant Address (1 bit)

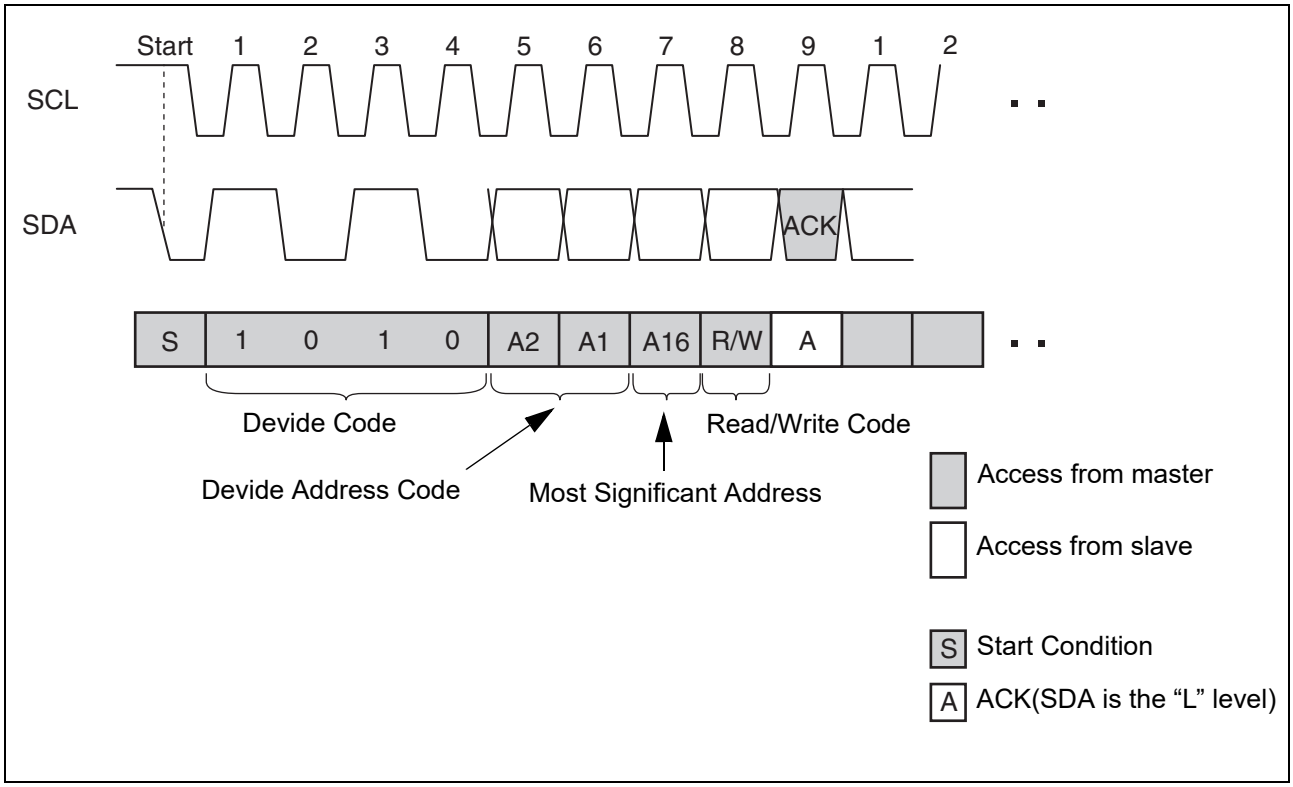
The 7th bit of the device address word is the most significant address bit of A16 (1 bit).

• Read/Write Code (1 bit)

The 8th bit of the device address word is the R/W (read/write) code. When the R/W code is “0”, a write operation is enabled, and the R/W code is “1”, a read operation is enabled for the MB85RC1MT.

It turns to a stand-by state if the device code is not “1010” or device address code does not equal to pin A2 and A1.

• Device Address Word



■ DATA STRUCTURE

In the I²C bus, the acknowledge “L” level is output on the 9th bit by a slave, after the 8 bits of the device address word following the start condition are input by a master. After confirming the acknowledge response by the master, the master outputs remaining 8 bits × 2 memory address to the slave. When the each memory address input ends, the slave again outputs the acknowledge “L” level. After this operation, the I/O data follows in units of 8 bits, with the acknowledge “L” level output after every 8 bits.

It is determined by the R/W code whether the data line is driven by the master or the slave. However, the clock line shall be driven by the master. For a write operation, the slave will accept 8 bits from the master, then send an acknowledge. If the master detects the acknowledge, the master will transfer the next 8 bits. For a read operation, the slave will place 8 bits on the data line, then wait for an acknowledge from the master.

■ FeRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC1MT performs the high speed write operations, so any waiting time for an ACK polling* does not occur.

*: In E²PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

■ WRITE PROTECT (WP)

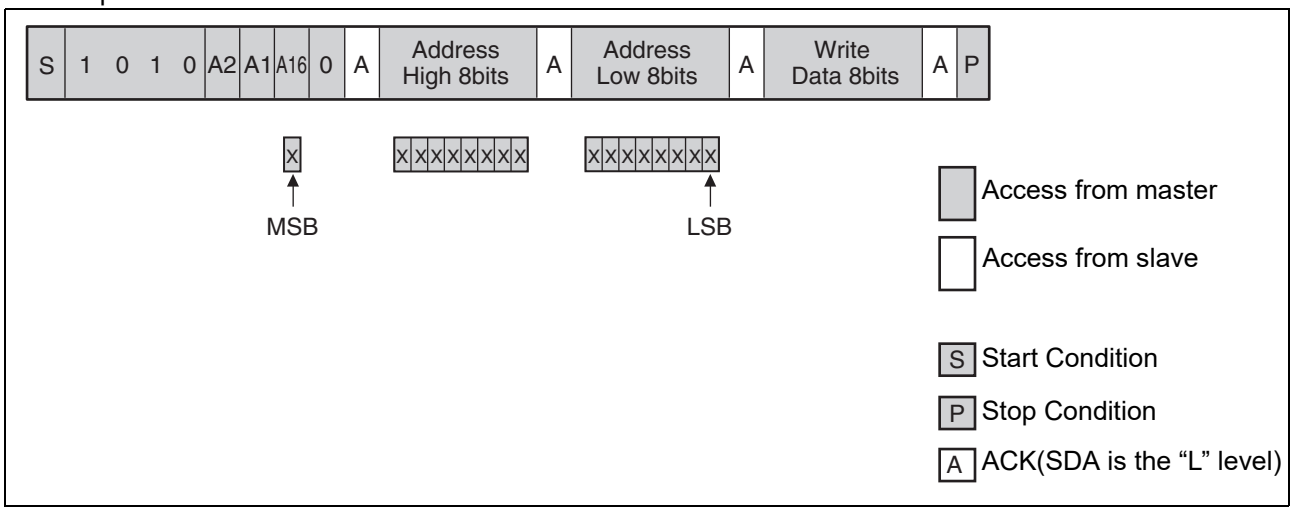
The entire memory array can be write protected using the Write Protect pin. When the Write Protect pin is set to the “H” level, the entire memory array will be write protected. When the Write Protect pin is the “L” level, the entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

Note : The Write Protect pin is pulled down internally to the VSS pin, therefore if the Write Protect pin is open, the pin status is detected as the “L” level (write enabled).

■ COMMAND

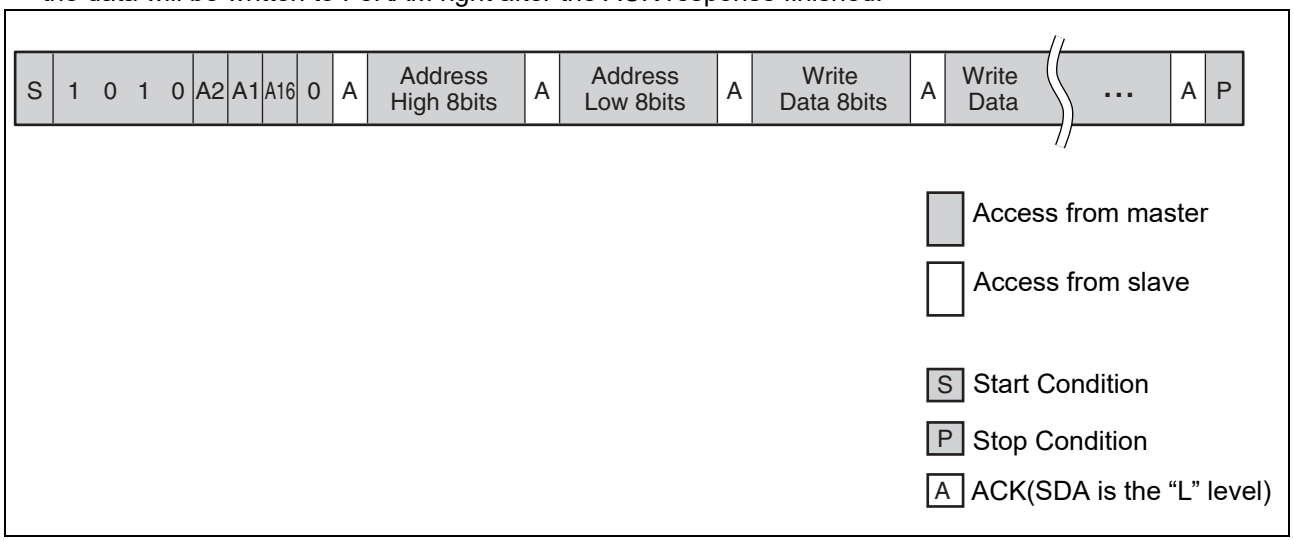
• Byte Write

If the device address word (R/W “0” input) is sent following the start condition, the slave responds with an ACK. After this ACK, write addresses and data are sent in the same way, and the write ends by generating a stop condition at the end.



• Page Write

If additional 8 bits are continuously sent after the same command (except stop condition) as Byte Write, a page write is performed. The memory address rolls over to first memory address (0 0000$_H$) at the end of the address. Therefore, if more than 128 Kbytes are sent, the data is overwritten in order starting from the start of the memory address that was written first. Because FeRAM performs the high-speed write operations, the data will be written to FeRAM right after the ACK response finished.

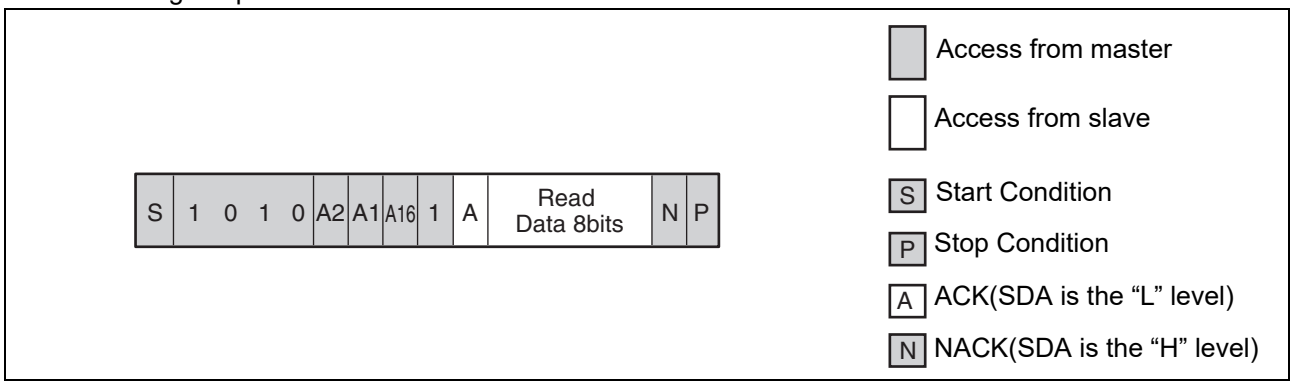


Note: It is not necessary to take a period for internal write operation cycles from the buffer to the memory after the stop condition is generated.

• Current Address Read

If the last write or read operation finished successfully up to the end of stop condition, the memory address that was accessed last remains in the memory address buffer (the length is 17 bits).

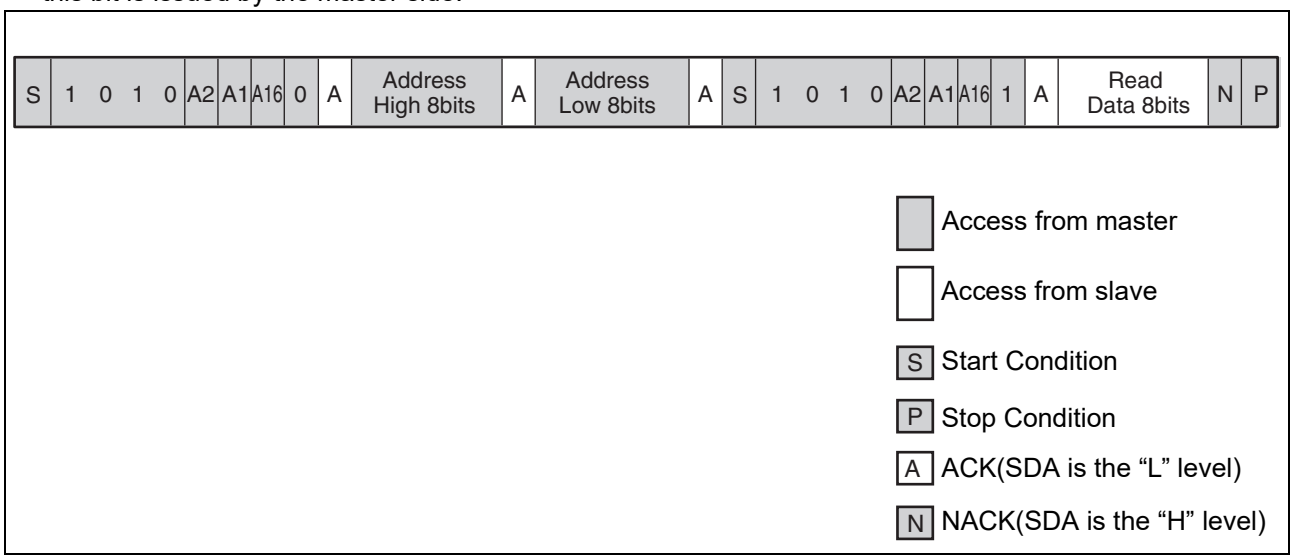
When sending this command without turning the power off, it is possible to read from the memory address n+1 which adds 1 to the total 17-bit memory address n, which consists of the most significant address bit from the device address word input and the lower 16 bits from the memory address buffer. If the memory address n is the last address, it is possible to read with rolling over to the head of the memory address (0 0000_H). The current address(address that the memory address buffer indicates) is undefined immediately after turning the power on.



• Random Read

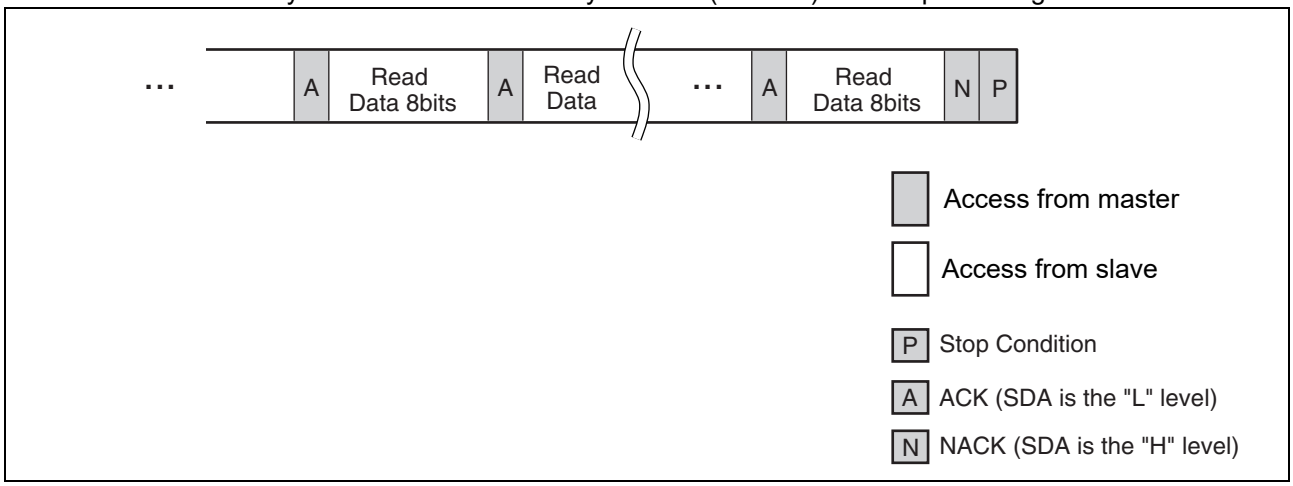
The one byte of data from the memory address saved in the memory address buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Device Address Word (R/W “1” input).

Setting value for the most significant address bit in the first and second Device Address Word shall be the same. The final NACK (SDA is the “H” level) is issued by the receiver that receives the data. In this case, this bit is issued by the master side.



• Sequential Read

Data can be received continuously following the Device address word (R/W “1” input) after specifying the address in the same way as for Random Read. If the read reaches the end of address, the internal read address automatically rolls over to first memory address (0 0000$_H$) and keeps reading.

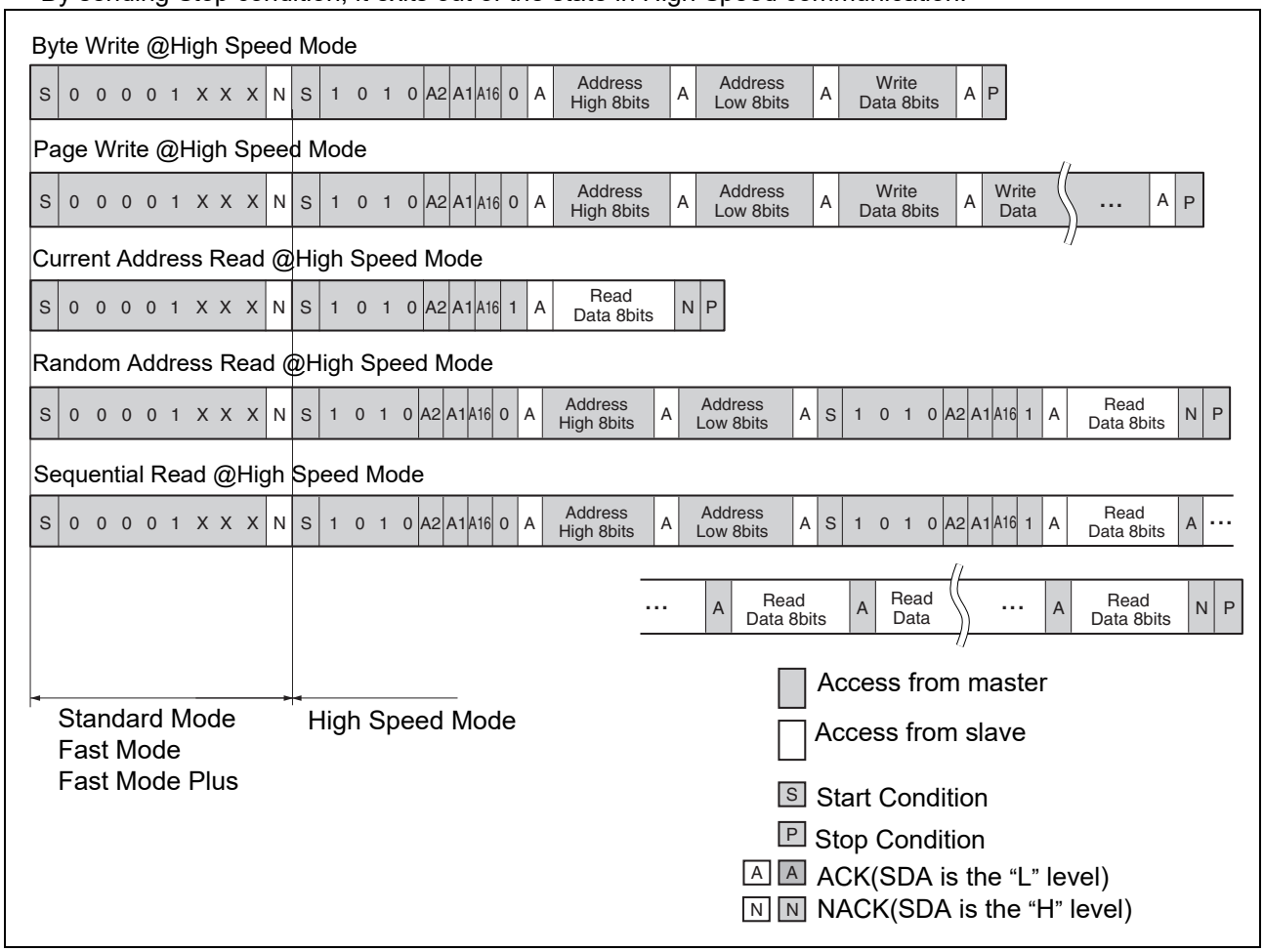


• High Speed Mode

MB85RC1MT supports High Speed mode up to 3.4 MHz. By sending an entry command (0000 1XXX) after start condition from the master side, it informs to the slave that the data transmission with High Speed mode will start.

Since there is no slave side which is allowed to respond to this entry command, NACK response continues from the slave side. After the master side recognizes this NACK response, the master side changes its state to High Speed mode and enables the bidirectional communication up to 3.4 MHz.

By sending Stop condition, it exits out of the state in High Speed communication.

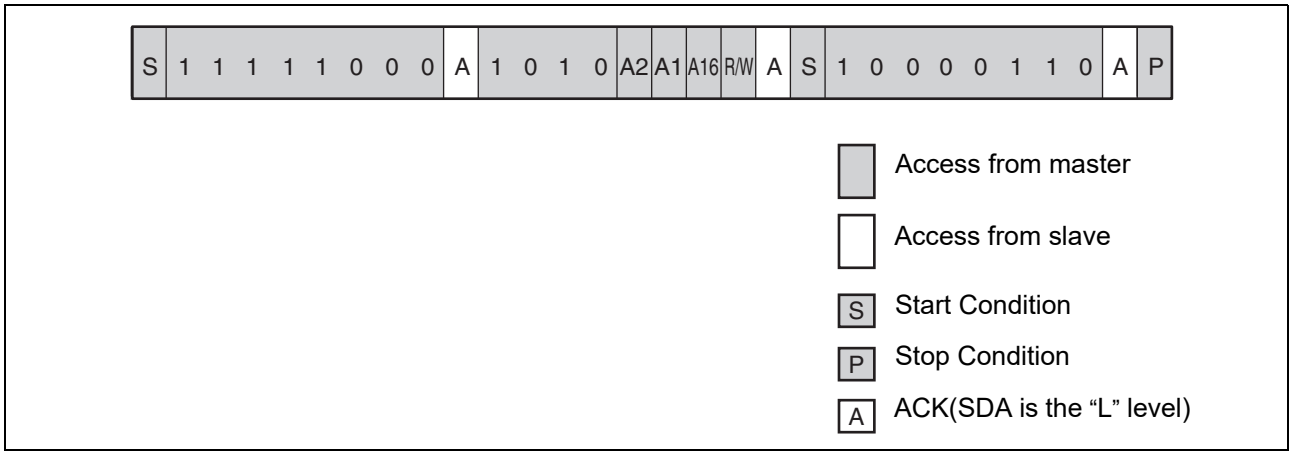


• Sleep Mode

MB85RC1MT provides Sleep mode which reduces less current consumption than Standby mode, by stooping the internal regulator circuits. Following sequences enable the Sleep mode transition.

<Transition to Sleep mode>

a) The master sends start condition followed by F8h.
b) After ACK response from slave, the master sends the device address word.
   In this device address word, the most significant address bit A16 and Read/Write code are Don't care.
c) After ACK response from slave, the master re-sends the start condition followed by 86h.
d) The slave moves to Sleep mode after ACK response to the master.

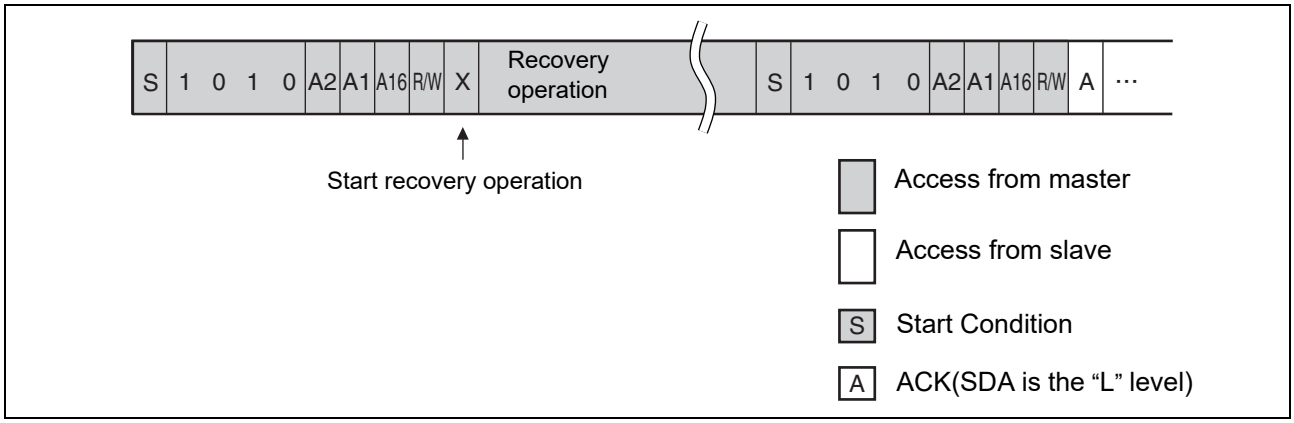


Even if the MB85RC1MT stays in the Sleep mode, SDA and SCL signals are monitored. Following sequences enable the transition to Standby mode after recovery time (t_{REC}) of internal regulator circuits.

<Exit from Sleep mode>

a) The master sends start condition followed by device address word.
   In this device address word, the most significant address bit A16 and Read/Write code are Don't care.
b) At the rising edge of 9th clock from start condition, an internal regulator starts to operate its recovery sequence.
c) After the recovery time (t_{REC}) passed, standby mode enabled.

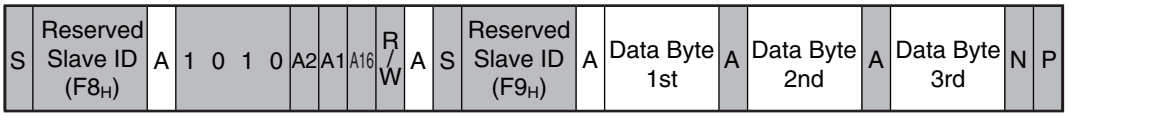
After returning to Standby mode, reading and writing are enabled by sending each command starts with start condition.

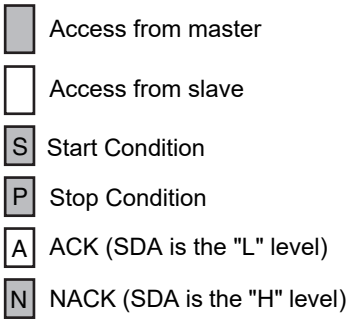


• Device ID

The Device ID command reads fixed Device ID. The size of Device ID is 3 bytes and consists of manufacturer ID and product ID. The Device ID is read-only and can be read out by following sequences.

a) The master sends the Reserved Slave ID $F8_H$ after the START condition.
b) The master sends the device address word after the ACK response from the slave.
   In this device address word, the most significant address and R/W code are “Don't care”.
c) The master re-sends the START condition followed by the Reserved Slave ID $F9_H$ after the ACK response from the slave.
d) The master read out the Device ID succeedingly in order of Data Byte 1st / 2nd / 3rd after the ACK response from the slave.
e) The master responds the NACK (SDA is the “H” level) after reading 3 bytes of the Device ID.
   In case the master respond the ACK after reading 3 bytes of the Device ID, the master re-reading the Device ID from the 1st byte.





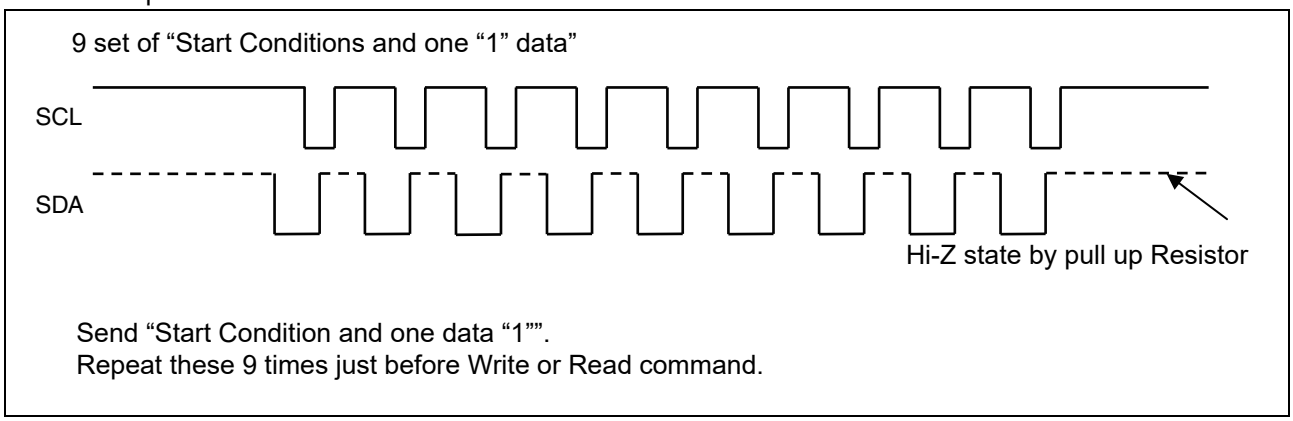
Data Byte 1st								Data Byte 2nd				Data Byte 3rd											
Manufacture ID = $00A_H$												Product ID = 758_H											
11	10	9	8	7	6	5	4	3	2	1	0	11	10	9	8	7	6	5	4	3	2	1	0
Fujitsu Semiconductor												Density = 7_H				Proprietary use							
0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	0	1	0	1	1	0	0	0

■ SOFTWARE RESET SEQUENCE OR COMMAND RETRY

In case the malfunction has occurred after power on, the master side stopped the I²C communication during processing, or unexpected malfunction has occurred, execute the following (1) software recovery sequence just before each command, or (2) retry command just after failure of each command.

(1) Software Reset Sequence

Since the slave side may be outputting “L” level, do not force to drive “H” level, when the master side drives the SDA port. This is for preventing a bus conflict. The additional hardware is not necessary for this software reset sequence.



(2) Command Retry

Command retry is useful to recover from failure response during I²C communication.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+4.0	V
Input voltage*	V_{IN}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Output voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Operation ambient temperature	T_A	− 40	+ 85	°C
Storage temperature	Tstg	− 55	+ 125	°C

*: These parameters are based on the condition that VSS is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	V_{DD}	1.8	—	3.6	V
Operation ambient temperature*2	T_A	− 40	—	+ 85	°C

*1: These parameters are based on the condition that VSS is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*1	$\|I_{LI}\|$	V_{IN} = 0 V to V_{DD}	—	—	1	μA
Output leakage current*2	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{DD}	—	—	1	μA
Operating power supply current	I_{DD}	SCL = 0.1 MHz	—	0.04	—	mA
		SCL = 1 MHz	—	0.24	0.44	mA
		SCL = 3.4 MHz	—	0.71	1.2	mA
Standby current	I_{SB}	SCL, SDA = V_{DD} A1, A2, WP = 0 V or V_{DD} or Open Under Stop Condition T_A = + 25 °C	—	15	120	μA
Sleep current	I_{ZZ}	SCL, SDA = V_{DD} A1, A2, WP = 0 V		4	10	μA
"H" level input voltage	V_{IH}	V_{DD} = 1.8 V to 3.6 V	$V_{DD} \times 0.7$	—	V_{DD}	V
"L" level input voltage	V_{IL}	V_{DD} = 1.8 V to 3.6 V	V_{SS}	—	$V_{DD} \times 0.3$	V
"L" level output voltage	V_{OL}	I_{OL} = 3 mA	—	—	0.4	V
Input resistance for WP, A1 and A2 pins	R_{IN}	$V_{IN} = V_{IL}$ (Max)	50	—	—	kΩ
		$V_{IN} = V_{IH}$ (Min)	1	—	—	MΩ

*1: Applicable pin: SCL,SDA

*2: Applicable pin: SDA

2. AC Characteristics

Parameter	Symbol	Value								Unit
		STANDARD MODE		FAST MODE		FAST MODE PLUS		HIGH SPEED MODE		
		Min	Max	Min	Max	Min	Max	Min	Max	
SCL clock frequency	FSCL	0	100	0	400	0	1000	0	3400	kHz
Clock high time	T_{HIGH}	4000	—	600	—	260*1	—	60	—	ns
Clock low time	T_{LOW}	4700	—	1300	—	500*2	—	160	—	ns
SCL/SDA rising time	T_r	—	1000	—	300	—	300	—	80	ns
SCL/SDA falling time	T_f	—	300	—	300	—	120	—	80	ns
Start condition hold	$T_{HD:STA}$	4000	—	600	—	250	—	160	—	ns
Start condition setup	$T_{SU:STA}$	4700	—	600	—	250	—	160	—	ns
SDA input hold	$T_{HD:DAT}$	0	—	0	—	0	—	0	—	ns
SDA input setup	$T_{SU:DAT}$	250	—	100	—	50	—	16*4	—	ns
SDA output hold	$T_{DH:DAT}$	0	—	0	—	0	—	0	—	ns
Stop condition setup	$T_{SU:STO}$	4000	—	600	—	250	—	160	—	ns
SDA output access after SCL falling	T_{AA}	—	3000	—	900	—	450*3	—	130	ns
Pre-charge time	T_{BUF}	4700	—	1300	—	500	—	300	—	ns
Noise suppression time (SCL and SDA)	T_{SP}	—	50	—	50	—	50	—	5	ns

*1: 300ns @VDD ≤ 2.7 V

*2: 600ns @VDD ≤ 2.7 V

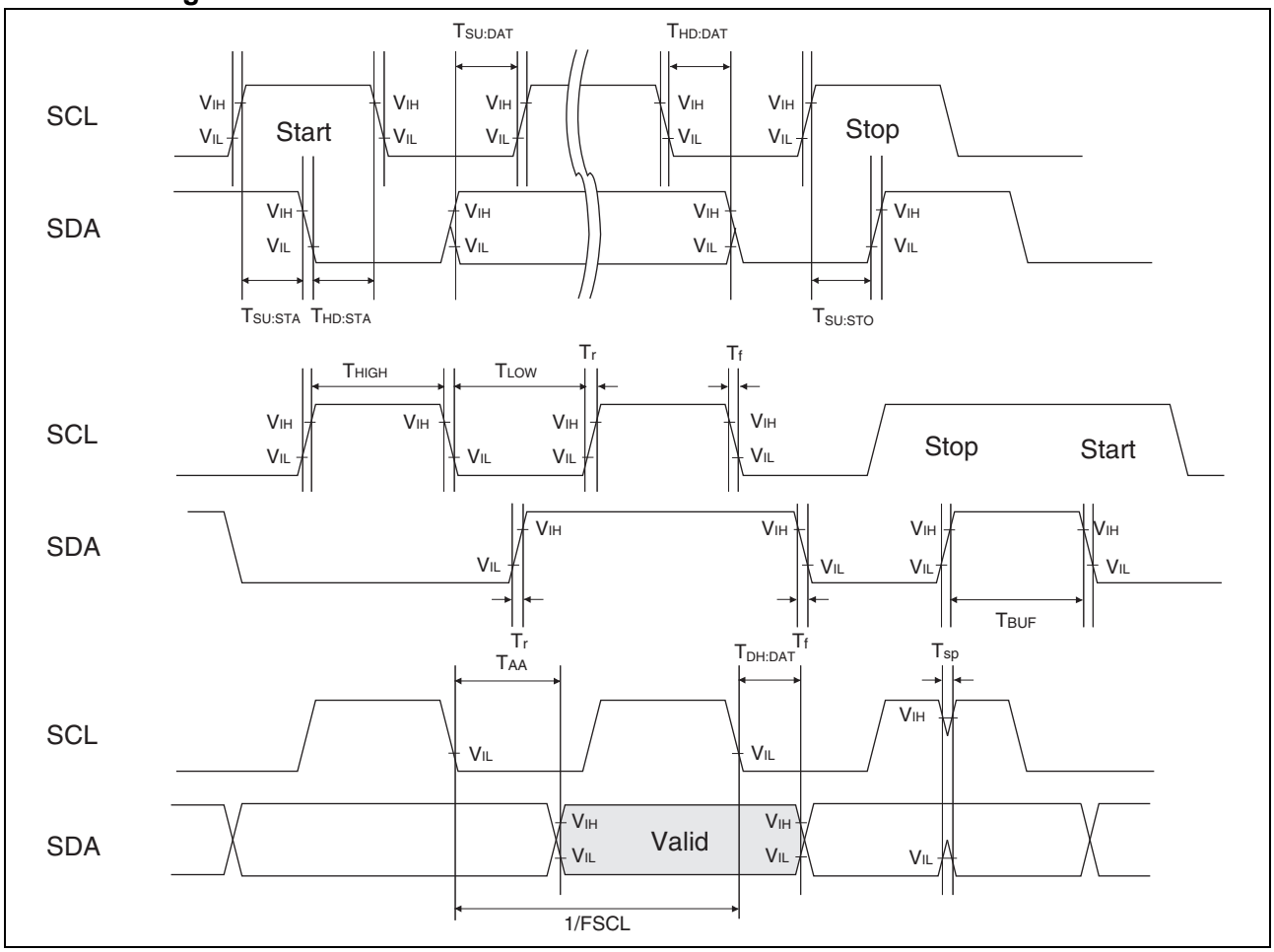
*3: 550ns @VDD ≤ 2.7 V

*4: 26ns @VDD ≤ 2.7 V

AC characteristics were measured under the following measurement conditions.

Power supply voltage	: 1.8 V to 3.6 V
Operation ambient temperature	: − 40 °C to + 85 °C
Input voltage magnitude	: $V_{DD} \times 0.3$ to $V_{DD} \times 0.7$
Input rising time	: 5 ns
Input falling time	: 5 ns
Input judge level	: $V_{DD}/2$
Output judge level	: $V_{DD}/2$
Output load capacitance	: 100 pF

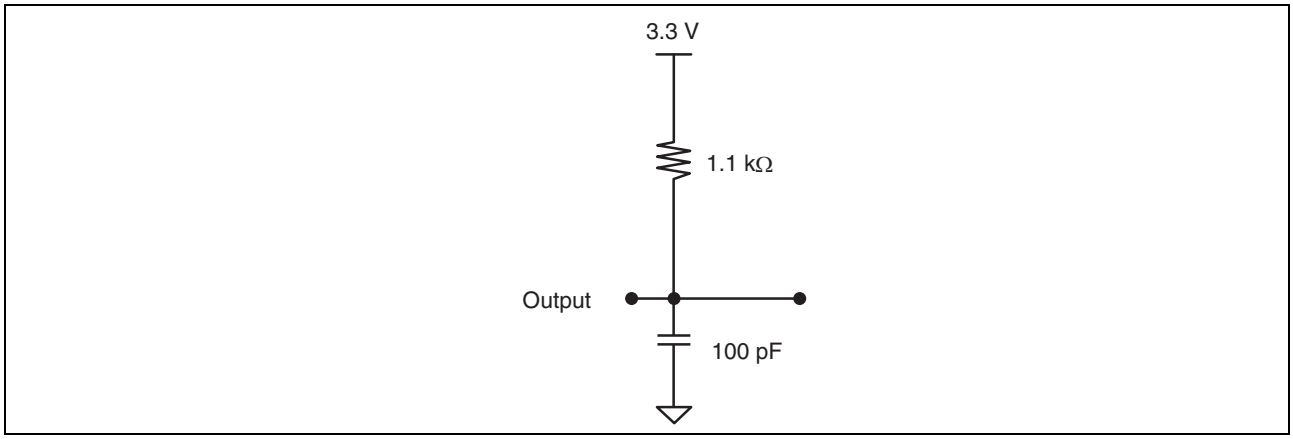
3. AC Timing Definitions



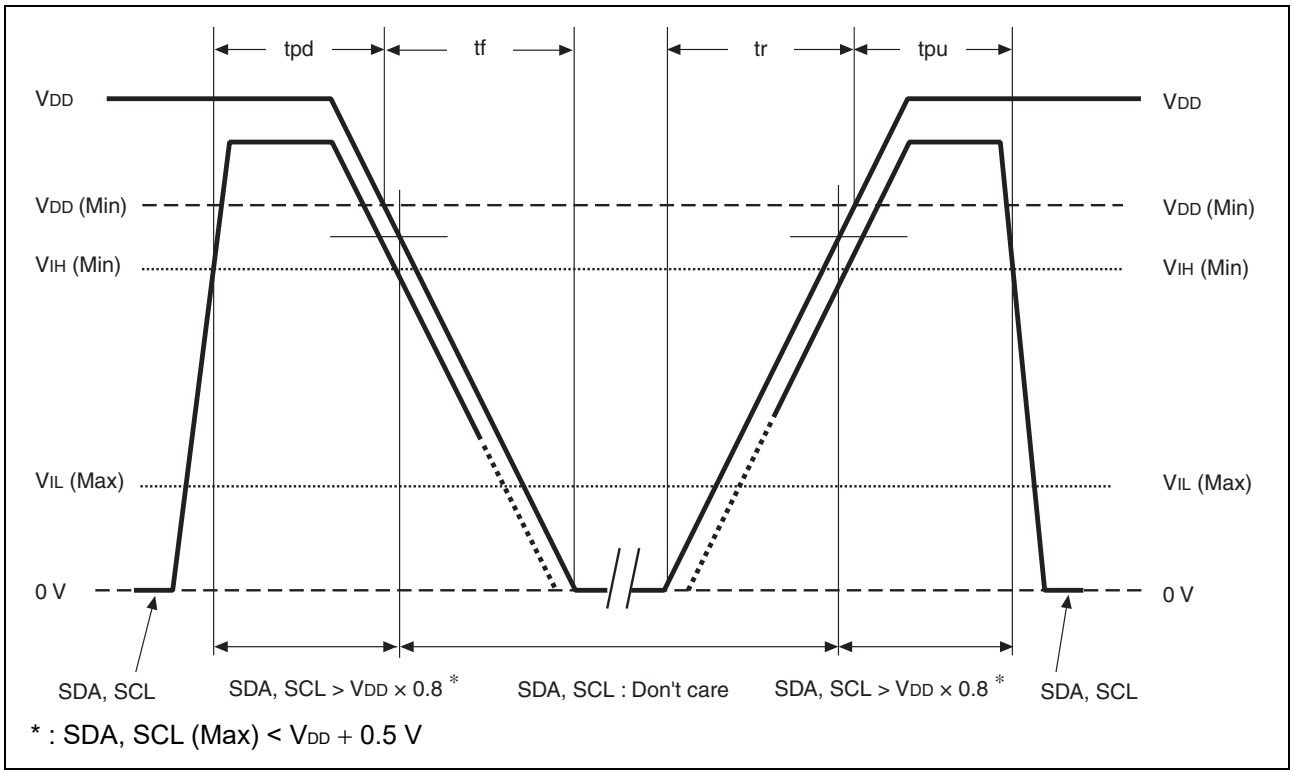
4. Pin Capacitance

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I/O capacitance	$C_{I/O}$	V_{DD} = 3.3 V, f = 1 MHz, T_A = + 25 °C	—	—	8	pF
Input capacitance	C_{IN}		—	—	8	pF

5. AC Test Load Circuit



■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value		Unit
		Min	Max	
SDA, SCL level hold time during power down	tpd	85	—	ns
SDA, SCL level hold time during power up	tpu	250	—	µs
Power supply rising time	tr	0.05	—	ms/V
Power supply falling time	tf	0.1	—	ms/V
Internal regulator recovery time	t_{REC}	—	400	µs

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{13}	—	Times/byte	Operation Ambient Temperature T_A = + 85 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 85 °C
	95	—		Operation Ambient Temperature T_A = + 55 °C
	≥ 200	—		Operation Ambient Temperature T_A = + 35 °C

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

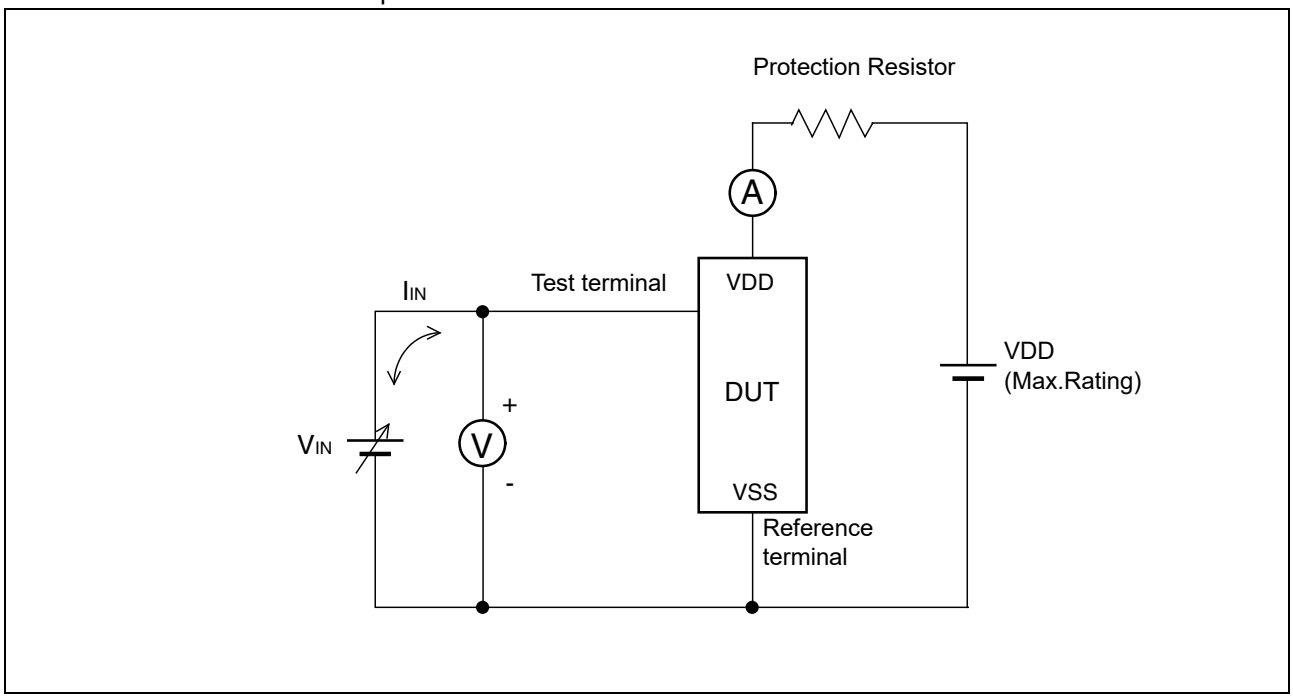
■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.
- During the access period from the start condition to the stop condition, keep the level of WP, A1 and A2 pins to the “H” level or the “L” level.

■ ESD AND LATCH-UP

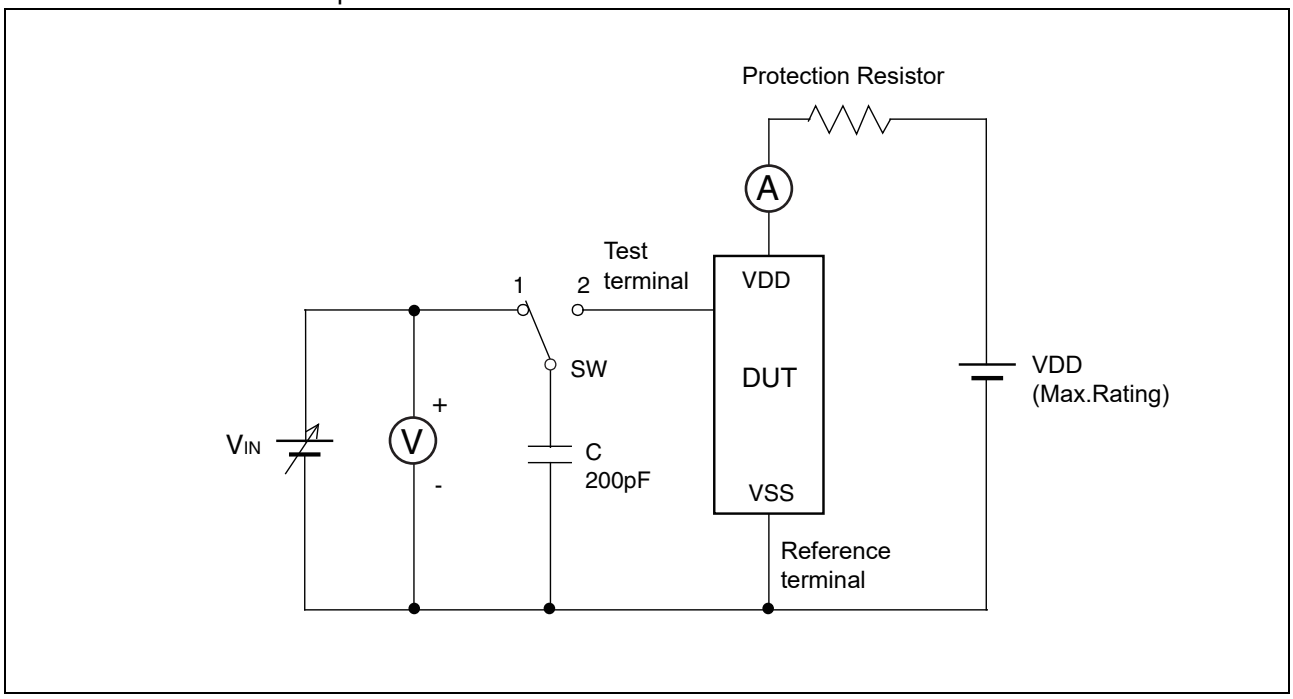
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RC1MTPNF-G-JNE1	≥ |2000 V|
ESD MM (Machine Model) JESD22-A115 compliant		≥ |200 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		≥ |1000 V|
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		—
Latch-Up (C-V Method) Proprietary method		≥ |200 V|

- Current method of Latch-Up Resistance Test



Note : The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow. Confirm the latch up does not occur under $I_{IN} = \pm 300$ mA.
In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

• C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

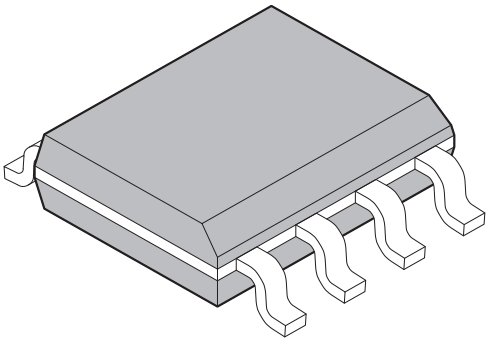
This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RC1MTPNF-G-JNE1	8-pin, plastic SOP (FPT-8P-M02)	Tube	—*
MB85RC1MTPNF-G-JNERE1	8-pin, plastic SOP (FPT-8P-M02)	Embossed Carrier tape	1500

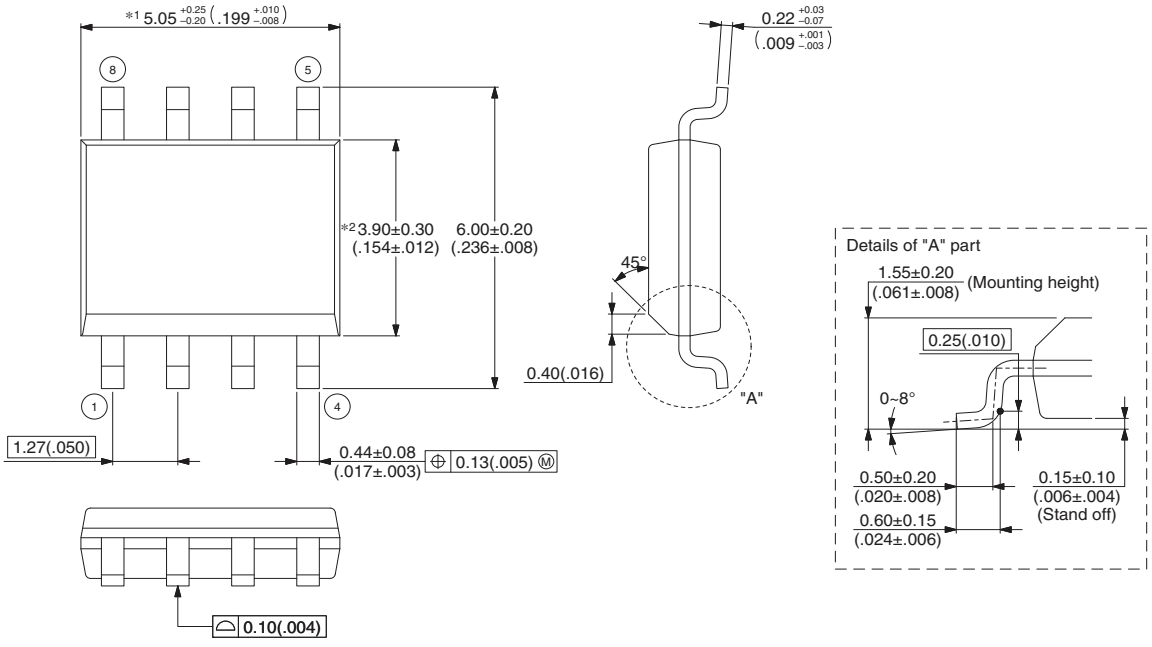
*: Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSION

8-pin plastic SOP		
 (FPT-8P-M02)	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g

8-pin plastic SOP
(FPT-8P-M02)

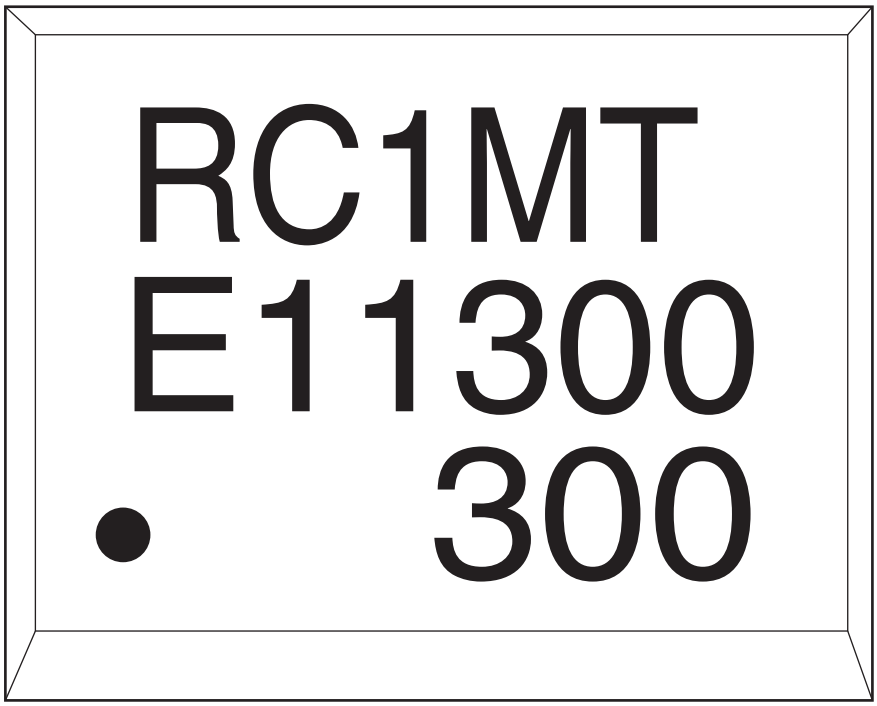
Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

■ MARKING

[MB85RC1MTPNF-G-JNE1]
[MB85RC1MTPNF-G-JNERE1]



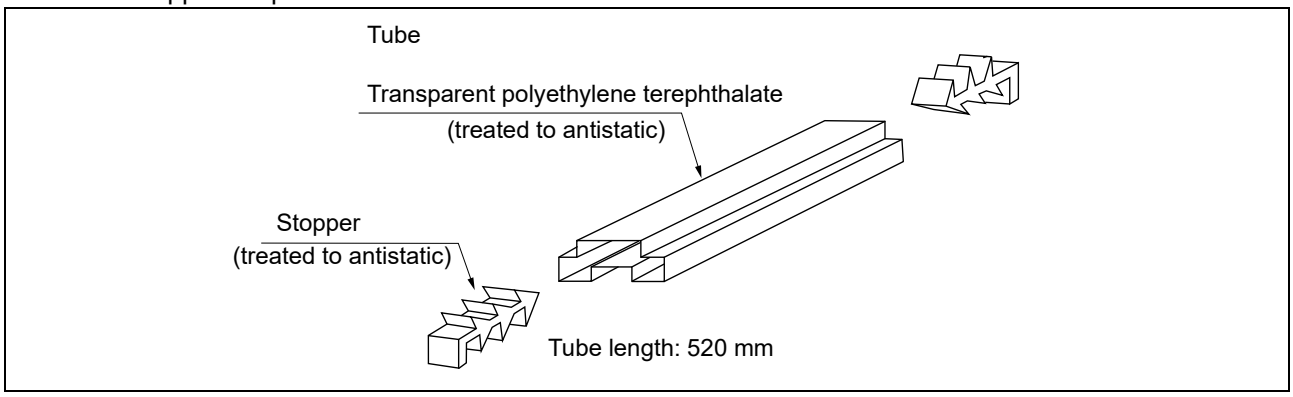
[FPT-8P-M02]

■ PACKING INFORMATION

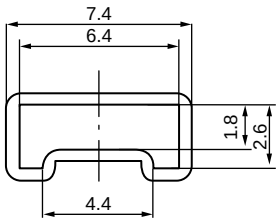
1. Tube

1.1 Tube Dimensions

- Tube/stopper shape

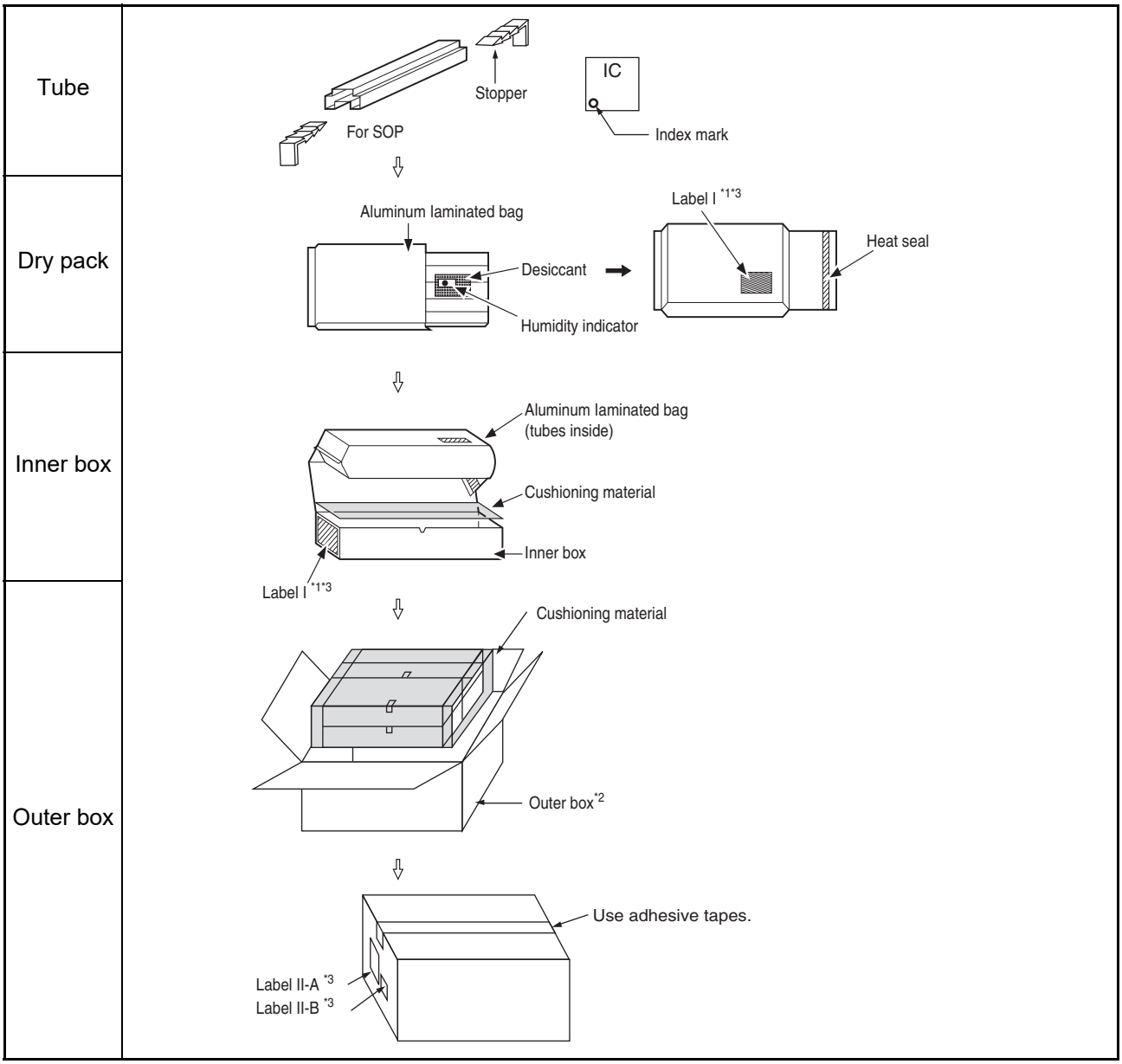


Tube cross-sections and Maximum quantity

Package form	Package code	Maximum quantity		
		pcs/ tube	pcs/inner box	pcs/outer box
SOP, 8, plastic (2)	FPT-8P-M02	95	7600	30400
 t = 0.5 Transparent polyethylene terephthalate				

(Dimensions in mm)

1.2 Tube Dry pack packing specifications



*1: For a product of witch part number is suffixed with “E1”, a “ G Pb ” marks is display to the moisture barrier bag and the inner boxes.

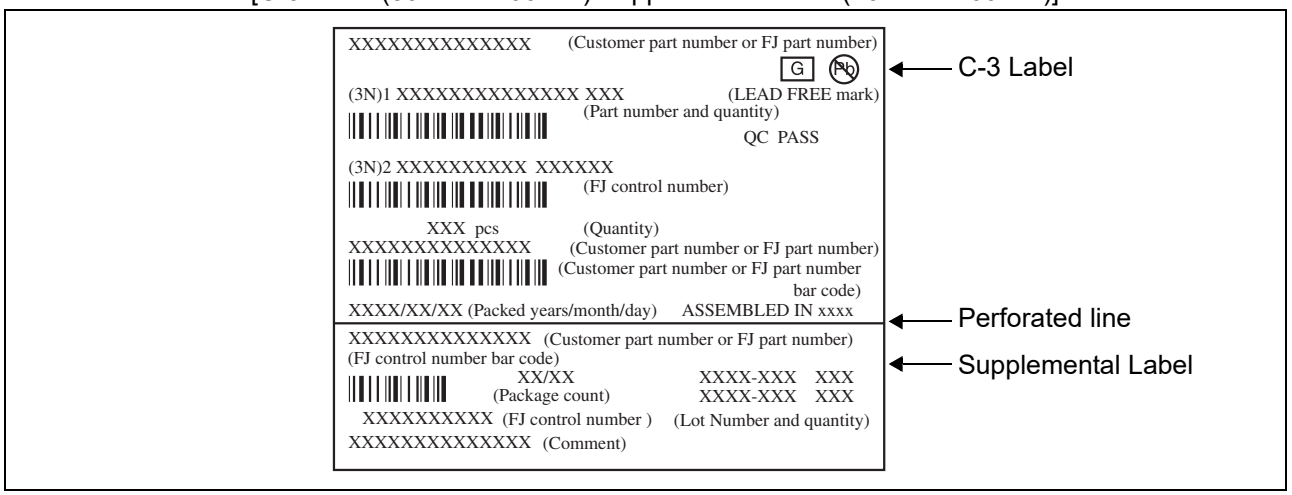
*2: The space in the outer box will be filled with empty inner boxes, or cushions, etc.

*3: Please refer to an attached sheet about the indication label.

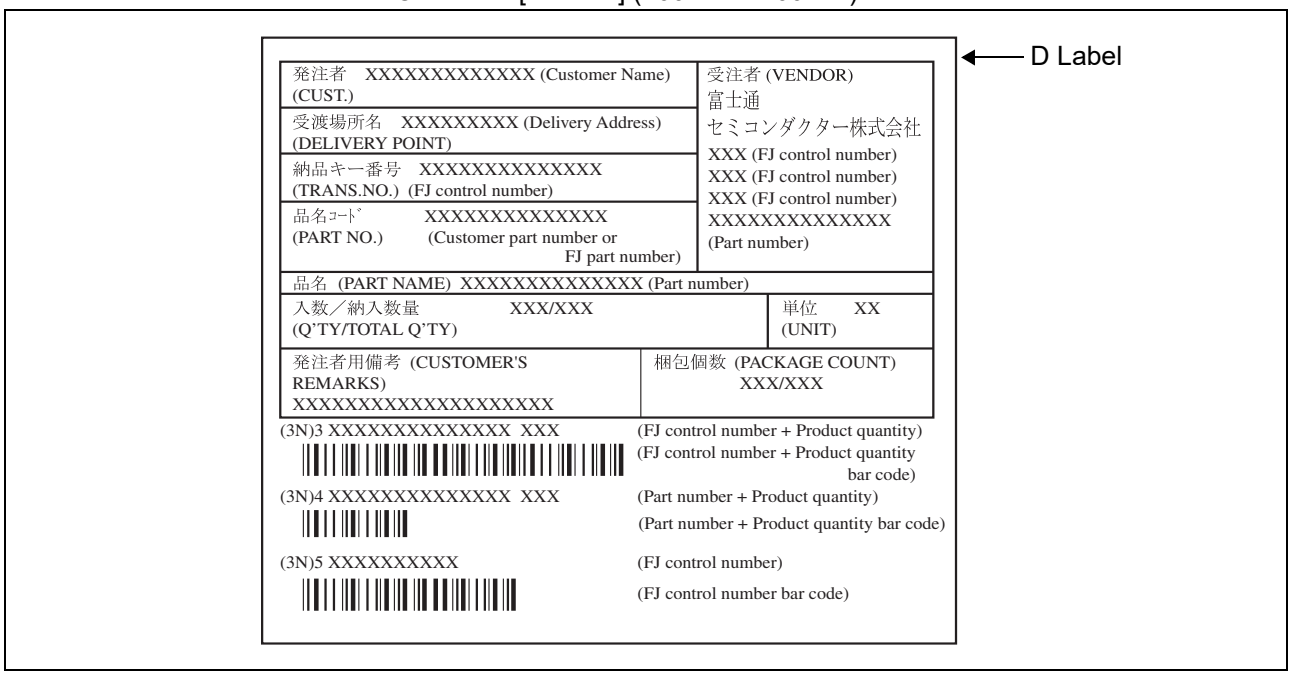
Note: The packing specifications may not be applied when the product is delivered via a distributor.

1.3 Product label indicators

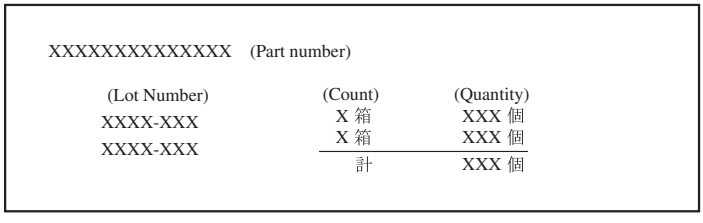
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



Label II-A: Label on Outer box [D Label] (100mm × 100mm)



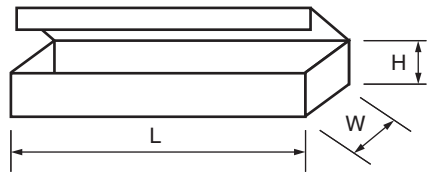
Label II-B: Outer boxes product indicate



Note: Depending on shipment state, “Label II-A” and “Label II-B” on the external boxes might not be printed.

1.4 Dimensions for Containers

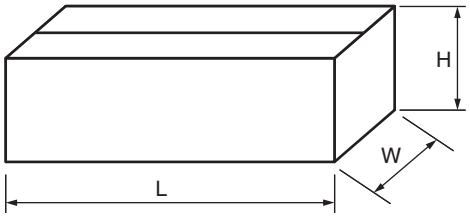
(1) Dimensions for inner box



L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box



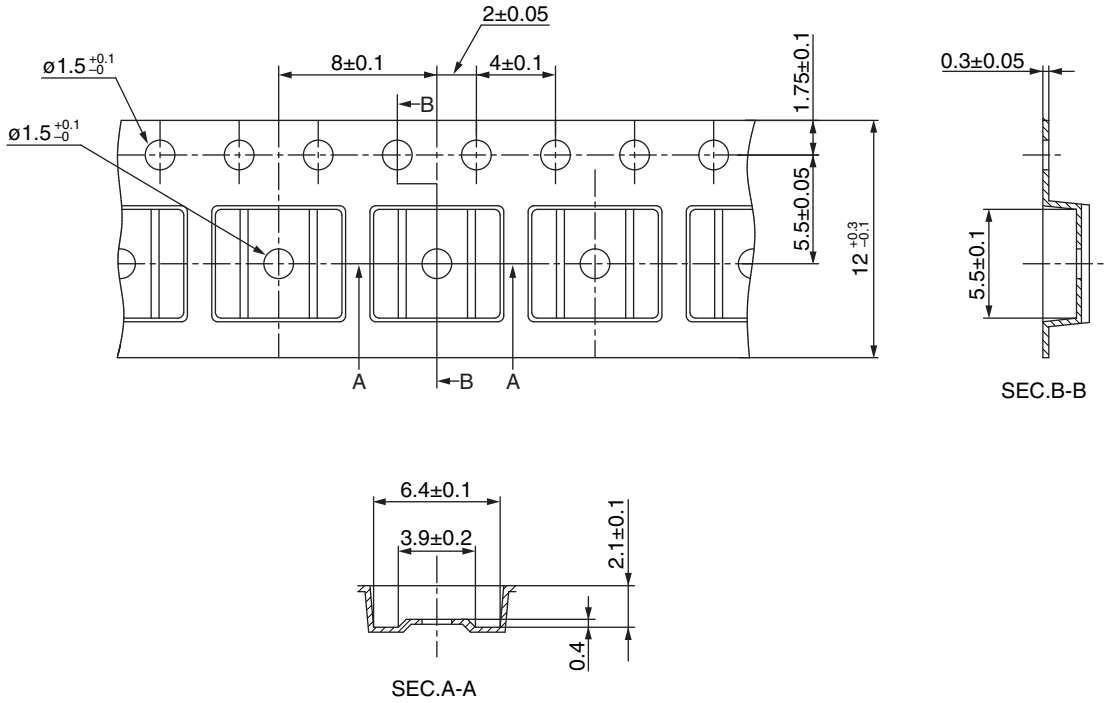
L	W	H
565	270	180

(Dimensions in mm)

2. Emboss Tape

2.1 Tape Dimensions

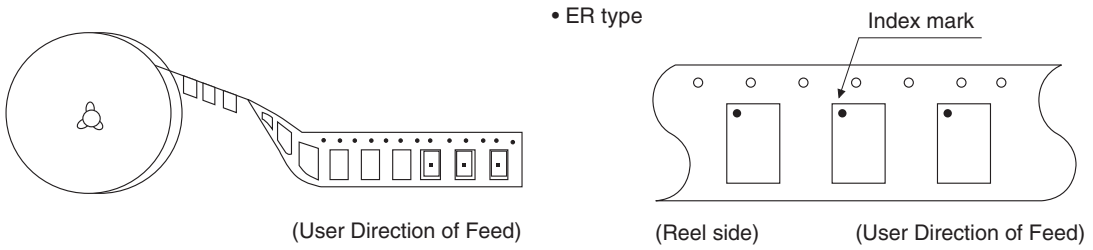
PKG code	Reel No	Maximum storage capacity		
		pcs/reel	pcs/inner box	pcs/outer box
FPT-8P-M02	3	1500	1500	10500



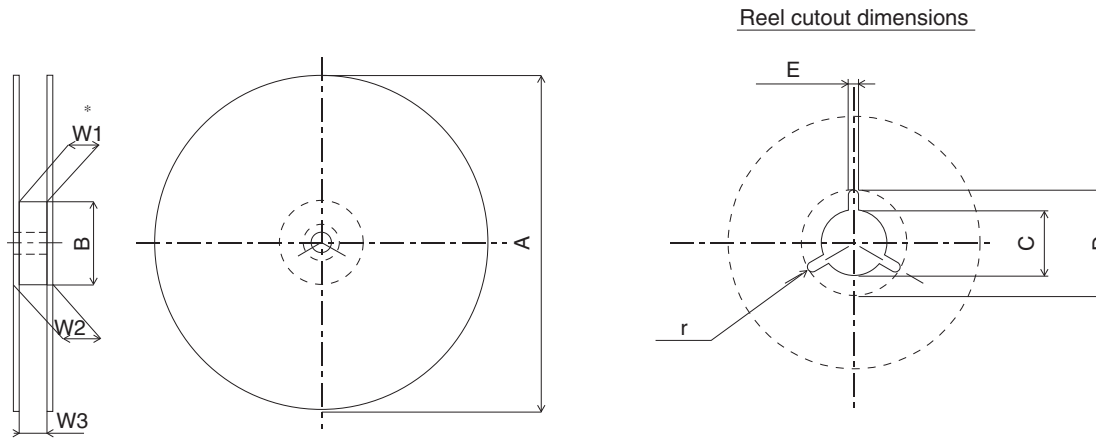
(Dimensions in mm)

Material : Conductive polystyrene
Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

2.2 IC orientation



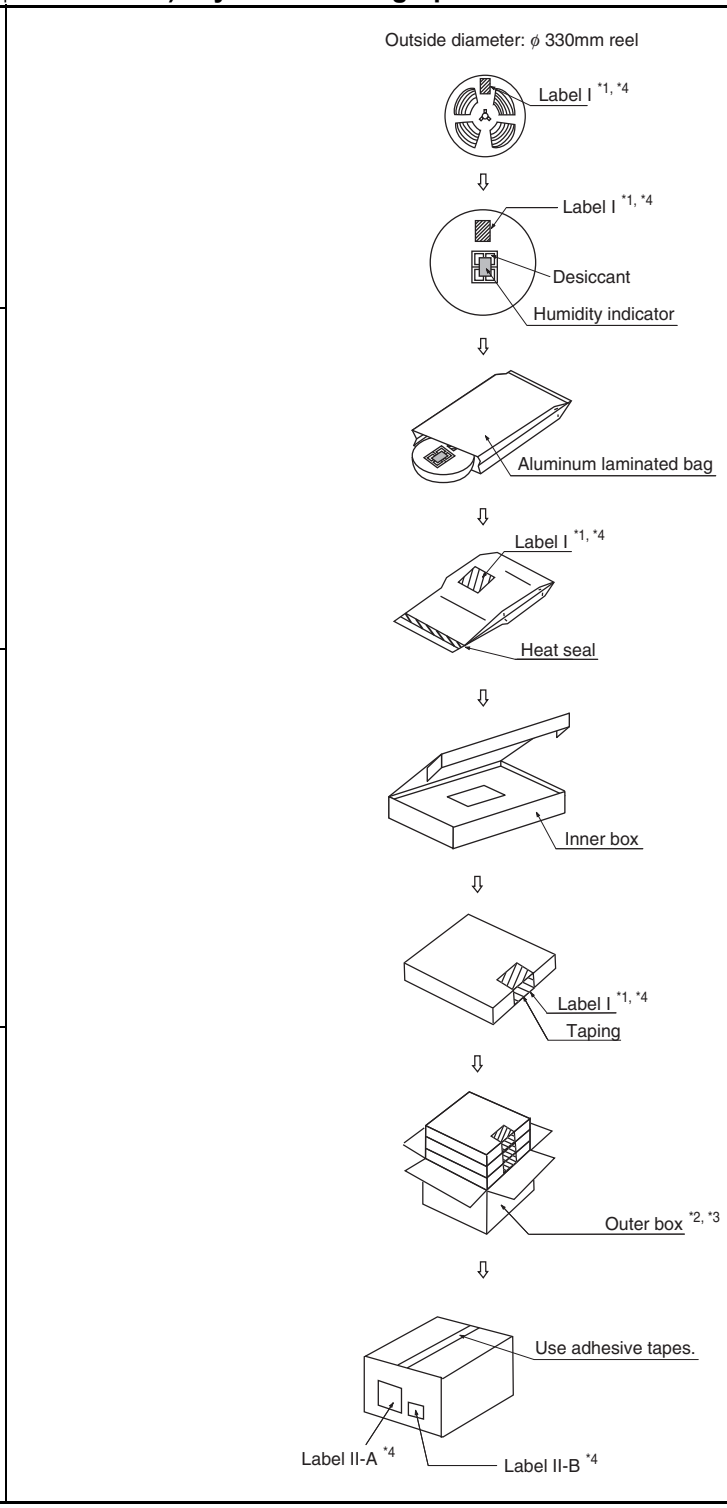
2.3 Reel dimensions



Dimensions in mm

Reel No	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Tape width / Symbol	8	12		16		24		32		44		56	12	16	24
A	254 ± 2	254 ± 2	330 ± 2	254 ± 2	330 ± 2	254 ± 2	330 ± 2	330 ± 2							
B	100^{+2}_{-0}							100^{+2}_{-0}	150^{+2}_{-0}	100^{+2}_{-0}	150^{+2}_{-0}	100^{+2}_{-0}	100 ± 2		
C	13 ± 0.2												$13^{+0.5}_{-0.2}$		
D	21 ± 0.8												$20.5^{+1}_{-0.2}$		
E	2 ± 0.5														
W1	8.4^{+2}_{-0}	12.4^{+2}_{-0}		16.4^{+2}_{-0}		24.4^{+2}_{-0}		32.4^{+2}_{-0}		44.4^{+2}_{-0}		56.4^{+2}_{-0}	12.4^{+1}_{-0}	16.4^{+1}_{-0}	$24.4^{+0.1}_{-0}$
W2	less than 14.4	less than 18.4		less than 22.4		less than 30.4		less than 38.4		less than 50.4		less than 62.4	less than 18.4	less than 22.4	less than 30.4
W3	7.9 ~ 10.9	11.9 ~ 15.4		15.9 ~ 19.4		23.9 ~ 27.4		31.9 ~ 35.4		43.9 ~ 47.4		55.9 ~ 59.4	12.4 ~ 14.4	16.4 ~ 18.4	24.4 ~ 26.4
r	1.0														

2.4 Taping (ϕ330mm Reel) Dry Pack Packing Specifications

Embossed tapes	
Dry pack	
Inner box	
Outer box	

*1: For a product of witch part number is suffixed with “E1”, a “ G Pb ” marks is display to the moisture barrier bag and the inner boxes.

*2: The size of the outer box may be changed depending on the quantity of inner boxes.

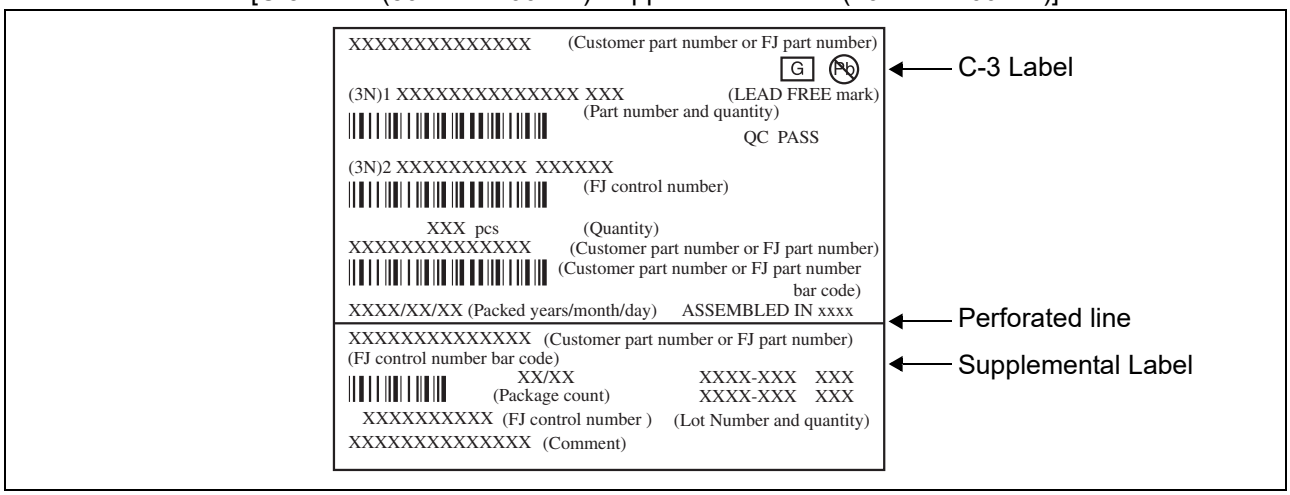
*3: The space in the outer box will be filled with empty inner boxes, or cushions, etc.

*4: Please refer to an attached sheet about the indication label.

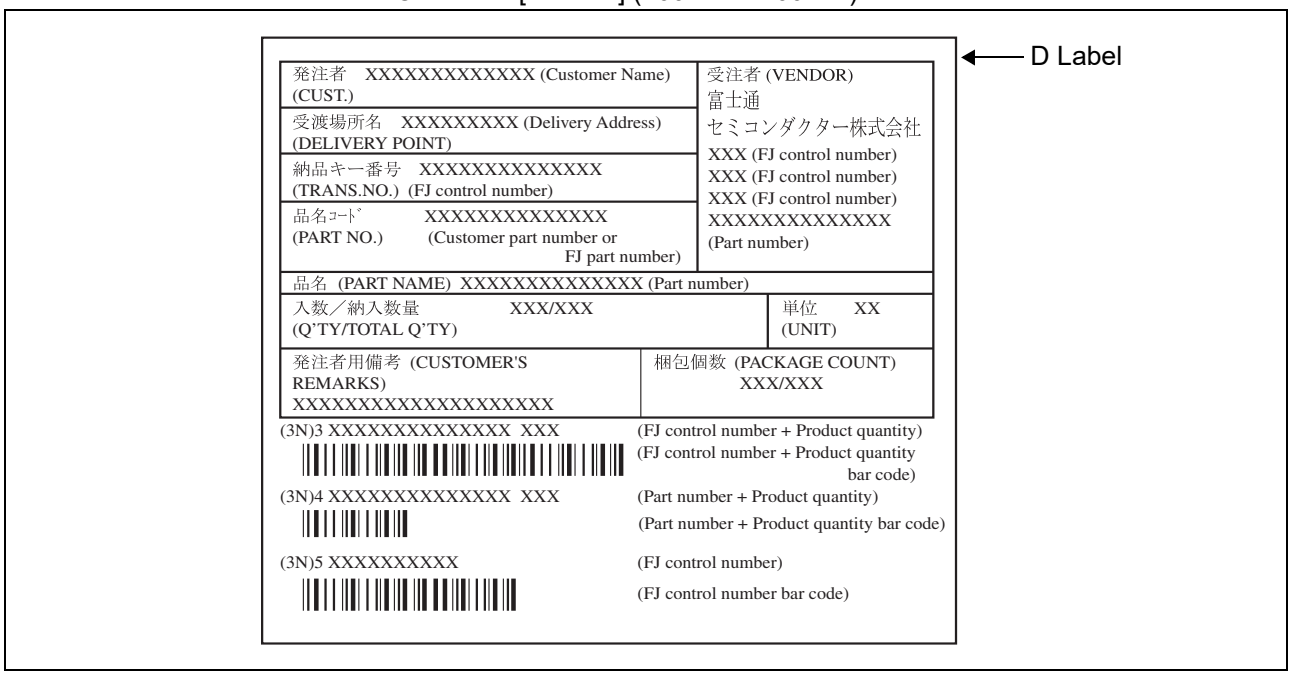
Note: The packing specifications may not be applied when the product is delivered via a distributor.

2.5 Product label indicators

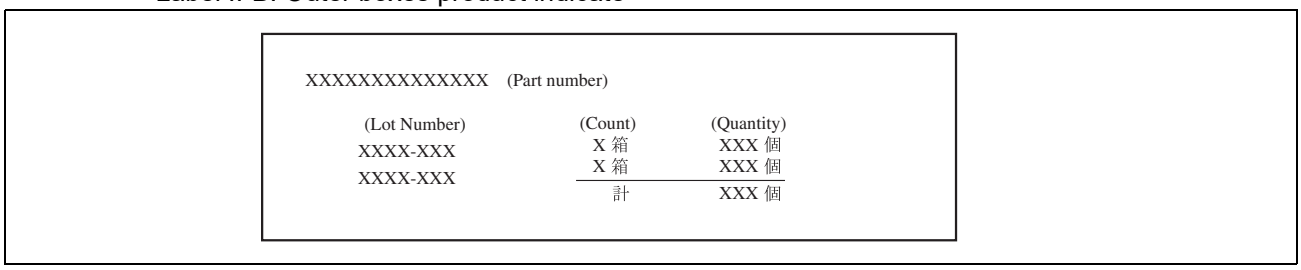
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



Label II-A: Label on Outer box [D Label] (100mm × 100mm)



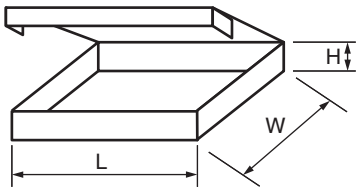
Label II-B: Outer boxes product indicate



Note: Depending on shipment state, “Label II-A” and “Label II-B” on the external boxes might not be printed.

2.6 Dimensions for Containers

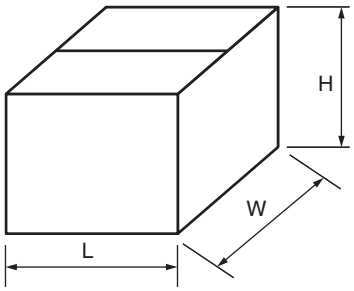
(1) Dimensions for inner box



Tape width	L	W	H
12, 16	365	345	40
24, 32			50
44			65
56			75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
415	400	315

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
—	Overall	Following technical word is revised to more commonly used one. FRAM to FeRAM

FUJITSU SEMICONDUCTOR MEMORY SOLUTION LIMITED
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Kohoku-ku, Yokohama, Kanagawa 222-0033, Japan
https://www.fujitsu.com/jp/fsm/en/

Edited: Sales and Marketing Division