

SPECIFICATION FOR LCM+CTP Module

MODULE No:	KD070WXFID050-C038A
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Part. No	KD070WXFID050-C038A	REV	V1.2	Page 1 of 38
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	



Revision History

[illegible]

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1. Basic Specifications

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, capacitance touch panel, back-light unit. The resolution of a 7.0" TFT-LCD contains 800x1280 pixels, and can display up to 16.7M colors.

1.1 TFT Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	94.2(H)*150.72(V) (7.0inch)	mm	
Driver element	TFT active matrix	-	
Display colors	16.7M	colors	
Number of pixels	800(RGB)*1280	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.11775(H)*0.11775(V)	mm	
Viewing angle	Free	o'clock	
Controller IC	ILI9881C	-	
Display mode	Transmissive /Normally Black	-	
LCM Interface	4-Lane MIPI	-	
Operating temperature	-20~+70	°C	
Storage temperature	-30~+80	°C	
Module bonding technology	Use Optical bonding between LCM and CTP	-	

1.2 CTP Features

General Information Items	Specification	Unit	Note
	Main Panel		
Resolution	800(H)*1280(V)	-	
Structure	G+G	-	
Controller IC	GT9271	-	
Interface	I2C	-	
Slave Address	0x5D(7bit) or 0x14(7bit)	-	Note1
Touch mode	Ten points and Gestures	-	-

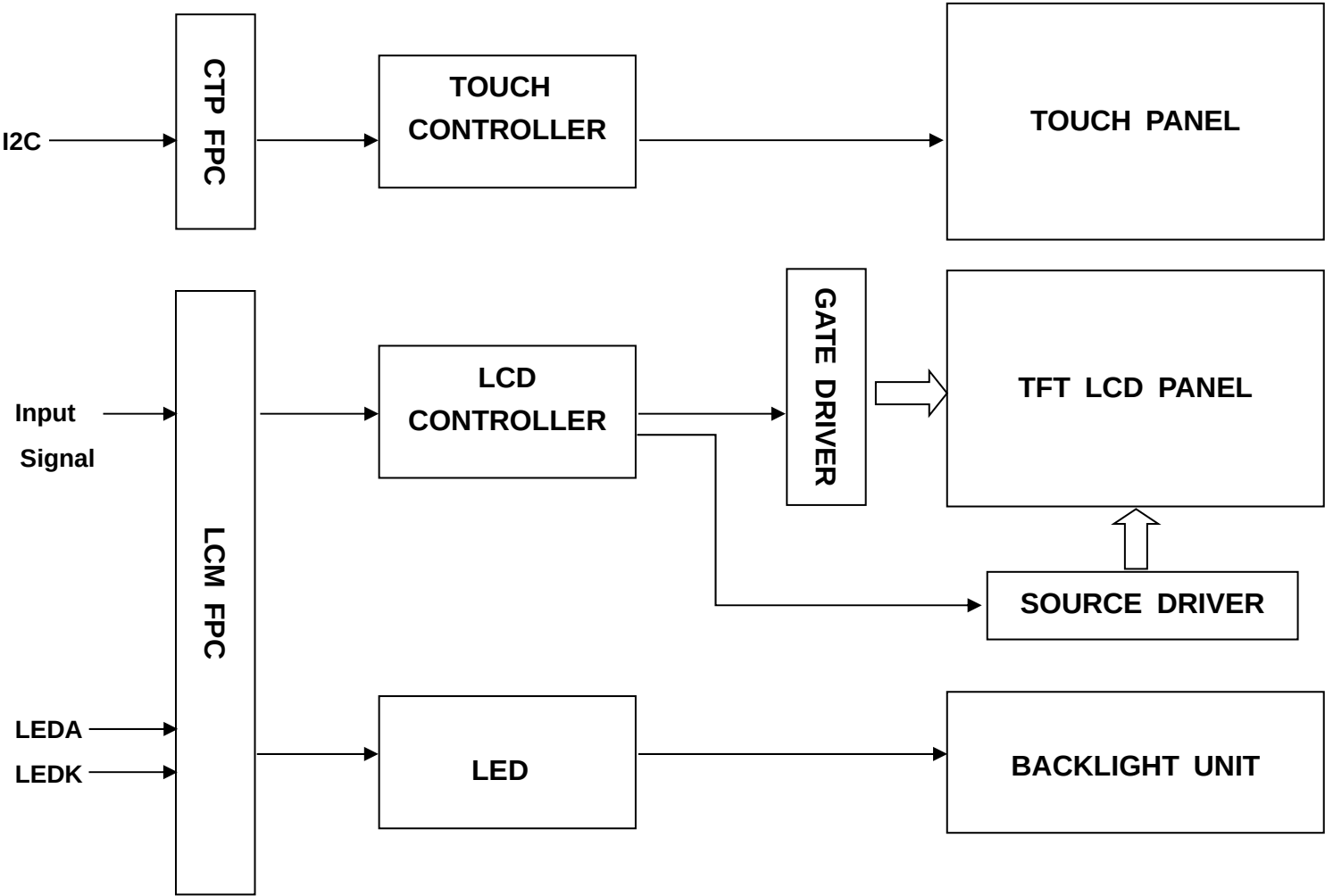
Note1: For specific configuration method, please refer to section 8.2

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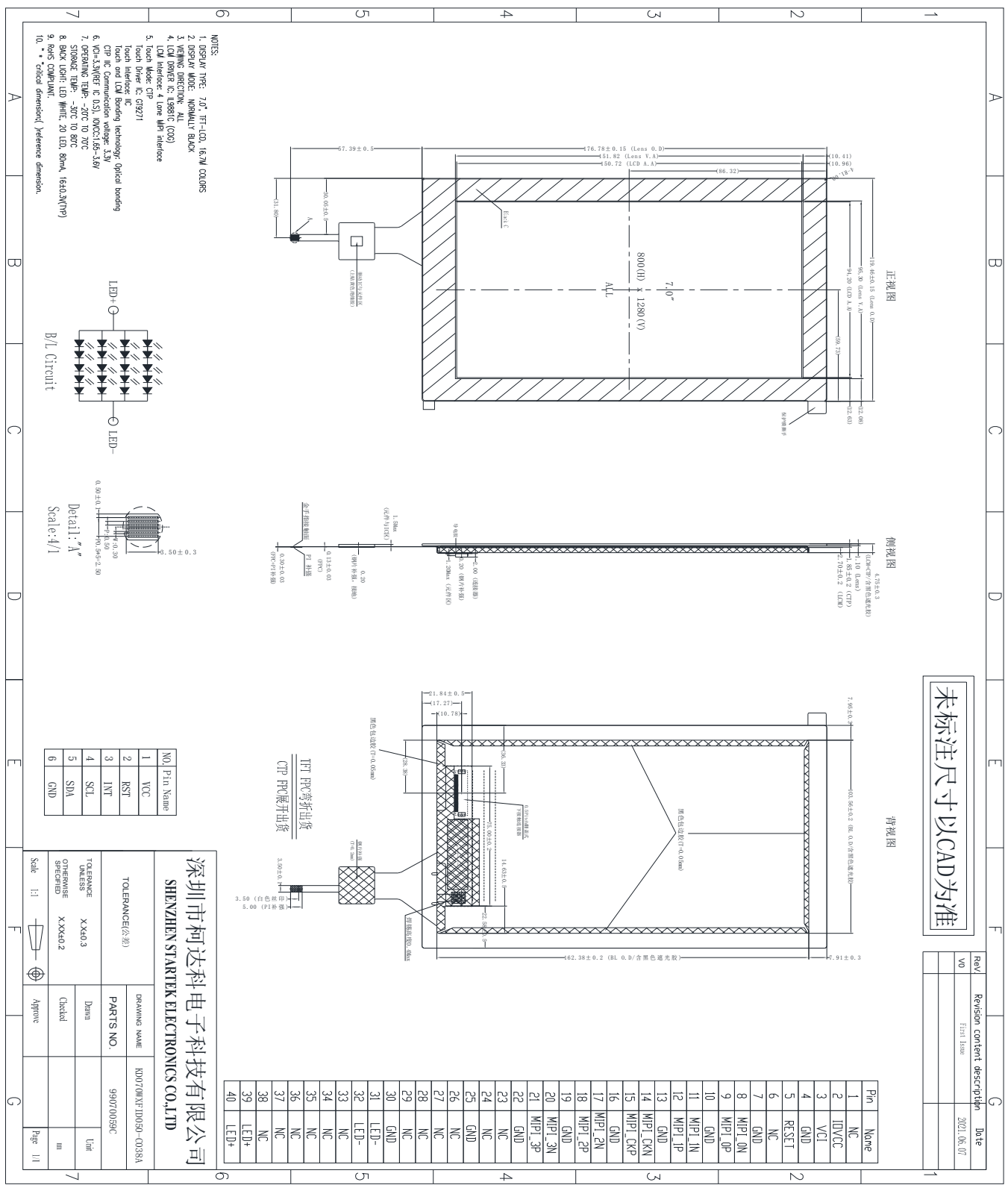
1.3 Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	119.46	-	mm	
	Vertical(V)	-	176.78	-	mm	
	Depth(D)	-	4.75	-	mm	
Weight		-	TBD	-	g	

2. Block Diagram



3. Outline dimension



4. Input terminal Pin Assignment

4.1 TFT PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	No connected	
2	IOVCC	A power supply for the I/O circuit. IOVCC=1.65 to 3.6V	P
3	VCI	A power supply for DC/DC circuit. VCI=2.5V to 4.8V	P
4	GND	Ground	P
5	RESET	Device reset signal.	I
6	NC	No connected	--
7	GND	Ground	P
8	MIPI_0N	MIPI Negative data signal (-)	I/O
9	MIPI_0P	MIPI Positive data signal (+)	I/O
10	GND	Ground	P
11	MIPI_1N	MIPI Negative data signal (-)	I/O
12	MIPI_1P	MIPI Positive data signal (+)	I/O
13	GND	Ground	P
14	MIPI_CKN	MIPI Negative clock signal (-)	I/O
15	MIPI_CKP	MIPI Positive clock signal (+)	I/O
16	GND	Ground	P
17	MIPI_2N	MIPI Negative data signal (-)	I/O
18	MIPI_2P	MIPI Positive data signal (+)	I/O
19	GND	Ground	P
20	MIPI_3N	MIPI Negative data signal (-)	I/O
21	MIPI_3P	MIPI Positive data signal (+)	I/O
22	GND	Ground	P
23	NC	No connected	
24	NC	No connected	
25	GND	Ground	P
26	NC	No connected	
27	NC	No connected	
28	NC	No connected	
29	NC	No connected	
30	GND	Ground	P

31	LED-	LED Cathode	P
32	LED-	LED Cathode	P
33	NC	No connected	
34	NC	No connected	
35	NC	No connected	
36	NC	No connected	
37	NC	No connected	
38	NC	No connected	
39	LED+	LED anode	P
40	LED+	LED anode	P

4.2 CTP PIN Define

NO.	SYMBOL	DISCRIPTION	I/O
1	VCC	Supply voltage	P
2	RST	External Reset, Low is active	I
3	INT	External interrupt to the host	I
4	SCL	I2C clock input	I/O
5	SDA	I2C data input and output	I
6	GND	Ground	P

5. LCD Optical Characteristics

5.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	700	850	--		(2)
Response time	Rising	T_{R+T_F}		--	30	40	msec	(3)
	Falling			--				
Color Gamut		S(%)		45	50	55	%	
Color Filter Chromaticity	White	W_X		0.25388	0.29388	0.33388		(4) CF glass
		W_Y		0.29506	0.33506	0.37506		
	Red	R_X		0.57322	0.59322	0.61322		
		R_Y		0.3375	0.3575	0.3775		
	Green	G_X		0.2987	0.3187	0.3387		
		G_Y		0.53652	0.55652	0.37652		
	Blue	B_X		0.1413	0.1613	0.1813		
		B_Y		0.11836	0.13836	0.15836		
Viewing angle	Hor.	Θ_L	CR>10	--	89	--		(1)
		Θ_R		--	89	--		
	Ver.	Θ_U		--	89	--		
		Θ_D		--	89	--		
Option View Direction		Free						

5.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: $25 \pm 2^\circ\text{C}$
- 15min. warm-up time.

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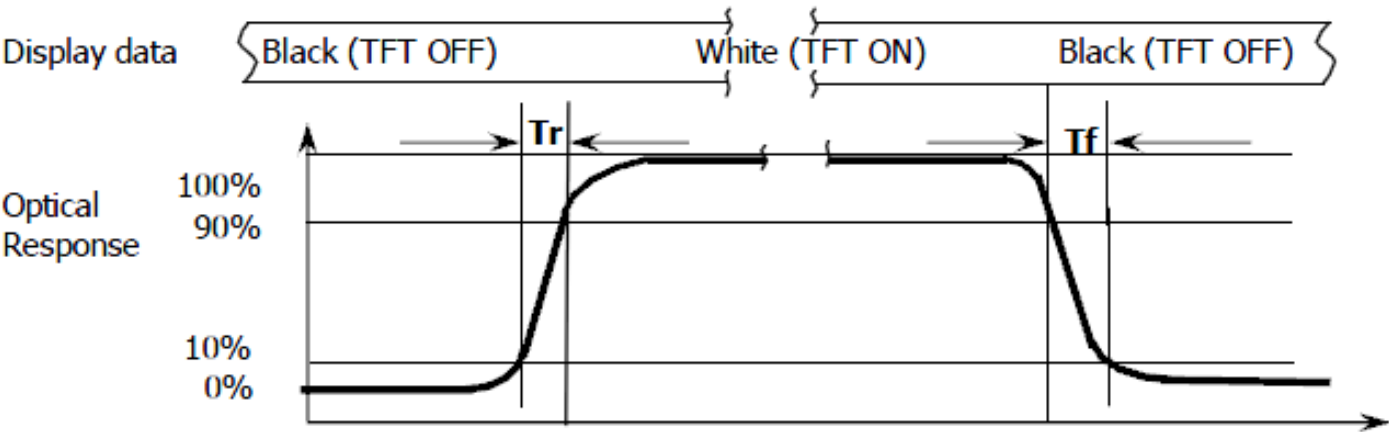
5.3 Measuring Equipment

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).
2. Contrast measurements shall be made at viewing angle of $\Theta=0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note3



Note4

The color chromaticity coordinates specified shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

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6. Electrical Characteristics

6.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	-0.3	3.6	V	Note1
Interface Supply Voltage	IOVCC	-0.3	3.6	V	
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

6.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	2.5	3.3	6.0	V	
Interface Supply Voltage	IOVCC	--	1.8	--	V	
Normal mode Current	I _{DD}	--	20	40	mA	
Level input voltage	V _{IH}	0.7V _{CI}		V _{CI}	V	
	V _{IL}	GND		0.3 V _{CI}	V	
Level output voltage	V _{OH}	V _{CI} -0.4		--	V	
	V _{OL}	GND		GND+0.4	V	

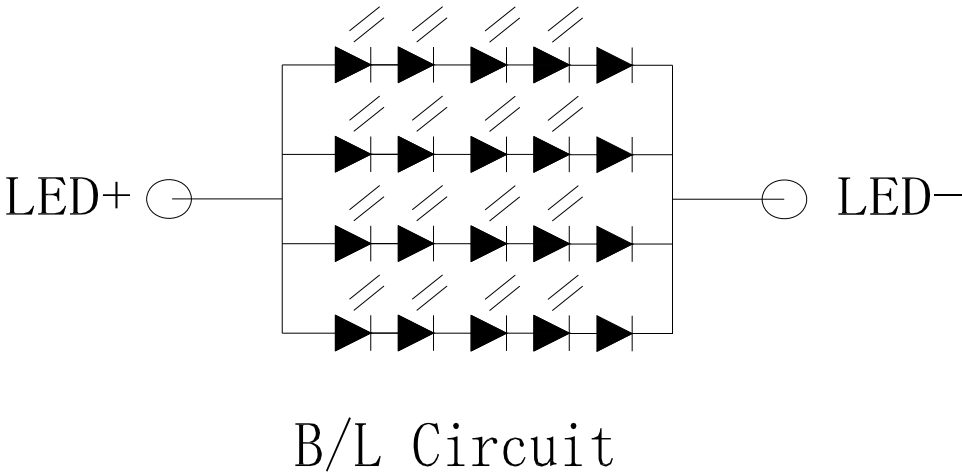
6.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 20 chips LED

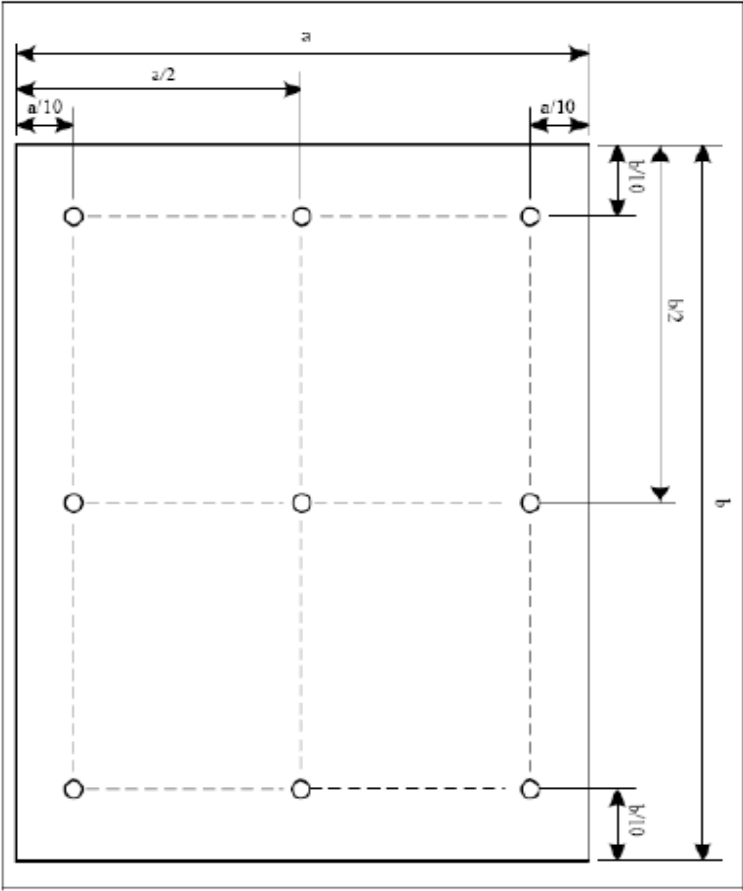
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F		80	--	mA	
Forward Voltage	V _F	--	16	--	V	
LCM Luminance	LV	360	400	--	cd/m2	Note3
LED life time	Hr	--	50000	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition:
Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at
Ta=25℃ and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The constant current driving method is suggested.



Note (3) Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

7. MIPI Interface Characteristics

7.1 High Speed Mode – Clock Channel Timing

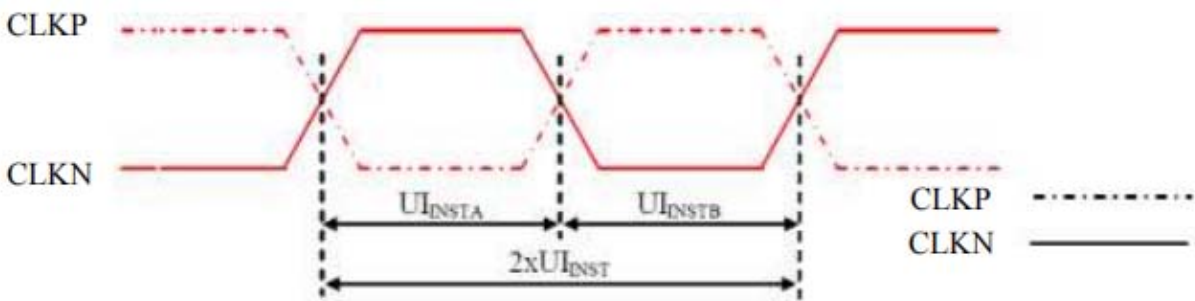


Figure 116: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	Note 2	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	Note 2	12.5	ns

Notes:

- $UI = UI_{INSTA} = UI_{INSTB}$
- Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps



7.2 High Speed Mode – Data Clock Channel Timing

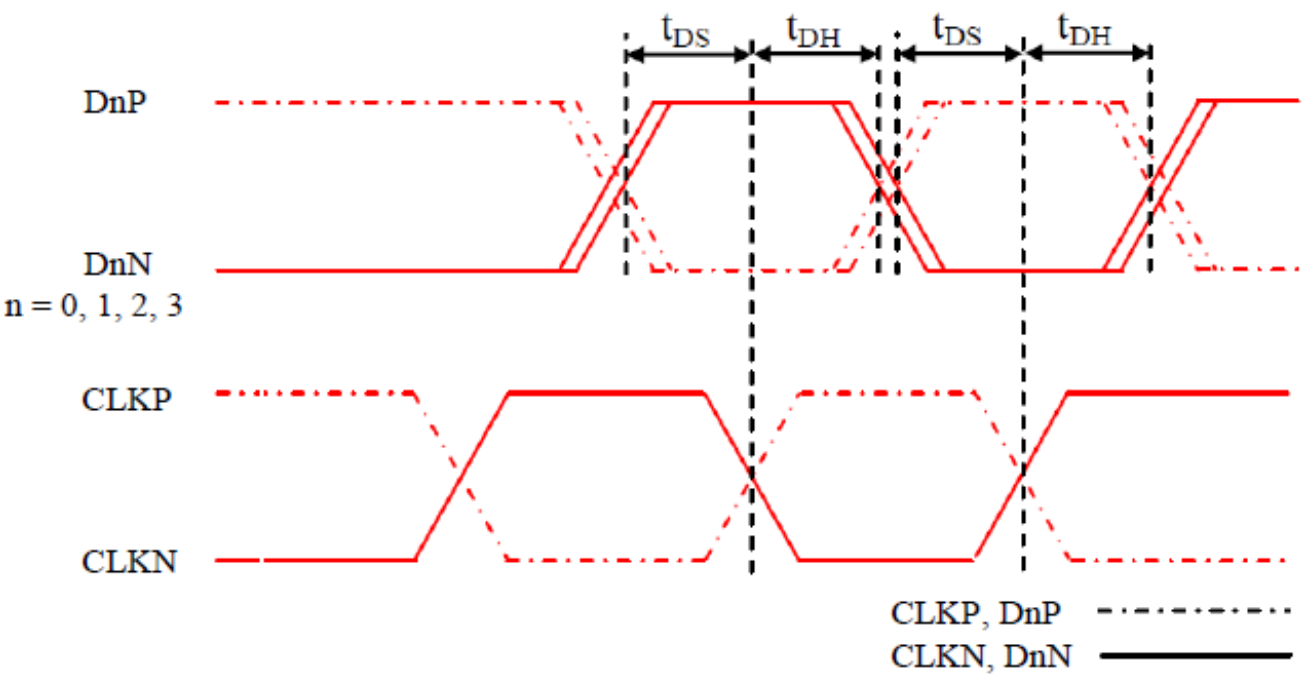


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

7.3 High Speed Mode – Rising and Fall Timings

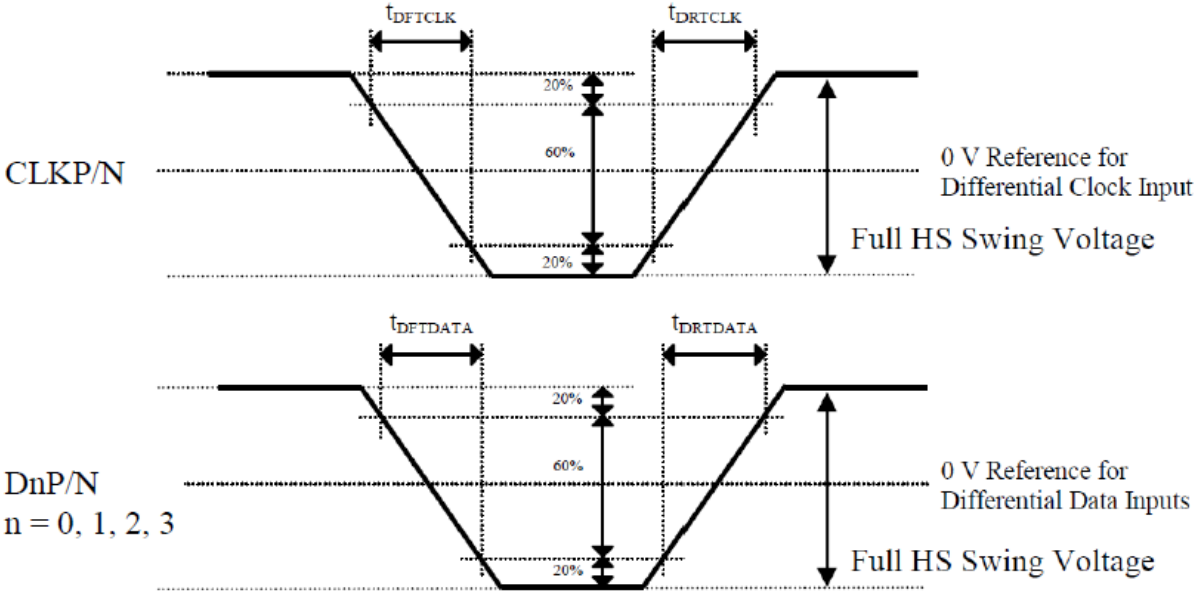


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	tDRTCLK	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	tDRTDATA	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	tDFTCLK	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	tDFTDATA	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

7.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

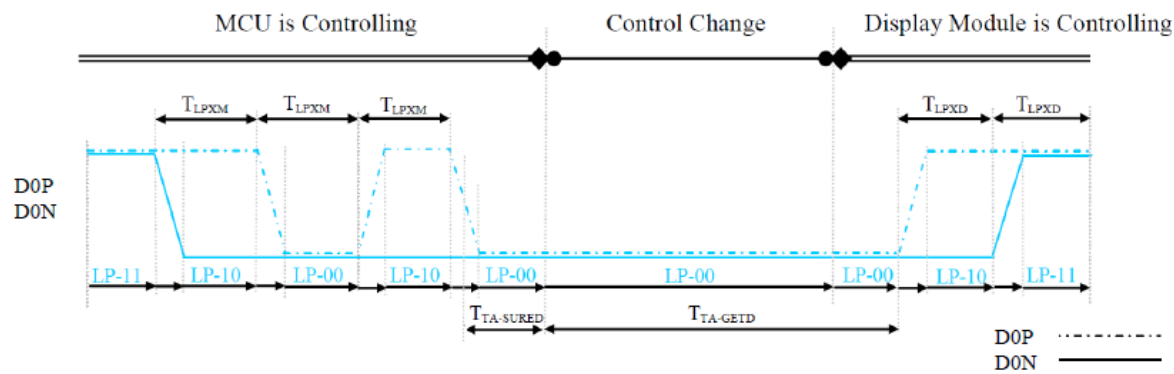


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

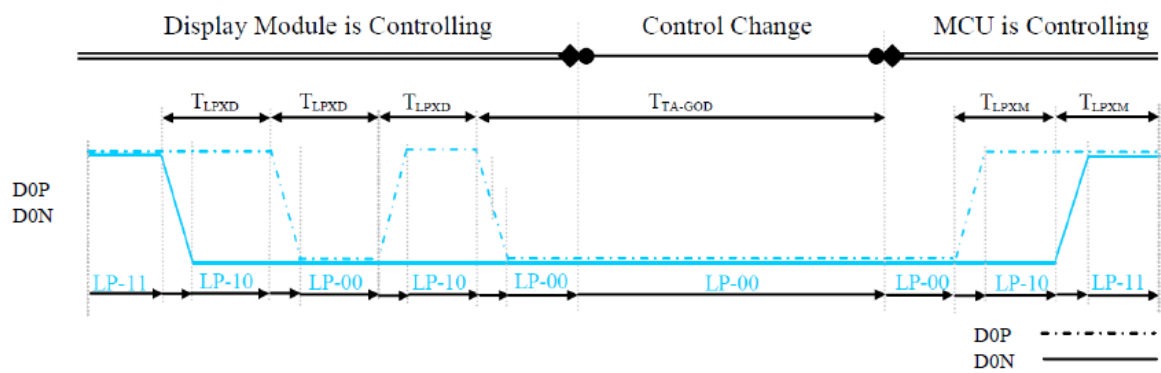


Figure 122: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5 \times T_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LPXD}$	ns

7.5 Data Lanes from Low Power Mode to High Speed Mode

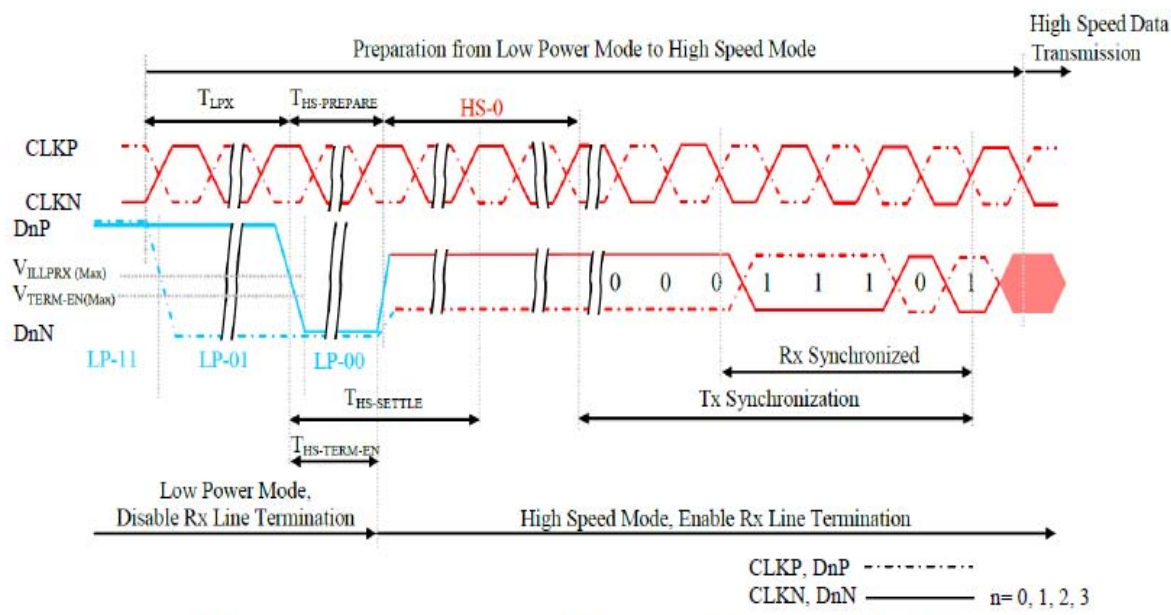


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T _{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	T _{HS-TERM-EN}	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

7.6 Data Lanes from High Power Mode to High Speed Mode

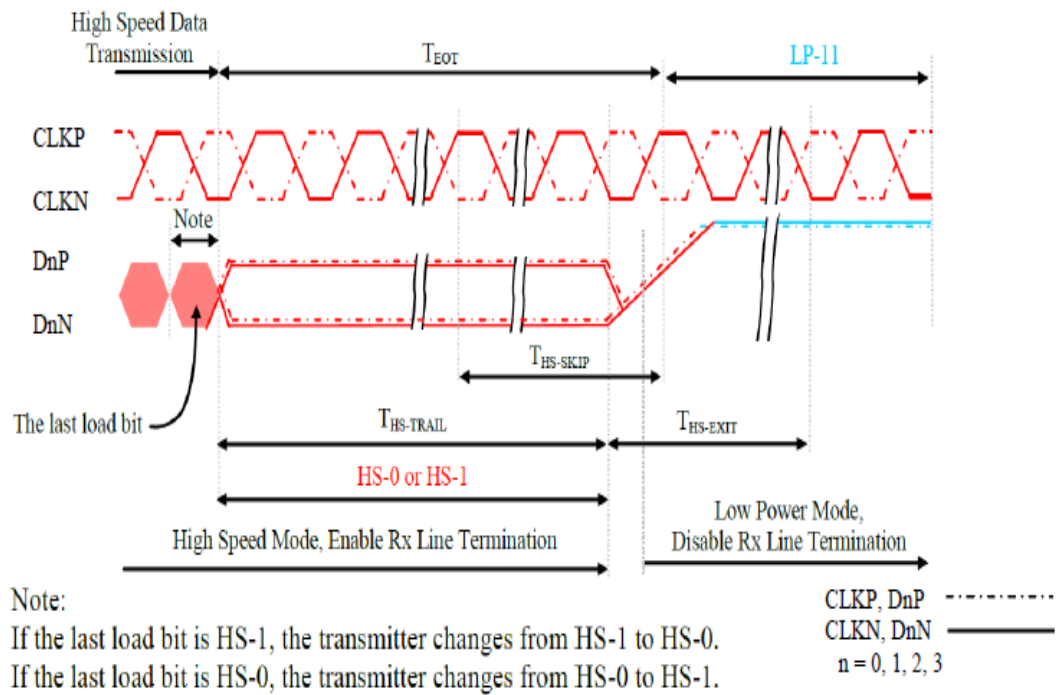


Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	$55+4 \times UI$	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

7.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

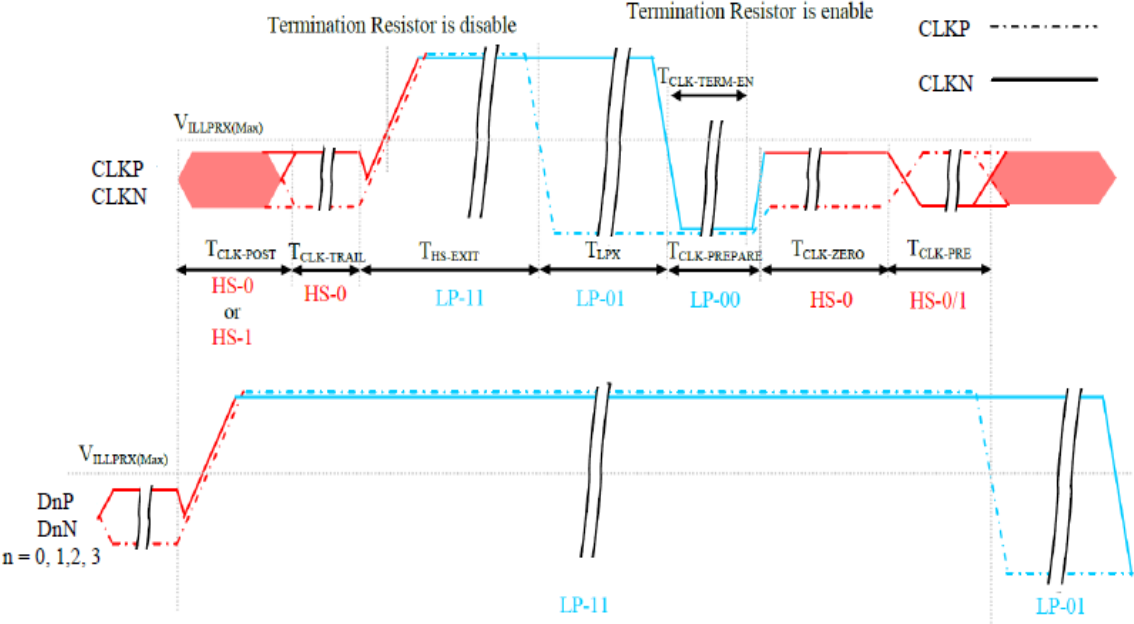


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	T _{CLK-POST}	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	T _{CLK-TRAIL}	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	T _{CLK-PREPARE}	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	T _{CLK-TERM-EN}	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	T _{CLK-PREPARE} + T _{CLK-ZERO}	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	T _{CLK-PRE}	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns



7.8 Timing for DSI video mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	(67)	--	MHz
Horizontal display area	HDISP	--	800	--	Clock
Horizontal Sync. Width	hpw	1	4	--	Clock
Horizontal Sync. Back Porch	hbp	1	38	-	Clock
Horizontal Sync. Front Porch	hfp	1	16	--	Clock
Vertical display area	VDISP	--	1280	--	Line
Vertical Sync. Width	vs	1	4	--	Line
Vertical Sync. Back Porch	vbp	1	10	--	Line
Vertical Sync. Front Porch	vfp	1	8	--	Line
Frame-Rate		--	60	--	Hz

Note:
The best frame rate setting : 2 data lanes : 50~60 Hz / 3 data lanes : 50~70 Hz / 4 data lanes : 50~70 Hz.

8. CTP Specification

8.1 Electrical Characteristics

8.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VCC	2.66	3.47	V	
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

8.1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient temperature:25°C, VCC=2.8V, VDDIO=1.8V or VDDIO=VCC)

Item	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage/VCC	2.66	3.3	3.47	V	
Normal mode operating current	--	13	--	mA	
Green mode operating current	--	4.5	--	mA	
Sleep mode operating current	70	--	120	uA	
Digital Input low voltage/VIL	-0.3	--	0.25*VCC	V	
Digital Input high voltage/VIH	0.75*VCC	--	VCC+0.3	V	
Digital Output low voltage/VOL	--	--	0.15*VCC	V	
Digital Output high voltage/VOH	0.85*VCC	--	--	V	

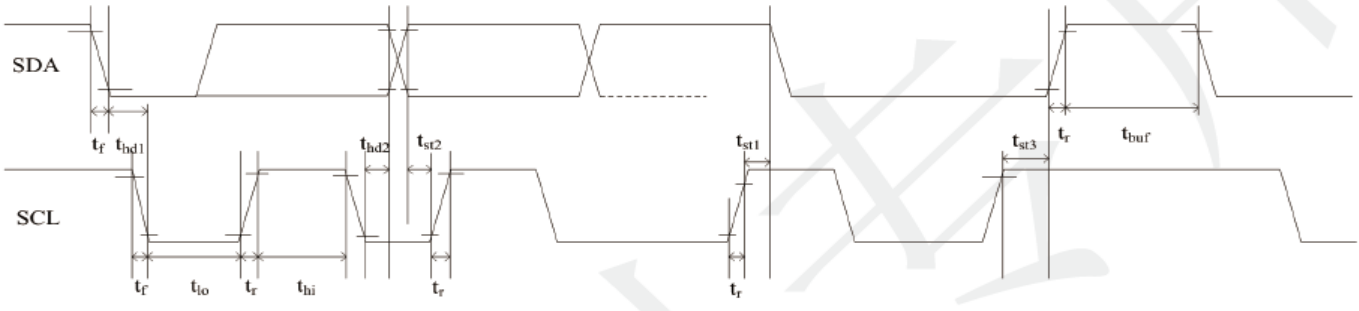
8.1.3 AC Characteristics

(Ambient temperature:25℃, VCC=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit	Note
OSC oscillation frequency	59	60	61	MHZ	
I/O output rise time,low to high	-	14	-	ns	
I/O output rfall time,high to low	-	14	-	ns	

8.2 I2C Timing

GT9271 provides a standard I2C interface for SCL and SDA to communicate with the host. GT9271 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

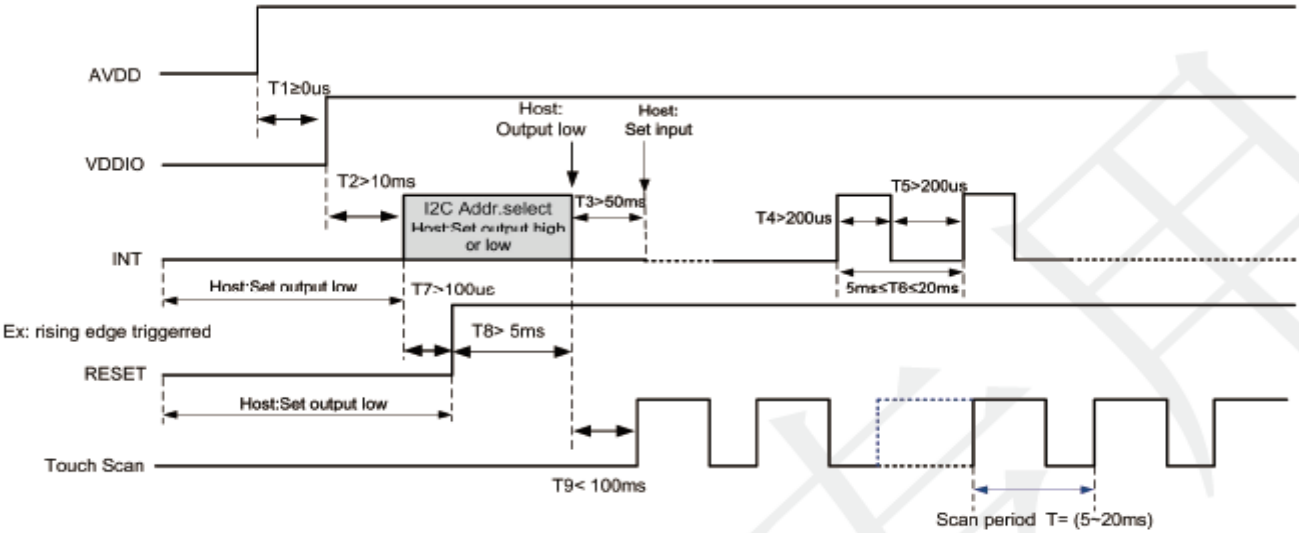
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t _{lo}	1.3	-	us
SCL high period	t _{hi}	0.6	-	us
SCL setup time for Start condition	t _{st1}	0.6	-	us
SCL setup time for Stop condition	t _{st3}	0.6	-	us
SCL hold time for Start condition	t _{hd1}	0.6	-	us
SDA setup time	t _{st2}	0.1	-	us
SDA hold time	t _{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t _{lo}	1.3	-	us
SCL high period	t _{hi}	0.6	-	us
SCL setup time for Start condition	t _{st1}	0.6	-	us
SCL setup time for Stop condition	t _{st3}	0.6	-	us
SCL hold time for Start condition	t _{hd1}	0.6	-	us
SDA setup time	t _{st2}	0.1	-	us
SDA hold time	t _{hd2}	0	-	us

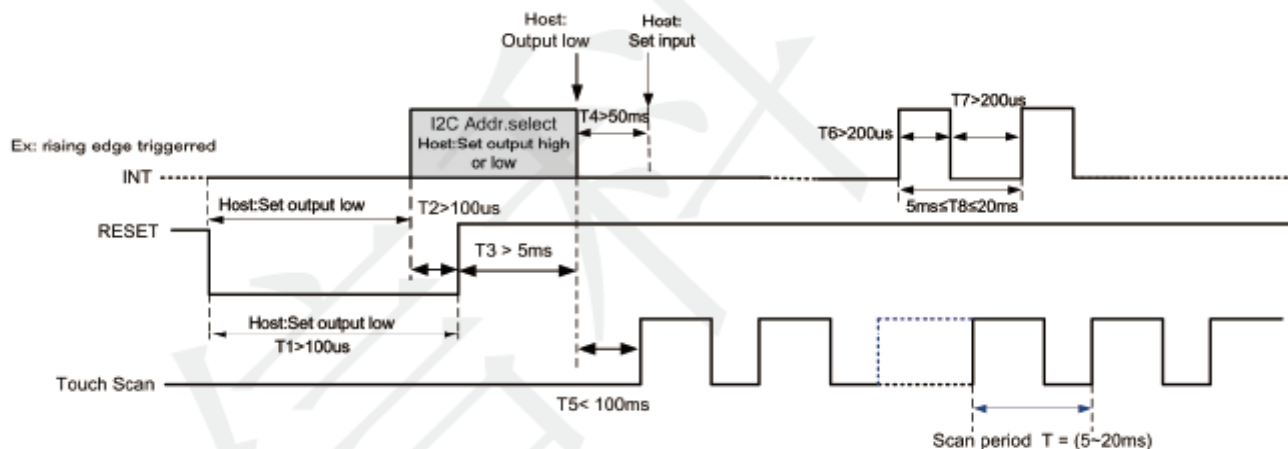
GT9271 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

Power-on Timing:

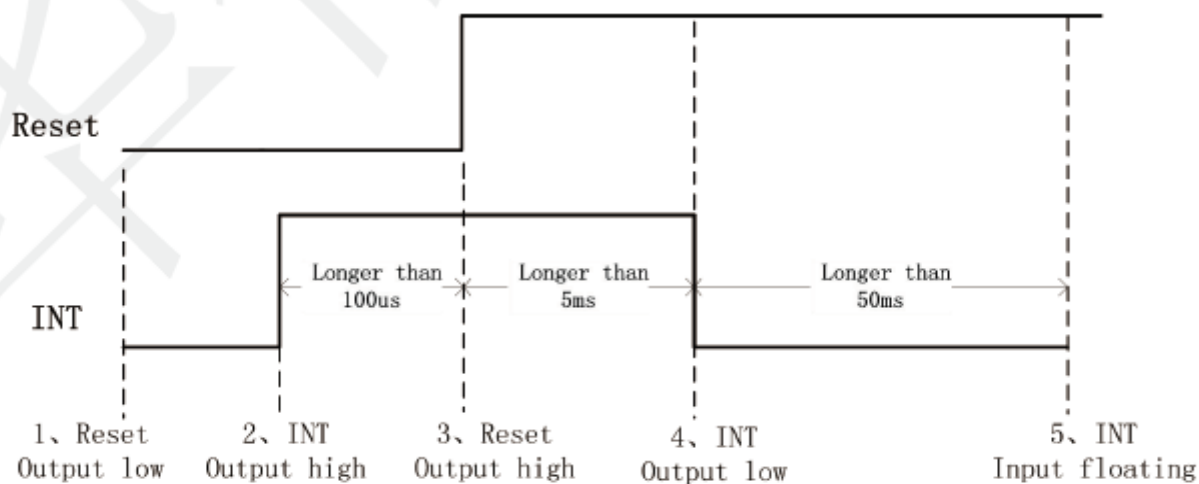




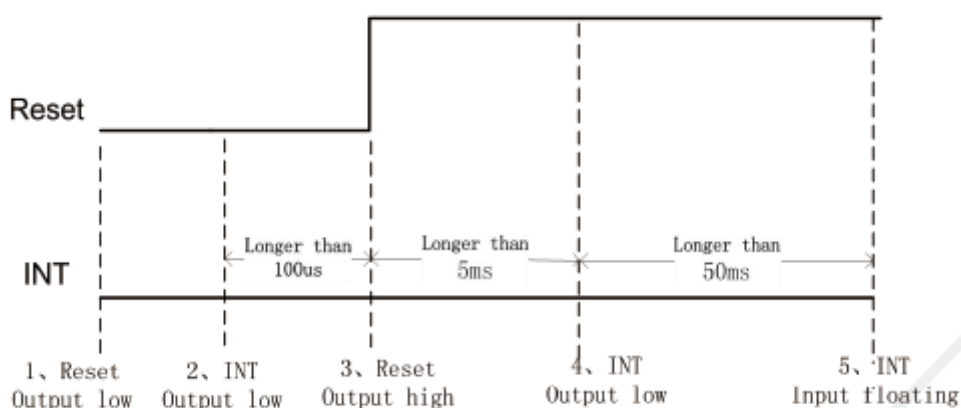
Timing for host resetting GT9271:



Timing for setting slave address to 0x28/0x29:



Timing for setting slave address to 0xBA/0xBB:



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a) Data Transmission

(For example: slave address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from high to low when SCL line is high. Data flow or address is transmitted after the Start condition.

All slave devices connected to I²C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT9271 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0xBA or 0xBB, GT9271 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is high.

When communication is completed, the host will issue the Stop condition which implies the transition of SDA line from low to high when SCL line is high.

b) Writing Data to GT9271

(For example: slave address is 0xBA/0xBB)



Timing for Write Operation

The diagram above displays the timing sequence of the host writing data onto GT9271. First, the host issues a Start condition. Then, the host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

c) Reading Data from GT9271

(For example: slave address is 0xBA/0xBB)



Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT9271. First, the host issues a Start condition and sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0xBB (Read Operation). After receiving ACK, the host starts to read data.

GT9271 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

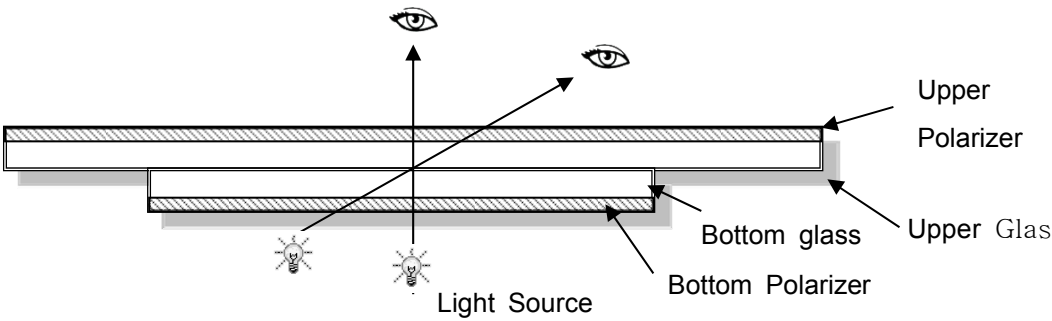
9. LCD Module Out-Going Quality Level

9.1 VISUAL & FUNCTION INSPECTION STANDARD

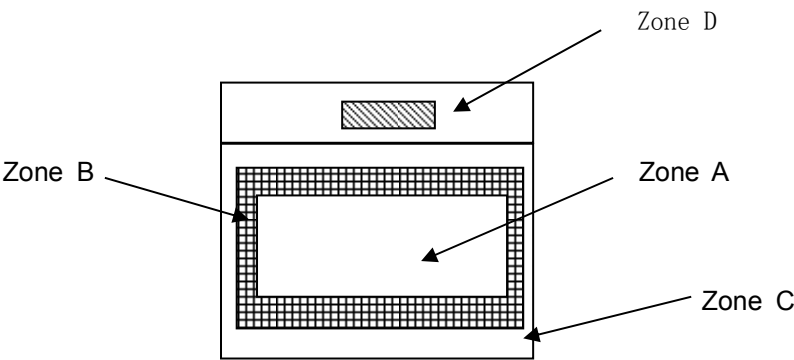
9.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : 25±5℃
- Humidity : 65%±10%RH
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance:30-50cm



9.1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
 - Zone B : Viewing Area except Zone A
 - Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)
 - Zone D : IC Bonding Area
- Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

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9.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module, CTP: Capacitive Touch Panel

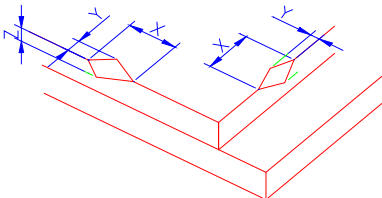
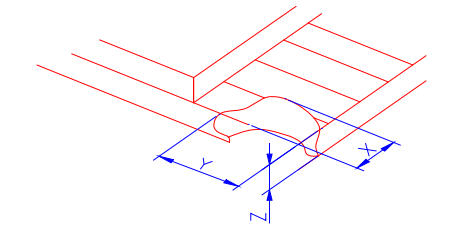
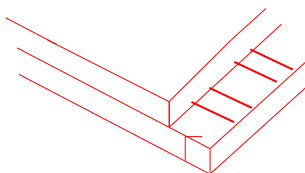
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc	Major
2	Missing	Missing components and etc	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc	
7	LCD/Polarizer/CTP	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

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9.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of IT O, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							

Spot defect

2.0

Y

X

Φ=(X+Y)/2

① light dot (black/white spot , pinhole, stain, etc.)

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance ≥ 10mm)		
0.25<Φ≤0.4	2(distance ≥ 10mm)		
Φ>0.4	0		

② Dim spot (light leakage、dent、dark spot, etc)

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.15	Ignore	Ignore	
0.15<Φ≤0.25	3(distance ≥ 10mm)		
0.25<Φ≤0.4	2(distance ≥ 10mm)		
Φ>0.4	0		

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.5	2(distance ≥ 10mm)		
Φ>0.5	0		

④Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.2<Φ≤0.4	2(distance ≥ 10mm)		
Φ>0.4	0		



Note:

A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

C) 2 dot adjacent = 1 pair = 2 dots

Picture:



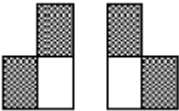
2 dot adjacent



2 dot adjacent (vertical)



2 dot adjacent

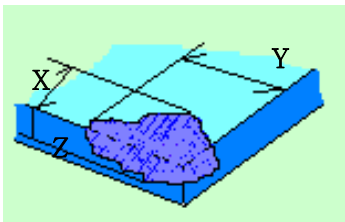


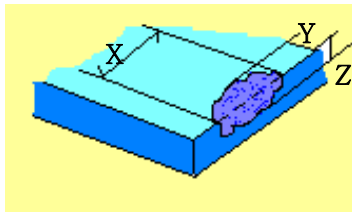
2 dot adjacent (slant)

常 备 库 存	长 期 供 货	支持小量	品 种 齐 全
Stock For Sale	Long Time supply	NO MOQ	In Full Range

4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)																										
																											
	W: width, L : length																										
	N : Count																										
	<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(m m)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.05$</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>$0.05 < W \leq 0.06$</td><td>$L \leq 5.0$</td><td colspan="2">$N \leq 3$</td></tr><tr><td>$0.06 < W \leq 0.08$</td><td>$L \leq 4.0$</td><td colspan="2">$N \leq 2$</td></tr><tr><td>$W > 0.08$</td><td colspan="4">Define as spot defect</td></tr></table>	Width(mm)	Length(m m)	Acceptable Qty			A	B	C	$\Phi \leq 0.05$	Ignore	Ignore		Ignore	$0.05 < W \leq 0.06$	$L \leq 5.0$	$N \leq 3$		$0.06 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$		$W > 0.08$	Define as spot defect			
Width(mm)	Length(m m)			Acceptable Qty																							
		A	B	C																							
$\Phi \leq 0.05$	Ignore	Ignore		Ignore																							
$0.05 < W \leq 0.06$	$L \leq 5.0$	$N \leq 3$																									
$0.06 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$																									
$W > 0.08$	Define as spot defect																										
5.0	Electronic Components SMT.	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite																									
6.0	Display color& Brightness.	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.																									
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.																									

8.0	CTP Related	CTP Cover sensor acc identified black/white spot				
			Size Φ (mm)	Acceptable Qty		
				A	B	C
			$\Phi \leq 0.15$	Ignore		Ignore
			$0.15 < \Phi \leq 0.25$	4 (distance $\geq 10\text{mm}$)		
			$0.25 < \Phi \leq 0.35$	3 (distance $\geq 10\text{mm}$)		
			$\Phi > 0.35$	0		

		CTP Cover scratch <table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Ignore (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.05$</td><td>Ignore</td><td colspan="3">Ignore</td></tr><tr><td>$0.05 < W \leq 0.06$</td><td>$L \leq 4.0$</td><td colspan="3">$N \leq 3$</td></tr><tr><td>$0.06 < W \leq 0.08$</td><td>$L \leq 3.0$</td><td colspan="3">$N \leq 2$</td></tr><tr><td>$0.08 < W$</td><td colspan="4">Define as spot defect</td></tr></table>	Width(mm)	Ignore (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.05$	Ignore	Ignore			$0.05 < W \leq 0.06$	$L \leq 4.0$	$N \leq 3$			$0.06 < W \leq 0.08$	$L \leq 3.0$	$N \leq 2$			$0.08 < W$	Define as spot defect			
Width(mm)	Ignore (mm)	Acceptable Qty																												
		A	B	C																										
$\Phi \leq 0.05$	Ignore	Ignore																												
$0.05 < W \leq 0.06$	$L \leq 4.0$	$N \leq 3$																												
$0.06 < W \leq 0.08$	$L \leq 3.0$	$N \leq 2$																												
$0.08 < W$	Define as spot defect																													
	CTP Cover Pinhole/ Lack of ink <table><tr><th rowspan="2">Zone Size (mm)</th><th>Acceptable Qty</th></tr><tr><th>C</th></tr><tr><td>$\Phi \leq 0.2$</td><td>Ignore</td></tr><tr><td>$0.2 < \Phi \leq 0.3$</td><td>4(distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.3 < \Phi \leq 0.4$</td><td>2(distance $\geq 10\text{mm}$)</td></tr><tr><td>$\Phi > 0.4$</td><td>0</td></tr></table>	Zone Size (mm)	Acceptable Qty	C	$\Phi \leq 0.2$	Ignore	$0.2 < \Phi \leq 0.3$	4(distance $\geq 10\text{mm}$)	$0.3 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)	$\Phi > 0.4$	0																		
Zone Size (mm)	Acceptable Qty																													
	C																													
$\Phi \leq 0.2$	Ignore																													
$0.2 < \Phi \leq 0.3$	4(distance $\geq 10\text{mm}$)																													
$0.3 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)																													
$\Phi > 0.4$	0																													
	CTP Bondi ng bubble/ accident spot <table><tr><th rowspan="2">Size $\Phi(\text{mm})$</th><th colspan="2">Acceptable Qty</th></tr><tr><th>A</th><th>B</th></tr><tr><td>$\Phi \leq 0.1$</td><td colspan="2">Ignore</td></tr><tr><td>$0.1 < \Phi \leq 0.2$</td><td colspan="2">3(distance $\geq 10\text{mm}$)</td></tr><tr><td>$0.2 < \Phi \leq 0.3$</td><td colspan="2">2(distance $\geq 10\text{mm}$)</td></tr><tr><td>$\Phi > 0.3$</td><td colspan="2">0</td></tr></table>	Size $\Phi(\text{mm})$	Acceptable Qty		A	B	$\Phi \leq 0.1$	Ignore		$0.1 < \Phi \leq 0.2$	3(distance $\geq 10\text{mm}$)		$0.2 < \Phi \leq 0.3$	2(distance $\geq 10\text{mm}$)		$\Phi > 0.3$	0													
Size $\Phi(\text{mm})$	Acceptable Qty																													
	A	B																												
$\Phi \leq 0.1$	Ignore																													
$0.1 < \Phi \leq 0.2$	3(distance $\geq 10\text{mm}$)																													
$0.2 < \Phi \leq 0.3$	2(distance $\geq 10\text{mm}$)																													
$\Phi > 0.3$	0																													
	Assembly deflection beyond the edge of backlight $\leq 0.2\text{mm}$																													
CTP cover broken X : length Y : width Z : height	<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$X \leq 0.5\text{mm}$</td><td>$Y \leq 0.5\text{mm}$</td><td>$Z < \text{cover thickness}$</td></tr></table> Circuitry broken is not allowed.	X	Y	Z	$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$																							
X	Y	Z																												
$X \leq 0.5\text{mm}$	$Y \leq 0.5\text{mm}$	$Z < \text{cover thickness}$																												

		CTP cover broken X : length Y : width Z : height	X	Y	Z	
			$X \leq 0.3\text{mm}$	$Y \leq 0.3\text{mm}$	$Z < \text{cover thickness}$	
* Circuitry broken is not allowed.						

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	CTP no function	Not allowed

10. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70°C,96HR	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96HR	
High Temperature Storage	80°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High Humidity Operating	+60°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10°C,30 min ↔ 60°C,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panelS Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

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11. Cautions and Handling Precautions

11.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

11.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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12. Packing

----TBD-----

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