IS2066B

Bluetooth® Wireless Stereo Technology ROM SoC Data Sheet

Introduction

The IS2066B is a low-power Bluetooth Audio System-on-Chip (SoC) with Microchip's Wireless Stereo Technology (WST) for Bluetooth Audio applications targeting wireless earbuds. Offered in a BGA package, the IS2066B product is part of the Bluetooth Dual Mode family of stereo audio devices. It allows audio playback on two wireless devices and a customizable internal EEPROM.

Features

- Qualified for Bluetooth v5.0 Specification
- Bluetooth 5.0 Core System Component (QDID 110017)
- Bluetooth Audio Profiles:
  - A2DP 1.3
  - AVRCP 1.6
  - HFP 1.6
  - HSP 1.2
- Bluetooth Low Energy (BLE):
  - Generic access service
  - Device information service
  - Proprietary services for data communication
- Supports 16 kHz Wideband Speech
- Audio Interfaces:
  - Analog output
  - Microphone input
- Integrated Battery Charger (up to 350 mA)

Audio Codec

- Sub-Band Coding (SBC) Decoding and Advanced Audio Coding (AAC) Decoding
- 20-bit Digital-to-Analog Converter (DAC) with 98 dB SNR

RF Features

- Transmit Output Power: +2 dBm (Typical) (maximum 4 dBm)
- Support BDR/EDR/1M-LE Data Rate
- Receive Sensitivity: -90 dBm (Typical) (2 Mbps Enhanced Data Rate (EDR))
- Combined Tx/Rx RF Terminal Simplifies External Matching and Reduces External Antenna Switches
- Tx/Rx RF Switch for Class 2 or Class 3 Applications
- Integrated Synthesizer Requires No External Voltage-Controlled Oscillator (VCO), Varactor Diode, and Resonator or Loop Filter
- Crystal Oscillator with Built-In Digital Trimming Compensates for Temperature or Process Variations

DSP Audio Processing

- Includes a 32-bit DSP Core
- Synchronous Connection-Oriented (SCO) Channel Operation
- 8/16 kHz Noise Suppression
- 8/16 kHz Acoustic Echo Cancellation
- Modified Sub-Band Coding (MSBC) Decoder for Wide Band Speech
- Packet Loss Concealment (PLC)
- Built-In Audio Effect Algorithms to Enhance Audio Streaming

Package Details

Table 1. Package Details

Parameter	IS2066B
Package type	BGA
Ball count	50
Contact/Lead pitch	0.5 mm
Package size	5 mm x 3.5 mm x 0.9 mm

Peripherals

- UART Interface for Host MCU Communication
- Built-In Lithium-Ion (Li-Ion) and Lithium-Polymer (Li-Po) Battery Charger (up to 350 mA)
- Integrated 1.5V, 1.8V, and 3V Configurable Switching Regulator and Low-Dropout (LDO) Regulator
- Dual Buck Configuration for Power Saving
- Successive Approximation Register Analog-to-Digital Converter (SAR ADC) with Dedicated Channels:
  – Battery voltage detection and adapter voltage detection
  – Ambient temperature detection
- Built-In Undervoltage Protection (UVP) and Overvoltage Protection (OVP)
- Two LED Drivers

Operating Conditions

- Operating Voltage: 3.2V to 4.2V
- Operating Temperature: -20℃ to +70℃

Applications

- WST (Wireless Stereo Technology) Earbuds and Headsets

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1. Device Overview

The IS2066B SoC integrates:

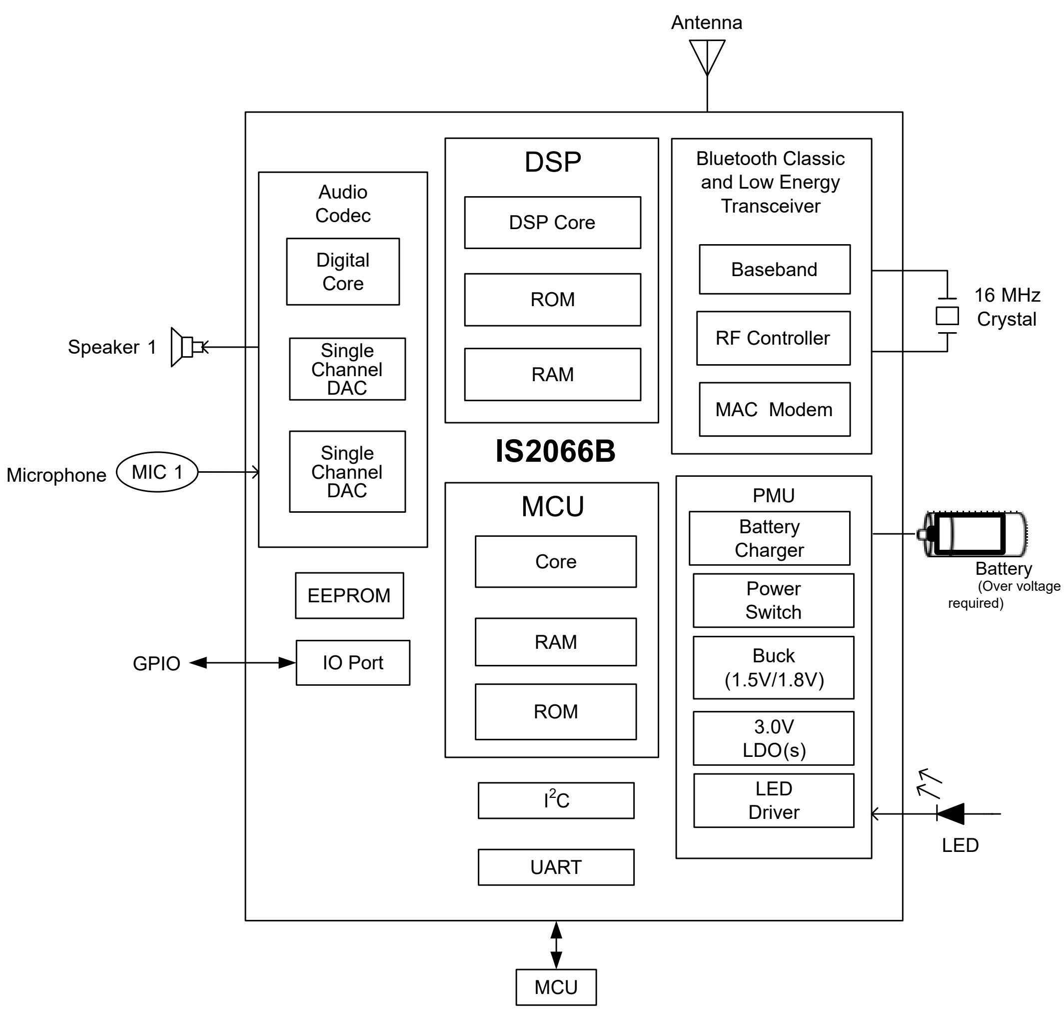
- Bluetooth 5.0 Dual-mode Radio Transceiver
- Power Management Unit (PMU)
- Microcontroller (MCU)
- Audio Codec
- Crystal Oscillator
- 32-bit DSP
- EEPROM

The IS2066B SoC is configured using a UI and DSP tool.

Note: The UI tool and DSP tool are Windows®-based configuration utility tools, which are available for download from the Microchip website: http://www.microchip.com/wwwproducts/en/IS2066.

The following figure illustrates the block diagram of the IS2066B SoC.

Figure 1-1. Block Diagram of IS2066B SoC



1.1 Key Features

The following table provides the key features of the IS2066B.

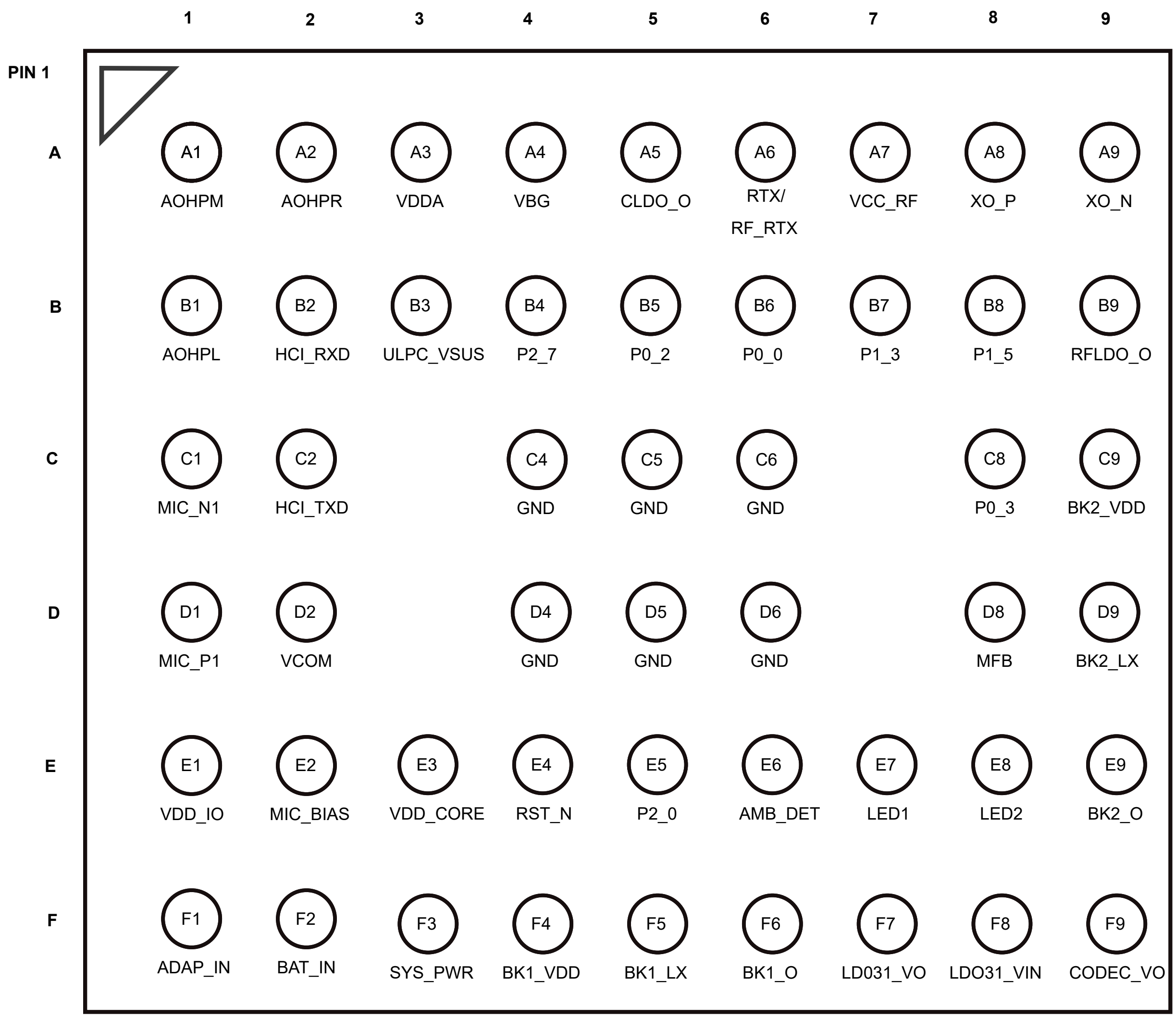
Table 1-1. Key Features

Feature	IS2066B
Application	Wireless Stereo Technology earbuds
Flash/ROM	ROM
Stereo mode	Yes
Package	BGA
Pin/Ball count	50
Dimensions (mm)	5x3.5
Audio DAC output	1-channel
DAC (BTL) SNR at 2.8V (dB)	-98
DAC (BTL) SNR at 1.8V (dB)	-95
Analog output	Yes
Mono microphone	1
UART	Yes
LED driver	2
Integrated DC-DC step-down regulator	2
Integrated LDO regulator	2
DC 5V adapter input	Yes
Battery charger (350 mA maximum)	Yes
ADC for charger thermal protection	Yes
Under Voltage Protection (UVP)	Yes
GPIO	6
EEPROM	128K
Multitone	Yes
DSP functions (audio playback and voice call)	Yes
Bluetooth Low Energy	Yes
A2DP	1.3
AVRCP	1.6
HFP	1.6
HSP	1.2

1.2 Pin Details

The following figure illustrates the pin diagram of the IS2066B.

Figure 1-2. IS2066B Pin Diagram



The following table provides the pin description of the IS2066B.

Note: The conventions used in the below table are indicated as follows:

- I = Input pin
- O = Output pin
- I/O = Input/Output pin
- P = Power pin

Table 1-2. Pin Description

Ball No	Pin Type	Pin Name	Description
A1	O	AOHPM	Headphone common mode output/sense input. For WST earbud application, do not connect.
A2	O	AOHPR	Right-channel, analog headphone output

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Ball No	Pin Type	Pin Name	Description
A3	P	VDDA	Analog reference voltage. Do not connect; for internal use only
A4	P	VBG	Bandgap output reference for decoupling interference, connect to GND through a 1 μF capacitor
A5	P	CLDO_O	1.2V core LDO output for internal use only. Connect to GND through a 1 μF capacitor
A6	I/O	RTX/ RF_RTX	RF path (transmit/receive)
A7	P	VCC_RF	RF power input (1.28V) for both synthesizer and Tx/Rx block, connect to RFLDO_O
A8	I	XO_P	16 MHz crystal input positive
A9	I	XO_N	16 MHz crystal input negative
B1	O	AOHPL	Left channel, analog headphone output
B2	O	HCI_RXD	HCI UART data input
B3	P	ULPC_VSUS	ULPC 1.2V output power, maximum loading 1 mA, connect to GND through a 1 μF capacitor
B4	I/O	P2_7	Configurable control or indication pin (internally pulled-up, if configured as an input) • Volume up key (default), active-low
B5	I/O	P0_2	Configurable control or indication pin (internally pulled-up, if configured as an input) • Play/Pause key (default)
B6	I/O	P0_0	Configurable control or indication pin (internally pulled-up, if configured as an input) • Optional in-out box detection pin (input)
B7	I/O	P1_3	I^2C SDA (Internal EEPROM data) requires external 4.7 kΩ pull-up resistor
B8	I	P1_5	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Out_Ind_1 (UART_TX_IND)
B9	P	RFLDO_O	1.28V RF LDO output for internal use only. Connect to GND through a 1 μF capacitor
C1	I	MIC_N1	MIC1 mono differential analog negative input
C2	I	HCI_TXD	HCI UART data output
C4, C5, C6, D4, D5, D6	P	GND	Ground reference
C8	I/O	P0_3	Configurable control or indication pin (Internally pulled-up, if configured as an input) • Optional event indication output for external MCU to indicate IS2066B keep-alive of power-off
C9	I	BK2_VDD	1.8V buck VDD power input; connect to SYS_PWR pin
D1	I	MIC_P1	MIC1 mono differential analog positive input

...........continued

Ball No	Pin Type	Pin Name	Description
D2	P	VCOM	Internal biasing voltage for codec, connect a 4.7 µF capacitor to ground
D8	P	MFB	• Multi-Function Button and power-on key • UART RX_IND, active-high (used by host MCU to wake up the Bluetooth system)
D9	I	BK2_LX	1.8V buck regulator feedback path
E1	P	VDD_IO	I/O power supply input (3V to 3.6V); connect to LDO31_VO pin, connect to GND through a 1 µF (X5R/X7R) capacitor
E2	P	MIC_BIAS	Electric microphone biasing voltage
E3	P	VDD_CORE	Core 1.2V power input; connect to CLDO_O pin; connect to GND through a 1 µF (X5R/X7R) capacitor
E4	I	RST_N	System Reset (active-low)
E5	I/O	P2_0	System configuration pin used to set IS2066B into different operation mode • High – Application mode (for normal operation) • Low – Test mode (to change EEPROM value)
E6	P	AMB_DET	Analog input for ambient temperature detection
E7	P	LED1	LED driver 1
E8	P	LED2	LED driver 2
E9	I	BK2_O	1.8V buck regulator output. Do not connect to other devices. For internal use only
F1	P	ADAP_IN	5V power adapter input, used to charge the battery in case of Li-Ion battery power applications
F2	P	BAT_IN	Power Supply input. Voltage range: 3.2V to 4.2V. Source can either be a Li-Ion battery or any other power rail on the host board
F3	P	SYS_PWR	System power output derived from the ADAP_IN or BAT_IN. Do not connect, for internal use only
F4	I	BK1_VDD	1.5V buck VDD power input; connect to SYS_PWR pin
F5	I	BK1_LX	1.5V buck regulator feedback path
F6	I	BK1_O	1.5V buck regulator output. Do not connect to other devices. For internal use only
F7	I	LDO31_VO	3V LDO output for VDD_IO power, do not calibrate
F8	P	LDO31_VIN	LDO input, connect to SYS_PWR
F9	P	CODEC_VO	LDO output for codec power

2. Audio

The input and output audio signals have different stages and each stage is programmed to vary the gain response characteristics. For microphones, both single-ended inputs and differential inputs are supported. To maintain a high-quality signal, a stable bias voltage source to the condenser microphone's FET is provided. The DC blocking capacitors are used at both positive and negative sides of the input. Internally, this analog signal is converted to 16-bit, 8/16 kHz linear PCM data.

2.1 Digital Signal Processor

A Digital Signal Processor (DSP) is used to perform speech and audio processing. The advanced speech features, such as acoustic echo cancellation and noise reduction, are built-in. To reduce nonlinear distortion and to help echo cancellation, an outgoing signal level to the speaker is monitored and adjusted to avoid saturation of speaker output or microphone input. Adaptive filtering is also applied to track the echo path impulse in response, to provide an echo free and full-duplex user experience.

The embedded noise reduction algorithm helps to extract clean speech signals from the noisy inputs captured by microphones and improves mutual understanding in communication. The advanced audio features, such as multi-band dynamic range control, parametric multi-band equalizer, audio widening and virtual bass are built-in. The audio effect algorithms improve the user's audio listening experience in terms of better-quality audio after audio signal processing.

The following figures illustrate the processing flow of speaker phone applications for speech and audio signal processing.

Figure 2-1. Speech Processing

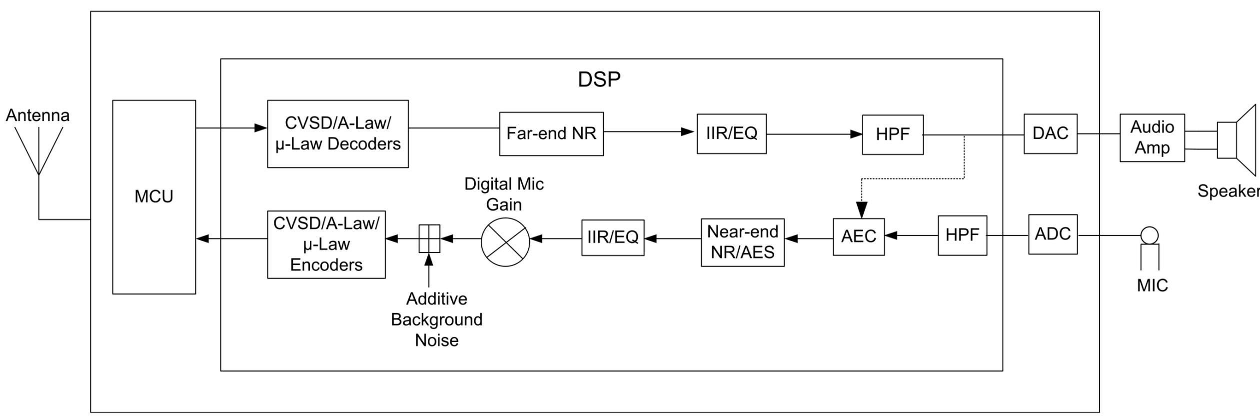
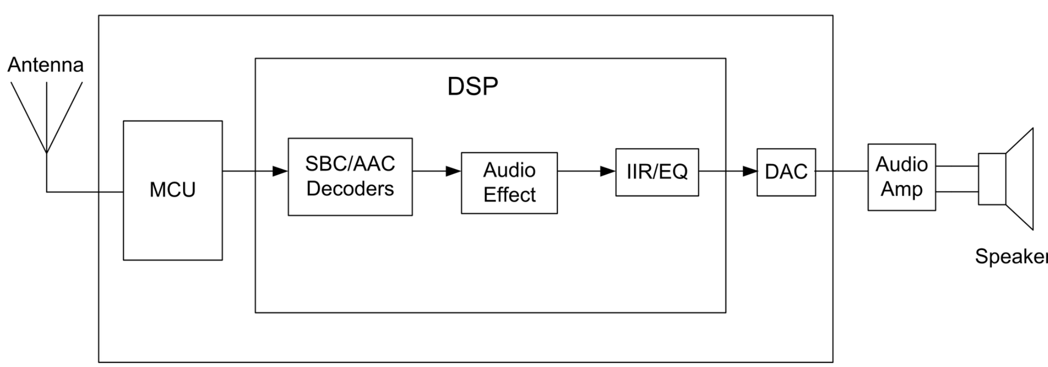


Figure 2-2. Audio Processing



The DSP parameters such as EQ, Speaker Gain, Mic Gain, Sound Effect etc. are configured using the DSP tool. For additional information on the DSP tool, refer to the *IS206x DSP Application Note*.

Note: The DSP tool and *IS206x DSP Application Note* are available for download from the Microchip website: http://www.microchip.com/wwwproducts/en/IS2066.

2.2 Codec

The built-in codec has a high Signal-to-Noise Ratio (SNR) performance and it consists of an ADC, a DAC and additional analog circuitry.

Note: The internal codec supports 16-bit resolution.

The following tables show the measurement results of noise, dynamic range, and THD+N in 1.8V and 2.8V codec voltage supply conditions.

Table 2-1. BTL Measurement Result @1.8V

Parameter (1)	Value
Noise	• DG = 0 FFS, 1 kHz • Volume = Maximum; AA readout = –96.1 dBV
Dynamic range	• Volume = Maximum • DG1 = 0.62 FFS, 1 kHz • AA1 = –2.18 dBV • Dynamic Range = –2.18 dBV – (–96.1 dBV) = 93.92 dB
THD+N	• Volume = Maximum • DG1 = 0.62 FFS, 1 kHz • AA1 THD+N Ratio = 0.044%

1. Measurement Conditions:
   1.1. CODEC_V=1.8V
   1.2. Waveform = Sine, Sample Rate 48 kHz.
   1.3. Bandwidth Low (30 kHz), Ext Gain = 0 dB, Measurement = LPF = 20 kHz, HPF = 22 Hz, A-Weighted, Detector RMS, Average point = 2.

Table 2-2. BTL Measurement Result @2.8V

Parameters (1)	Value
Noise	• DG = 0 FFS, 1 kHz • Volume = Maximum; AA readout = –95.9 dBV
Dynamic range	• Volume = Maximum • DG1 = 0.66 FFS, 1 kHz • AA1 = 3.36 dBV • Dynamic Range = 3.36 dBV – (–95.9 dBV) = 99.26 dB
THD+N	• Volume = Maximum • DG1 = 0.62 FFS, 1 kHz • AA1 THD+N Ratio = 0.044%

1. Measurement Conditions:
   1.1. CODEC_V=2.8V
   1.2. Waveform = Sine, Sample Rate 48 kHz.
   1.3. Bandwidth Low (30 kHz), Ext Gain = 0 dB, Measurement = LPF = 20 kHz, HPF = 22 Hz, A-Weighted, Detector RMS, Average point = 2.

Figure 2-3. Codec DAC Input power vs Output Power 1.8V

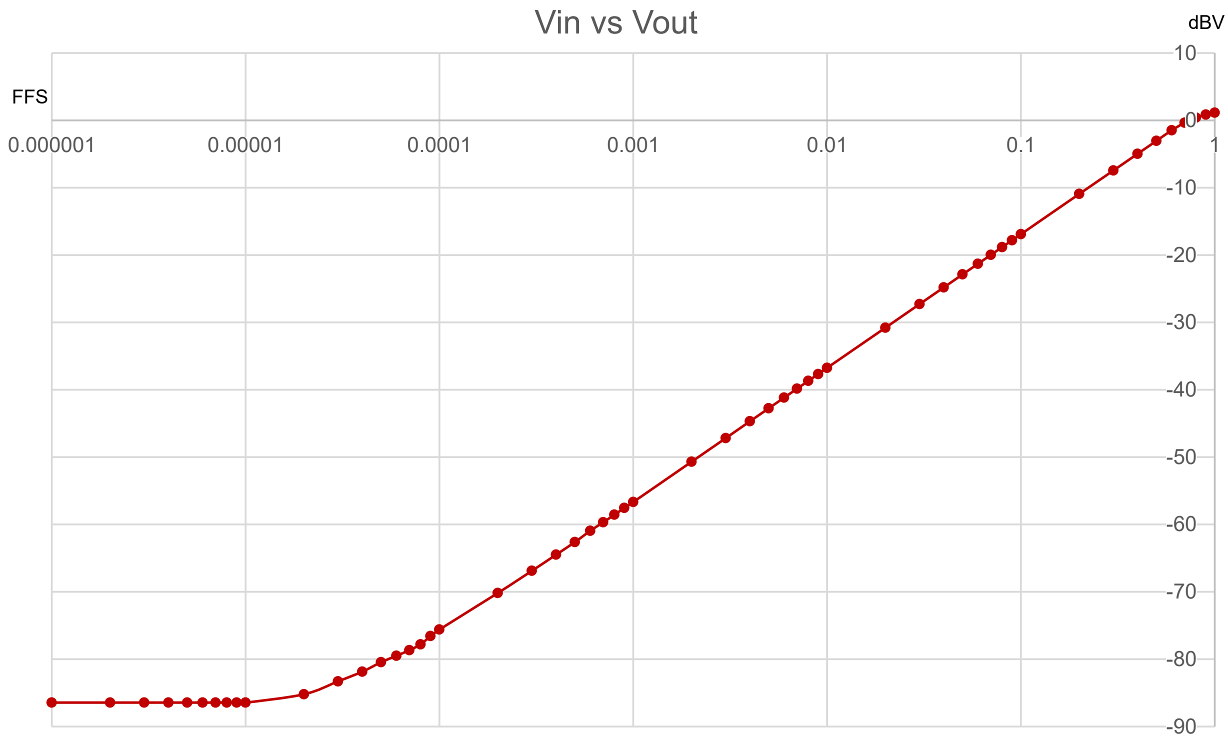


Figure 2-4. Codec DAC Input power vs Output Power 2.8V

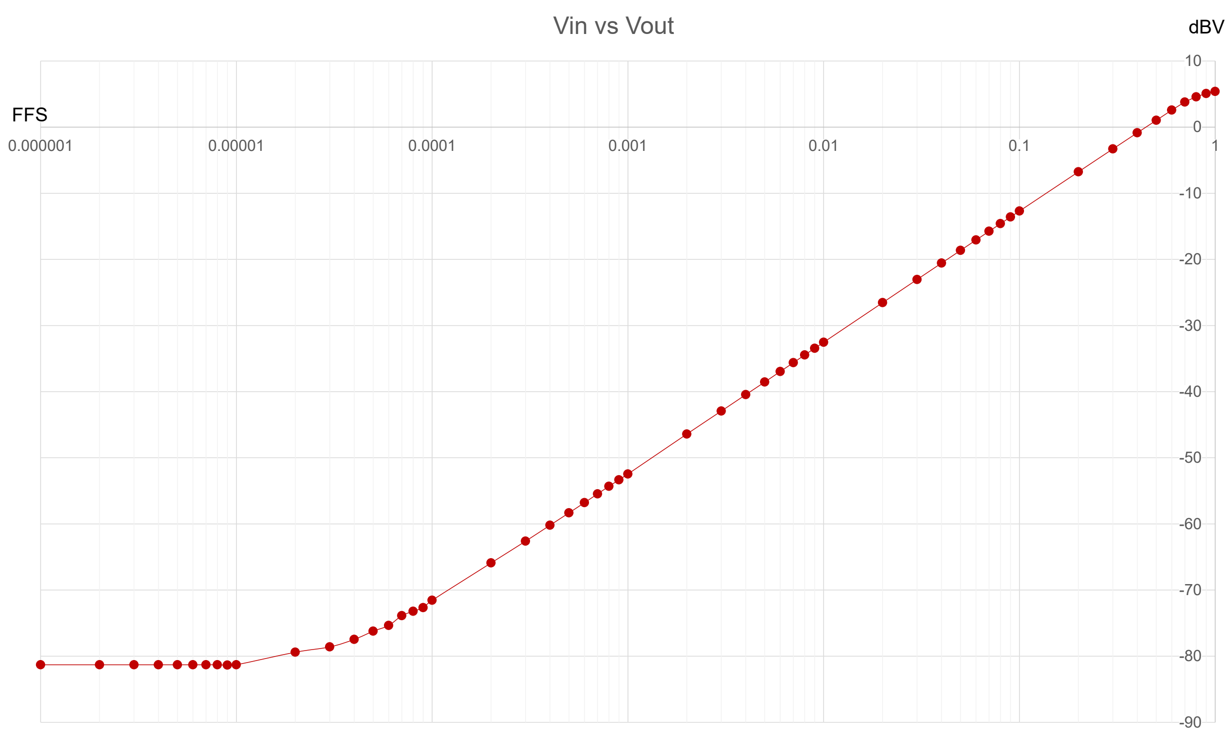


Figure 2-5. Codec DAC THD+N vs Input Power 1.8V codec

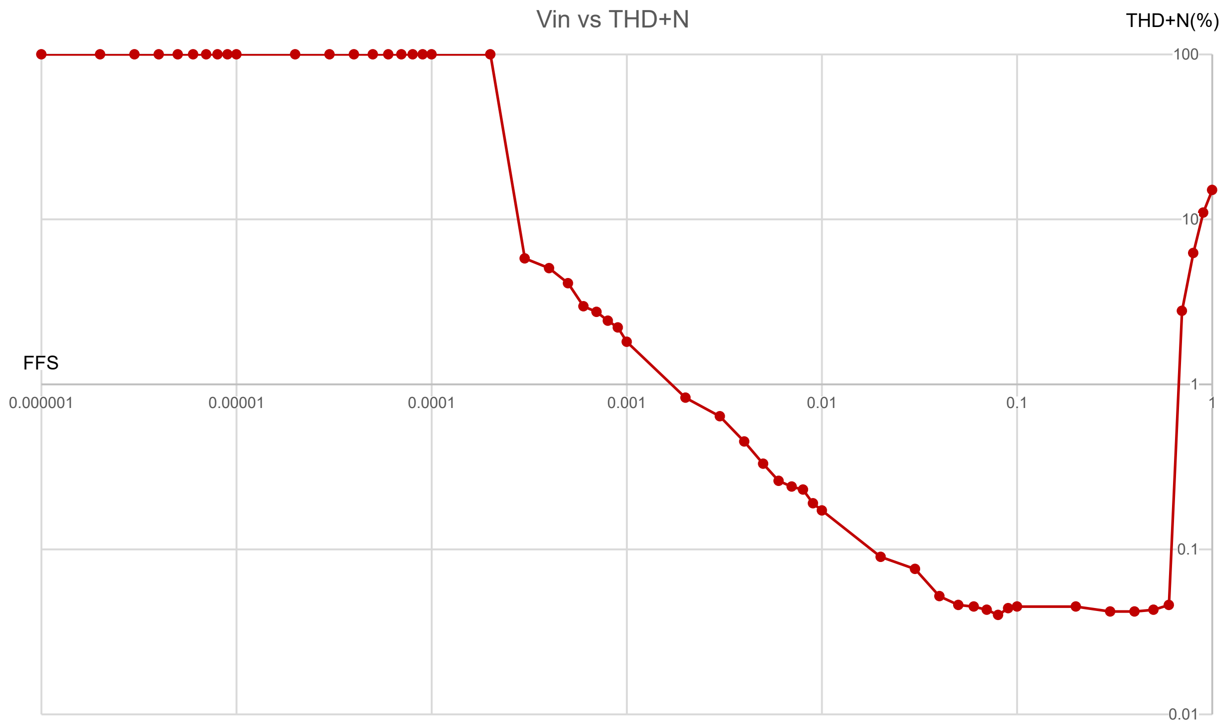


Figure 2-6. Codec DAC THD+N vs Input Power 2.8V codec

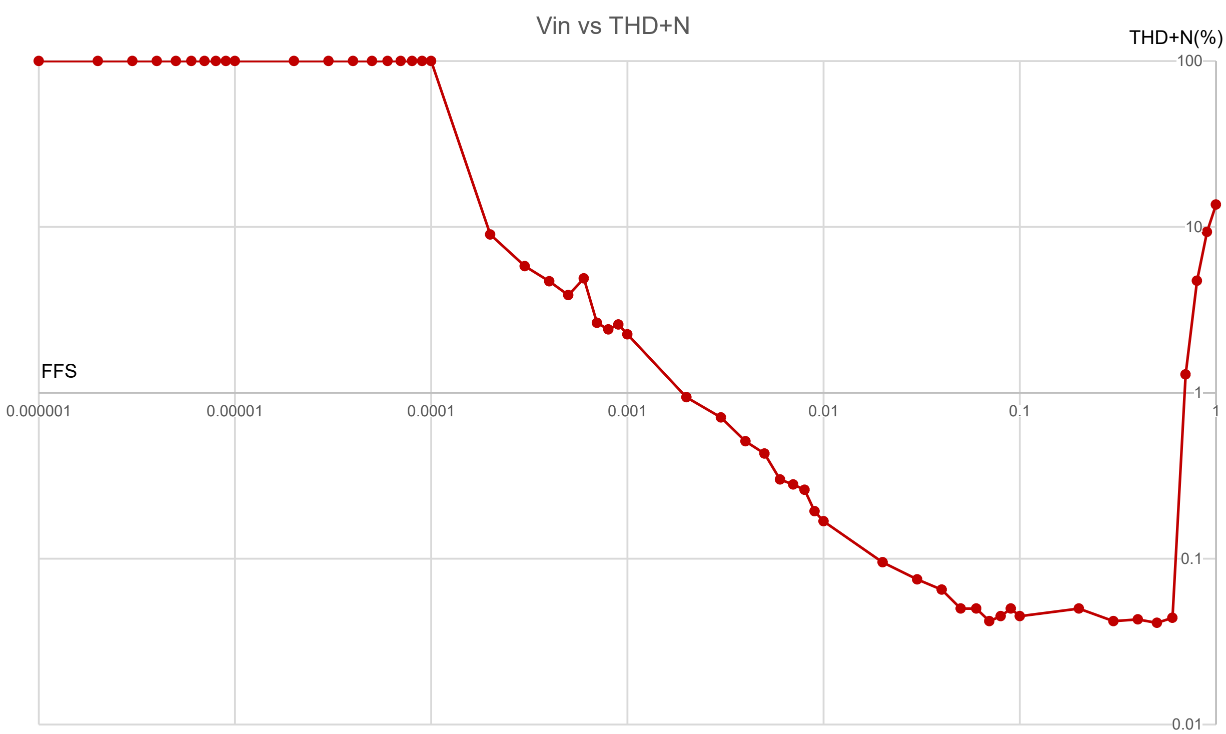


Figure 2-7. Codec DAC THD+N vs frequency 1.8V codec

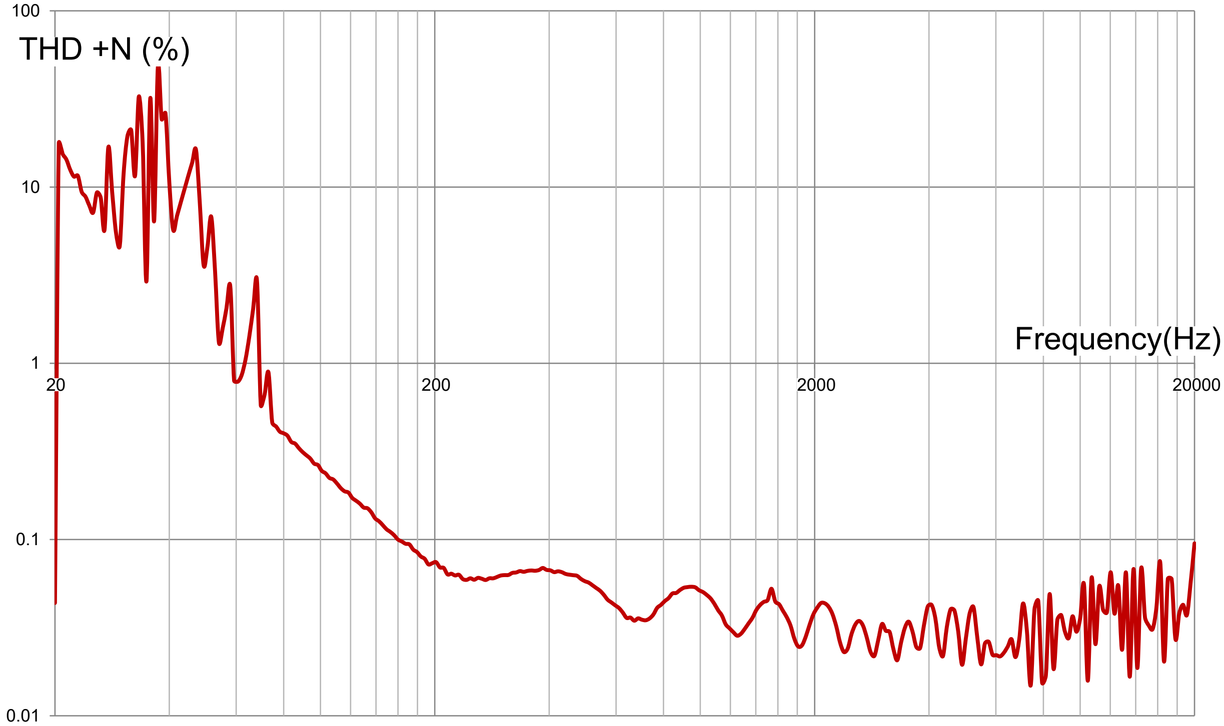
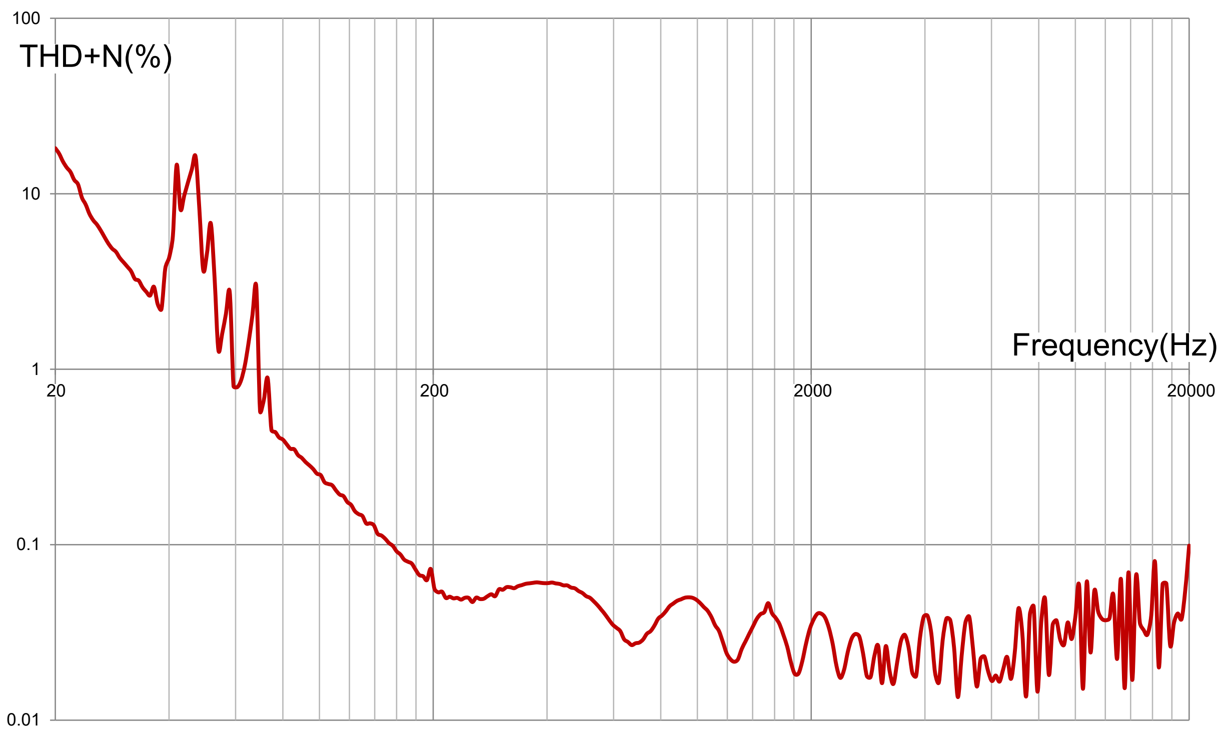


Figure 2-8. Codec DAC THD+N vs frequency 2.8V codec

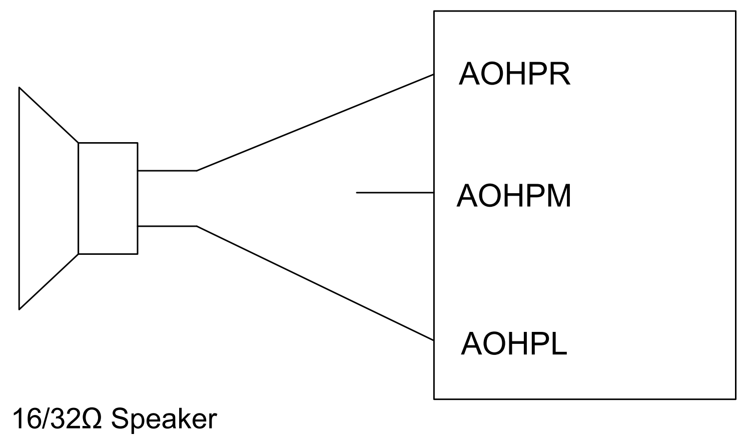


2.3 Analog Speaker Output

The IS2066B SoC supports the following speaker output mode:

- BTL (Bridge-tied load) mode — Recommended for WST earbud applications in which capless and differential output connection helps to save the BOM cost by avoiding a large DC blocking capacitor. The following figure illustrates the analog speaker output BTL mode.

Figure 2-9. Analog Speaker Output BTL Mode



3. Transceiver

The IS2066B SoC is designed and optimized for Bluetooth 2.4 GHz systems. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock to synchronize with another device.

3.1 Transmitter

The internal Power Amplifier (PA) has a maximum output power of +4 dBm. This is applied to Class 2 or Class 3 radios, without an external RF PA. The transmitter directly performs the IQ conversion to minimize the frequency drift.

3.2 Receiver

The Low-Noise Amplifier (LNA) operates with TR-combined mode for the single port application. It saves the pin on the package without having an external Tx/Rx switch.

The ADC is used to sample the input analog signal and convert it into a digital signal for demodulator analysis. A channel filter is integrated into a receiver channel before the ADC to reduce the external component count and increase the anti-interference capability.

The image rejection filter is used to reject the image frequency for the low-IF architecture, and it also is intended to reduce external Band Pass Filter (BPF) component for a super heterodyne architecture.

The Received Signal Strength Indicator (RSSI) signal feedback to the processor is used to control the RF output power to make a good trade-off for effective distance and current consumption.

3.3 Synthesizer

A synthesizer generates a clock for radio transceiver operation. The VCO inside, with a tunable internal LC tank, can reduce any variation for components. A crystal oscillator with an internal digital trimming circuit provides a stable clock for the synthesizer.

3.4 Modem

For Bluetooth 1.2 specification and below, 1 Mbps is the standard data rate based on the Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets Basic Data Rate (BDR) requirements of Bluetooth 2.0 with EDR specifications.

For Bluetooth 2.0 and above specifications, EDR is introduced to provide the data rates of 1/2/3 Mbps. For baseband, both BDR and EDR utilize the same 1 MHz symbol rate and 1.6 kHz slot rate. For BDR, symbol 1 represents 1-bit. However, each symbol in the payload part of EDR packets represent 2-bit or 3-bit. This is achieved by using two different modulations, π/4 DQPSK and 8 DPSK.

3.5 Adaptive Frequency Hopping (AFH)

The IS2066B SoC has an AFH function to avoid RF interference. It has an algorithm to check the nearby interference and to choose the clear channel for transceiver Bluetooth signal.

4. Microcontroller

A microcontroller is built into the SoC to execute the Bluetooth protocols. It operates from 16 MHz to higher frequencies, where the firmware dynamically adjusts the trade-off between the computing power and the power consumption. In the ROM version, the MCU firmware is hard-wired to minimize power consumption for the firmware execution and to save the external Flash cost.

4.1 Memory

There are sufficient ROM and RAM to fulfill the processor requirements, in which a synchronous single port RAM interface is used. The register bank and dedicated single port memory are connected to the processor bus. The processor coordinates with all link control procedures and the data movement happens using a set of pointer registers.

4.2 External Reset

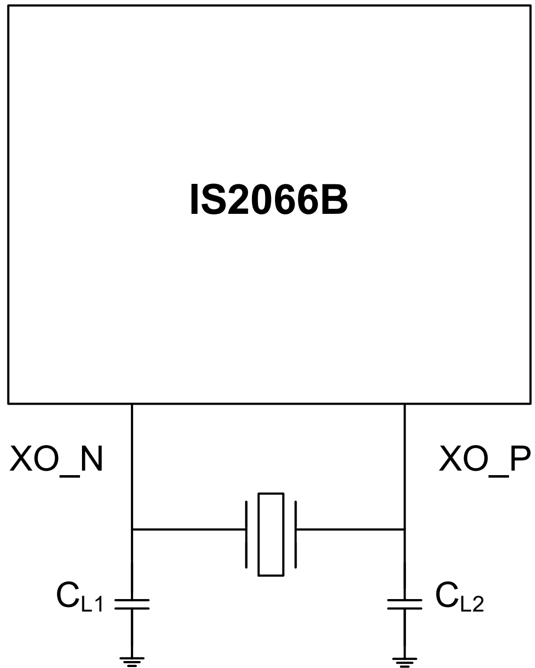
The IS2066B SoC provides a Watchdog Timer (WDT) to reset the SoC. It has an integrated Power-on Reset (POR) circuit that resets all circuits to a known Power-on state. This action is also driven by an external Reset signal, which is used to control the device externally by forcing it into a POR state. The RST_N signal input is active-low and no connection is required in most of the applications.

4.3 Reference Clock

The IS2066B SoC is composed of an integrated crystal oscillation function that uses a 16 MHz±10 ppm external crystal and two specified loading capacitors to provide a high quality system reference timer source. This feature is typically used to remove the initial tolerance frequency errors, which are associated with the crystal and its equivalent loading capacitance in the mass production. Frequency trim is achieved by adjusting the crystal loading capacitance through the on-chip trim capacitors (C_{trim}).

The value of trimming capacitance is 200 fF (200×10^{-15} F) per LSb at 5-bit word and the overall adjustable clock frequency is ±40 kHz (based on the crystal with load capacitance, C_L spec = 9 pF). The following figure illustrates the crystal connection of the IS2066B SoC with two capacitors.

Figure 4-1. Crystal Connection



Note:

1. C_{trim}= 200 fF * (1 to 31); C_{int} = 3 pF.
2. C_L= [C_{L1} x C_{L2})/(C_{L1}+C_{L2})]+(C_{trim}/2)+C_{int} (set trim value as 16, then C_{trim} = 3.2 pF).
3. For a 16 MHz crystal, in which C_L= 9 pF, then the C_{L1} = C_{L2} = 9.1 pF).
4. For C_L selection, refer to the data sheet of the crystal.

5. Power Management Unit

The IS2066B SoC has an integrated Power Management Unit (PMU). The main features of the PMU are a lithium-ion and lithium-polymer battery charger, and a voltage regulator. The power switch is used to exchange the power source between a battery and an adapter. In addition, the PMU provides current to the LED drivers.

5.1 Battery Charger

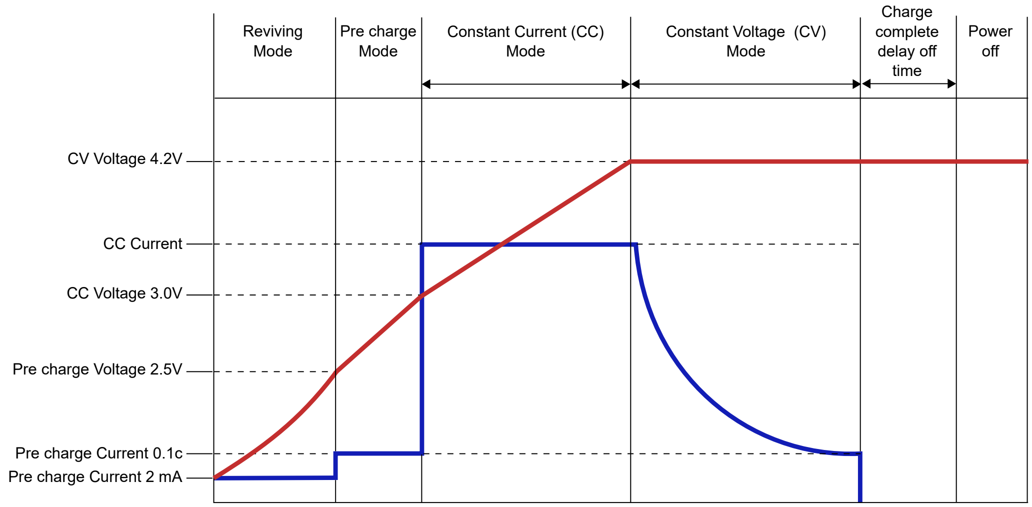
The IS2066B SoC has a built-in battery charger, which is optimized with lithium-ion and lithium-polymer batteries. The battery charger includes a current sensor for charging control, user programmable current regulator, and high accuracy voltage regulator.

The charging current parameters are configured by using the UI tool. An adapter is plugged in to activate the charging circuit. Reviving, Pre-Charging, Constant Current and Constant Voltage modes functions are included. The maximum charging current is 350 mA. The following figure illustrates the charging curve of a battery.

When the charging current is lower than a preset percentage (set by UItool) of CC mode current, charging will stop and charging LED will be turned off for an indication. A configurable period (set by UItool) of time is able to set for power off the unit after charging complete in order to save power consumption.

Microchip suggests following the charging box reference design for WST earbud. The IS2066B “Charge complete delay off time” should be configured as shorter than charging box low current detection off time, so correct in-out box behavior can be maintained.

Figure 5-1. Battery Charging Curve



Reviving Mode
This mode is entered when the VBAT senses the voltage between the range of 0V to 2.5V. During this mode, the charging current is controlled by IS2066B internally with a fixed current of 2 mA.

Pre-charge mode
The mode is entered when VBAT senses the voltage between the range of 2.5V to 3.0V. During this mode, the battery is charged with a fixed rate of 10% of configurable charging current (UItool setting: Charging current)

Constant Current Mode
The Constant Current (CC) mode is entered when VBAT senses the voltage between the range of 3.0V to 4.2V. During this mode, the battery is charged in a configurable constant current (UItool setting: Charging current), until the Constant Voltage (CV) is reached.

Constant Voltage Mode

The CV voltage (Constant Voltage mode voltage) is 4.2V (fixed). The mode is entered when VBAT senses the CV voltage (4.2V). During this mode, battery charging current is constantly decreased to maintain voltage at the CV voltage level.

Charge Complete state is entered when charging current is lower than a configurable percentage (UItool setting: Constant Voltage charging OK Current) of the CC mode current.

Device is powered off to save power after a configurable delay off time (UItool setting: Charge Complete Delay Off Time). External charging requires a light load detection feature to sense this low-power consumption and perform a charging supply power cut off.

Special Mode

Special mode with initial 4.0V to CV voltage. Two special modes are there with different initial VBAT conditions:

1. During the adapter voltage ramp-up, if the VBAT is higher than 4.1V, device enters to charge complete state directly. This is to provide a hysteresis on charging to charge complete by 100 mV.
2. During the adapter voltage ramp-up, if the VBAT is between 4.0V to 4.1V, the device enters lower re-charging current state, a fixed 25% of the CC mode current charges the battery until it reaches CV voltage. This is to provide a slow charge rate to the battery when it is close to the CV voltage.

5.2 Battery Protection

Microchip requires that all applications using IS2066B include a battery protection. It is common to have this built-in protection circuit, as a secondary protection for the battery. This protection disconnects the battery from the IS2066B when the voltage is too high or too low. As an example, battery specification with built-in OVP (overvoltage protection) and UVP (undervoltage protection) is given below:

Table 5-1. Recommended Battery Specifications

Parameters	Values
Nominal voltage	3.7V
Charge ending voltage	4.2V
Discharge ending voltage	3.0V
Max charge current	1C or higher
Overcharge protection voltage	4.25V – 4.30V
Over discharge detection voltage	2.8V – 3.2V

The following table provides the manufacturer and model information of the example batteries with built-in protection.

Table 5-2. Battery Manufacturers and Model Information

Manufacturer Name	Model Number
VDL Electronics	VDL10100
VDL Electronics	VDL1254
VDL Electronics	VDL10100
JuHeYuan	JHY451225
Great Power	GSP061021
Jin Yu Zhou energy	601015

5.3 Low Dropout Regulator

A built-in Low Dropout (LDO) Regulator is used to convert the battery or adapter power for power supply. It also integrates the hardware architecture to control the power-on/off procedure. The built-in programmable LDOs provide power for codec and digital I/O pads. In addition, it is used to buffer the high input voltage from battery or adapter. This LDO requires 1 μF bypass capacitor.

5.4 Switching Regulator

The IS2066B has two built-in programmable switching regulators, which convert the battery voltage to different power supply levels. Buck 1 supplies the RF and core domain, and Buck 2 supplies the audio codec domain. This converter has a high conversion efficiency and a fast transient response.

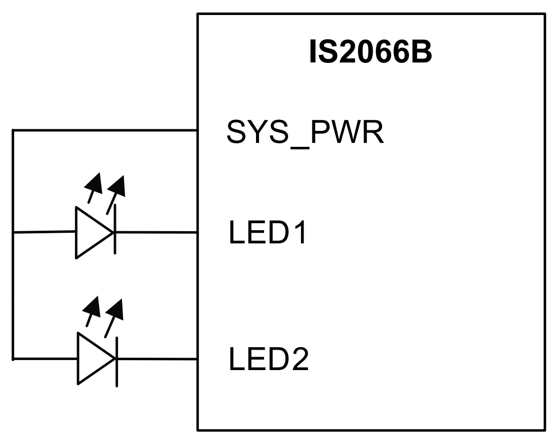
Buck 2 layout design requires extra attention due to the codec loading; thus, ensure that no capacitor is placed next to pin #C9 (BK2_VDD). However, place the capacitor as close as possible to pin #F3 (SYS_PWR). Placing a capacitor next to pin #C9 may affect the IS2066B system stability. For more details on the schematic, refer to 12. Reference Circuit.

5.5 LED Driver

The IS2066B contains two LED drivers to control the LEDs. The LED drivers provide enough sink current (16-step control and 0.35 mA for each step) and the LED is connected directly to the IS2066B SoC. The LED settings are configured using the UI tool.

The following figure illustrates the LED driver in the IS2066B SoC.

Figure 5-2. LED Driver



5.6 Undervoltage Protection

When the voltage of BAT_IN pin drops below the voltage level of 3.0V, the system shuts down automatically.

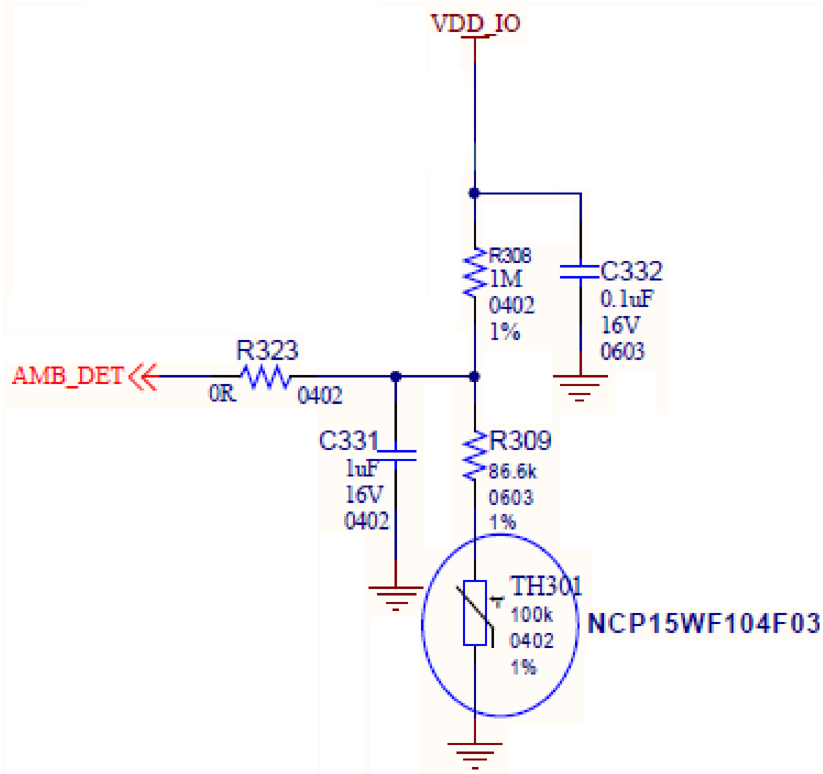
5.7 Ambient Detection

The IS2066B SoC contains a built-in ADC for charger thermal protection.

The following figure illustrates the Murata NCP15WF104F thermistor with suggested circuit schematics. The charger thermal protection avoids battery charge in the restricted temperature range. Battery with NTC (Negative Temperature Coefficient) sensor can be supported by this same ADC. The upper and lower limits for temperature values are configured by using the UI tool for stop charging and reset operation.

Note: The thermistor must be placed close to the battery in the user application for accurate temperature measurements and to enable the thermal shutdown feature.

Figure 5-3. Ambient Temperature Detector



6. Application Information

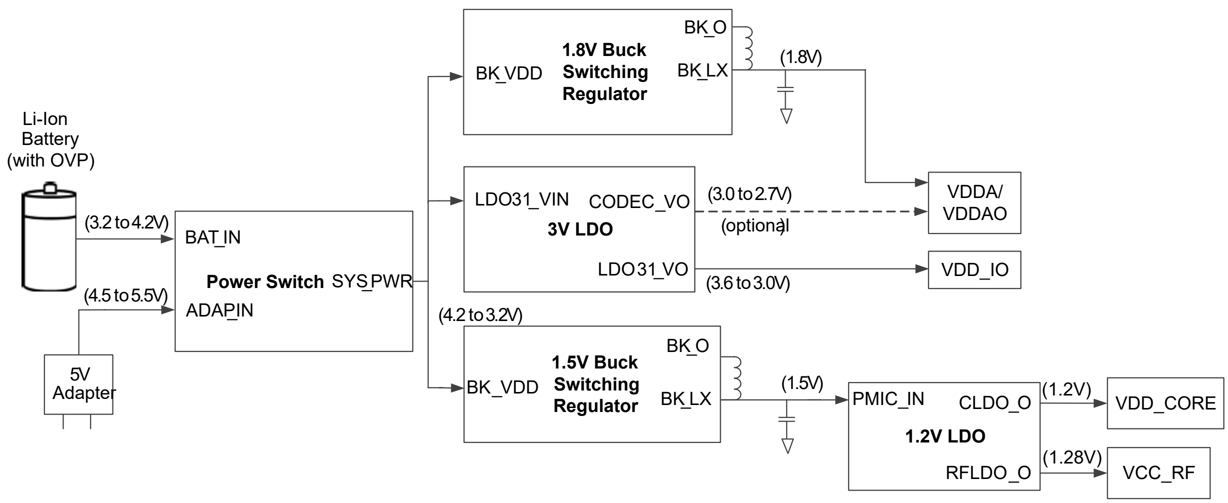
This section describes the power supply connection, host MCU UART interface, and various modes in detail.

6.1 Power Supply

The following figure illustrates the connection from the BAT_IN pin to various other voltage supply pins of the IS2066B SoC.

The IS2066B SoC is powered through the BAT_IN input pin. The external 5V power adapter can be connected to ADAP_IN in order to charge the battery.

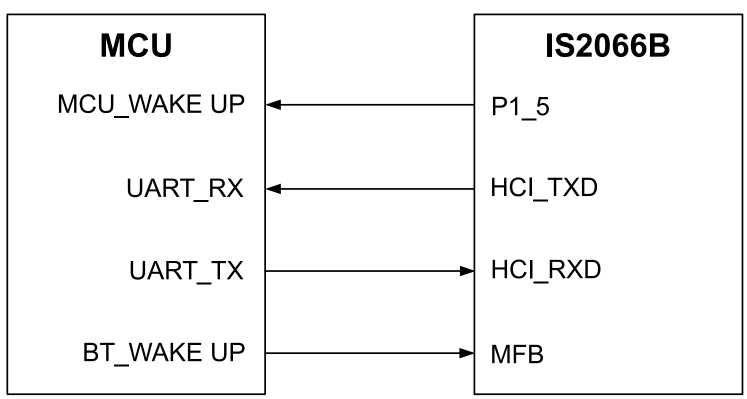
Figure 6-1. Power Tree Diagram



6.2 Host MCU Interface

The following figure illustrates the UART interface between the IS2066B SoC and an external MCU.

Figure 6-2. Host MCU Interface over UART



The MCU controls the IS2066B SoC over the UART interface and wakes up the SoC using the MFB and P1_5 pins.

Refer to the "*UART_CommandSet*" document for a list of functions that theIS2066B SoC supports and how to use the UI tool to set up the system using the UART command.

Note: The "*UART_CommandSet*" document is available for download from the Microchip website: http://www.microchip.com/wwwproducts/en/IS2066.

The following figures illustrate the various UART control signal timing sequences.

Figure 6-3. Power ON/OFF Sequence

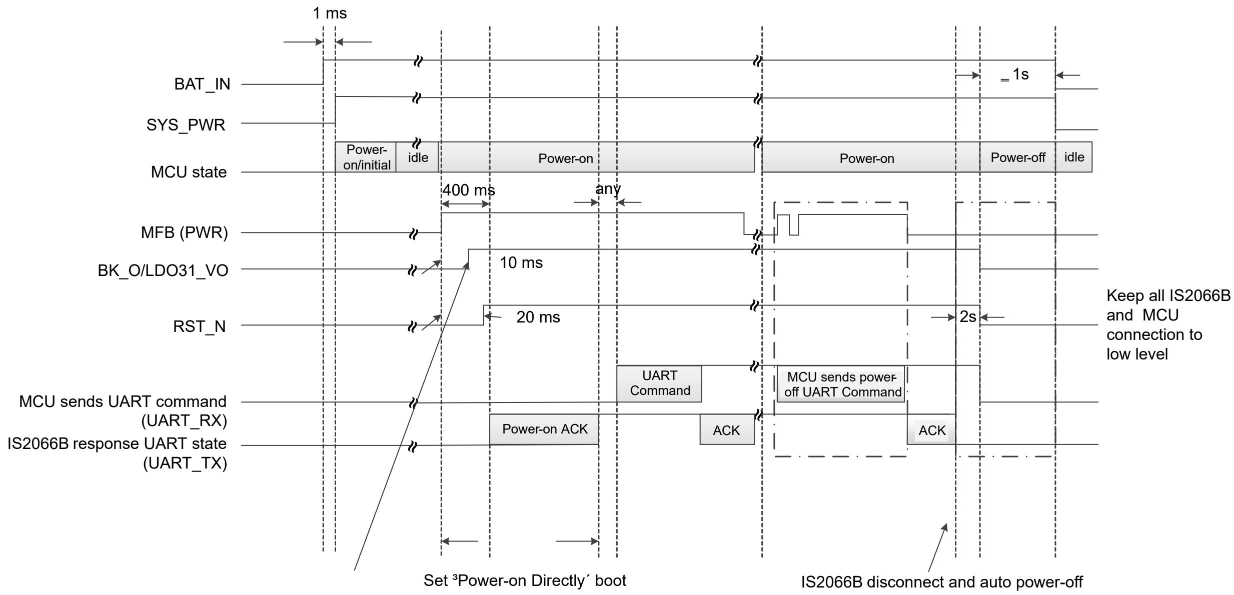


Figure 6-4. Timing Sequence of RX Indication after Power ON

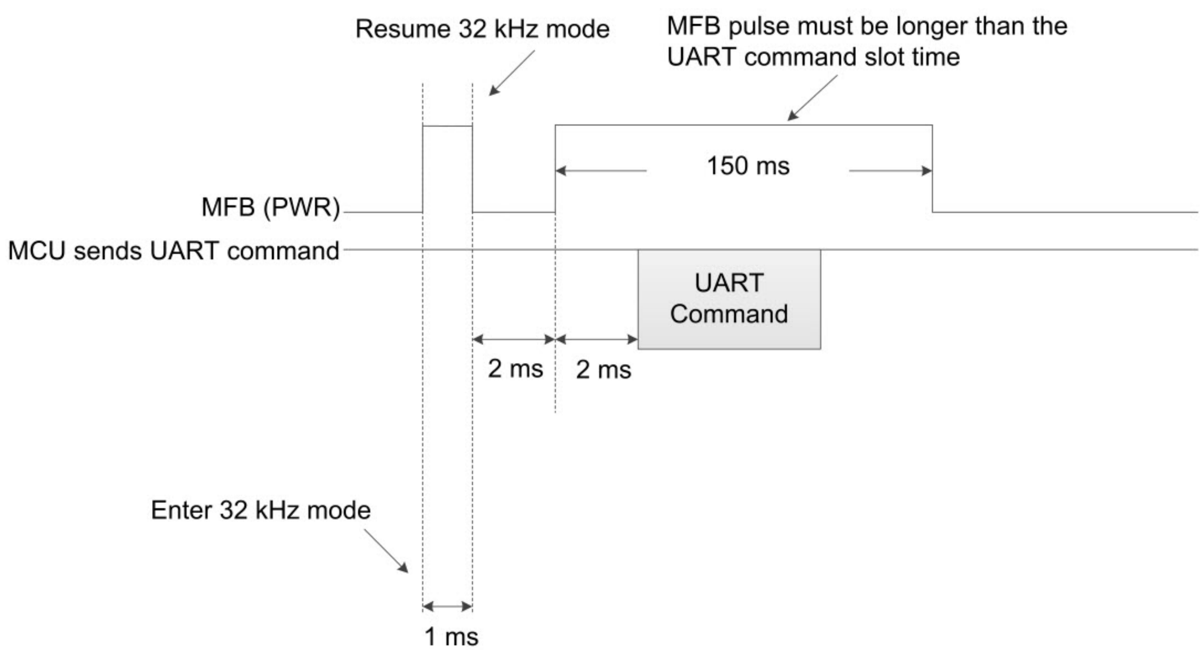
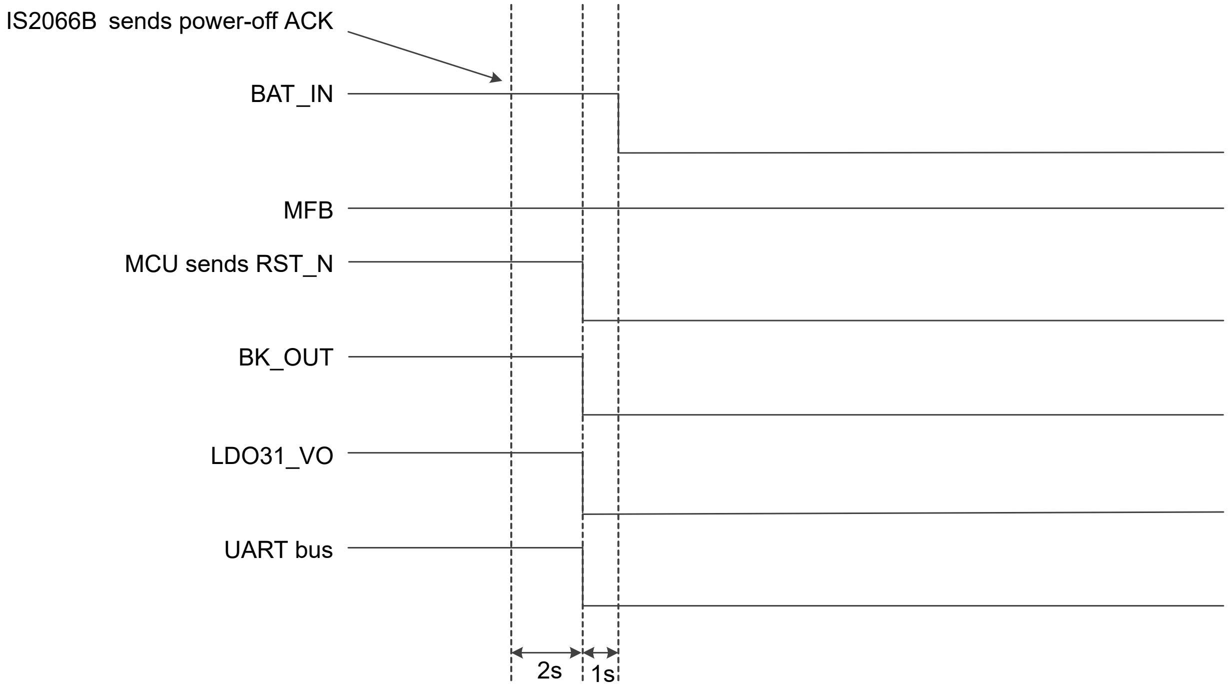


Figure 6-5. Timing Sequence of Power OFF



Note:
1. EEPROM clock = 100 kHz.
2. For a byte wire, 0.01 ms x 32 clock x 2 = 640 μs.
3. It is recommended to have ramp-down time more than 640 μs during the power-off sequence to ensure safe operation of the device.

Figure 6-6. Timing Sequence of Power-ON (NACK)

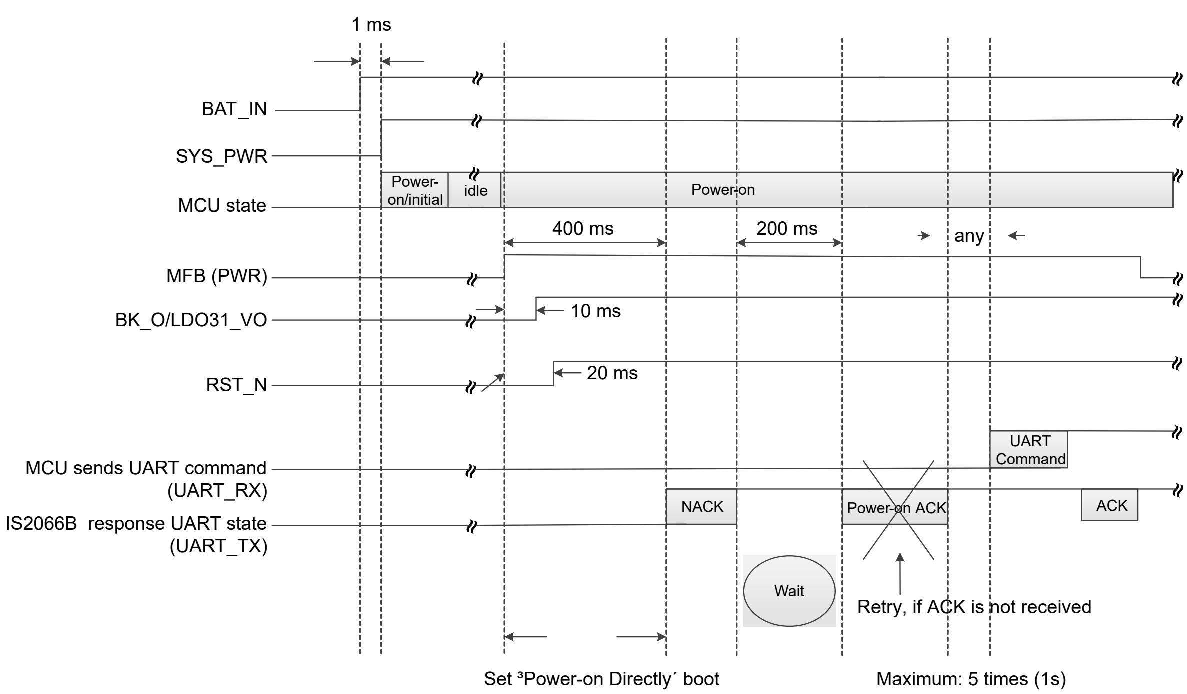
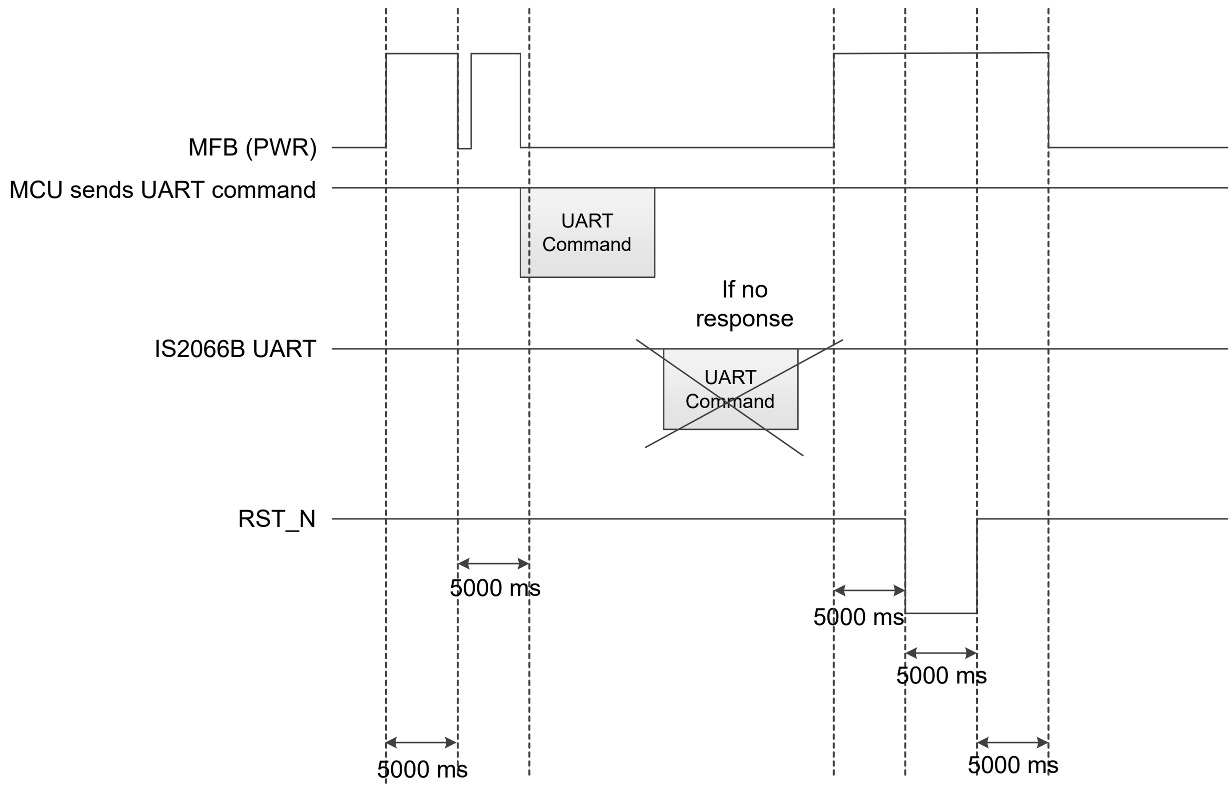


Figure 6-7. Reset Timing Sequence in case of No Response from SoC to Host MCU

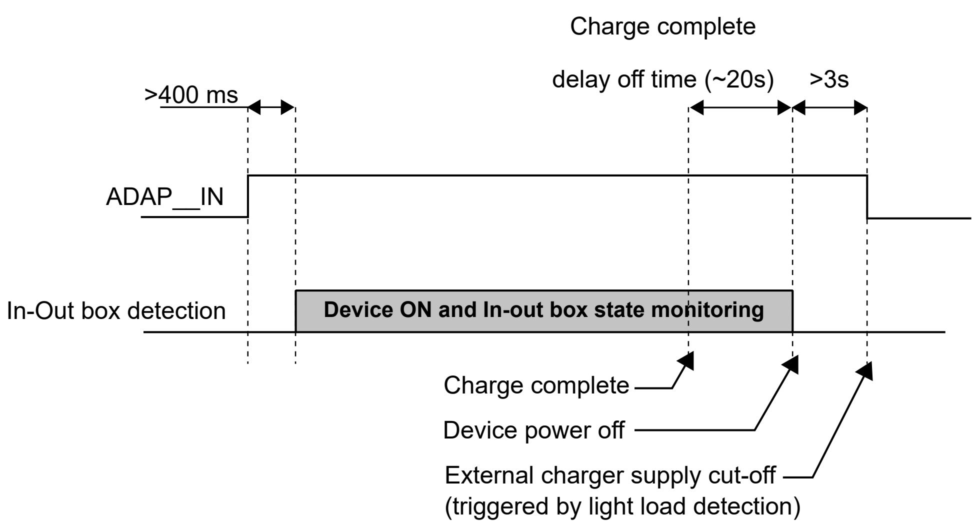


Note: The MCU sends the UART command again, when SoC is not responding to its first UART command. If the SoC is not responding to the second UART command within 5 secs, then the MCU forces the system to reset.

6.3 In-out Box Detection

This helps to turn ON the device at the time of adapter input detection.

Figure 6-8. In-out Box Timing Diagram



6.4 General Purpose I/O pins

The following table details the various functions that are mapped to the I/O pins of IS2066B SoC and configured using the UI tool.

Note: The MFB pin must be configured as the power-ON/OFF key and the remaining pins are configured for any one of the default functions, as provided in the following table.

Table 6-1. GPIO Pin Description

S.No	Pin Name	IS2066B
1	MFB	• Button 0 • UART RX_IND
2	P1_5	Out_Ind_1 (UART_TX_IND)
3	P0_0	Optional in-out box detection
4	P0_3	Optional charging completed event
5	P0_2	Button configuration
6	P2_0	System config
7	P2_7	Button configuration

6.5 EEPROM Content Corruption During Power Drop

Microchip's EEPROM 24CW128x (128-Kbit and 32-byte page size) is integrated in the IS2066B device.

The power supply to the IS2066B device must remain above the minimum operating voltage during an EEPROM write operation to ensure data integrity.

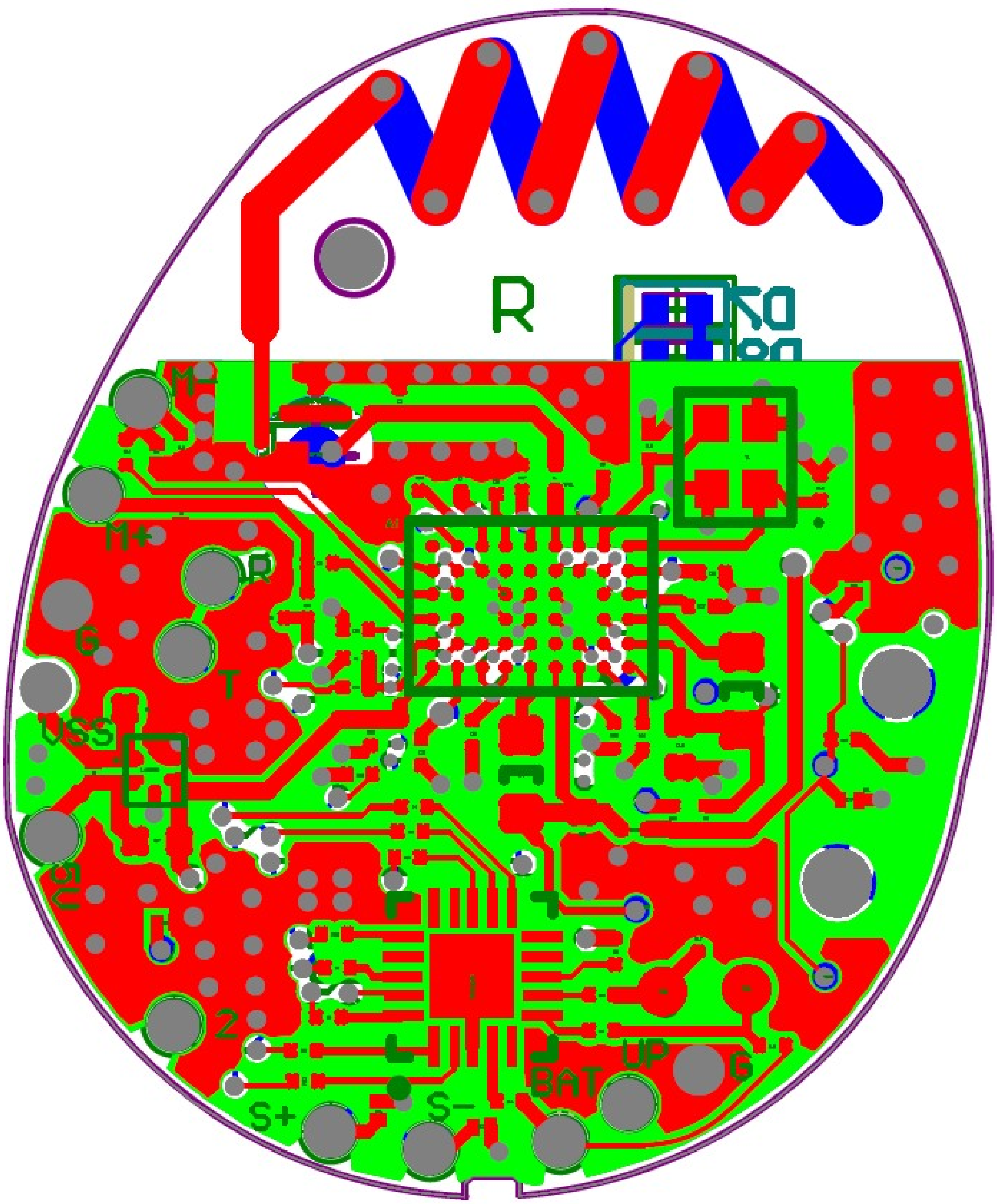
⚠ CAUTION A sudden power drop during an EEPROM Write operation may trigger a 32-bytes page erase.

7. Antenna Placement Rule

For Bluetooth-enabled products, the antenna placement affects the overall performance. The antenna requires free space to radiate RF signals and it must not be surrounded by the GND plane.

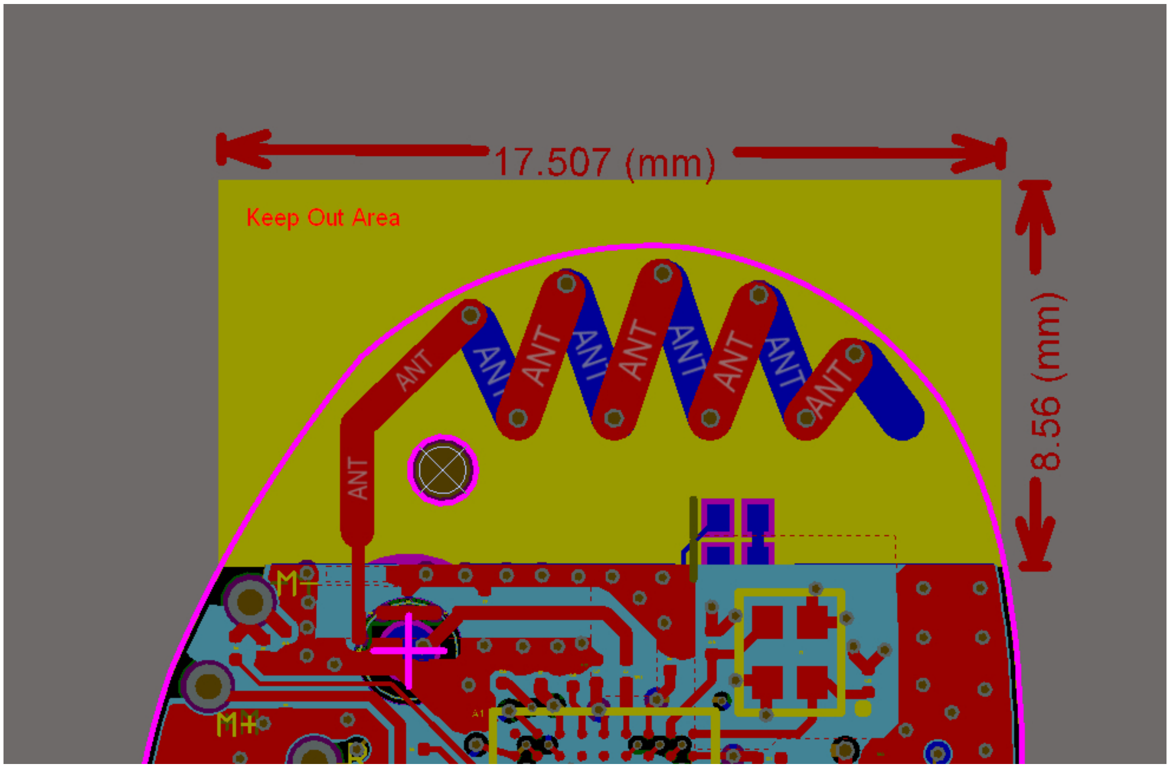
The following figure illustrates reference earbud antenna example.

Figure 7-1. Example Antenna



The following figure illustrates the keep out area recommended for the PCB antenna.

Figure 7-2. Keep-out Area Recommended for PCB Antenna



Note: It is recommended to keep the antenna free from any metal objects or components on top or bottom of the keep out area. For other antennas (for example, chip antenna), follow the recommended keep out and design requirements as specified by the antenna vendor in their data sheet.

8. Electrical Characteristics

This section provides an overview of the IS2066B SoC electrical characteristics. Additional information is to be provided in future revisions of this document, once it is available.

Table 8-1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Ambient temperature under bias	—	-20	+70	℃
Storage temperature	—	-65	+150	℃
Digital core supply voltage	VDD_CORE	0	1.35	V
RF supply voltage	VCC_RF	0	1.35	V
SAR ADC supply voltage	SAR_VDD	0	2.1	V
Codec supply voltage	VDDA/VDDAO	0	3.3	V
I/O supply voltage	VDD_IO	0	3.6	V
Buck supply voltage	BK_VDD	0	4.3	V
Supply voltage	LDO31_VIN	0	4.3	V
Battery input voltage	BAT_IN	0	4.3	V
Adapter input voltage	ADAP_IN	0	7.0	V

⚠ CAUTION Stresses listed on the preceding table cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions and those indicated in the operation listings of this specification are not implied. Exposure to maximum rating conditions for extended periods affects device reliability.

The following tables provide the recommended operating conditions and the electrical specifications of the IS2066B SoC.

Table 8-2. Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital core supply voltage	VDD_CORE	1.14	1.2	1.26	V
RF supply voltage	VCC_RF	1.22	1.28	1.34	V
SAR ADC supply voltage	SAR_VDD	1.62	1.8	1.98	V
Codec supply voltage	VDDA/VDDAO	1.8	2.8	3.0	V
I/O supply voltage	VDD_IO	3.0	3.3	—	V
Buck supply voltage	BK_VDD	3	3.8	4.25	V
Supply voltage	LDO31_VIN	3	3.8	4.25	V
Input voltage for battery	BAT_IN	3.2	3.8	4.25	V
Input voltage for adapter	ADAP_IN	4.5	5	5.5	V
Operation temperature	$T_{OPERATION}$	-20	+25	+70	℃

Note: The PMU output powers, BK_O, CODEC_VO, RFLDO_O, and CLDO_O are programmed through the EEPROM parameters.

Table 8-3. I/O and RESET Level

Parameter		Min.	Typ.	Max.	Unit
I/O supply voltage (VDD_IO)		3.0	3.3	3.6	V
I/O voltage levels					
VIL input logic levels low		0	—	0.8	V
VIH input logic levels high		2.0	—	3.6	V
VOL output logic levels low		—	—	0.4	V
VOH output logic levels high		2.4	—	—	V
RST_N	Input Low to High Threshold Point	—	—	1.87	V
	Input High to Low Threshold Point	1.25	—	—	V
Threshold voltage		—	1.6	—	V

Note:

1. These parameters are characterized, but not tested on the manufactured device.

Table 8-4. Buck Regulator

Parameter	Min.	Typ.	Max.	Unit
Input voltage	3.0	3.8	4.25	V
Output voltage (I_{load} = 70 mA and V_{in} = 4V)	1.7	1.8	2.05	V
Output voltage accuracy	—	±5	—	%
Output voltage adjustable step	—	50	—	mV/Step
Output adjustment range	-0.1	—	+0.25	V
Average load current (I_{LOAD})	120	—	—	mA
Conversion efficiency (BAT = 3.8V and I_{load} = 50 mA)	—	88[(1)]	—	%
Quiescent current (PFM)	—	—	40	µA
Output current (peak)	200	—	—	mA
Shutdown current	—	—	<1	µA

Note:

1. Test condition: Temperature +25℃ and wired inductor 10 µH.
2. These parameters are characterized, but not tested on the manufactured device.

Table 8-5. Low Drop Regulator

Parameter		Min.	Typ.	Max.	Unit
Input voltage		3.0	3.8	4.25	V
Output voltage	CODEC_VO	—	2.8	—	V
	LDO31_VO	—	3.3	—	

...........continued

Parameter	Min.	Typ.	Max.	Unit
Output accuracy (V_{IN} = 3.7V, I_{LOAD} = 100 mA and +27°C)	—	±5	—	%
Output current (average)	—	—	100	mA
Drop-out voltage (I_{load} = maximum output current)	—	—	300	mV
Quiescent current (excluding load and I_{load} < 1 mA)	—	45	—	µA
Shutdown Current	—	—	<1	µA

Note:
1. Test condition: Temperature +25℃.
2. These parameters are characterized, but not tested on manufactured device.

Table 8-6. Battery Charger

Parameter		Min.	Typ.	Max.	Unit
Input voltage (ADAP_IN)		4.5	5.0	5.5	V
Supply current to charger only		—	3	4.5	mA
Maximum Battery Fast Charge Current	Headroom > 0.7V (ADAP_IN = 5V)	—	350	—	mA
	Headroom = 0.3V to 0.7V (ADAP_IN = 4.5V) (**Note 2**)	—	175	—	mA
Trickle charge voltage threshold		—	3	—	V
Battery charge termination current (% of Fast Charge Current)		—	10	—	%

Note:
1. Headroom = V_{ADAP_IN} - V_{BAT}.
2. When V_{ADAP_IN} - V_{BAT} > 2V, the maximum fast charge current is 175 mA for thermal protection.
3. These parameters are characterized, but not tested on manufactured device.

Table 8-7. LED Driver

Parameter	Min.	Typ.	Max.	Unit
Open-drain voltage	—	—	3.6	V
Programmable current range	0	—	5.25	mA
Intensity control	—	16	—	step
Current step	—	0.35	—	mA
Power down open-drain current	—	—	1	µA
Shutdown current	—	—	1	µA

Note:

1. Test condition: BK_O = 1.8V with temperature +25°C.
2. These parameters are characterized, but not tested on manufactured device.

Table 8-8. Audio Codec Digital-to-Analog Converter

Parameter (Condition)		Min.	Typ.	Max.	Unit
Output sampling rate		—	128	—	f_s
Resolution		16	—	20	Bit
Output sample frequency		8	—	48	kHz
Signal-to-Noise Ratio (**Note 2**) (SNR @capless mode) for 48 kHz		—	96	—	dB
Signal-to-Noise Ratio (**Note 2**) (SNR @single-ended mode) for 48 kHz		—	98	—	dB
Digital gain		-54	—	4.85	dB
Digital gain resolution		—	2 to 6	—	dB
Analog gain		-28	—	3	dB
Analog gain resolution		—	1	—	dB
Output voltage full-scale swing (AVDD = 2.8V)		495	742.5	—	mV/rms
Maximum output power (16Ω load)		—	34.5	—	mW
Maximum output power (32Ω load)		—	17.2	—	mW
Allowed load	Resistive	—	16	O.C.	Ω
	Capacitive	—	—	500	pF
THD+N (16Ω load) (**Note 3**)		—	0.05	—	%
Signal-to-Noise Ratio (SNR @ 16Ω load) (**Note 4**)	—	—	98	—	dB

Note:

1. T = +25°C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz to 20 kHz.
2. f_{in} = 1 kHz, B/W = 20 HZ to 20 kHz, A-weighted, THD+N < 0.01%, 0 dBFS signal, Load = 100 kΩ.
3. f_{in} = 1 kHz, B/W = 20 HZ to 20 kHz, A-weighted, -1 dBFS signal, Load = 16Ω.
4. f_{in} = 1 kHz, B/W = 20 HZ to 20 kHz, A-weighted, THD+N < 0.05%, 0 dBFS signal, Load = 16Ω.
5. These parameters are characterized, but not tested on manufactured device.

Table 8-9. Audio Codec Analog-to-Digital Converter

Parameter (Condition)	Min.	Typ.	Max.	Unit
Resolution	—	—	16	Bit
Output Sample Rate	8	—	48	kHz

...........continued				
Parameter (Condition)	**Min.**	**Typ.**	**Max.**	**Unit**
Signal-to-Noise Ratio (**Note 2**) (SNR @MIC or Line-in mode)	—	92	—	dB
Digital Gain	-54	—	4.85	dB
Digital Gain Resolution	—	2 to 6	—	dB
MIC Boost Gain	—	20	—	dB
Analog Gain	—	—	60	dB
Analog Gain Resolution	—	2.0	—	dB
Input full scale at maximum gain (differential)	—	4	—	mV/rms
Input full scale at minimum gain (differential)	—	800	—	mV/rms
3 dB bandwidth	—	20	—	kHz
Microphone mode (input impedance)	—	24	—	kΩ
THD+N (microphone input) at 30 mVrms input	—	0.02	—	%

Note:
1. T = +25°C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz to 20 kHz
2. f_{in} = 1 kHz, B/W = 20 Hz to 20 kHz, A-weighted, THD+N < 1%, 150 mVpp input.
3. These parameters are characterized, but not tested on manufactured device.

Table 8-10. Transmitter Section for BDR and EDR

Parameter	Bluetooth Specification	Min.	Typ.	Max.	Unit
Transmit power	-6 to 4	—	2(3)	4	dBm
EDR/BDR relative transmit power	-4 to 1	-4	-1.8	1	dB

Note:
1. The RF Transmit power is modulation value.
2. The RF Transmit power is calibrated during production using the MP tool software and MT8852 Bluetooth test equipment.
3. Test condition: VCC_RF = 1.28V, temperature +25℃.

Table 8-11. Receiver Section for BDR and EDR

Parameter	Packet Type	Min.	Typ.	Max.	Unit
Sensitivity at 0.1% BER	GFSK	—	-89	—	dBm
Sensitivity at 0.01% BER	π/4 DQPSK	—	-93	—	dBm
	8 DPSK	—	-86	—	dBm

Note:

1. Test condition: VCC_RF = 1.28V, temperature +25ºC.
2. These parameters are characterized, but not tested on manufactured device.

Table 8-12. IS2066B System Current Consumption(1-6, 8)

Modes	Condition	WST Connection Role	Average Current (ROM)	Unit
A2DP (1 kHz tone, mute, no load) (Enable AAC) (iPhone 7)	BAT_IN	Primary	10.98	mA
		Secondary	11.94	
SCO/eSCO (mute at both far end and near end) (Android)		Primary	9.99	
		Secondary	10.28	
Power OFF		Primary	0.002	
		Secondary	0.002	
Power OFF(7)	ADAP_IN (5V)	-	1.4	

Note:

1. The measurements are taken on the IS2066B EVB v2.0.
2. BAT_IN = 3.8V, and current is measured across BAT_IN.
3. The measurements are taken without LED and speaker loading.
4. The distance between the DUT (IS2066B EVB) and the smartphone is 20 cm.
5. Smartphone used for measurement is iPhone 7 and HTC 10.
6. The current consumption values reflect the average current consumption.
7. IS2066B-237 is completely shut down; 5V adapter connected to ADAP_IN; current measured across ADAP_IN.
8. Please contact Microchip for a detailed test report on IS2066B current consumption.

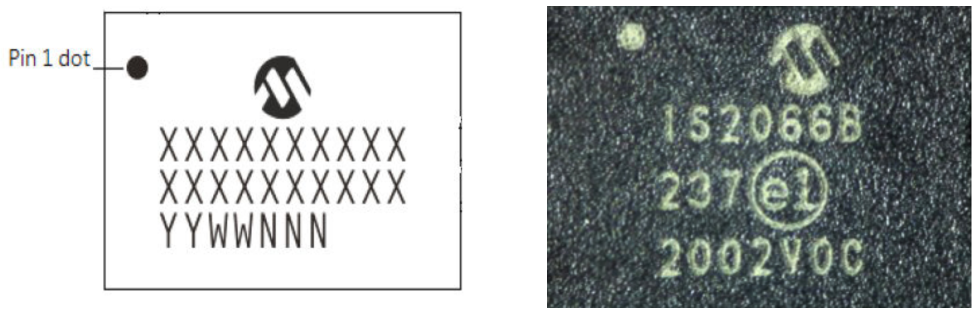
9. Packaging Information

This section details the package marking information, package details and footprint dimensions of the IS2066B SoC.

9.1 Package Marking Information

The following figures illustrate the package marking information for the IS2066B.

Figure 9-1. Package Marking Information



XXX: Chip serial number version and

(e1) Pb-free JEDEC designator for SAC305

YY: Year code (last 2 digits of calendar year)
WW: Week code (week of January 1 is week "01")
NNN: Alphanumer traceability code

9.2 IS2066B Package Details

The following figures illustrate the package details of the IS2066B.

Note: For the most current package drawings, see the Microchip Packaging Specification located at www.microchip.com/packaging.

Figure 9-2. 50-Ball Very Thin Fine Pitch Ball Grid Array (3KX) - 5x3.5 mm Body [VFBGA]

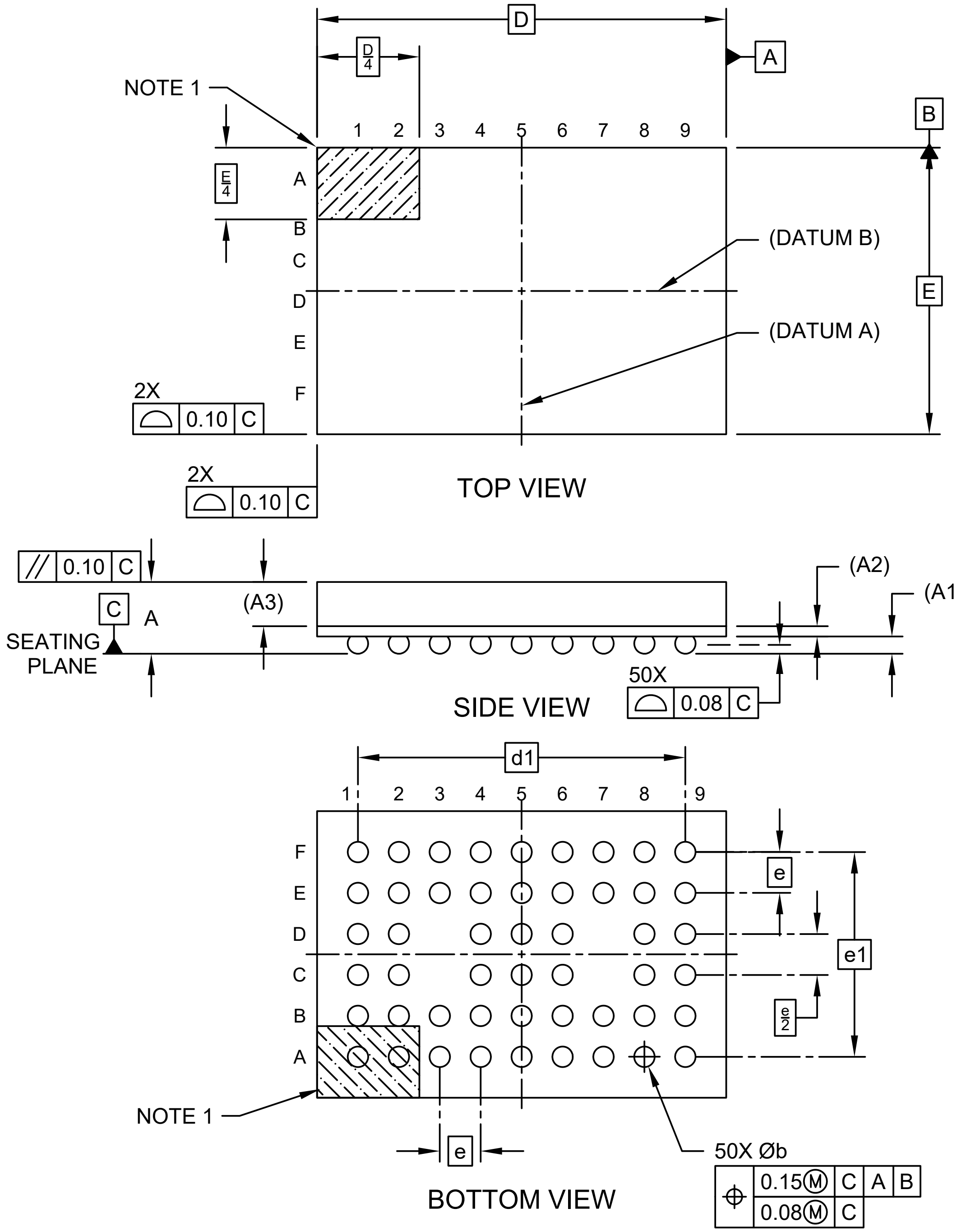
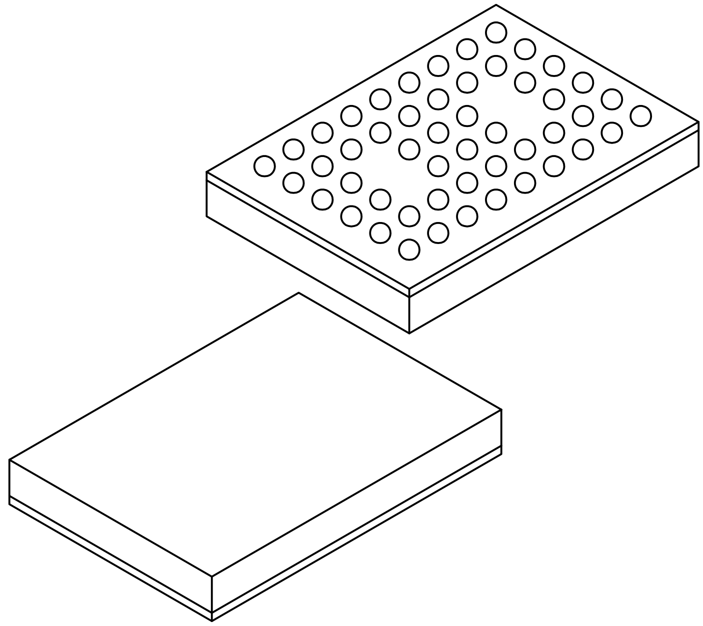


Figure 9-3. 50-Ball Very Thin Fine Pitch Ball Grid Array (3KX) – 5x3.5 mm Body [VFBGA] – Contd.



		Units	MILLIMETERS		
		Dimension Limits	MIN	NOM	MAX
Number of Terminals	N			50	
Pitch	e			0.50 BSC	
Overall Height	A		-	-	0.90
Standoff	A1		0.11	-	0.21
Substrate Thickness	A2			0.125 REF	
Mold Cap Thickness	A3			0.54 REF	
Overall Length	D			5.00 BSC	
Overall Pitch	D2			4.00 BSC	
Overall Width	E			3.50 BSC	
Overall Pitch	E2			2.50 BSC	
Terminal Width	b		0.20	0.25	0.30

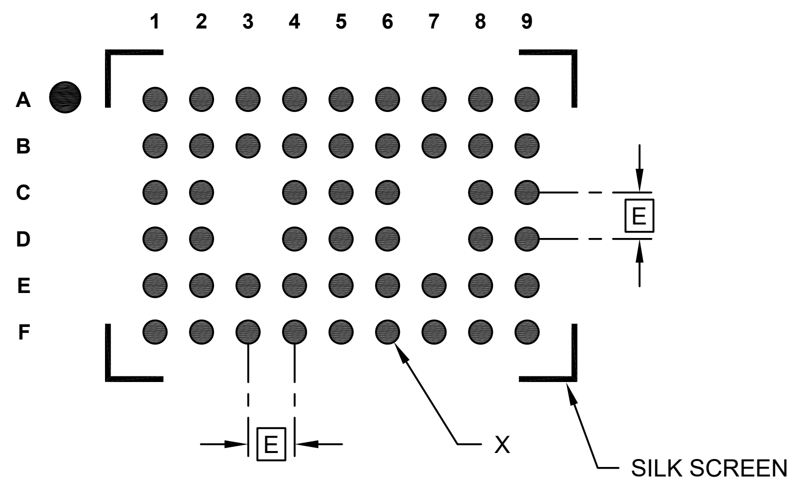
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Figure 9-4. IS2066B Recommended Land Pattern



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Diameter (X50)	X		0.25	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

10. Reflow Profile and Storage Condition

This section describes the Solder Reflow Recommendation and Storage Condition of the IS2066B SoC.

10.1 Solder Reflow Recommendation

For the soldering reflow recommendations, refer to the Microchip Technology application note *AN233 Solder Reflow Recommendation* (DS00233) at http://ww1.microchip.com/downloads/en/appnotes/00233d.pdf.

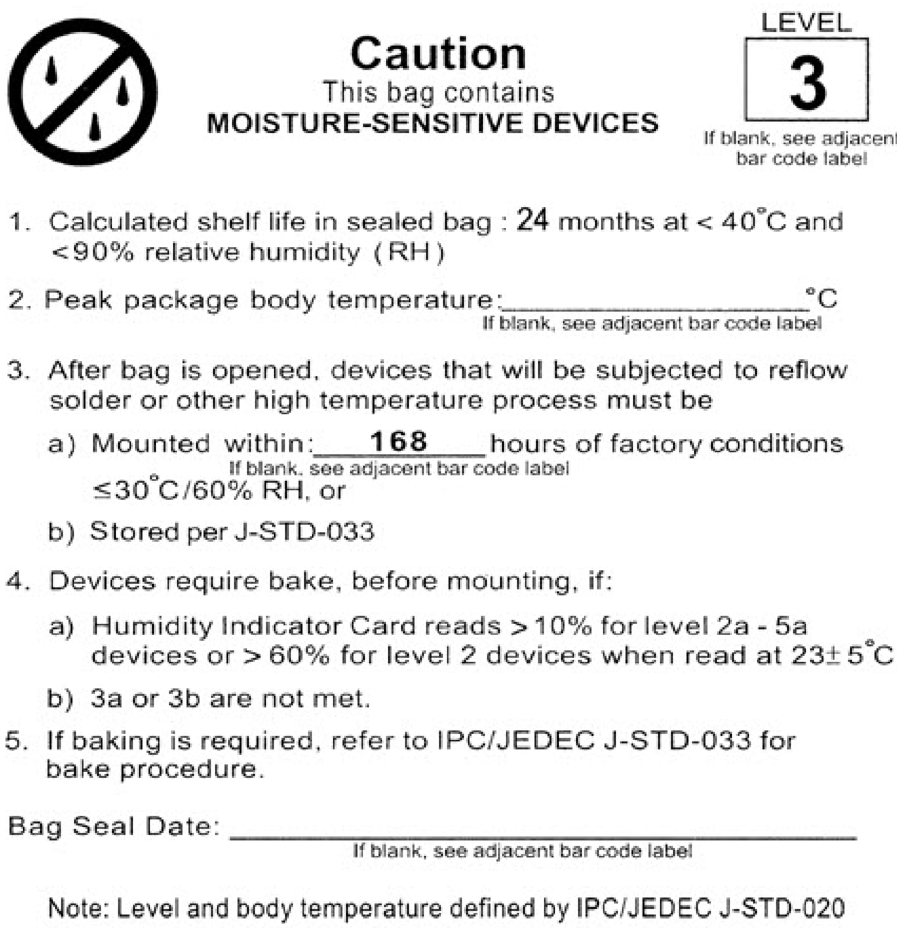
10.2 Storage Condition

Users must follow these specific storage conditions for the IS2066B SoC.

- Calculated shelf life in the sealed bag: 24 months at <40℃ and <90% Relative Humidity (RH)
- Once the bag is opened, devices that are subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions, that is <30℃ /60% RH

The following figure illustrates the IS2066B SoC bag label details.

Figure 10-1. Storage Conditions Caution Label



11. Ordering Information

The following table provides the ordering information for the IS2066B SoC.

Table 11-1. Ordering Information

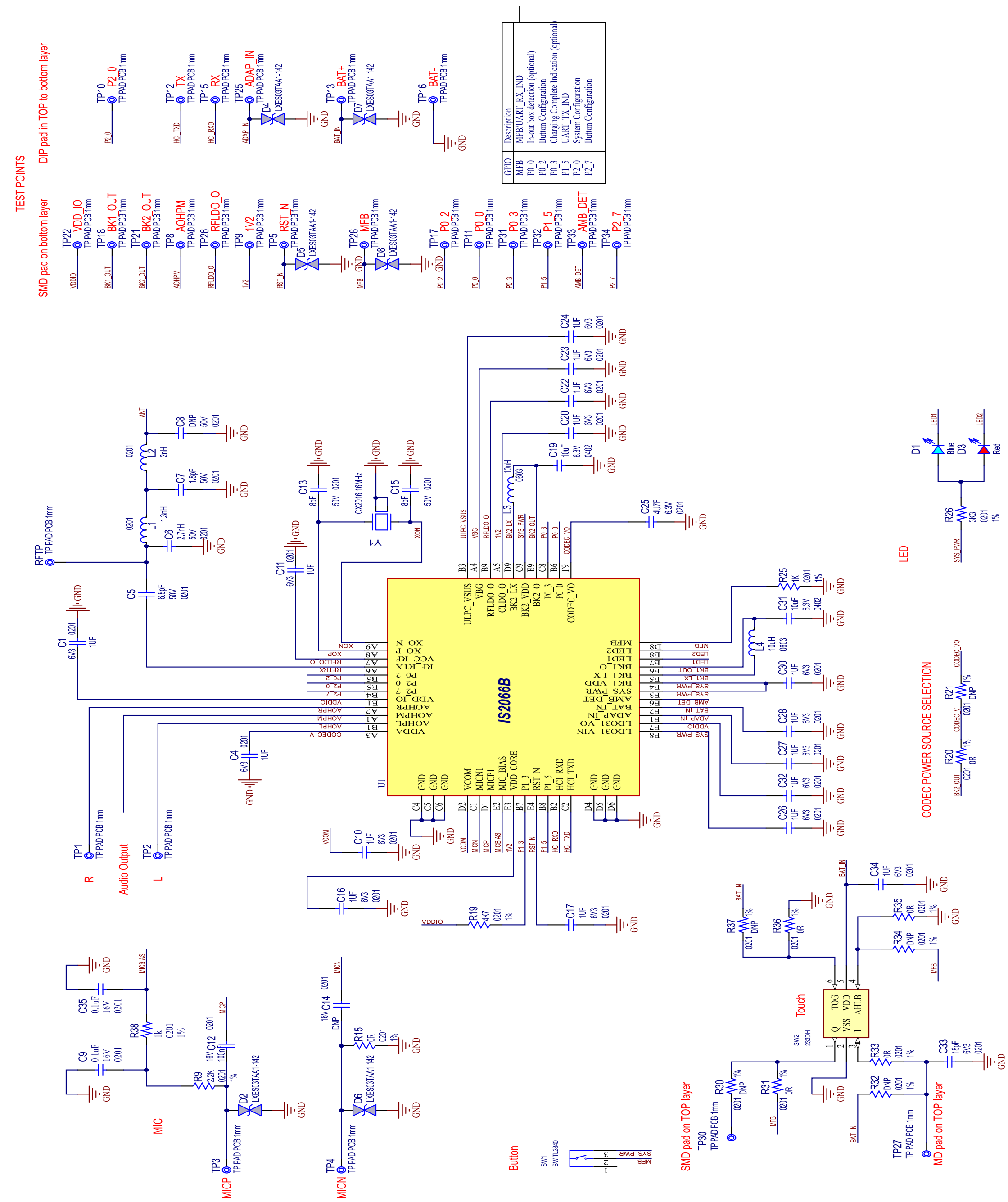
Device	Description	Package	Part Number
IS2066B	Bluetooth 5.0, Low Power ROM SoC, 1 microphone, Analog output	5x3.5x0.9 mm, 50-BGA package	IS2066B-237

Note: The IS2066B SoC is purchased through a Microchip representative. Go to http://www.microchip.com/ for ordering information.

12. Reference Circuit

This section provides the reference schematics of the IS2066B used in a stereo headset application. The following figures illustrate the IS2066B reference schematics for the WST earbud application.

Figure 12-1. IS2066B Reference Circuit for WST Left Earbud



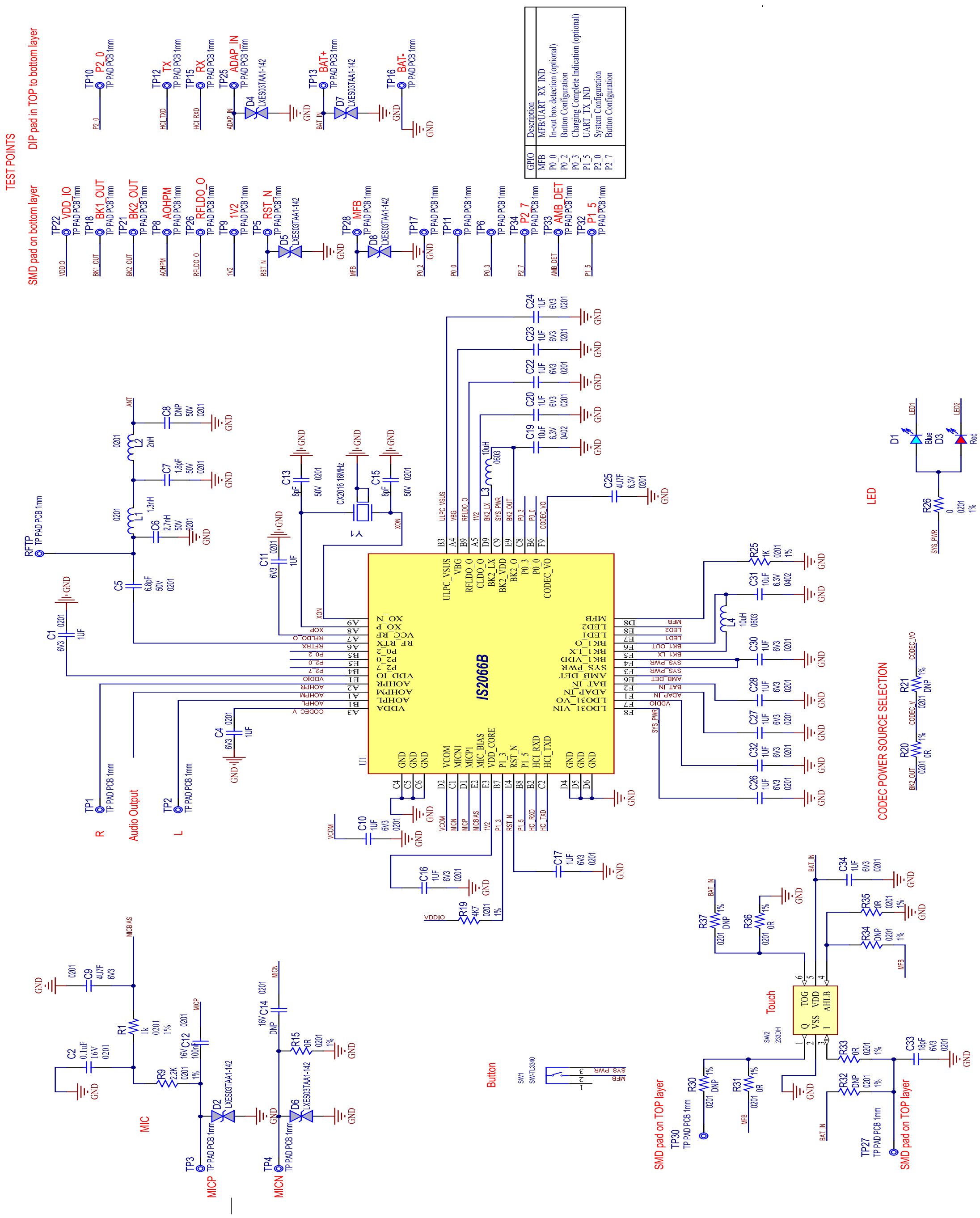


Figure 12-2. IS2066B Reference Circuit for WST Right Earbud

13. Document Revision History

Revision	Date	Section	Description
C	03/2020	Document	Minor updates and edits
		8. Electrical Characteristics	Updated Table 8-12
		11. Ordering Information	Updated
		12. Reference Circuit	Updated the following figures • Figure 12-1 • Figure 12-2
		9.1 Package Marking Information	Updated the following figure • Figure 9-1
B	11/2019	Document	Minor updates and edits
		2.2 Codec	Dynamic range values updated in the Table 2-1
		5.4 Switching Regulator	Updated
		6.5 EEPROM Content Corruption During Power Drop	New section
		12. Reference Circuit	Updated • Figure 12-1 • Figure 12-2
A	05/2019	Document	Initial revision

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