ML7125-001/ML7125-002

Bluetooth® Smart LSI supporting Core Specification v4.1

■ Overview

ML7125-00X (-001/-002) is a series of Bluetooth® Smart LSI integrating Ultra Low Power RF, Baseband, microproccessor core and peripherals, which has Bluetooth® LE compliant 2.4GHz band radio communication capability. ML7125-00X is supporting Bluetooth® core specification v4.1, it is suitable for applications such as Wrist Watch, Remote Controller or PC peripherals. The differences in ML7125-00X series are operating mode that is supported by each product.

■ Features

- Bluetooth® SIG Core Spec v4.1 compliant, supporting master and slave role function
- Ultra Low Power RF block
- Cortex-M0+ microprocessor core integrated
- 96KB ROM (CODE_ROM) for Program code.
- 28KB RAM (CODE/DATA_RAM) for user program and data processing
- Memory retention function while the chip is in deep sleep mode with partial power shutdown (8KB/28KB scalable)
- Bluetooth® LE single mode compliant Baseband controller
- 3 Operating modes
  - BACI (Bluetooth Application Controller Interface) mode : Lapis original application interface to HOST MCU.*1
  - HCI (Host Controller Interface) mode : Bluetooth® standard interface between controller (LL+RF-PHY) and protocol stack.
  - Application mode : Download user application into embedded SRAM, two type of application are supported, “Standalone type”, “Add-on type”. *2
- Simultaneous connection up to 2 devices. (support all master/slave combinations)*1
- UART interface
- SPI (Slave mode) interface *1
- I2C (Master & Slave) interface
- GPIO ports
- On chip Regulator Linear regulator (MAIN Regulator) or Switching regulator
- Low Power Operating mode
- Single power supply 1.6V to 3.6V
- Operating Temperature -20 deg.C to +75deg.C
- Current Consumptions
  - Deep Sleep Mode with external Low Power Clock
    0.35μA *3, 0.90μA *4
  - Deep Sleep Mode with internal Low Power Clock oscillator circuit)
    2.60μA(TYP) *3, 3.15μA(TYP) *4
  - Idle Mode below 2.0mA(TYP) (Memory retention, 26MHz clock enabled)
  - Active TX below 6.7mA(TYP) (power supply using Switching regulator)
  - Active RX below 6.2mA(TYP) (power supply using Switching regulator)
- Package 7row x 10column pad WCSP (0.4mm pad pitch LGA type, 4.69 x 3.12)
- Pb Free, RoHS compliant

*1 : Supported by ML7125-001 only
*2 : Supported by ML7125-002 only
*3 : APPLICATION RAM no retention
*4 : APPLICATION RAM retention
Note : Unless otherwise stated, features listed above supported by both products.(*1*2)

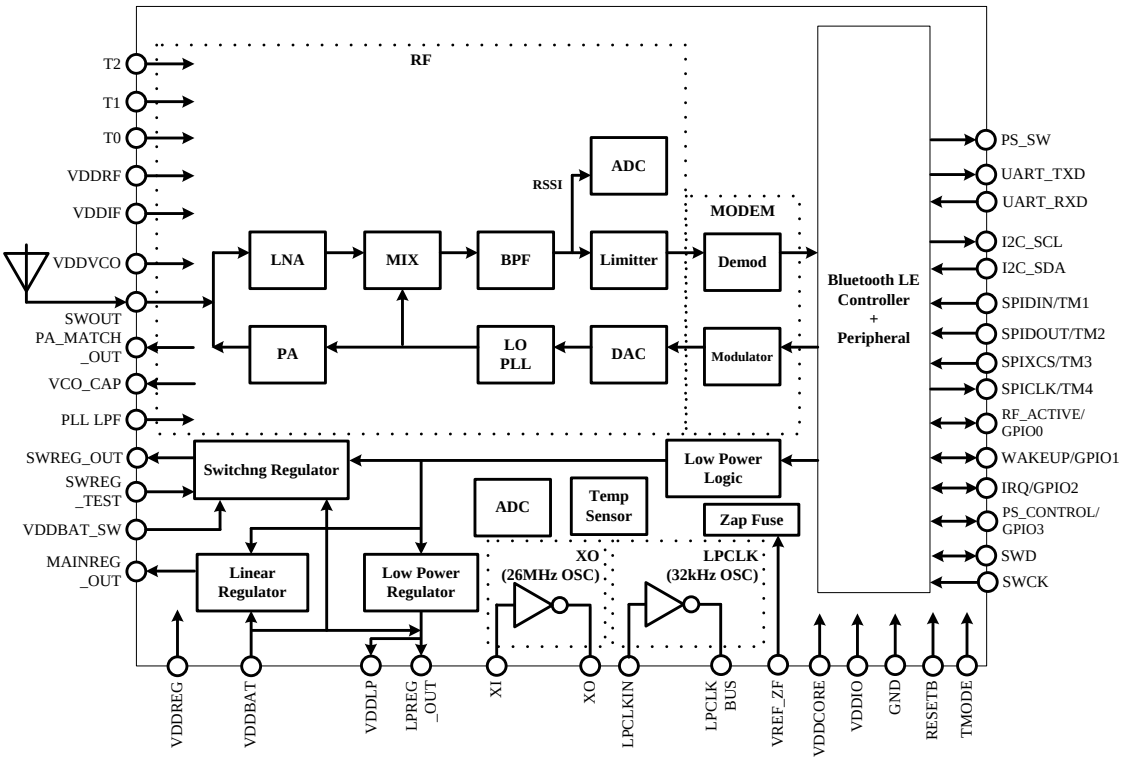
ROHM SEMICONDUCTOR

■ Support Function List

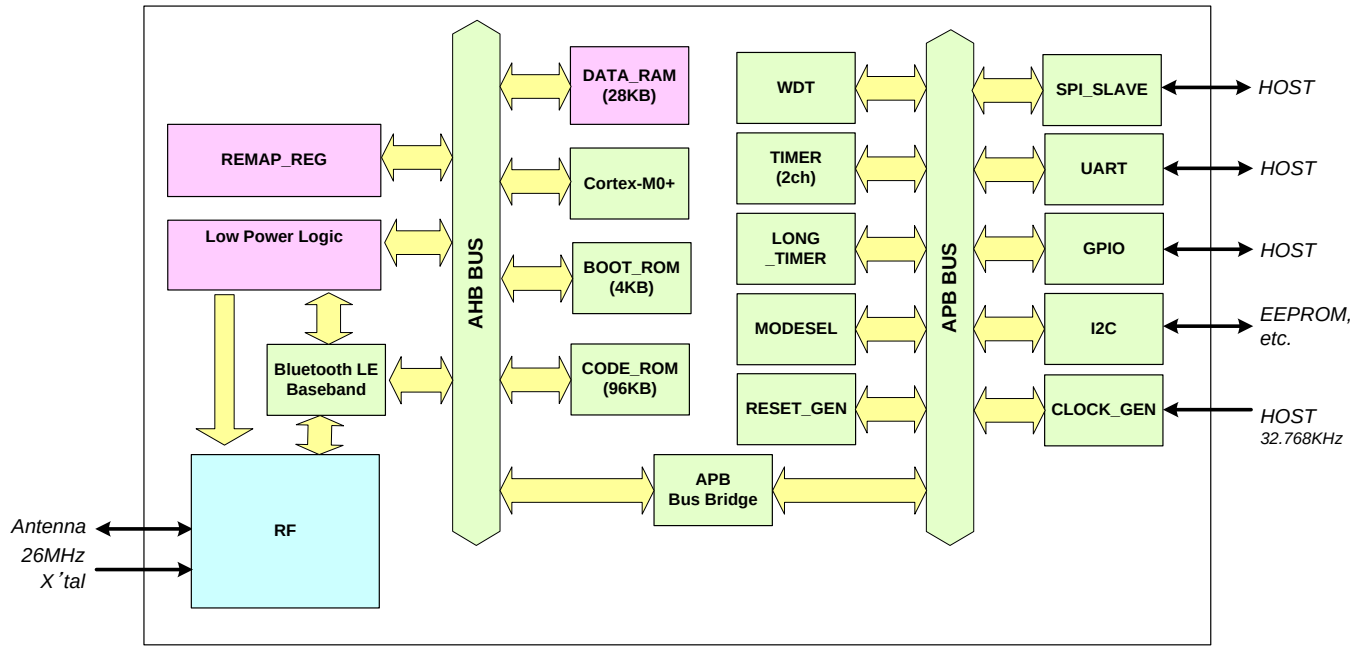
Function	ML7125-001	ML7125-002
Role	Master/Slave	Slave
Number of connectable device(s)	2	1
BACI Mode	○	×
HCI Mode	○	○
Application Mode	×	○
UART interface	○	○
SPI interface	○	×
I2C interface	○	○
GPIO	None	4CH
Host interface	BACI	AT-Command (Lapis original)

■ Block Diagram

- 1chip overview



- Bluetooth® LE Platform



■ PIN ASSIGNMENT

	K	J	H	G	F	E	D	C	B	A
7	MAINREG_ OUT	VDDREG	VDDBAT	LPREG_OUT	VDDIF	LPCLKIN	VDDLP	GND	SWREG_OUT	VDDBAT_SW
6	GND	T1	T0	T2	GND	LPCLKBUS	RESETB	TMODE	SWREG_TEST	GND
5	SWOUT	−	GND	GND	GND	GND	GND	GND	SWD	SWCK
4	−	VDDRF	GND	GND	GND	GND	GND	GND	PS_CONTROL/ GPIO3	IRQ/ GPIO2
3	PA_MATCH_ OUT	VCO_CAP	GND	GND	GND	GND	GND	GND	WAKEUP/ GPIO1	RF_ACTIVE/ GPIO0
2	−	VDDVCO	GND	GND	PS_SW	SPICLK/ TM4	SPIDOUT/ TM2	I2C_SDA	I2C_SCL	VDDIO
1	PLLLPF	VDDCORE	XI	XO	VREF_ZF	SPIXCS/ TM3	SPIDIN/ TM1	UART_RXD	UART_TXD	GND

BOTTOM VIEW

■ PIN definition

I/O definitions

I_{RF}	:	RF input and output
I	:	Digital input
I_{SH}	:	Low-Power Clock input
Ipd	:	Digital input with pull-down resistor
I_A	:	Analog input
I_{AH}	:	Analog input support 3V
I_{SH}	:	Low-Power Clock input
X_{SH}	:	X'tal pin for Low-Power Clock
X_M	:	X'tal pin for Master Clock
O_2	:	Digital output with 2mA load capability
B2	:	Digital inout with 2mA load capability
B2pd	:	Digital inout with 2mA load capability with pull-down resistor
O_A	:	Analog output

● RF analog pins

No	Pin Name ML7125-001	Pin Name ML7125-002	Status in reset	I/O	Active Level	Function
K5	SWOUT	*1	Hi-Z	I_{RF}	---	RF signal RX/TX inout
H6	T0	*1	Hi-Z	I_{AH}	---	Test input signal
J6	T1	*1	Hi-Z	$I_{AH,}$	---	Test input signal
G6	T2	*1	Hi-Z	$I_{AH,}$	---	Test input signal
K1	PLLLPF	*1	Hi-Z	O_A	---	PLL Loop Filter
K3	PA_MATCH_ OUT	*1				Output for PA matching circuit
J3	VCO_CAP	*1				Output for VCO capacitor

*1: Same as ML7125-001

● XO, LPCLK pins

No	Pin Name ML7125-001	Pin Name ML7125-002	Status in reset	I/O	Active Level	Function
H1	XI	*1	Hi-Z	X_M	---	Input pin for Master clock oscillator block
G1	XO	*1	Hi-Z	X_M	---	Outputpin for Master clock oscillator block
E6	LPCLKBUS	*1	0V	X_{SH}	---	Low power clock Xtal output
E7	LPCLKIN	*1	I_{SH}	X_{SH}, I_{SH}	---	Low power clock/Xtal input

*1: Same as ML7125-001

● SPI pins

No	Pin Name ML7125-001	Pin Name ML7125-002	Status in reset	I/O	Active Level	Function
D1	SPIDIN	TM1	Input	I	---	SPIDIN : SPI SLAVE Data input TM1 : Test mode definition input
D2	SPIDOUT	TM2	Input	B2pd	---	SPIDOUT : SPI SLAVE Data output TM2 : Test mode definition input
E1	SPIXCS	TM3	Input	I	Low	SPIXCS : SPI SLAVE Chip Select TM3 : Test mode definition input

E2	SPICLK	TM4	Input	I	---	SPICLK : SPI SLAVE Clock TM4 : Test mode definition input

- UART pins

No	Pin Name ML7125-001	Pin Name ML7125-002	Status in reset	I/O	Active Level	Function
B1	UART_TXD	*1	High output	O_2	---	UART TXD output
C1	UART_RXD	*1	input	B_{2pd}	---	UART RXD input

*1: Same as ML7125-001

- I2C pins

No	Pin Name ML7125-001	Pin Name ML7125-002	Status in reset	I/O	Active Level	Function
B2	I2C_SCL	*1	Input	B_2	---	I2C_SCL
C2	I2C_SDA	*1	Input	B_2	---	I2C_SDA

*1: Same as ML7125-001

- GPIO pins

No	Pin Name ML7125-001	Pin Name ML7125-002	Status in reset	I/O	Active Level	Function
A3	RF_ACTIVE	GPIO0	Low output	B_2	---	RF_ACTIVE : Status pin indicates RF access activity. GPIO0 : GPIO inout
B3	WAKEUP	GPIO1	Input	B_2	---	WAKEUP : Control pin from HOST to wakeup ML7125-001 GPIO1 : GPIO inout/
A4	IRQ	GPIO2	High output	B_2	---	IRQ : Status pin indicates interruption reason taken place in ML7125-001 GPIO2 : GPIO inout
B4	PS_CONTROL	GPIO3	Low output	B_2	---	PS_CONTROL : Status pin indicates deep sleep mode status. GPIO3 : GPIO inout

- Debugger pins

No	Pin Name ML7125-001	Pin Name ML7125-002	Status in reset	I/O	Active Level	Function
B5	SWD	*1	input	B_2	---	SWD data inout
A5	SWCK	*1	input	I	---	SWD clock input

*1: Same as ML7125-001

- Miscellaneous pins

No	Pin Name ML7125-001	Pin Name ML7125-002	Status in reset	I/O	Active Level	Function

D6	RESETB	*1	input	I_S	Low	Reset input (Low = Reset)
F1	VREF_ZF	*1	---	---	---	Test input (fix to low)
C6	TMODE	*1	input	I	---	TESTMODE input (Low = normal mode)
F2	PS_SW	*1	output	O_2	---	Status pin indicates deep sleep mode status. (Control for Powe switch)

*1: Same as ML7125-001

- Regulator pins

No	Pin Name ML7125-001	Pin Name ML7125-002	Status in reset	I/O	Active Level	Function
K7	MAINREG_OUT	*1	1.35V output	---	---	Linear Regulator output Note) please do not shortcut this pin to GND, IC may be damaged.
G7	LPREG_OUT	*1	0.90V output	---	---	Low Power Regulator output
B7	SWREG_OUT	*1	1.35V output	---	---	Switching Regulator output
J7	VDDREG	*1	1.35V/3.3V input	---	---	Feedback input for Switching Regulator and Power supply input for Linear Regulator.
B6	SWREG_TEST	*1	---	---	---	Switching Regulator test pin

*1: Same as ML7125-001

- Power Supply pin

No	Pin Name ML7125-001	Pin Name ML7125-002	Status in reset	I/O	Active Level	Function
A7	VDDBAT_SW	*1	---	---	---	Power supply from Battery (=VDDIO) (1.6V to 3.6V)
H7	VDDBAT	*1	---	---	---	Power supply from Battery (=VDDIO) (1.6V to 3.6V)
A2	VDDIO	*1	---	---	---	Power supply for digital IO (1.6V to 3.6V)
J4	VDDRF	*1	---	---	---	Power supply for RF block (1.35V)
F7	VDDIF	*1	---	---	---	Power supply for IF block (1.35V)
J2	VDDVCO	*1	---	---	---	Power supply for RF-VCO (1.35V)
J1	VDDCORE	*1	---	---	---	Power supply for digital core (1.35V)
D7	VDDLP	*1	---	---	---	Power supply for low power digital core (1.35V)
C7	GND	*1	---	---	---	GND (Mandatory)
K6	GND	*1	---	---	---	GND (Mandatory)
F6	GND	*1	---	---	---	GND (Mandatory)
A6	GND	*1	---	---	---	GND (Mandatory)
H5	GND	*1	---	---	---	GND (Mandatory)
G5	GND	*1	---	---	---	GND
F5	GND	*1	---	---	---	GND
E5	GND	*1	---	---	---	GND
D5	GND	*1	---	---	---	GND
C5	GND	*1	---	---	---	GND
H4	GND	*1	---	---	---	GND (Mandatory)
G4	GND	*1	---	---	---	GND
F4	GND	*1	---	---	---	GND

E4	GND	*1	---	---	---	GND
D4	GND	*1	---	---	---	GND
C4	GND	*1	---	---	---	GND
H3	GND	*1	---	---	---	GND (Mandatory)
G3	GND	*1	---	---	---	GND
F3	GND	*1	---	---	---	GND
E3	GND	*1	---	---	---	GND
D3	GND	*1	---	---	---	GND
C3	GND	*1	---	---	---	GND
H2	GND	*1	---	---	---	GND (Mandatory)
G2	GND	*1	---	---	---	GND (Mandatory)
A1	GND	*1	---	---	---	GND (Mandatory)

*1: Same as ML7125-001

- Unused pins

Followings are recommendation for pins are not used.

No	Pin Name	Recommendation
E6	LPCLKBUS	Open
K1	PLLLPF	Open (Optionally, PLL loop filter may be required)
F1	VREF_ZF	Fix to GND
D1	SPIDIN/TM1	Fix to VDDIO
D2	SPIDOUT/TM2	Open
E1	SPIXCS/TM3	Fix to VDDIO
E2	SPICLK/TM4	Fix to VDDIO
B1	UART_TXD	Open
C1	UART_RXD	Fix to GND (See operating mode section)
B2	I2C_SCL	Fix to VDDIO
C2	I2C_SDA	Fix to GND
A3	RF_ACTIVE/GPIO0	Open
B3	WAKEUP/GPIO1	Fix to VDDIO or GND (See operating mode section)
A4	IRQ/GPIO2	Open
B4	PS_CONTROL/GPIO3	Open
F2	PS_SW	Open
H6	T0	Open
B5	SWD	Fix to GND
A5	SWCK	Fix to GND
J6	T1	Open
G6	T2	Open

Note

Leaving input pins open with Hi-Z status, current consumption will be increased. It is highly recommended that input or in-out pins should not be left open.

■ Electrical Characteristics

● Absolute Maximum Rating

Item	Symbol	Condition	Rating	Unit
Power supply 3.3V (*1)	V_{DDHV1} V_{DDHV2}	Ta = −20 to +75 deg.C GND= 0 V (*3) VDDRF=VDDVCO =VDDCORE, VDDBAT= VDDBAT _SW, =VDDIO,	–0.3 to +4.6	V
Power supply 1.35V (*2)	V_{DDLV}		–0.3 to +1.8	V
Digital input voltage (*4)	V_{DIN}		–0.3 to V_{DDHV*}+0.3	V
Digital output voltage (*5)	V_{DO}		–0.3 to V_{DDHV*}+0.3	V
Analog IO voltage (*6)	V_A		–0.3 to V_{DDLV}+0.3	V
Analog HV IO voltage (*7)	V_{AH}		–0.3 to V_{DDHV*}+0.3	V
Digital IO load current (*4)(*5)	I_{DO}		–10 to +10	mA
Analog IO current (*6)(*7)	I_A		–2 to +2	mA
Power Dissipation	P_D		1.0	W
Storage temperature	T_{stg}	–	–55 to +125	deg.C

(*1) VDDBAT, VDDBAT_SW, VDDIO pins
(*2) VDDRF, VDDVCO, VDDCORE,
(*3) GND: GND pin (Package GND)
(*4) IO pins with I, I_{PD}, B_2 symbol in pin definition
(*5) IO pins with O_2,B_2, B_{2pd} symbol in pin definition
(*6) IO pins with I_A, O_A, X_M symbol in pin definition
(*7) IO pins with I_{AH}, I_{SH}, X_{SH}, symbol in pin definition

● Recommended Operating Conditions

Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply	V_{DDHV1}	VDDIO pin （VDDBAT, VDDBAT_SW≧ VDDIO）	1.60	3.00	3.60	V
Power Supply (Linear Regulator used)	V_{DDHV2_1}	VDDBAT,VDDBAT_SW pin （VDDBAT, VDDBAT_SW≧ VDDIO）	1.60	3.00	3.60	V
Power Supply (Switching Regulator used)	V_{DDHV2_2}	VDDBAT,VDDBAT_SW pin （VDDBAT, VDDBAT_SW≧ VDDIO）	2.00	3.00	3.60	V
Power Supply (IDLE/RF_ACTIVE)	V_{DDLCV1}	VDDCORE pin	1.25	1.35	1.55	V
	V_{DDLRV1}	VDDRF pin, VDDVCO pin	1.25	1.35	1.55	V
Power Supply (Deep Sleep)	V_{DDLCV2}	VDDCORE pin	0.70	0.90	1.00	V
	V_{DDLRV2}	VDDRF pin, VDDVCO pin	-	Hi-Z	-	V
Ambient Temperature	T_a	–	–20	+25	+75	°C
Rising time digital input pins	t_{IR1}	Digital input pins	–	–	20	ns
Falling time digital input pins	t_{IF1}	Digital input pins	–	–	20	ns
Load capacitance digital	C_{DL}	Digital output pins	–	–	20	pF
Master Clock (26 MHz) crystal oscillator frequency	F_{MCK1}	Connect cristal oscillator between XI－XO pins （*1）, (*2)	–40 ppm	26	+40 ppm	MHz
Low Power Clock (32.768 kHz) crystal oscillator frequency	F_{LPCK1}	LPCLKIN pin, LPCLKBUS pin (*2)	–500 ppm	32.768	+500 ppm	kHz
Low Power Clock Input Duty Ratio	D_{LPCK1}	External input from LPCLKIN, LPCLKBUS pin left OPEN	30	50	70	%
RF Channel frequency (*3)	F_{RF}	SWOUT pin	2402	–	2480	MHz
RF input level	P_{RFIN}		-70	–	-10	dBm

(*1) Cristal oscillator is recommended
(*2) The cristal should be used the one that meet the specification include peripheral circuit.
(*3) Frequency range F = 2402 + 2 x k [MHz] here k=0, 1,2,…,39.

- Current consumption

<<Linear Regulator case >>

(Ta = –20 to +75 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Current Consumption	IDD_DSM1	Deep Sleep State (External Low Power Clock) *1	---	0.35	---	μA
	IDD_DSM2	Deep Sleep State (Internal Low Power Clock oscillator) *1	---	2.60	---	μA
	IDD_IDLE	Idle State	---	3.2	---	mA
	IDD_RX1	RF RX State (High Sense Mode)	---	10.8	---	mA
	IDD_RX2	RF RX State (Mid Sense Mode)	---	10.5	---	mA
	IDD_RX3	RF RX State (Low Sense Mode)	---	10.0	---	mA
	IDD_TX1	RF TX State (TX power at +4dBm)	---	17.1	---	mA
	IDD_TX2	RF TX State (TX power at 0dBm)	---	11.4	---	mA
	IDD_TX3	RF TX State (TX power at -18dBm)	---	7.4	---	mA

*1 Additional 0.55μA required in case of APPLICATION RAM retention

<<Switching Regulator case >>

(Ta = –20 to +75 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Current Consumption	IDD_DSM1	Deep Sleep State (External Low Power Clock) *1	---	0.35	---	μA
	IDD_DSM2	Deep Sleep State (Internal Low Power Clock oscillator) *1	---	2.60	---	μA
	IDD_IDLE	Idle State	---	2.0	---	mA
	IDD_RX1	RF RX State (HighSense Mode)	---	6.4	---	mA
	IDD_RX2	RF RX State (Mid Sense Mode)	---	6.2	---	mA
	IDD_RX3	RF RX State (Low Sense Mode)	---	5.8	---	mA
	IDD_TX1	RF TX State (TX power at +4dBm)	---	10.3	---	mA
	IDD_TX2	RF TX State (TX power at 0dBm)	---	6.7	---	mA
	IDD_TX3	RF TX State (TX power at -18dBm)	---	4.3	---	mA

*1 Additional 0.55μA required in case of APPLICATION RAM retention

● DC characteristics

(Ta = –20 to +75 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
H level Voltage Input	V_{IH1}	(*1) (*2) (*5) (*6)	V_{DDIO} X0.7	–	V_{DDIO}	V
L level Voltage input	V_{IL1}	(*1) (*2) (*5) (*6)	0	–	V_{DDIO} X0.3	V
LPCLKIN pin H level Voltage Input	V_{IH2}	(*3)	1	–	V_{DDIO}	V
LPCLKIN pin L level Voltage input	V_{IL2}	(*3)	0	–	0.3	V
Input leak current	I_{IH1}	$V_{IH} = V_{DDIO}$ (*1) (*5)	–1	–	1	μA
	I_{IH2}	$V_{IH} = V_{DDIO}$ (*2)(*6)	5	–	250	μA
	I_{IL1}	V_{IL} = 0 V (*1) (*2) (*5)(*6)	–1	–	1	μA
Tri-state output leak current	I_{OZH}	$V_{OH} = V_{DDIO}$ (*4) (*5)	–1	–	1	μA
	I_{OZL}	V_{OL} = 0 V (*4) (*5)	–1	–	1	μA
H level Voltage Output	V_{OH1}	I_{OH} = –2mA (*4) (*5)(*6) $V_{DDIO} = V_{DDBAT}$ = 2.0V to 3.6V	V_{DDIO} × 0.75	–	V_{DDIO}	V
	V_{OH2}	I_{OL} = –1mA (*4) (*5)(*6) $V_{DDIO} = V_{DDBAT}$ = 1.6V to 2.0V	V_{DDIO} × 0.65	–	V_{DDIO}	V
L level Voltage Output	V_{OL1}	I_{OH} = 2mA (*4) (*5)(*6) $V_{DDIO} = V_{DDBAT}$ = 2.0V to 3.6V	0	–	V_{DDIO} × 0.25	V
	V_{OL2}	I_{OL} = 2mA (*4) (*5)(*6) $V_{DDIO} = V_{DDBAT}$ = 1.6V to 2.0V	0	-	V_{DDIO} × 0.35	V
Regulator output voltage	V_{MAIN_OUT}	MAINREG_OUT pin	1.25	1.35	1.55	V
	V_{SW_OUT}	SWREG_OUT pin	1.25	1.35	1.55	V
	V_{LP_OUT}	LPREG_OUT pin	0.70	0.90	1.10	V
Input pin capacitance	C_{IN}	F=1MHz (*1) (*2) (*4) (*5)	–	8	–	pF

(*1) IO pins with I symbol in pin definition
(*2) IO pins with I_{PD} symbol in pin definition
(*3) IO pins with I_{SH} symbol in pin definition
(*4) IO pins with O_2 symbol in pin definition
(*5) IO pins with B_2 symbol in pin definition
(*6) IO pins with B_{2pd} symbol in pin definition

● RF Characteristics

(Ta = –20 to +75 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
TX						
TX power	P_{OUT1}	TX- 4dBm setting *1	--	4	–	dBm
	P_{OUT2}	TX- 0dBm setting	–	0	–	dBm
	P_{OUT3}	TX- -18dBm setting	–	-18	–	dBm
TX power control	P_{STEP1}	The number of power control step in TX-Normal mode	–	4	–	Step
	P_{STEP2}	Power control step gain in TX-Normal mode	–	6	–	dB
Centre Frequency tolerance	F_{CERR}	Master Clock tolerance < 40 ppm	–40	0	40	Ppm
Modulation data rate	D_{RATE}	–	–	1	–	Mbps
Modulation index	F_{IDX}	–	0.45	0.50	0.55	–
Bandwidth-bit rate products BT	BT	GFSK	–	0.5	–	–
Modulation characteristics	F_{1avg}	Frequency deviation of 10101010 pattern	225	250	275	kHz
	F_{RATE}	Frequency deviation ratio between 10101010 and 00001111 sequence	80	–	–	%
	F_{DELTA}	Minimum Frequency Deviation	185	–	–	kHz
In-band spurious	P_{OS1}	2MHz apart from carrier frequency in a 1MHz bandwidth	–	–	-20	dBm
	P_{OS2}	3MHz apart from carrier frequency in a 1MHz bandwidth	–	–	-30	dBm
Out-band spurious	P_{OB}	ARIB STD-T66 (RBW=VBW=100kHz)	–	–	-26	dBm
Ramping Up/Down	T_{RMP}	Time required for Ramping up and Ramping down	0	2	8	μs
RX						
Receiver Sensitivity	P_{SENS1}	PER = 30.8% (High Sense Mode)	–	-88	-70	dBm
	P_{SENS2}	PER = 30.8% (Mid Sense Mode)	–	-85	-70	dBm
	P_{SENS3}	PER = 30.8% (Low Sense Mode)	–	–	-70	dBm
Interference performance PER<30.8% Wanted signal :-67dBm Interfering signal : modulated signal (1*)(*2)(*3)	CI_{CO}	Co-channel interference C/I	21	–	–	dB
	CI_{S1}	Adjacent (1MHz) interference C/I	15	–	–	dB
	CI_{S2}	Adjacent (2MHz) interference C/I	-17	–	–	dB
	CI_{S3}	Adjacent (>=3MHz) interference C/I	-27	–	–	dB

	CI_{IMG}	Image frequency interference (-4MHz) C/I	-9	–	–	dB
	CI_{IMGS1}	Adjacent (1MHz) interference to image frequency (-3MHz,-5MHz)) C/I	-15	–	–	dB
Out of band blocking PER<30.8% Wanted signal :-67dBm Interfering signal:CW (*1) (*2) (*3)	P_{BLK1}	30MHz to 2000MHz BW 10MHz	-30	–	–	dBm
	P_{BLK2}	2003 to 2399MHz BW 3MHz	-35	–	–	dBm
	P_{BLK3}	2484 to 2997MHz BW 3MHz	-35	–	–	dBm
	P_{BLK4}	3000MHz to 12.75GHz BW 25MHz	-30	–	–	dBm
Intermodulation PER<30.8% Wanted signal :-64dBm (*1)(*3)	P_{IM}	CW interering signal +/-3MHz Modulated interfering signal +/-6MHz or CW interfering signal +/-4MHz Modulated interfering signal +/-8MHz or CW interfering signal +/-5MHz Modulated interfering signal +/-10MHz	-50	–	–	dBm
Spurious Emission level (ARIB STD-T66)	P_{SPR1}	30 MHz ～ 1 GHz (RBW=VBW=100kHz)	–	–	-54	dBm
	P_{SPR2}	1 GHz ～ 12.75 GHz (RBW=VBW=100kHz)	–	–	-47	dBm
Maximum input level(*1)	P_{RXMAX}	PER = 30.8% (*1)	–	–	-10	dBm
RSSI detection range (*1)(*3)	$P_{RSSIMAX}$	Upper	-40	–	–	dBm
	$P_{RSSIMIN}$	Lower	–	–	-85	dBm

(*1) Condition: Ta = 25deg.、VDDHV1 = VDDHV2= 3.0V
(*2) Follow RCV-LE/CA/04/C test spec of Bluetooth SIG
(*3) exclude Low Sense Mode

● Analog Characteristics・Regulators

(Ta = –20 to +75 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Internal Regulator						
Input Voltage Range	V_{REG1IN}	Linear Regulator is used	1.60	3.00	3.60	V
	V_{REG2IN}	Switching Regulator is used	2.00	3.00	3.60	V
Output Voltage	$V_{REG2OUT1}$	Idle, Active mode	1.25	1.35	1.55	V
	$V_{REG2OUT1}$	Deep Sleep mode	0.85	0.90	0.95	V
Output load current	$I_{REG2OUT}$		8	10	–	mA
Start up time	T_{REG2}		–	–	200	μs
Low-Power Regulator						
Input Voltage Range	$V_{LPREGIN}$		1.60	3.00	3.60	V
Output Voltage	$V_{LPREGOUT}$	Partial down, Sleep mode	0.70	0.90	1.10	V
Output load current	$I_{LPREGOUT}$		8	10	–	μA
Start up time	T_{LPREG}		–	5	–	ms

● Analog Characteristics・Miscellaneous

Item	Symbol	Condition	Min	Typ	Max	Unit
Temperature Sensor						
Detection Range	T_{RANGE}		-20	–	75	°C
Relative Detection Accuracy	T_{SLOPE}		-4	-5	-6	°C /code
Battery Monitor						
Detection Range	V_{BRANGE}		1.6	–	3.6	V
Detection Accuracy	V_{BACC}		–0.05	–	0.05	V

● SPI interface

SPI block is available to use only ML7125-001

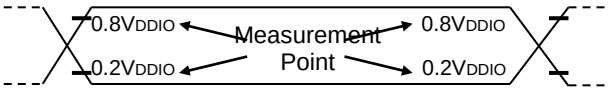
(Ta = –20 to +75 deg.C)

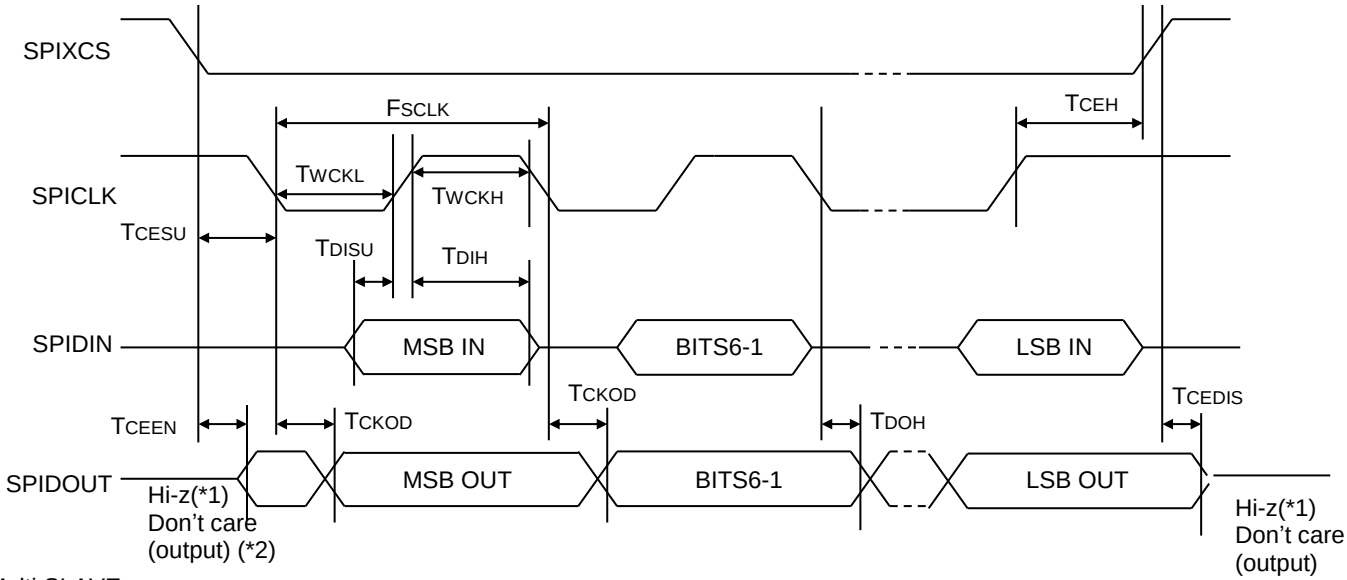
Item	Symbol	Condition	Min	Typ	Max	Unit
SPICLK Clock Frequency	FSCLK	Load capacitance CL=20pF	16.384	32.768	1625*1	kHz
SPIXCS input setup time	TCESU		1/Fsclk	–	–	ms
SPIXCS input hold time	TCEH		1/Fsclk	–	–	ms
SPICLK minimum high pulse width	TWCKH		250	–	–	ns
SPICLK minimum low pulse width	TWCKL		250	–	–	ns
SPIDIN input setup time	TDISU		5	–	–	ns
SPIDIN input hold time	TDIH		250	–	–	ns
SPICLK output delay time	TCKOD		–	–	250	ns
SPIDOUT output hold time	TDOH		5	–	–	ns
SPIXCS enable delay time	TCEEN		0	–	300	ns
SPIXCS disable delay time	TCEDIS		150	–	–	ns

Note: When using the width of the following SPICLK edge from the data output trigger SPICLK edge within 250 ns, there is possibility that the output timing of SPIDOUT becomes simultaneous with the following edge. Consider the data input setup time of HOST and set pulse width.
*1 : Practical maximam SPICLK clock frequency is limited to 475kHz when multiple bytes of data are transmitted consecutively without time interval between each byte transfer.

Remarks: All timing specification is defined at V_{DDIO} x 20% and V_{DDIO} x 80%
SPIXCS input setup/hold time have to be at least 1cycle of SPICLK clock frequency

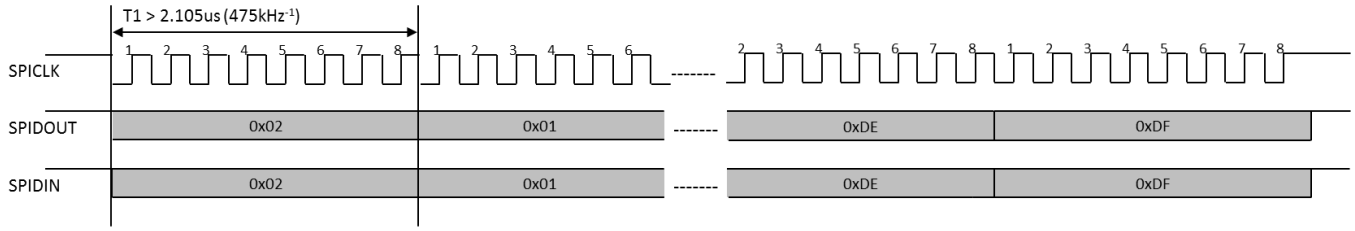
Measurement point



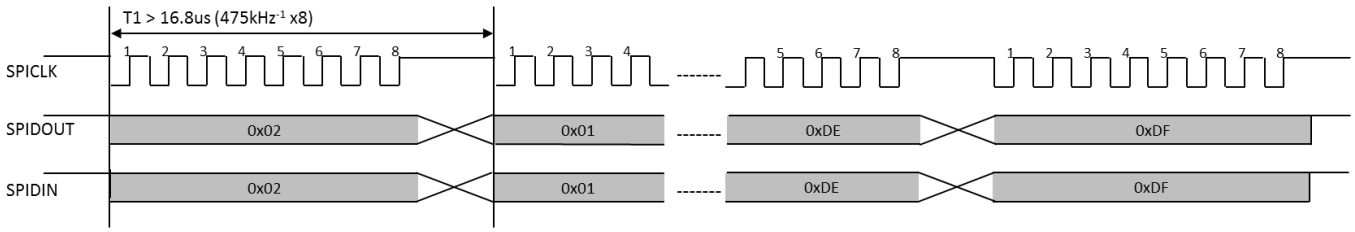


(*1) Multi SLAVE
(*2) Single SLAVE

No Time interval between byte transfer (t=0)



Time interval between byte transfer (t>0)

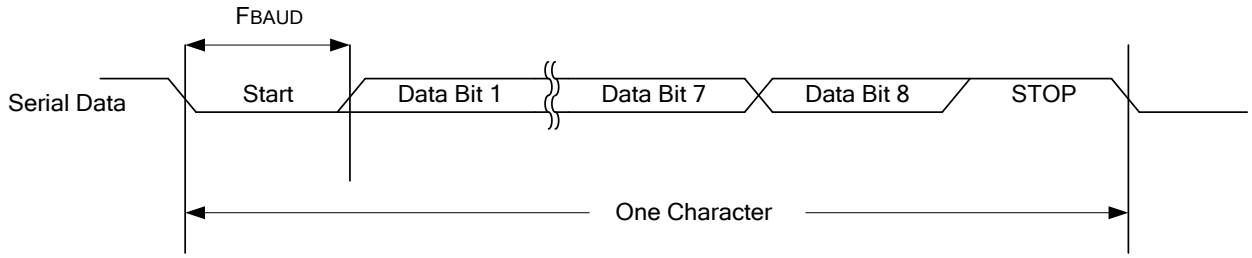


SPICLK frequency [kHz]	T1 : transmit 1byte data [us]	Minimum Time interval t [us]
475	16.8	0.0
512	15.6	1.2
1000	8.0	8.8
1600	5.0	11.8

- UART interface

(Ta = –20 to +75 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Baud Rate	FBAUD	Load capacitance CL=20pF	–	57600	–	bps(Hz)



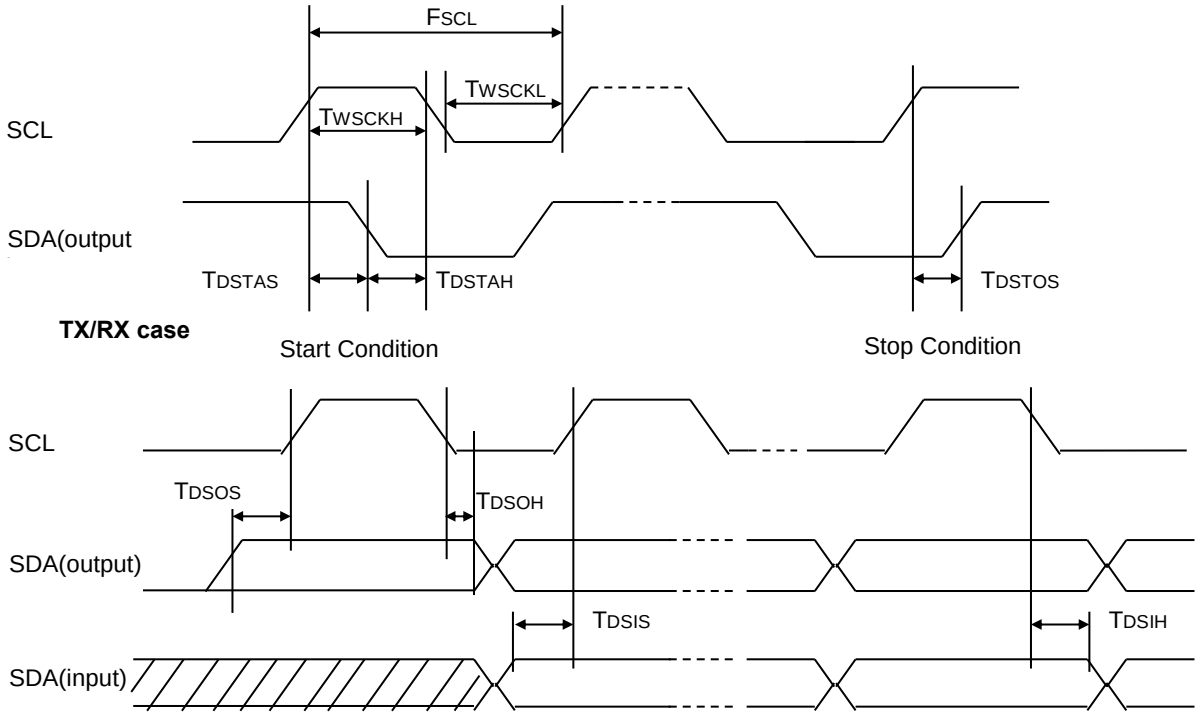
- I2C interface

(Ta = –20 to +75 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
SCL clock frequency	FSCL	Load capacitance CL=20pF	–	–	400	kHz
SCL minimum high pulse width	TWSCKH		10	–	–	µs
SCL minimum low pulse width	TWSCKL		10	–	–	µs
Start condition hold time	TDSTAH		5	–	–	µs
Start condition setup time	TDSTAS		5	–	–	µs
Stop condition setup time	TDSTOS		5	–	–	µs
SDA output hold time	TDSOH		5	–	–	µs
SCL output delay time	TDSOS		5	–	–	µs
SDA input setup time	TDSIS		80	–	–	ns
SDA input hold time	TDSIH		0	–	–	ns

Note: SCL clock frequency is fixed to 400kHz

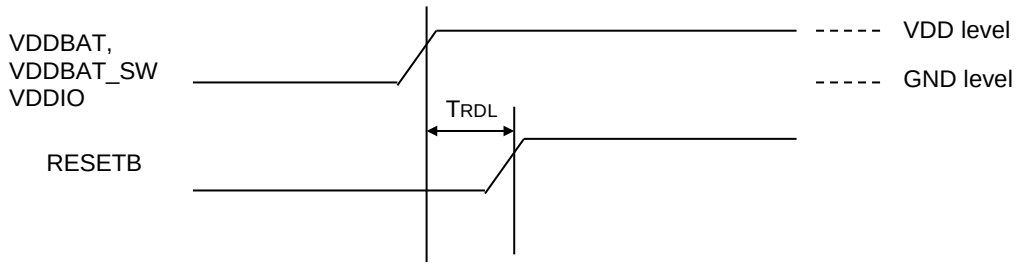
Start condition（SDA falling edge while SCL=1）, Stop condition（SDA rising edge while SCL=1）



● Reset operation

(Ta = –20 to +75 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
RESETB propagation delay time （Power on）	TRDL	Start supplying power (VDDBAT,VDDBAT_SW, VDDIO)	20	–	–	ms
RESETB Pulse width	TRPLS	RESETB pin	1	–	–	μs



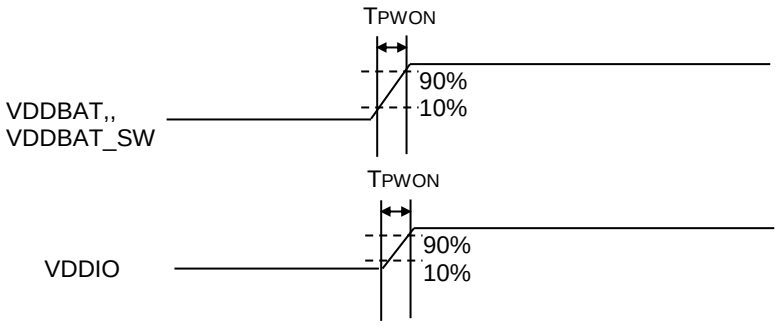
Power on reset function

Reset function from RESETB pin
It is possible to reset internal circuit by asserting RESETB after power supply is on.
It is possible to reset internal circuit by same way even if it is not power sequence. Internal circuit will move to normal state after oscillation circuit become stable by clock stabilizing circuit after reset function.

● Power on

(Ta = –20 to +75 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
VDD pin rising time	TPWON	While power on VDD pins (VDDBAT, VDDBAT_SW,VDDIO)	0.2	1	5	ms
Time difference between VDD pin while power on state	TPWONdly	While power on VDD pins (VDDBAT, VDDBAT_SW,VDDIO)	0	-	-	ms
Time difference between VDD pin while power off state	TPWOFdly	While power off VDD pins (VDDBAT, VDDBAT_SW,VDDIO)	0	-	-	ms

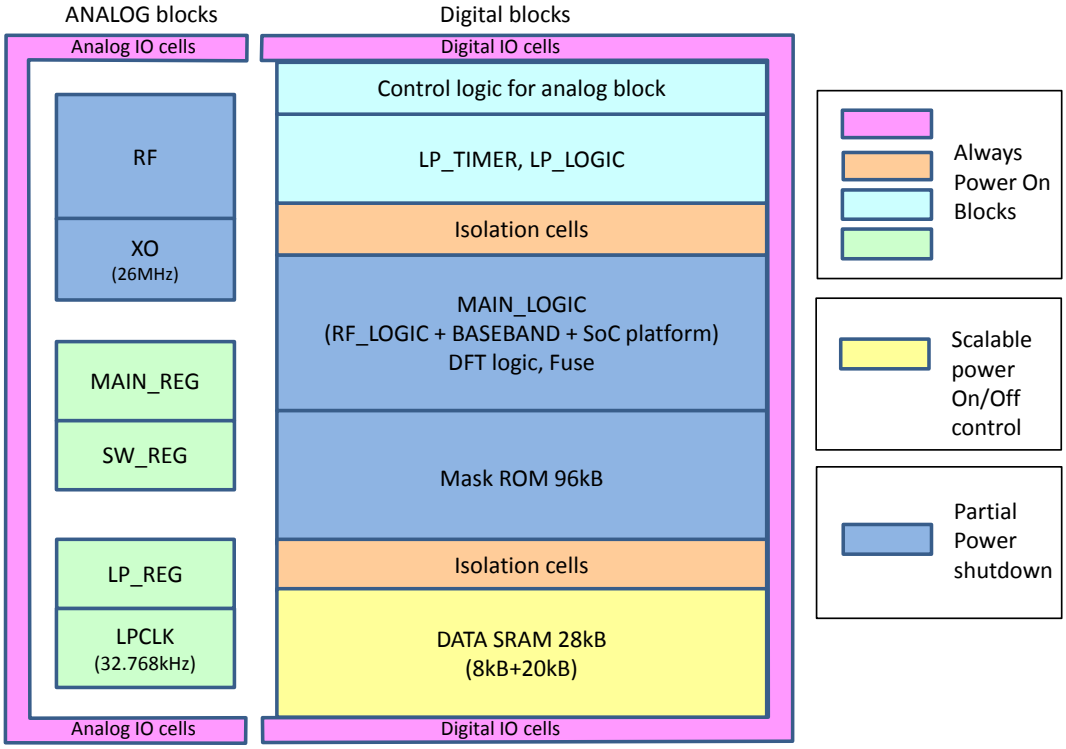


■ Power Supply system and Operating status

Overview: ML7125-00X integrate 3 regulators which are Linear Regulator (here in after MAIN_REG) providing power supply to MAIN logiv block, RF block, Switching Regulator (here in after SW_REG) and Low Power Regulator (here in after LP_REG) mainly used during power saving mode. Choice of regulator gives efficient low power saving mode depending on operating status.

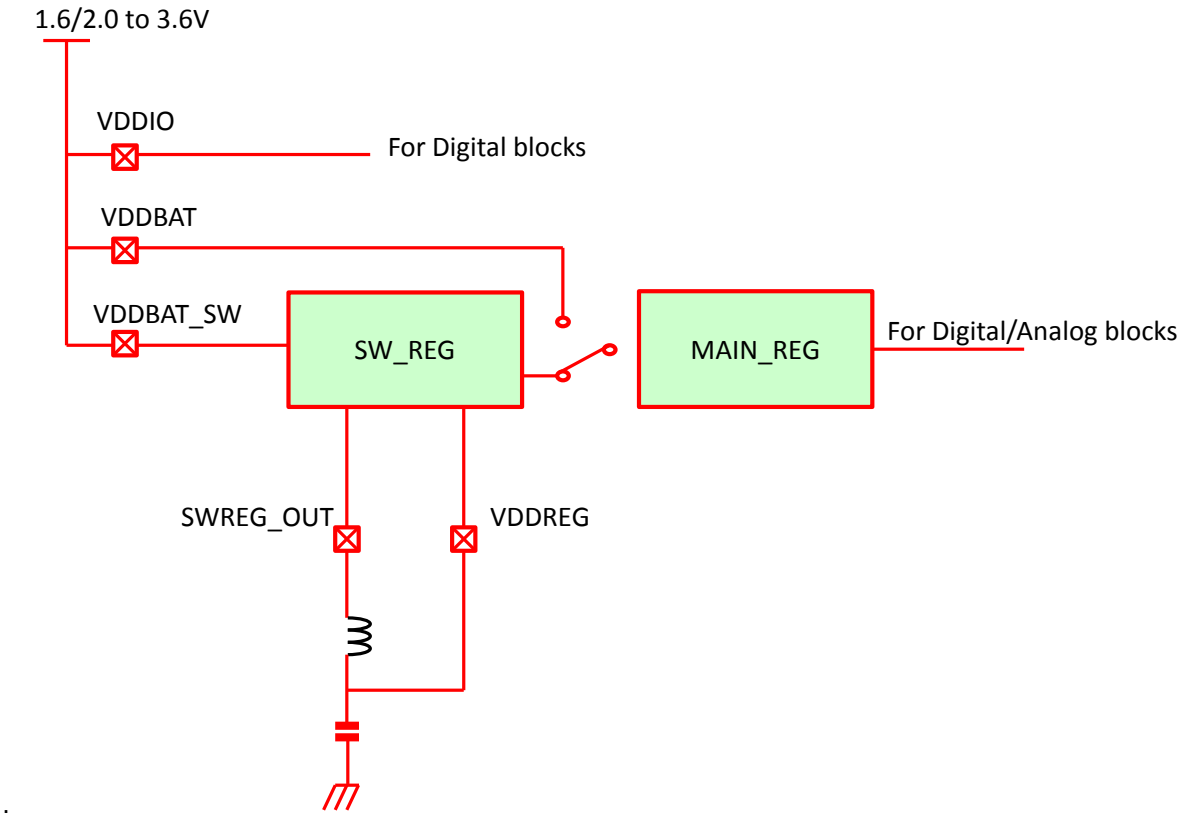
● Power Supply domain

Figure below shows block diagram by power supply domain in ML7125-00X. Those blocks indicated by "Partial Power Shutdown" will be stop supplying power during power saving mode so called Deep Sleep Mode.



- Internal Regulator

ML7125-00X has internal regulator which are Linear Regulator (MAIN_Reg) and Switching Regulator(SW_REG). Figure shown below depict internal regulator blocks and related pins.



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POWER MODE

ML7125-00X has Power mode shown below. Each state and these state transitions are explained in following section.

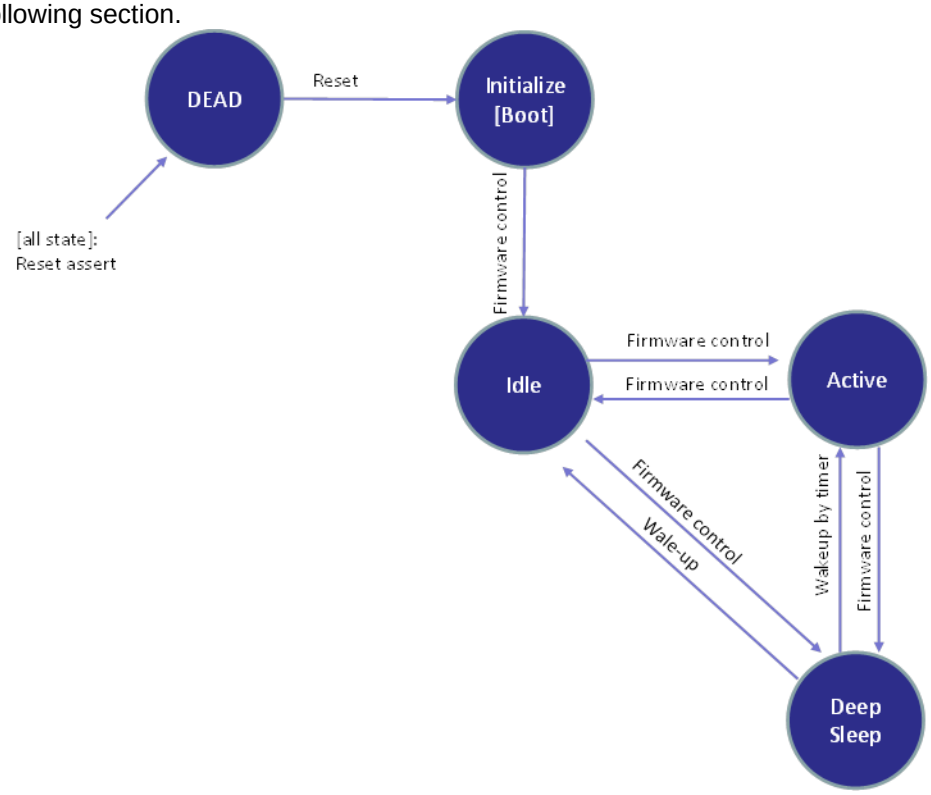


Fig.1 Power state transition and operating mode

[DEAD]

Assert hardware reset after start supplying power. ML7125-00X will move to Initialize/Boot state after power on reset event.

[Initialize/Boot]

ML7125-00X will start boot process after hardware reset. Boot program will initialize peripheral blocks nd start loading parameters. When Boot process completed, it will move to Idle state byfirmware control.

[Idle]

Idle state is the state that inernal MCU is available to process. User application can be execute in this state. Hence power supply for RF block will be suspended. Systtem clock 26MHz will be supplied while in Idle state.

[Active]

Active state is the state that RF communication shall be perfomed. In this state, most of blocks such as RF block, internal MCU, 26MHz clock oscillator are available to use. Peripheral block may be configured to stop clock supplying in order to save redundant power consumption.

[Deep Sleep]

Deep Sleep mode is power saving mode when the chip is in between connection event or application is not used for certain amount of time. Transition to Deep Sleep Mode is controlled by firmware. In Deep Sleep Mode, power supply to part of blocks are suspended in order to reduce standby current consumption. (Deep Sleep with Shutdown) Deep Sleep Mode uses 32.768kHz clock only, recovery to other state is initiated by Wake Up timer or Wakeup Factor condition.

- Wakeup Factor

Wakeup Factor is necessary to return from Deep sleep mode or Application Sleep. Wakeup Factor, low state of GPIO1 pin or WAKEUP pin, will be detected, and RF block clock will start to oscillate.

- Operating Status

Table shown below indicate operating status of internal clock by power mode.
LP_REG and MAIN_REG is powered all the time. Enable and Disable control will be done for MAIN_REG.

Block	Power Mode				
	DEAD	**Initialize [Boot]**	**Idle**	**Active**	**Deep Sleep**
LP_REG	DISABLE	ENABLE	ENABLE	ENABLE	ENABLE
MAIN_REG / SW_REG	DISABLE	ENABLE	ENABLE	ENABLE	DISABLE
XO	DISABLE	ENABLE	SELECTABLE	ON	OFF
LPCLK	DISABLE	SELECTABLE	SELECTABLE	SELECTABLE	SELECTABLE
RF	DISABLE	ON	OFF	ON	OFF
IO CELLS	OFF	ON	ON	ON	ON
LP_TIMER, LP_LOGIC etc.	OFF	ON	ON	ON	ON
SRAM 8kB	OFF	ON	ON	ON	ON
SRAM 20kB	OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF
Mask ROM 96kB	OFF	ON	ON	ON	OFF
MAIN_LOGIC	OFF	ON	ON	ON	OFF

ENABLE:ENABLE while POWER is ON
DISABLE:DISABLE while POWER is ON
ON: POWER is ON
OFF: POWER is OFF
ON/OFF: Available to select ON or OFF
SELECTABLE:Available to select ENABLE or DISABLE

■ Operating Mode

ML7125-00X support 3 operating modes, outline of each operating mode and supported product is shown in table shown below.

Operating mode		Outline	ML7125-001	ML7125-002
BACI mode		Lapis original application interface mode, it require HOST MCU externally. SPI is used in order to exchange command/event between ML7125-00X and Host MCU.	Supported	Not Supported
HCI mode		Bluetooth standard compatible mode, UART interface is used in order to exchange command/event between ML7125-00X and Host MCU.	Supported	Supported
APPLICATION mode	Standalone type	Application mode donwload its program code into internal SRAM. Standalone type of application perform without external Host MCU.	Not supported	Supported
	Add-on type	Application mode download its profram code into internal SRAM. Add-on type of application provide command base control and data transmission based on Lapis original AT-command.	Not supported	Supported

ML7125-00X will choose operating mode while it is boot process, the choice will be made depending on pin condition shown below. Additionally in Application mode, it is decided to move appropriate operating mode depending on contents of configuration parameter which is read during boot process. It is not possible to transit one mode to another while ML7125-00X is working. Reset process has to be made if mode change is required.

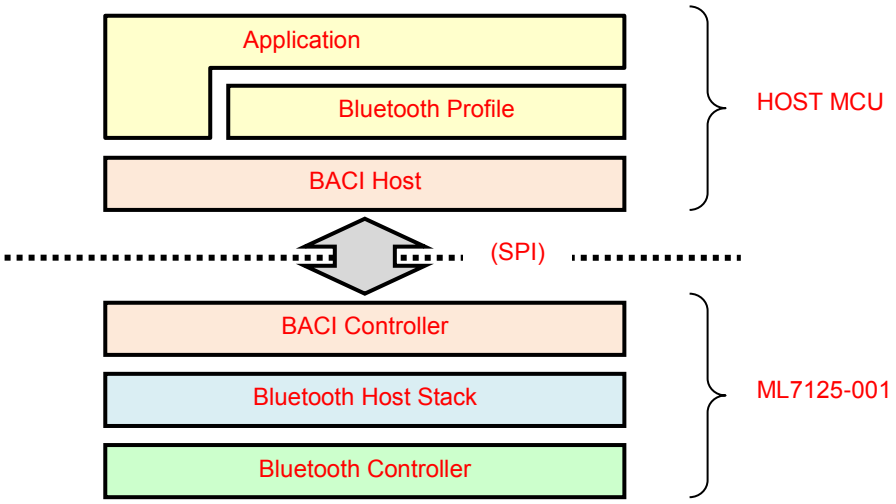
Operating Mode		Pin condition of ML7125-001 during boot sequence		Pin condition of ML7125-002 during boot sequence	
		UART_RXD	GPIO3 (PS_CONTROL)	UART_RXD	GPIO3
BACI Mode		Low	X	Not supported	
HCI Mode		High	X	High	Pull-Up
APPLICATION Mode	Standalone type	Not supported		Low/High	Low
	Add-on type	Not supported		High	Low

Low:Low input
High:High input
Pull-Up:Pull-Up to VDDHV
X:OPEN(output)

Details of each Operating Modes are shown in following sections.

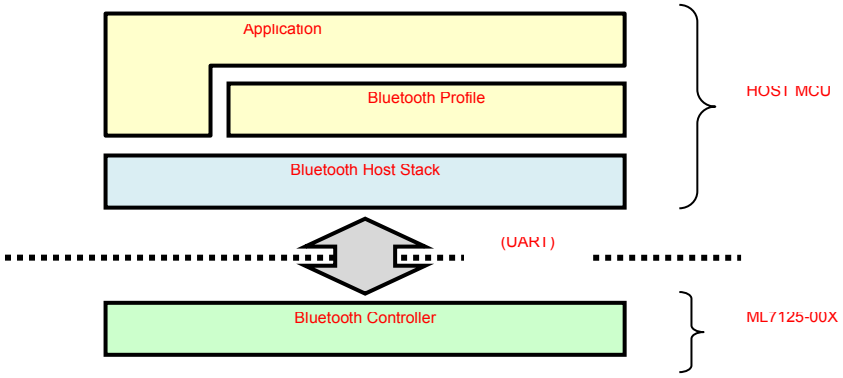
- BACI Mode

Protocol stack structure when ML7125-00X is in BACI mode is shown below. ML7125-00X will communicate with HOST-CPU by SPI interface or UART interface. Lapis original API called Bluetooth Application Controller Interface (BACI) will be used in order to exchange messages (command, event and data)



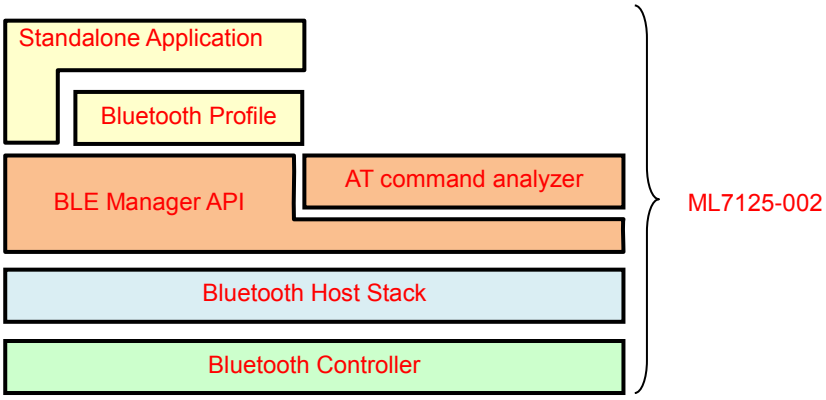
- HCI Mode

Protocol stack structure when ML7125-00X is in HCI mode is shown below.
ML7125-00X will communicate with HOST-CPU by UART interface. HCI command, event defined by Bluetooth Core Specification is available to use. Vendor specific HCI command is defined in our user's application.
Note: ML7125-002 will start up by HCI mode if UART interface is connected and configuration parameter indicates Add-on mode is disabled. Power saving control using WAKEUP signal is available to use.



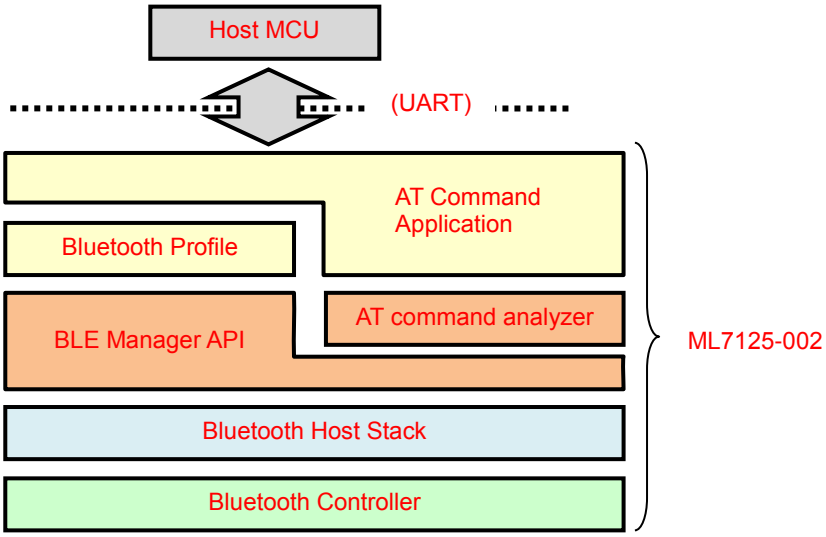
- Application Mode – Standalone type

When EEPROM is attached and configuration parameter is indicated, ML7125-002 will work as Application mode. With this Mode, Firmware stored in CODE_RAM area in EEPROM will be downloaded and executed after boot process. In this type of application mode, HOST MCU is not mandatory required. This type of application code is assuming to collect data from sensor devices and transmit to other device through Bluetooth radio.
Protocol stack structure when ML7125-002 is in Application mode – Standalone type is shown below.



- Application Mode – Add-on type

When EEPROM is attached and configuration parameter is indicated, ML7125-002 will work as Application mode. With this Mode, Firmware stored in CODE_RAM area in EEPROM will be downloaded and executed after boot process. Add-on type of application mode is assuming to use with HOST MCU using simple command and data interface defined by Lapis. It is possible to work
Protocol stack structure when ML7125-002 is in Application mode – Standalone type is shown below.

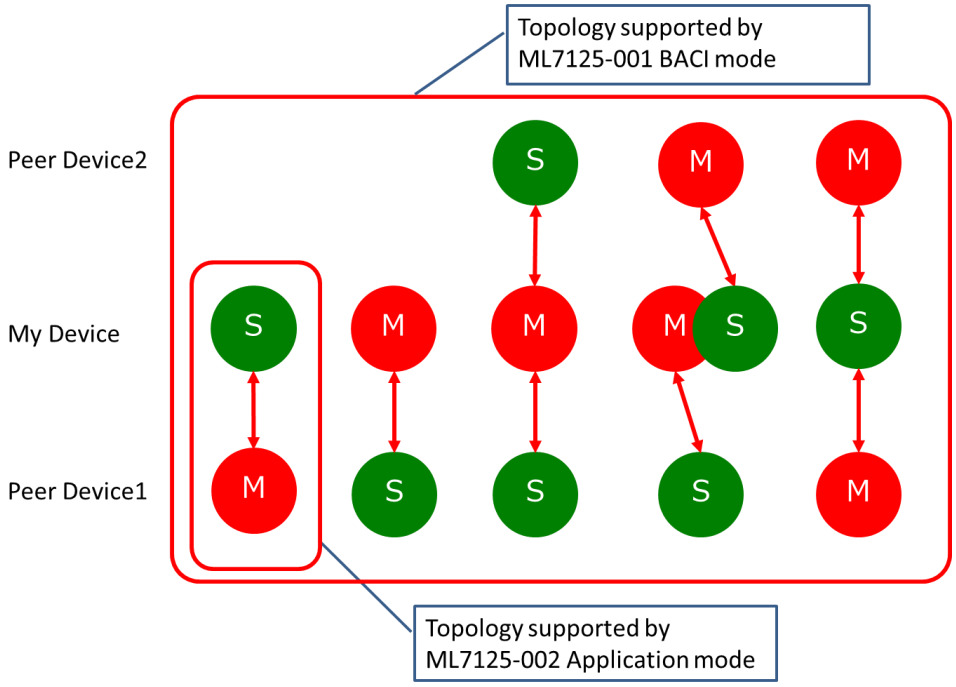


■ Functional features

● Bluetooth® feature

ML7125-00X is Bluetooth® Core Specification v4.1 compatible, it is supporting Low Energy Feature. Following table and figure shows part of Link layer features supported by ML7125-00X.

Product name	core spec version	Supported role	number of connectable device(s)	Number of connectable device(s)
ML7125-001	v4.1	Master or Slave	2 devices	2 devices
ML7125-002	v4.1	Slave only	1 device	1 device



● SPI interface description

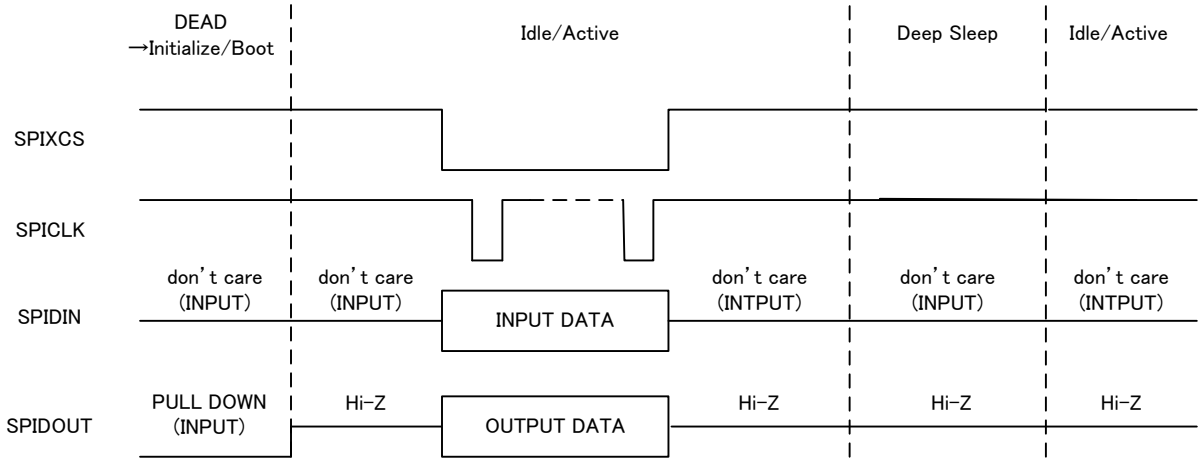
Possible combination of parameters are described below when SPI-SLAVE block are used as HOST interface.

Table 1 SPI_SLAVE Settings

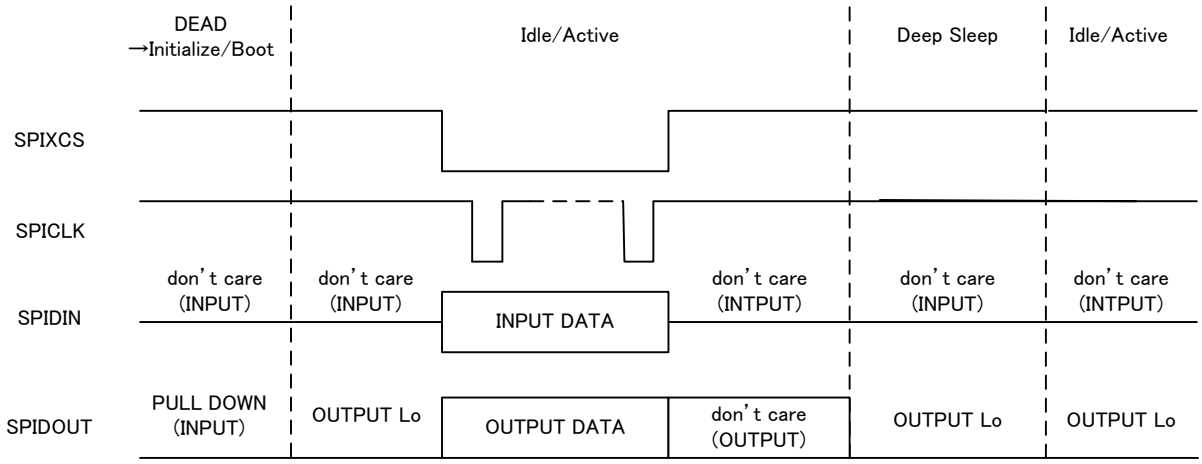
Parameter	Spec
Bit rate	Typ. 32.768KHz Max. 1.625MHz
SPI mode	Motorola SPI (Mode 3)
Data size	8 bits
Chip select	Low Active

Possible selection of SLAVE MODE, MULTI SLAVE or SINGLE SLAVE.
Sequences is shown below.

MULTI SLAVE



SINGLE SLAVE



● UART interface description

Possible combination of parameters are described below when UART block are used as HOST interface.

Table 2 UART Settings

Parameter	Spec
Baud rate	57600bps
Data size	8 bits
Parity bit	No parity
Stop bit	1 stop bit
Flow control	No

● I2C Interface description

Parameters related to I2C interface are shown below.

Table 3 I2C Settings

Parameter	Configuration
Master/Slave	Master
Data rate	400KHz/220kHz
Address bit	7 bit
Data bit	8 bit
Protocol	None

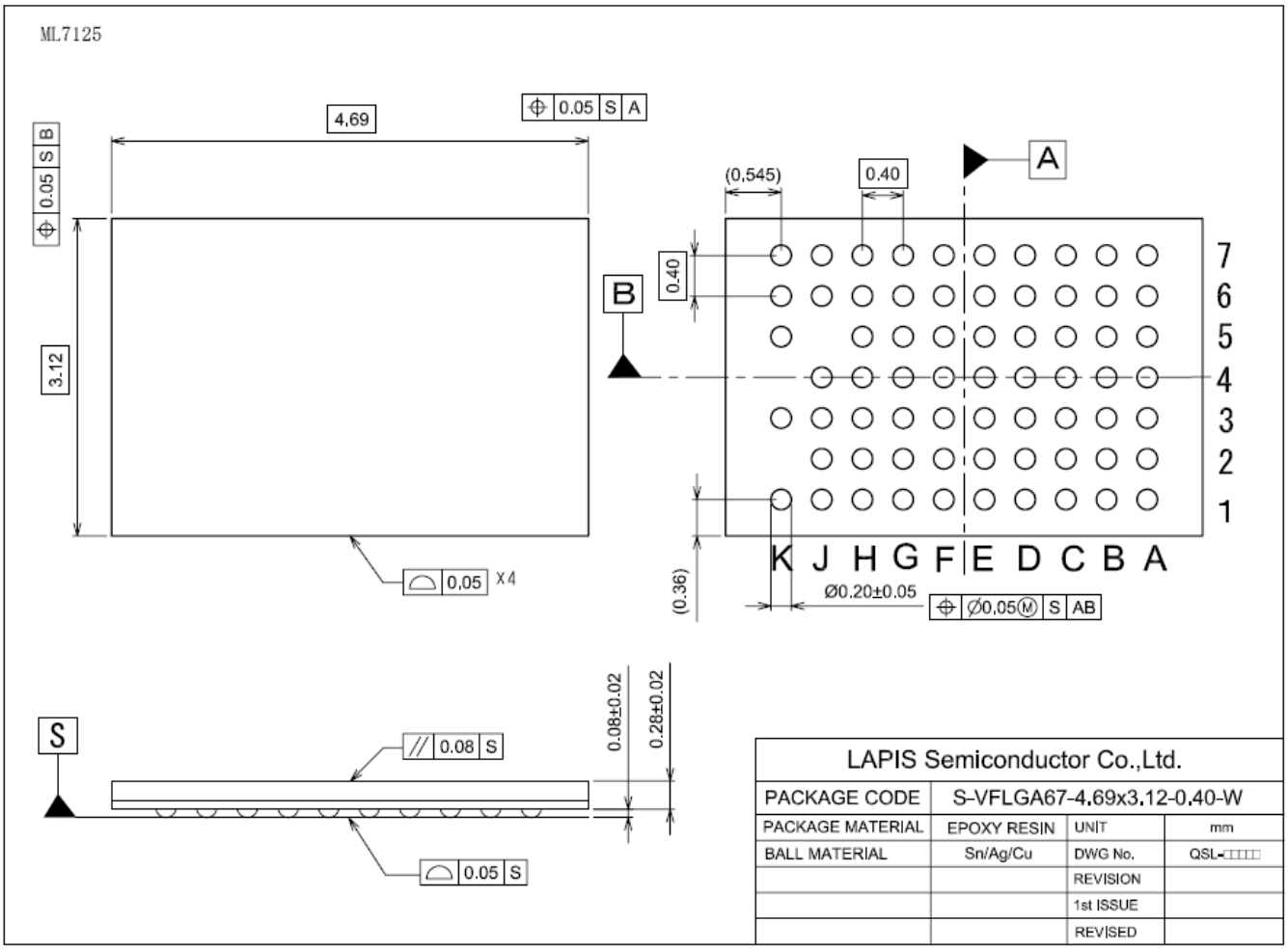
● LPCLK description

LPCLK (from external or oscillator) is used while ML7125 is in deep sleep mode in order to reduce power consumption. It is possible to choose either 32.768kHz or 16.384kHz

Table 4 LPCLK Settings

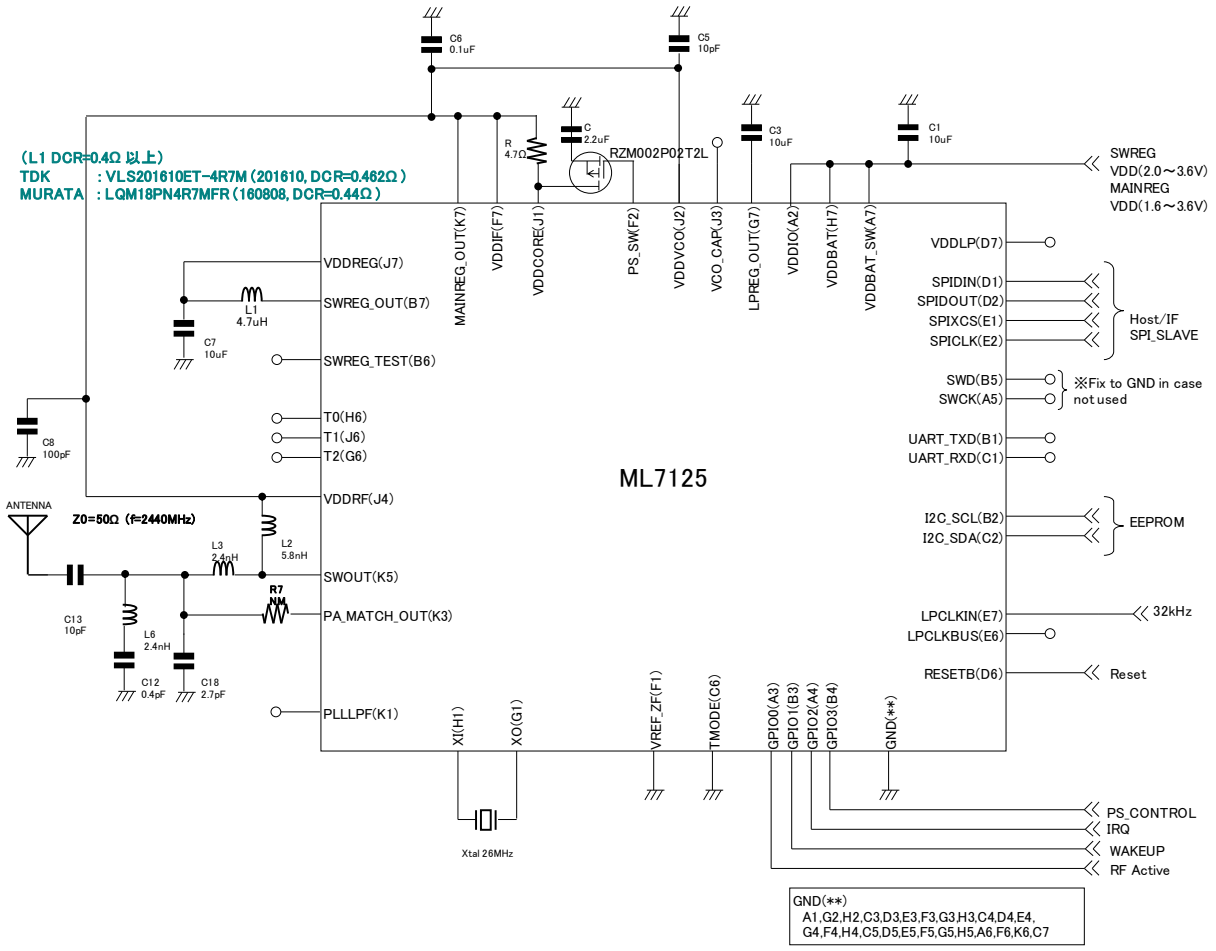
Parameter	Configuration
Frequency	32.768KHz or 16.384KHz
Duty	None (32.768KHz), 50% (16.384KHz)

■ Package dimensions



■ Application example

The following circuit shows the typical application circuit. This circuit shows ML7125-00X Application example and does not guarantee the characteristics. It is recommended that choosing and finalizes the best component value by evaluation on the target board.



■ Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7125--01	November,30,2015	–	–	1st Edition
FEDL7125--02	December,10,2015	1	1	Current Consumptions condition added
		-	2	Support Function List added
		2	2	Block Diagram modified
		6	6	PS_SW pin description changes
		7	7	Unused pins SPIDOUT/TM2 definition changes SWD/SWCK definitionadded
		14	14	Delete GPADC Characteristic
		16	16	SPI interface description modified
		28	28	SPI Sequences added
FEDL7125-03	January,26,2016	24	24	Pin condition of ML7125-002 during boot sequence modified Footnote added
FEDL7125-04	April,5,2016	1	1	Featire condition modified
		2	2	Block Diagram modified
		3	3	PIN ASSIGNMENT SPIDIN/SPIDOUT/SPICLK/SPIXCS PIN ASSIGNMENT modified
		4	4	LPXO renamed LPCLK
		6	6	FUCNTION modified MAIN Regulator→Linear Regulator
		8	8	VDDBAT_SW added in Condition
		9	9	
		19	19	
		9	9	Master Clock Condition modified
		11	11	H level Voltage Output Condition modified
		12	12	TX power Condition modified
		20	20	LPXO in figure renamed LPCLK
		21	21	Change pin name SWREG_FB to VDDREG in Internal Regulator figure.
		29	29	LPCLK description modified

		31	31	Change pin name SWREG_FB to VDDREG in Application Example.

NOTES

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