

**SPECIFICATIONS FOR
LCD MODULE**

**MODEL NO.
BL12864I1WRNHn\$
VER01**

OR MESSRS:

ON DATE OF:

APPROVED BY:

BOLYMIN, INC.
13F-1, 20, TA-LONG RD., TAICHUNG CITY 403, TAIWAN, R.O.C.
WEB SITE: <http://www.bolymin.com.tw> TEL:+886-4-23293029 FAX:+886-4-23293055

History of Version

Version	Contents	Date	Note
01	NEW VERSION	2008/12/22	SPEC.

CONTENTS

1. Numbering System
2. General Specification
3. Absolute Maximum Ratings
4. Electrical Characteristics
5. Optical Characteristics
6. Panel Layout Diagram
7. Interface Pin Function
8. Power Supply For LCD Module
9. Timing Characteristics
10. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT
11. Display Control Instruction
12. Reliability
13. Appendix

1. Numbering System

<u>B</u>	<u>L</u>	<u>12864</u>	<u>I1</u>	<u>W</u>	<u>R</u>	<u>N</u>	<u>:</u>	<u>H</u>	<u>n\$</u>
0	1	2	3	4	5	6	7	8	9

0	Brand	Bolymin	
1	Module Type	C= character type G= graphic type P= TAB/TCP type	O= COG type F= COF type L=PLED/OLED
2	Format	2002=20 characters, 2 lines 12232= 122 x 32 dots	
3	Version No.	A type	
4	LCD Color	G=STN/gray Y=STN/yellow-green PLED/yellow-green C=color STN,OLED/RGB W= OLED white	B=STN/blue,OLED/blue F=FSTN T=TN D=OLED/blue+yellow A=OLED/blue+yellow+green
5	LCD Type	R=positive/reflective P=positive/transflective	M=positive/transmissive N=negative/transmissive
6	Backlight type/color	L=LED array/ yellow-green H=LED edge/white R=LED array/red G=LED edge/yellow-green F=RGB array I=RGB edge Q=LED edge/red N=No backlight	D=LED edge/blue E=EL/white B=EL/blue C=CCFL/white Y=LED Bottom/yellow O=LED array/orange K=LED edge/green A=LED edge/amber
7	CGRAM Font (applied only on character type)	J=English/Japanese Font E=English/European Font G=Chinese(simple) F=Chinese(traditional)	C=English/Cyrillic Font H=English/Hebrew Font A=English/Arabic Font
8	View Angle/ Operating Temperature	B=Bottom/Normal Temperature H=Bottom/Wide Temperature U=Bottom/Ultra wide Temperature	T=Top/Normal Temperature W=Top/Wide Temperature C=9H/Normal Temperature E=Top/ultra wide temperature
9	Special Code	3=3 volt logic power supply n=negative voltage for LCD c=cable/connector xxx=to be assigned on datasheet	t=temperature compensation for LCD p=touch panel \$=RoHS

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	128x64	dots
Module dimension (L*W*H)	40*35*2.65(MAX)	mm
Active area	23.02*11.5	mm
Dot size	0.16(W)×0.16(H)	mm
Dot pitch	0.18(W)×0.18 (H)	mm
Color	White	

(2) Controller IC: SSD1303 Controller

(3) Temperature Range

Operating	-40 ~ +70°C
Storage	-40 ~ +85°C

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+70	°C
Storage Temperature	TST	-40	—	+85	°C
Humidity		—	—	85	%
Supply Voltage For Logic	VDD	-0.3	—	3.5	V
Supply Voltage For Panel	Vcc	8	—	16	V
Operating lifetime			20000(*)		Hrs

*:80cd/m² light on

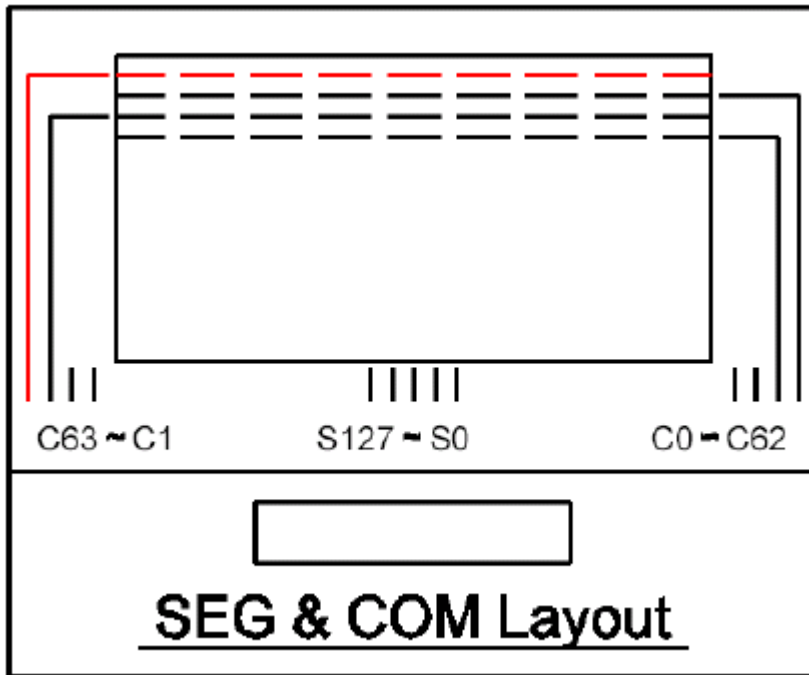
4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$	—	2.4	3.3	3.5	V
Supply Voltage For Panel	$V_{CC}-V_{SS}$	—	11.5	12	12.5	V
Input High Vol	V_{IH}	—	$0.8V_{DD}$	—	V_{DD}	V
Input Low Vol	V_{IL}	—	0	—	$0.2V_{DD}$	V
Output High Vol	V_{OH}	—	$0.9V_{DD}$	—	V_{DD}	V
Output Low Vol.	V_{OL}	—	0	—	$0.1V_{DD}$	V
Supply Current For Logic (with built-in positive voltage)	I_{DD}	—	—	90	—	mA

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	—	—	deg
Dark Room contrast	2000:1	—	—	—
Response Time	—	10	—	us

6. Panel Layout Diagram



7. Interface Pin Function

Pin No.	Symbol	Level	Description
1	Vdd	3.3V	Supply voltage for logic
2	Vss	0V	Ground
3	NC	—	No connection
4	DB0	H/L	Data bus line
5	DB1	H/L	Data bus line
6	DB2	H/L	Data bus line
7	DB3	H/L	Data bus line
8	DB4	H/L	Data bus line
9	DB5	H/L	Data bus line
10	DB6	H/L	Data bus line
11	DB7	H/L	Data bus line
12	CS	H/L	Chip select pin
13	NC	—	No connection
14	/RES	H/L	Hardware Reset pin
15	WR	H/L	write signal pin
16	D/C	H/L	H: Data; L: Command.
17	RD	H/L	Read signal pin
18	NC	—	No connection
19	DISP	L	L:LCM display off
20	NC	—	No connection

Default: Parallel 8-Bit 8080 Interface

68j : Parallel 8-Bit 6800 Interface Special Code

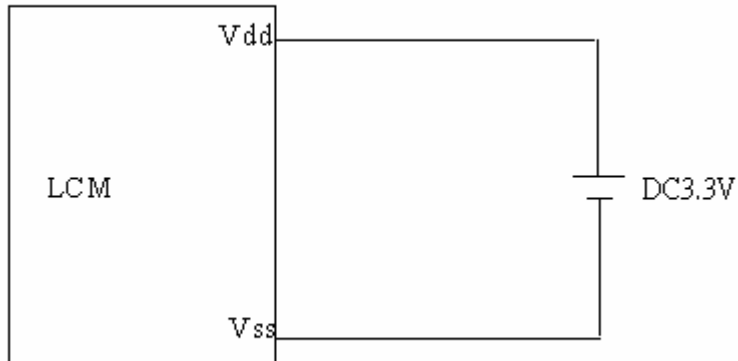
20i : SPI Interface Special Code

20a: I2C Interface Special Code

PIN NAME Bus Interface	Data/Command Interface								Control Signal				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD	W/R#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
SPI	Tie LOW					LOW	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#
I2C	Tie LOW					SDA _{out}	SDA _{in}	SCL	Tie LOW		CS#	SA0	RES#

8. Power Supply For LCD Module

* LCM operating on "DC 3.3V " input with built-in positive voltage

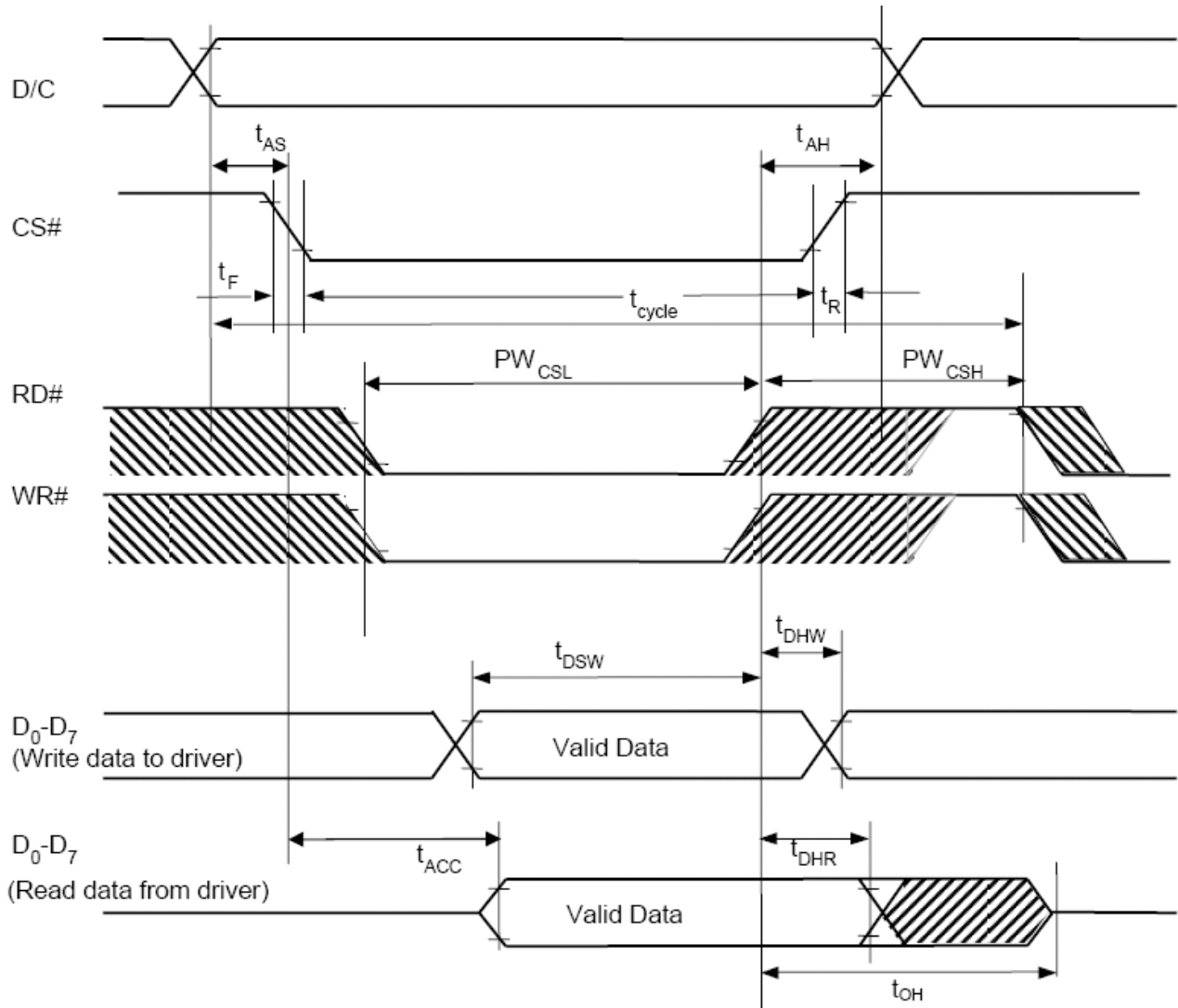


9. Timing Characteristics

9-1.8080 MPU Interface

($V_{DD} - V_{SS} = 2.4$ to $3.5V$, $T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	150	-	-	ns
PW_{CSH}	Chip Select Low Pulse Width (write)	60	-	-	ns
	Chip Select High Pulse Width (read)	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

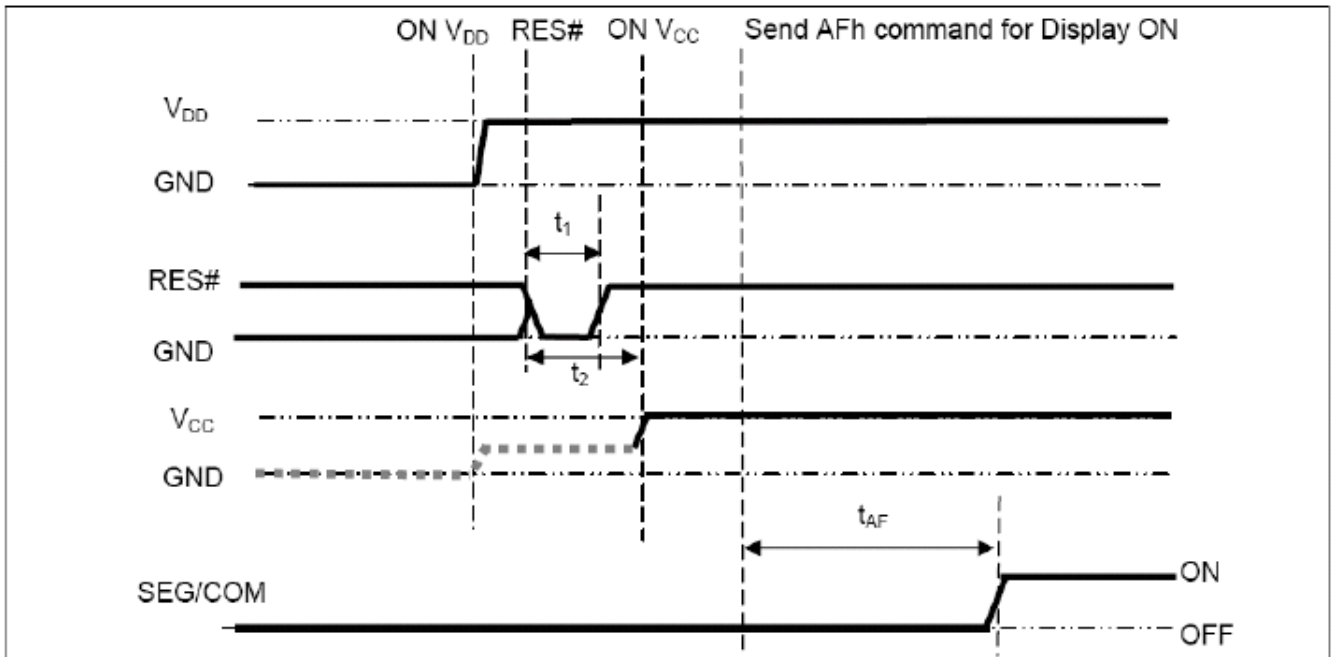


10. Power ON / OFF Sequence & Application Circuit

10.1 POWER ON / OFF SEQUENCE

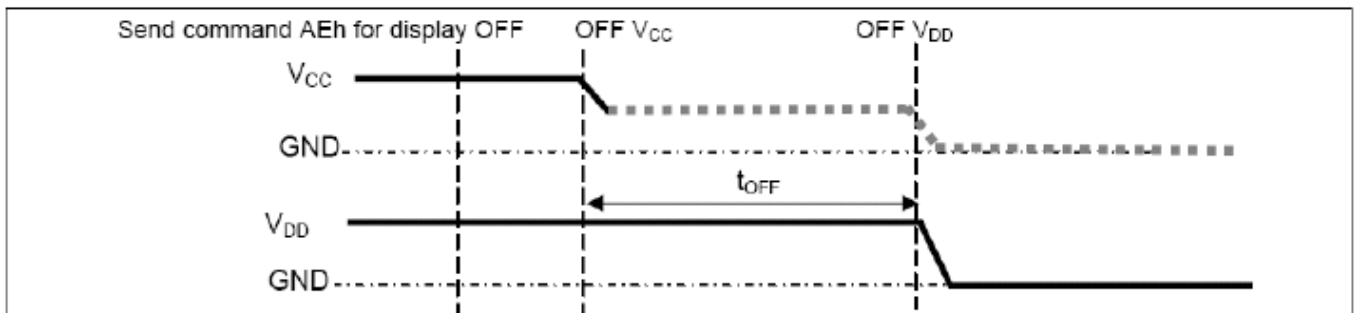
Power ON sequence:

1. Power ON V_{DD} .
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least $3\mu s(t_1)$ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least $3\mu s(t_2)$. Then Power ON V_{CC} . (1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after $100ms(t_{AF})$.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC} . (1), (2)
4. Wait for t_{OFF} . Power OFF V_{DD} . (where Minimum $t_{OFF}=80ms$, Typical $t_{OFF}=100ms$)



Note:

- (1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} , V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
- (2) V_{CC} should be disabled when it is OFF.

11. Display Control Instruction

(D/C = 0, R/W (WR) = 0, E(RD) = 1) unless specific setting is stated

Single byte command (D/C = 0), Multiple byte command (D/C = 0 for first byte, D/C = 1 for other bytes)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X3	X2	X1	X0	Set Lower Column Address **	Set the lower nibble of the column address register using X3X2X1X0 as data bits. The initial display line register is reset to 0000b after POR.
0	10~1F	0	0	0	1	X3	X2	X1	X0	Set Higher Column Address **	Set the higher nibble of the column address register using X3X2X1X0 as data bits. The initial display line register is reset to 0000b after POR.
0	26	0	0	1	0	0	1	1	0	Horizontal scroll setup	A[2:0] Set the number of column scroll per step Valid value: 001b, 010b, 011b, 100b B[2:0] Define start page address C[1:0] Set time interval between each scroll step in terms of frame frequency 00b – 12 frame 01b – 64 frames 10b – 128 frames 11b – 256 frames D[2:0] Define end page address Set the value of D[2:0] larger or equal to B[2:0]
0	A[2:0]	*	*	*	*	*	A2	A1	A0		
0	B[2:0]	*	*	*	*	*	B2	B1	B0		
0	C[1:0]	*	*	*	*	*	*	C1	C0		
0	D[2:0]	*	*	*	*	*	D2	D1	D0		
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Start horizontal scrolling
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling
0	40-7F	0	1	X5	X4	X3	X2	X1	X0	Set Display Start Line	Set display TAM display start line register from 0-63 using X5X3X2X1X0. Display start line register is reset to 000000 during POR
0 0	81 A[7:0]	1 A7	0 A6	0 A5	0 A4	0 A3	0 A2	0 A1	1 A0	Set Contrast Control Register **	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 80h)
0	82	1	0	0	0	0	0	1	0	Brightness for color banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (POR = 80h)
	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		
0	91	1	0	0	1	0	0	0	1	Set Look Up Table (LUT) for area color	Set current drive pulse width of Bank 0, Color A, B and C. Bank 0: X[5:0] = 0... 63; for pulse width set to 1 ~ 64 clocks (POR = 110001b) Color A: A[5:0] same as above (POR = 111111b) Color B: B[5:0] same as above (POR = 111111b) Color C: C[5:0] same as above (POR = 111111b) Note: color D pulse width is fixed at 64 clocks pulse .
0	X[5:0]	*	*	X5	X4	X3	X2	X1	X0		
0	A[5:0]	*	*	A5	A4	A3	A2	A1	A0		
0	B[5:0]	*	*	B5	B4	B3	B2	B1	B0		
0	C[5:0]	*	*	C5	C4	C3	C2	C1	C0		

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	92	1	0	0	1	0	0	1	0	Set bank color of for bank 1-16 (Page 0)	A[1:0] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 1
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		A[3:2] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 2
0	B[7:0]	B7	B6	B5	B4	B3	B2	B1	B0		:
0	C[7:0]	C7	C6	C5	C4	C3	C2	C1	C0		:
0	D[7:0]	D7	D6	D5	D4	D3	D2	D1	D0		D[7:6]: 00, 01, 10, or 11 for Color = A, B, C or D of bank 16
0	93	1	0	0	1	0	0	1	1	Set bank color of for bank 17-32 (Page 1)	A[1:0] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 17
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		A[3:2] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 18
0	B[7:0]	B7	B6	B5	B4	B3	B2	B1	B0		:
0	C[7:0]	C7	C6	C5	C4	C3	C2	C1	C0		:
0	D[7:0]	D7	D6	D5	D4	D3	D2	D1	D0		D[7:6]: 00, 01, 10, or 11 for Color = A, B, C or D of bank 32
0	A0~A1	1	0	1	0	0	0	0	X0	Set Segment Re-map **	X0=0: column address 0 is mapped to SEG0 (POR) X0=1: column address 131 is mapped to SEG0
0	A4~A5	1	0	1	0	0	1	0	X0	Set Entire Display ON/OFF **	X0=0: normal display (POR) X0=1: entire display ON
0	A6~A7	1	0	1	0	0	1	1	X0	Set Normal/Inverse Display **	X0=0: normal display (POR) X0=1: inverse display
0 0	A8 A[5:0]	1 *	0 *	1 A5	0 A4	1 A3	0 A2	0 A1	0 A0	Set Multiplex Ratio **	The next command, A[5:0] determines multiplex ratio N from 16MUX-64MUX, POR= 64MUX
0	AA	1	0	1	0	1	0	1	0	NOP	Reserved, do not use
0	AB	1	0	1	0	1	0	1	1	NOP	Reserved, do not use
0 0	AD	1 1	0 0	1 0	0 0	1 1	1 0	0 1	1 X0	Set DC-DC on/off	X0 : 1 DC-DC will be turned on when (POR) display on 0 DC-DC is disable
0	AE~AF	1	0	1	0	1	1	1	X0	Set Display ON/OFF **	X0=0: turns OFF OLED panel (POR) X0=1: turns ON OLED panel
0	B0~BF	1	0	1	1	X3	X2	X1	X0	Set Page Address **	Set GDDRAM Page Address (0~7) for read/write using X3X2X1X0
0	C0/C8	1	1	0	0	X3	*	*	*	Set COM Output Scan Direction **	X3=0: normal mode (POR) Scan from COM 0 to COM [N -1] X3=1: remapped mode. Scan from COM [N-1] to COM0 Where N is the Multiplex ratio.
0	D0-D1	1	1	0	1	0	0	0	X0	Reserved	Reserved, do not use

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	D3 A[5:0]	1 *	1 *	0 A5	1 A4	0 A3	0 A2	1 A1	1 A0	Set Display Offset **	Set vertical scroll by COM from 0-63. The value is reset to 00H after POR.
0 0	D5 A[7:0]	1 A7	1 A6	0 A5	1 A4	0 A3	1 A2	0 A1	1 A0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] Define the divide ratio of the display clocks (DCLK): Divide ratio= A[3:0] + 1, POR is 0000b (divide ratio = 1) A[7:4] Set the Oscillator Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa. POR is 0111b
0 0	D8	1 0	1 0	0 X5	1 X4	1 0	0 X2	0 0	0 X0	Set area color mode on/off & low power display mode	X5X4= 00 (POR) : mono mode X5X4= 11 Area Color enable X2=0 and X0=0: Normal (POR) power mode X2=1 and X0=1: Set low power save mode
0 0	D9 A[7:0]	1 A7	1 A6	0 A5	1 A4	1 A3	0 A2	0 A1	1 A0	Set Pre-charge period**	A[3:0] Phase 1 period of up to 15 dclk clocks [POR=2h]; 0 is invalid entry A[7:4] Phase 2 period of up to 15 dclk clocks [POR=2h]; 0 is invalid entry
0 0	DA	1 0	1 0	0 0	1 X4	1 0	0 0	1 1	0 0	Set COM pins hardware configuration	X4=0, Sequential COM pin configuration (i.e. COM31, 30, 29....0 ; SEG0-132; COM31,32....62,63) X4=1(POR), Alternative COM pin configuration (i.e. COM62,60,58,...2,0; SEG0-132; COM1,3,5....61,63)
0 0	DB A[6:0]	1 *	1 A6	0 A5	1 A4	1 A3	0 A2	1 A1	1 A0	Set VCOM Deselect Level	A[6:0] 0000000 low VCOM deselect level (~ 0.43 Vref) 0110101 normal VCOM deselect level (~ 0.77*Vref (POR)) 1111111 high VCOM deselect level (equal Vref)
0	E2	1	1	1	0	0	0	1	0	Reserved	Reserved
0	E3	1	1	1	0	0	0	1	1	NOP **	Command for No Operation
0	F*	1	1	1	1	*	*	*	*	Reserved	Reserved, do not use

Note: Remark "**" stands for "Don't Care"

12. Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	—
2	High temp. (Operation)	70°C, 120hrs	—
3	Low temp. (Operation)	-40°C, 120hrs	—
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	—
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	—
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	—
7	Drop	Height: 120cm Sequence : 1 angle、 3 edges and faces Cycles: 1	—
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	—

13. Appendix (Drawing)

