Datasheet

200mA LDO Regulator with Voltage Detector and Watchdog Timer

BD3010AFV

General Description
BD3010AFV is a regulator with an integrated WDT (Watch Dog Timer), a high output voltage accuracy of ±2.0 % and a low circuit current consumption of 80 μA (Typ). BD3010AFV is suitable to use with low ESR ceramic capacitor to attain good output stability. BD3010AFV also integrates an automatic WDT ON/OFF feature using an output current detection and an output clamping circuit to prevent output overshoot caused by current flow. The reset detection voltage can be adjusted by connecting resistors on the RADJ terminal. BD3010AFV can be used as a stable power supply for any applications while detecting malfunction of microcontrollers.

Key Specifications
- Regulator Supply Voltage Range: 5.6 V to 36 V
- WDT Supply Voltage Range: 6.0 V to 36 V
- High Output Voltage Accuracy: (Ta = −40 °C to +125 °C) ±2.0 %
- Low Circuit Current: 80 μA (Typ)
- Operating Temperature Range: -40 °C to +125 °C

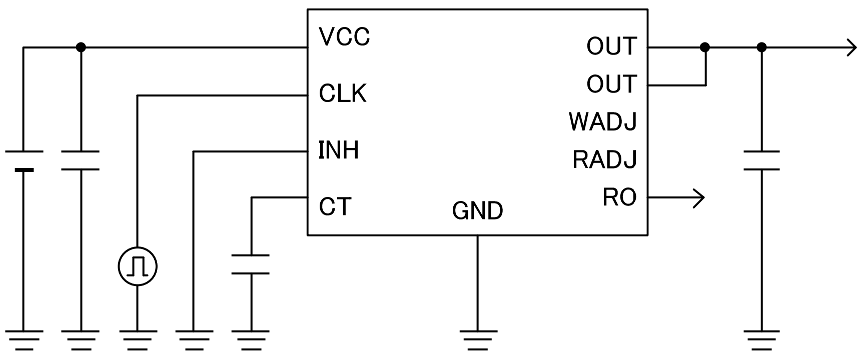
Package
W(Typ) × D(Typ) × H(Max)

SSOP-B20
6.50mm × 6.40mm × 1.45mm

Features
- V_{CC} Max Voltage: 50 V
- Output Circuit: P-ch DMOS
- Supports Low ESR Ceramic Capacitor
- Integrated Over Current Protection and Thermal Shut Down
- Integrated WDT Reset Circuit (Adjustable Detection Voltage through RADJ pin)
- Integrated Automatic WDT ON/OFF Function Through Output Current Detection
- WDT can be Switched ON/OFF by Using INH Pin
- Integrated Output Voltage Clamping Circuit

Applications
Any application using a microcontroller or a DSP such as automotive (body control), display, server, DVD, phone, etc

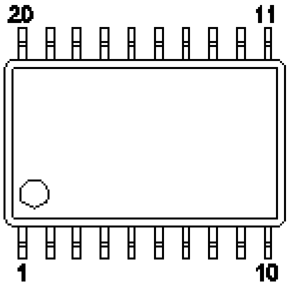
Typical Application Circuit



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

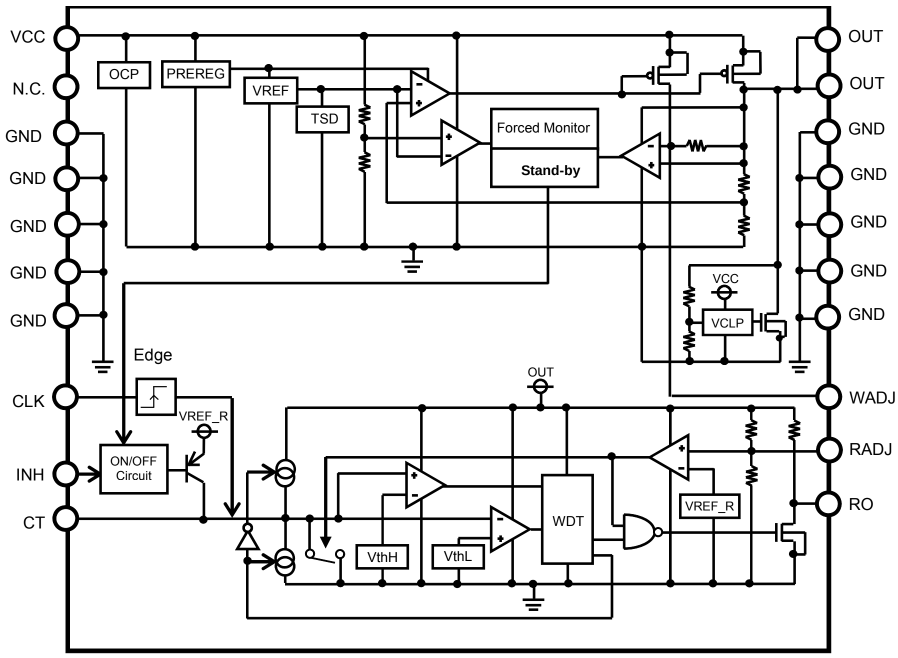
(TOP VIEW)



Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	VCC	Power supply pin	11	RO	Reset output pin
2	N.C.	−	12	RADJ	Reset detection voltage set pin
3	GND		13	WADJ	WDT operating current set pin
4	GND		14	GND	
5	GND	GND	15	GND	
6	GND		16	GND	GND
7	GND		17	GND	
8	CLK	Clock input from microcontroller	18	GND	
9	INH	WDT ON / OFF function pin	19	OUT	Voltage output pin
10	CT	External capacitance for reset output delay time, WDT monitor time setting connection pin	20	OUT	

Block Diagram



Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage (Note 1)	V_{CC}	-0.3 to +50	V
VADJ Set Pin Voltage	V_{RADJ}	-0.3 to +7	V
Regulator Output Pin Voltage	V_{OUT}	-0.3 to +7	V
INH Pin Voltage	V_{INH}	-0.3 to +15	V
Reset Output Pin Voltage	V_{RO}	-0.3 to +7	V
Watchdog Input Pin Voltage	V_{CLK}	-0.3 to +15	V
Watchdog Time Set Pin Voltage	V_{CT}	-0.3 to +7	V
Watchdog Operation Current Set Pin Voltage	V_{WADJ}	-0.3 to +7	V
Power Dissipation (Note 2)	Pd	1.25	W
Operating Temperature Range	Topr	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note 1) Should not exceed Pd.
(Note 2) Reduced by 10.0 mW / °C over Ta = 25 °C, when mounted on 70 mm × 70 mm × 1.6 mm glass epoxy board:
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Note 3)	V_{CC}	5.6	36.0	V
Supply Voltage (Note 4)	V_{CC}	6.0	36.0	V
Output Current	I_{OUT}	0	200	mA

(Note 3) For the output voltage, consider the voltage drop (dropout voltage) due to the output current.
(Note 4) Operating condition for automatic WDT ON / OFF.

Electrical Characteristics

(Unless otherwise specified, Ta = -40 °C to +125 °C, V_{CC} = 13.5 V, INH = 5 V, CLK = GND, I_{OUT} = 0 mA)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[Entire Device]						
Circuit Current 1	I_{CC1}	-	80	140	μA	
Circuit Current 2	I_{CC2}	-	110	170	μA	I_{OUT} = 50 mA (Ta = 25 °C)
[Regulator]						
Output Voltage	V_{OUT}	4.90	5.00	5.10	V	
Line Regulation	Line.Reg	-	5	30	mV	V_{CC} = 5.6 V to 36 V
Load Regulation	Load.Reg	-	20	60	mV	I_{OUT} = 5 mA to 150 mA
Dropout Voltage	ΔV_D	-	0.25	0.50	V	V_{CC} = 4.75 V, I_{OUT} = 150 mA
Ripple Rejection	R.R.	45	55	-	dB	f = 120 Hz, E_{IN} = 1 Vrms, I_{OUT} = 100 mA
WADJ Mirror Current Ratio	ΔI	0.002	0.010	0.025	-	I_{OUT} = 50 mA (output)
Output Voltage Clamp (Comparator)	V_{CLP}	5.2	5.5	5.8	V	I_{OUT} = 20 mA (input)
[Reset]						
Detection Voltage	V_{DET}	4.12	4.25	4.38	V	RADJ = Open
Hysteresis Width	V_{HYS}	35	70	150	mV	
Output Delay Time L to H (Power On Reset)	t_{dLH}	1.8	2.3	2.8	ms	V_{OUT} = V_{DET} ± 0.5 V, C_{CT} = 0.01 μF
Low Output Voltage	V_{RST}	-	0.1	0.4	V	V_{OUT} = 4.0 V
Minimum Operating Voltage	V_{OPL}	1.5	-	-	V	
[Watchdog Timer]						
Upper Switching Threshold Voltage	V_{thH}	1.08	1.15	1.25	V	WDT ON, INH = Open
Lower Switching Threshold Voltage	V_{thL}	0.13	0.15	0.17	V	WDT ON, INH = Open
WDT Charge Current	I_{CTC}	3.5	5.0	6.5	μA	WDT ON, INH = Open, V_{CT} = 0 V
WDT Discharge Current	I_{CTD}	0.8	1.3	1.7	μA	WDT ON, INH = Open, V_{CT} = 1.3 V
WDT Watch Time (Note 5)	t_{WH}	6.4	8.0	9.6	ms	WDT ON, INH = Open, C_{CT} = 0.01 μF (Ceramic Cap)
WDT Reset Time (Note 5)	t_{WL}	1.6	2.0	2.4	ms	
WDT Operating Current (Note 6)	I_{OA}	0.3	1.7	4.0	mA	WDT ON, INH open, 5 kΩ resistor is placed between WADJ and OUT pins.
[INH]						
WDT OFF Threshold Voltage	V_{HINH}	V_{OUT} ×0.8	-	V_{OUT}	V	
WDT ON Threshold Voltage	V_{LINH}	0	-	V_{OUT} ×0.3	V	Pulled down inside the IC when INH = open
INH Input Current	I_{INH}	-	15	30	μA	V_{INH} = 5 V
[CLK]						
CLK OFF Threshold Voltage	V_{LCLK}	0	-	V_{OUT} ×0.3	V	
CLK ON Threshold Voltage	V_{HCLK}	V_{OUT} ×0.8	-	V_{OUT}	V	
CLK Input Pulse Width	t_{WCLK}	500	-	-	ns	

(Note 5) Characteristics of ceramic cap not considered.
(Note 6) Characteristics of external resistor not considered.

Typical Performance Curves
(Unless otherwise specified, Ta = 25 °C, V_{CC} = 13.5 V, INH = 5 V, CLK = GND, I_{OUT} = 0 mA)

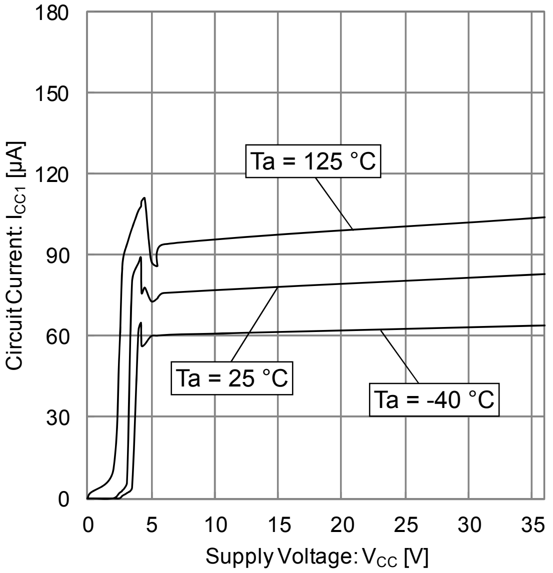


Figure 1. Circuit Current 1 vs Supply Voltage

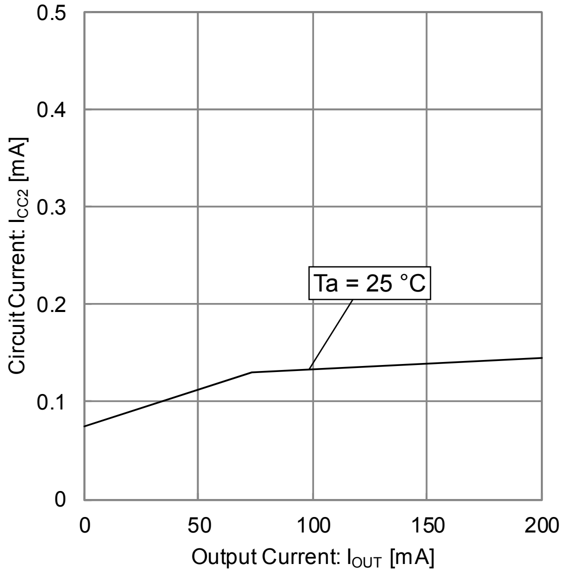


Figure 2. Circuit Current 2 vs Output Current

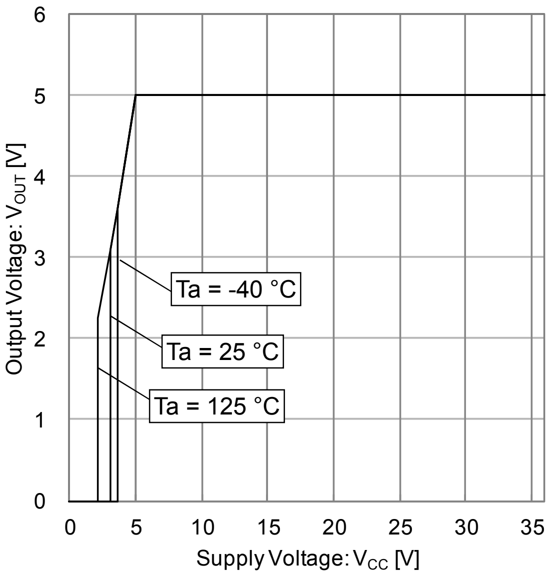


Figure 3. Output Voltage vs Supply Voltage

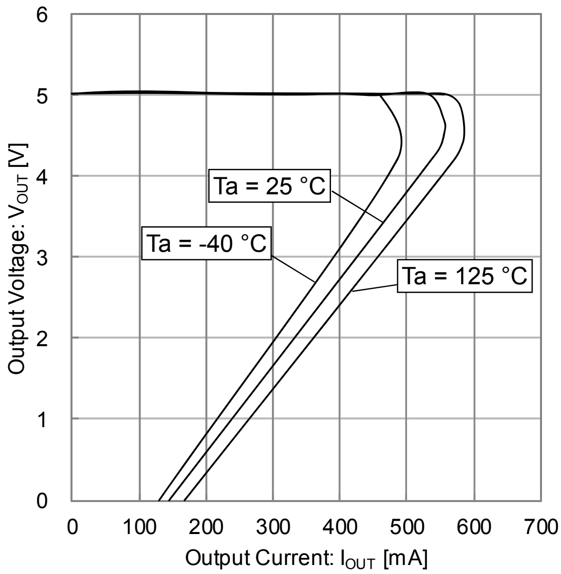


Figure 4. Output Voltage vs Output Current

Typical Performance Curves - continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 13.5 V, INH = 5 V, CLK = GND, I_{OUT} = 0 mA)

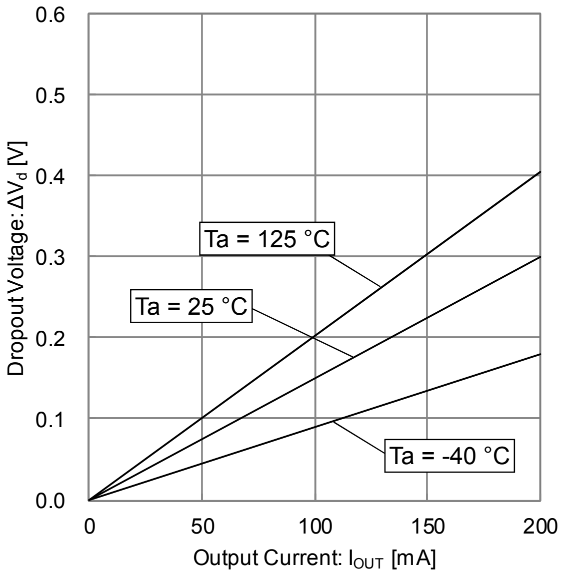


Figure 5. Dropout Voltage vs Output Current
(V_{CC} = 4.75 V)

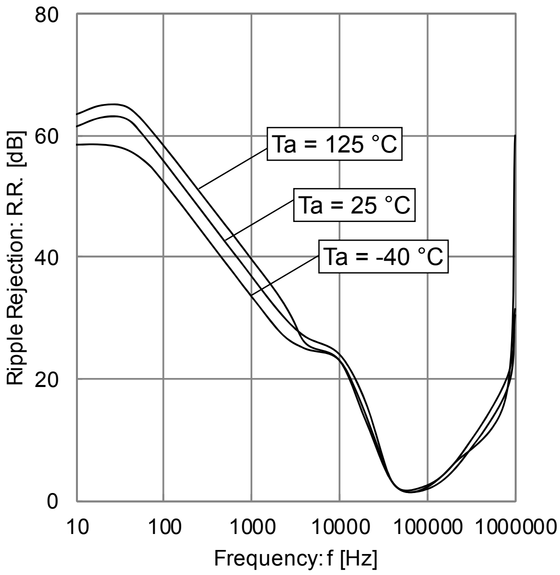


Figure 6. Ripple Rejection vs Frequency
(ein = 1 Vrms, I_O = 100 mA)

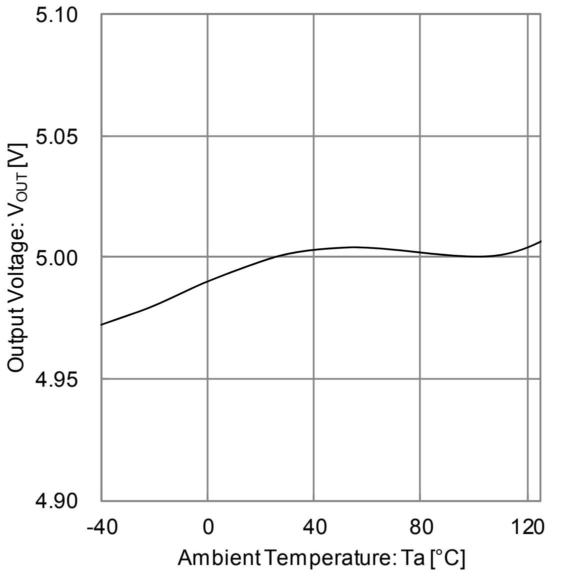


Figure 7. Output Voltage vs Ambient Temperature

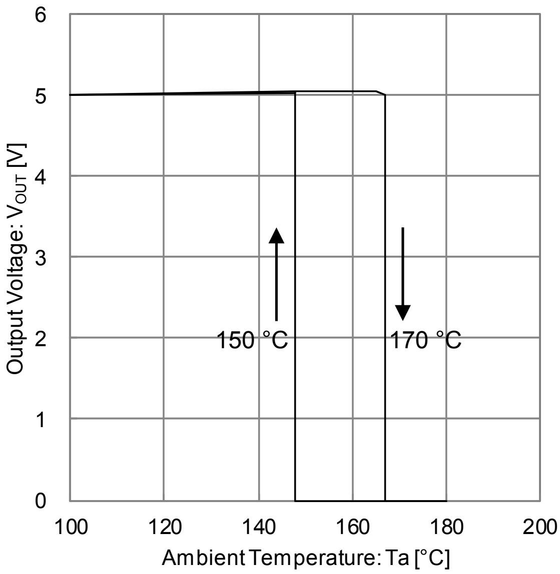


Figure 8. Output Voltage vs Ambient Temperature

Typical Performance Curves – continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 13.5 V, INH = 5 V, CLK = GND, I_{OUT} = 0 mA)

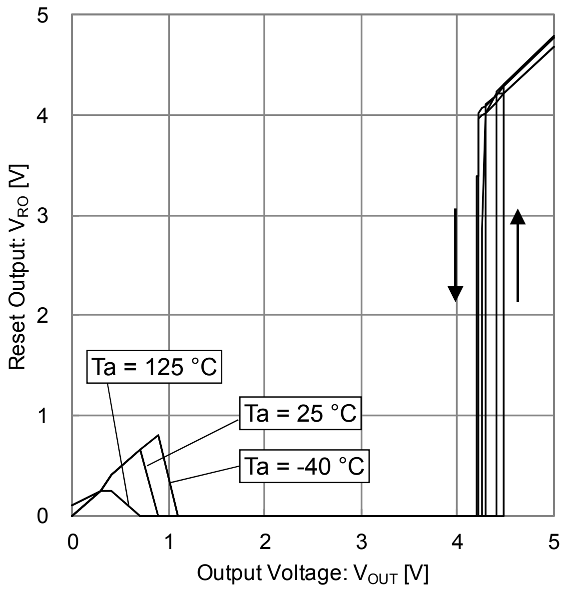


Figure 9. Reset Output vs Output Voltage
(RADJ = Open)

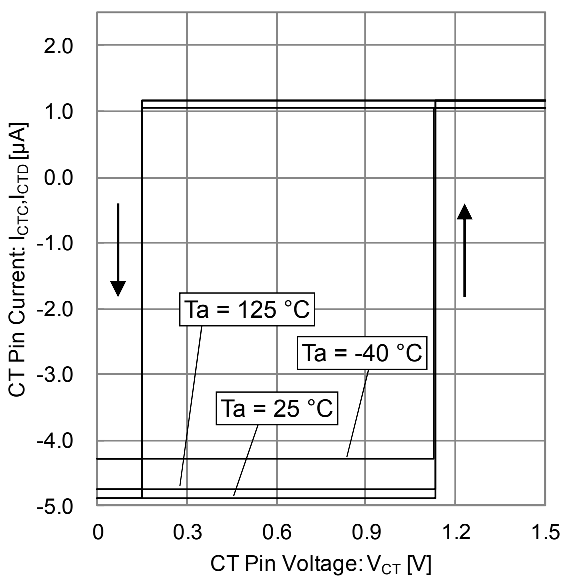


Figure 10. CT Pin Current vs CT Pin Voltage
(V_{CC} = 5 V, INH = Open)

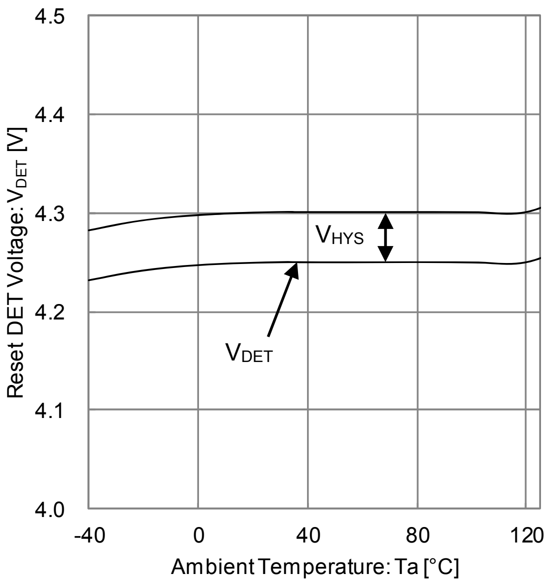


Figure 11. Reset DET Voltage vs Ambient Temperature

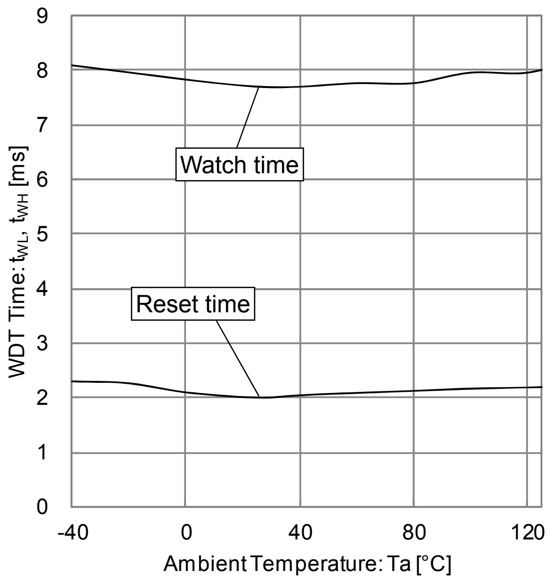


Figure 12. WDT Time vs Ambient Temperature
(C_{CT} = 0.01 μF, V_{CC} = 5 V, INH = Open)

Typical Performance Curves – continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 13.5 V, INH = 5 V, CLK = GND, I_{OUT} = 0 mA)

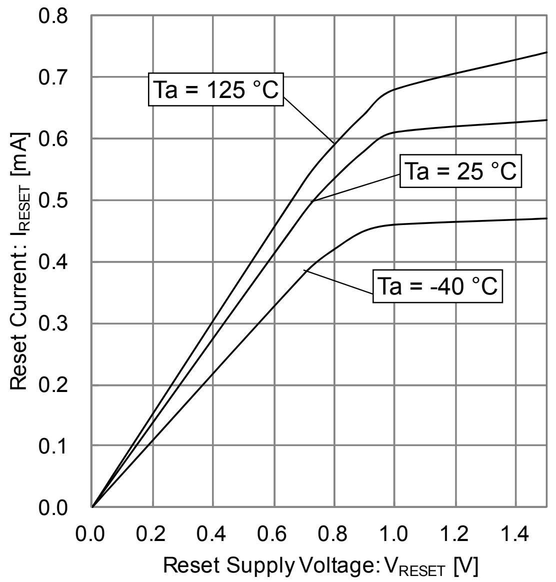


Figure 13. Reset Current vs Reset Supply Voltage
(V_{OUT} = 1.5 V, V_{RO} = 0.5 V)

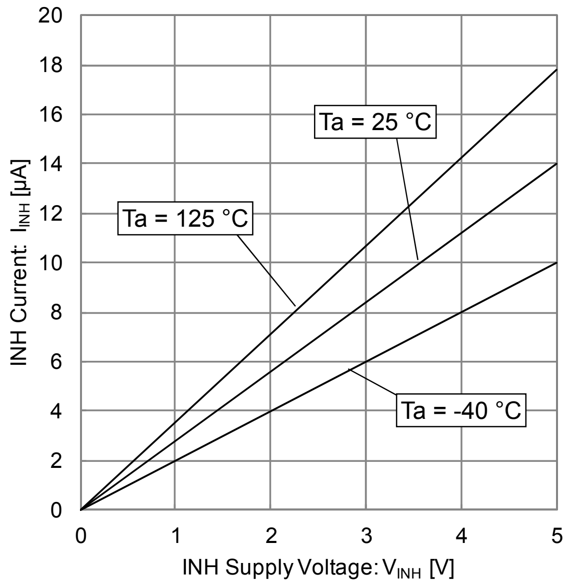


Figure 14. INH Current vs INH Supply Voltage

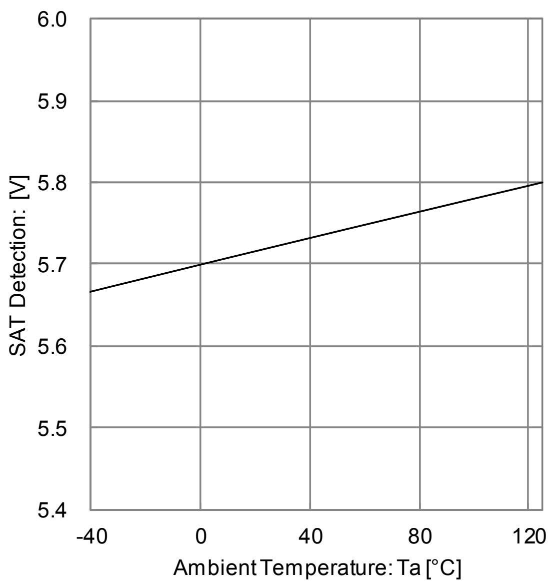


Figure 15. SAT Detection vs Ambient Temperature
(INH = Open)

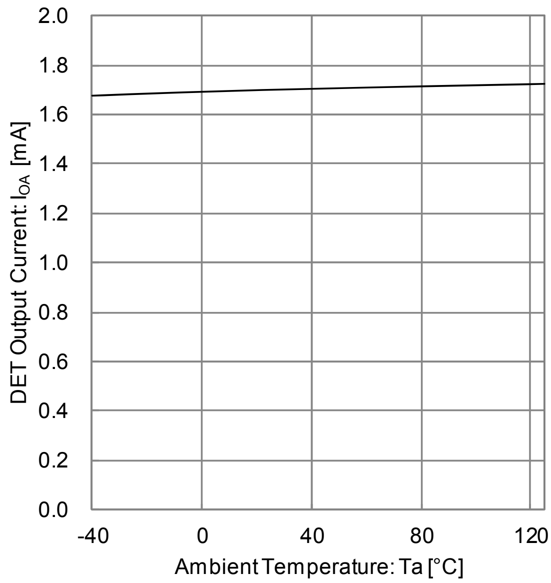


Figure 16. DET Output Current vs Ambient Temperature
(WADJ - OUT = 5 kΩ, INH = Open)

Typical Performance Curves – continued

(Unless otherwise specified, Ta = 25 °C, V_{CC} = 13.5 V, INH = 5 V, CLK = GND, I_{OUT} = 0 mA)

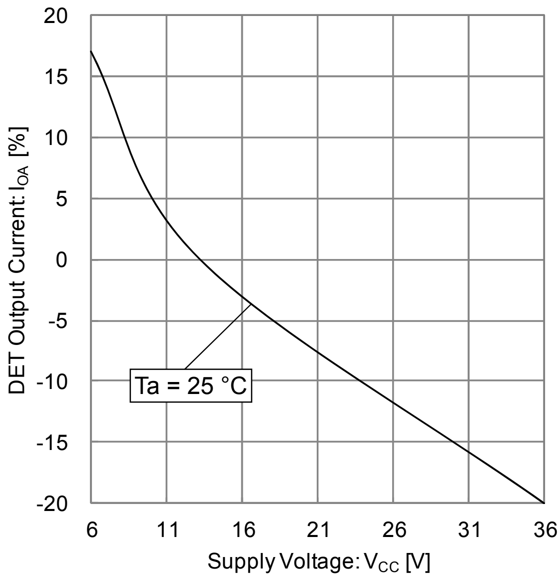
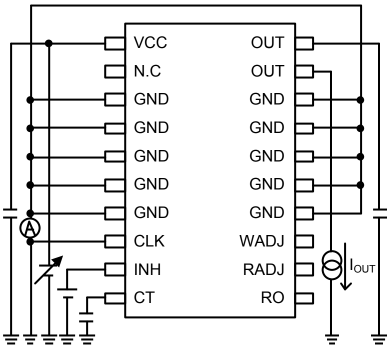
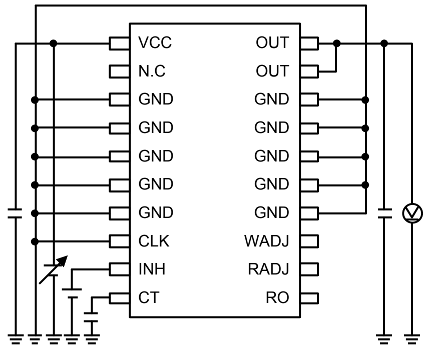


Figure 17. DET Output Current vs Supply Voltage
(WADJ - OUT = 5 kΩ, INH =Open)

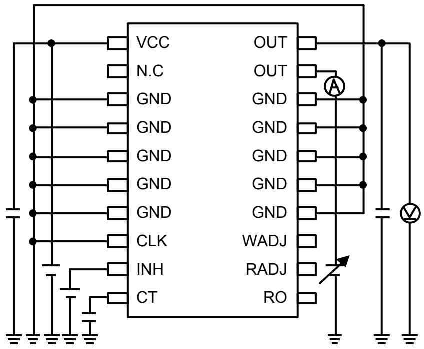
Measurement Circuit for Electrical Data



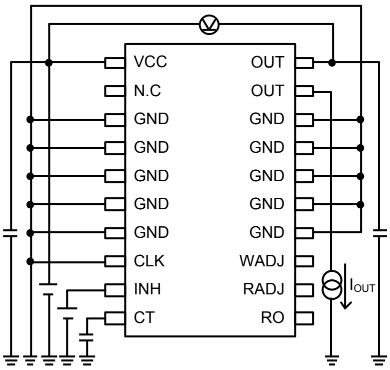
Measurement Circuit of Figure1
and Figure 2



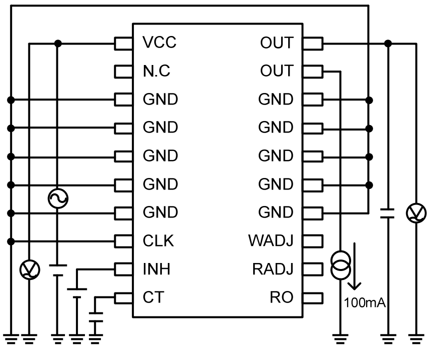
Measurement Circuit of Figure3,
Figure 7 and Figure 8



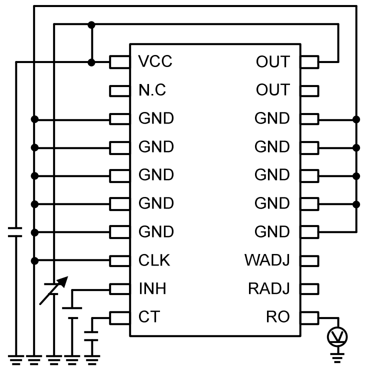
Measurement Circuit of Figure 4



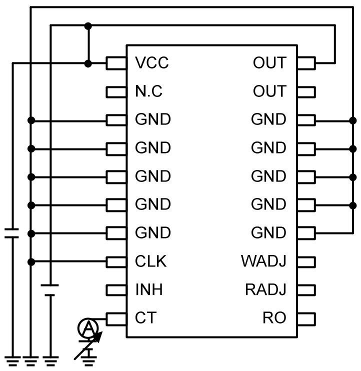
Measurement Circuit of Figure 5



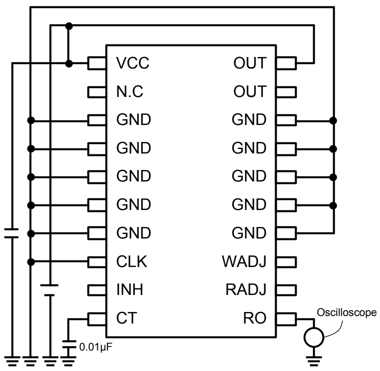
Measurement Circuit of Figure 6



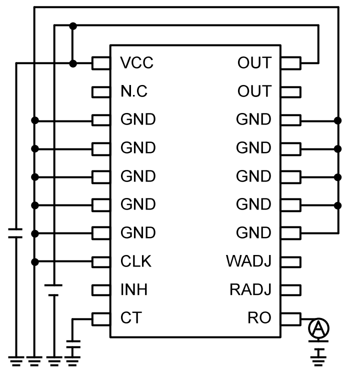
Measurement Circuit of Figure9
and Figure 11



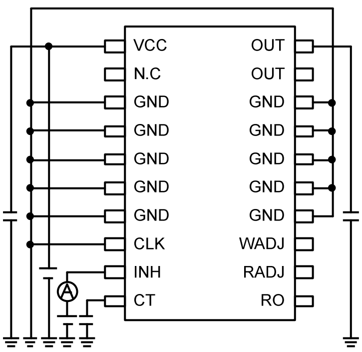
Measurement Circuit of Figure 10



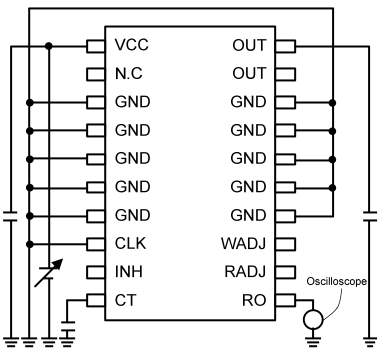
Measurement Circuit of Figure 12



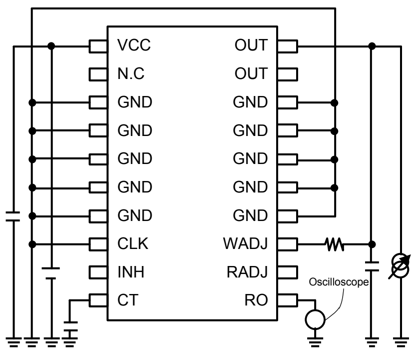
Measurement Circuit of Figure 13



Measurement Circuit of Figure 14



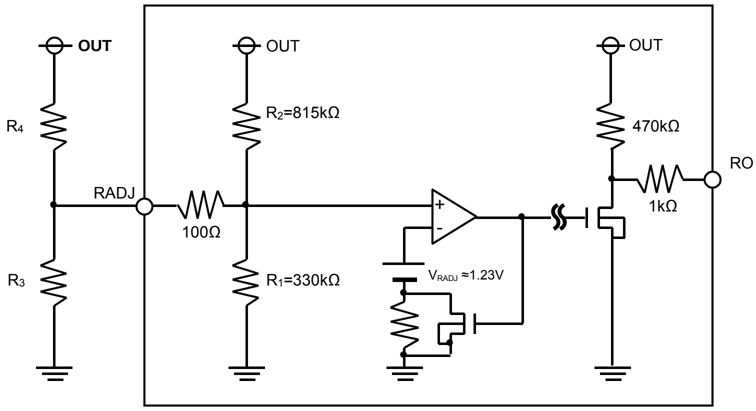
Measurement Circuit of Figure 15



Measurement Circuit of Figure16
and Figure 17

Application Information

1. Detection Voltage Adjustment (Resistance Value is Typical Value)



IC Internal Block Diagram

When typical detection voltage is 4.25 V

$$\mathrm{V}_{DET} \approx V_{RADJ} \times (R_1 + R_2) \;/\; R_1$$

where:
V_{DET} is the reset detection voltage
V_{RADJ} is the internal reference voltage (MOS input)
R_1, R_2 is the IC internal resistor (Voltage detection precision is tightened up to ±3 % by laser-trimming R_1 and R_2)

V_{RADJ} will fluctuate 1.23 V ±6.0 %
Insert pull down resistor R_3 (lower resistance than R_1) in between RADJ-GND, and pull-down resistor R_4 (lower resistance than R_2) in between RADJ-OUT to adjust the detection voltage.
By doing so, the detection voltage can be adjusted using the formula below.

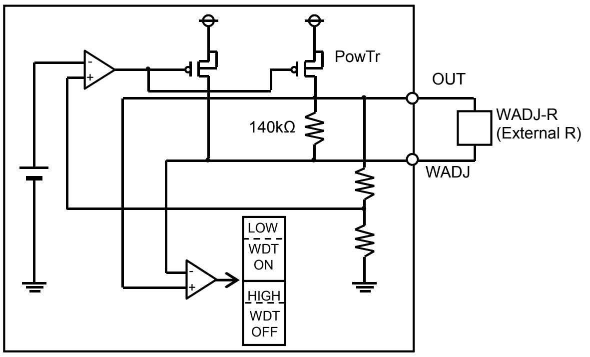
$$\mathrm{V}_{DET} = V_{RADJ} \times [\{R_2 \times R_4/(R_2 + R_4)\} + \{R_1 \times R_3/(R_1 + R_3)\}]/\{R_1 \times R_3/(R_1 + R_3)\}$$

When the output resistance value is as small enough to ignore the IC internal resistance, you can find the detection voltage by the formula below.

$$\mathrm{V}_{DET} \approx V_{RADJ} \times (R_3 + R_4) \;/\; R_3$$

Adjust the resistance value by application as the circuit current increases due to the added resistor.

2. WDT Voltage Detection (Resistance Value is Typical Value)



IC Internal Block Diagram

WDT can be automatically switched ON/OFF by the output load current. To detect the output load current, insert a resistor between OUT-WADJ. Current detection is adjustable by varying the resistance value from 1 kΩ to 15 kΩ.

Calculation:

I_{OUT} (Desired load current value) × ΔI (WADJ current mirror ratio) × (External R / 140 kΩ (Note 1)) ≥ 100 mV (Note 2)

(Note 1) is the IC internal resistance between WADJ - OUT (tolerance approx ±30 %, temperature coefficient approx 2000 ppm)

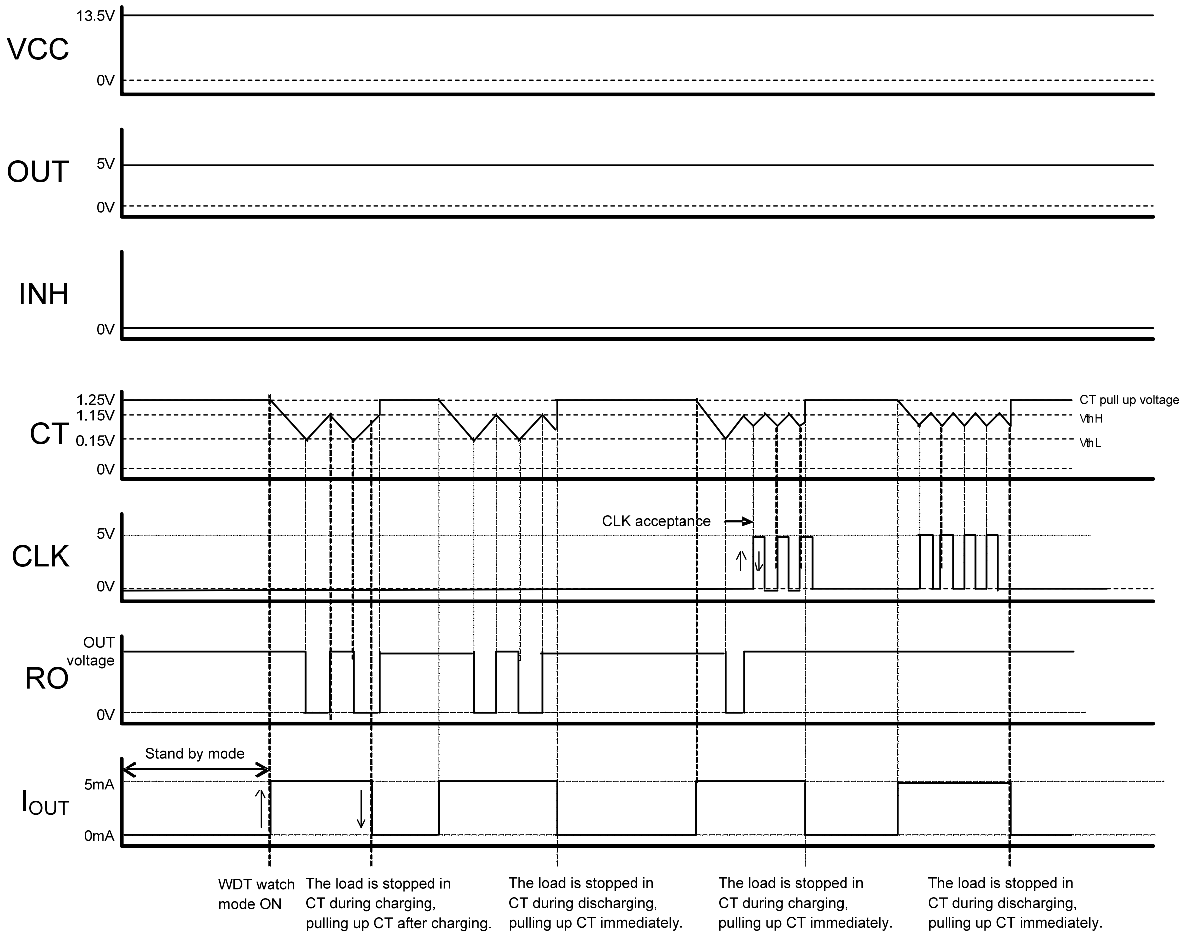
(Note 2) is an offset of the detection comparator (tolerance approx 100 mV ±10 %)

When there is no resistor between WADJ - OUT, I_{OUT} = 70 µA can be detected by the formula below

I_{OUT} (Desired load current value) × ΔI (WADJ current mirror ratio) × 140 kΩ ≥ 100 mV

(Note) If the OUT - WADJ resistance value is not same as the condition on the electrical characteristics table, i.e. 5 KΩ, choose the resistance value in ratio referring to the above equation.

<Timing Chart> Timing Chart on no load condition (Stand-by Mode)



3. Power ON Reset

Power ON reset (output delay time) is adjustable by CT pin capacitor.

$$t_{dLH}(S) \approx 1.15V \times CT\ capacitance(\mu F)/I_{CTC}(\mu A) \quad (Typ)$$

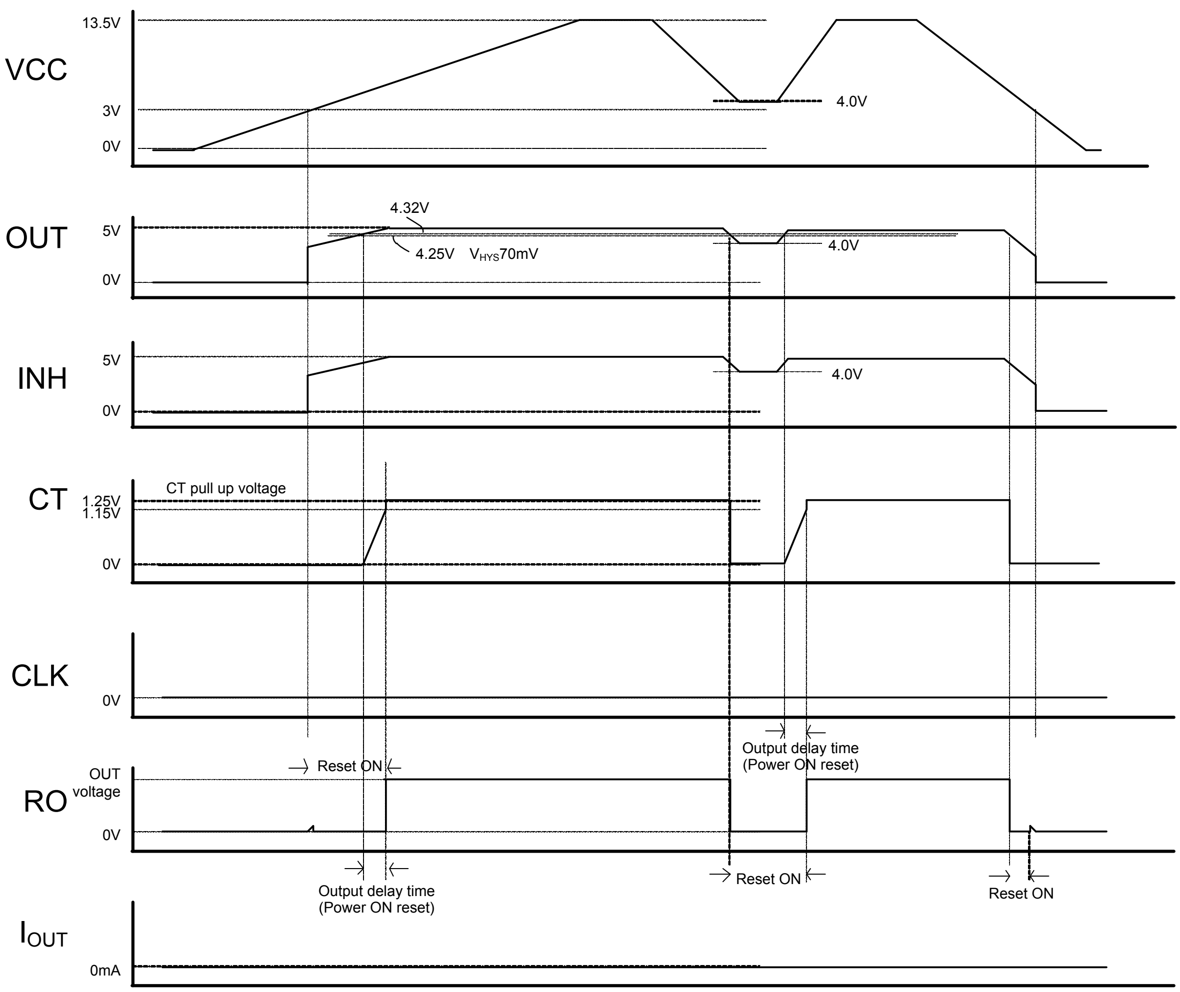
where:
t_{dLH} is the output delay time (power ON reset)
$1.15\ V$ is the upper switching threshold voltage (Typ)
$CT\ capacitance$ is the capacitor connected to CT pin
I_{CTC} is the WDT charge current

<Calculation example > with 0.01 µF CT pin capacitor

$$t_{dLH}(S) = 1.15V \times 0.01\mu F/5.0\mu A$$
$$\approx 2.3msec$$

If the CT capacitance is not the same as the condition on the electrical characteristics table, i.e., 0.01 µF, choose the capacitance value in ratio referring to the above equation.

<Timing Chart> Note: Watchdog Timer OFF (INH ON)



4. Watchdog Timer

Watch Dog Timer (WDT watch time, reset time) is adjustable by the CT pin capacitor

$$t_{WH}(S) \approx 1.00V \times CT\ capacitance(\mu F))/I_{CTD}(\mu A) \quad (Typ)$$

$$t_{WL}(S) \approx 1.00V \times CT\ capacitance(\mu F))/I_{CTC}(\mu A) \quad (Typ)$$

where:
t_{WH} is the WDT watch time (delay time to turn the reset ON)
t_{WL} is the WDT reset time (time the reset is ON)
$1.00V$ is the upper switching threshold voltage - lower switching threshold voltage
$CT\ capacitance$ is the CT pin capacitor (Shared with power ON reset)
I_{CTC} is the WDT charge current
I_{CTD} is the WDT discharge current

WDT time's accuracy is ±20 % by trimming

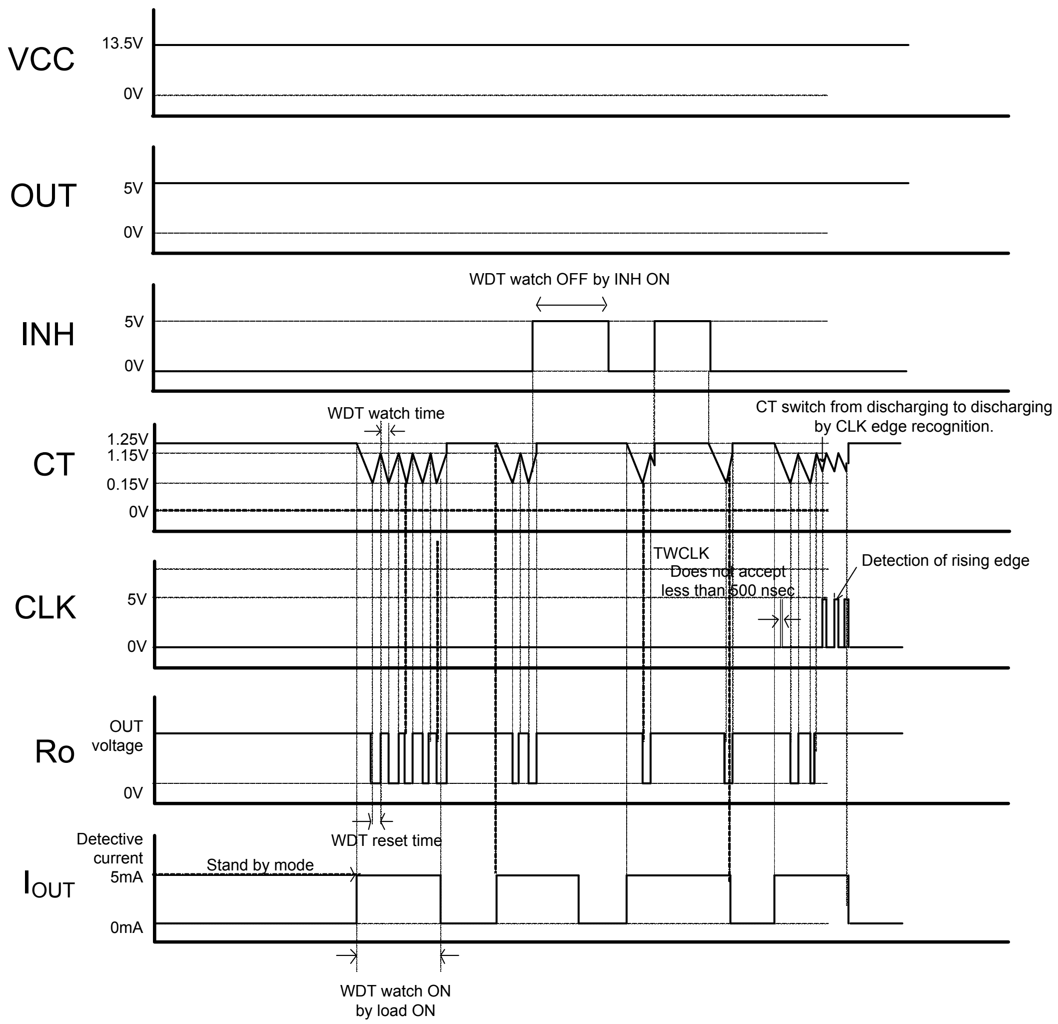
<Calculation example > with 0.01 μF CT pin capacitor

$$t_{WH}(S) \approx 1.00V \times 0.01\mu F/1.3\mu A \approx 8.0msec \quad (Typ)$$

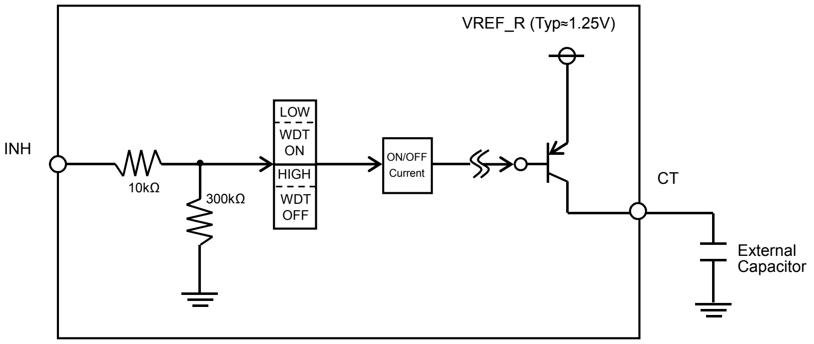
$$t_{WL}(S) \approx 1.00V \times 0.01\mu F/5.0\mu A \approx 2.0msec \quad (Typ)$$

If the CT capacitance is not the same as the condition on the electrical characteristics table, choose the capacitance value in ratio referring to the above equation.

<Timing Chart>



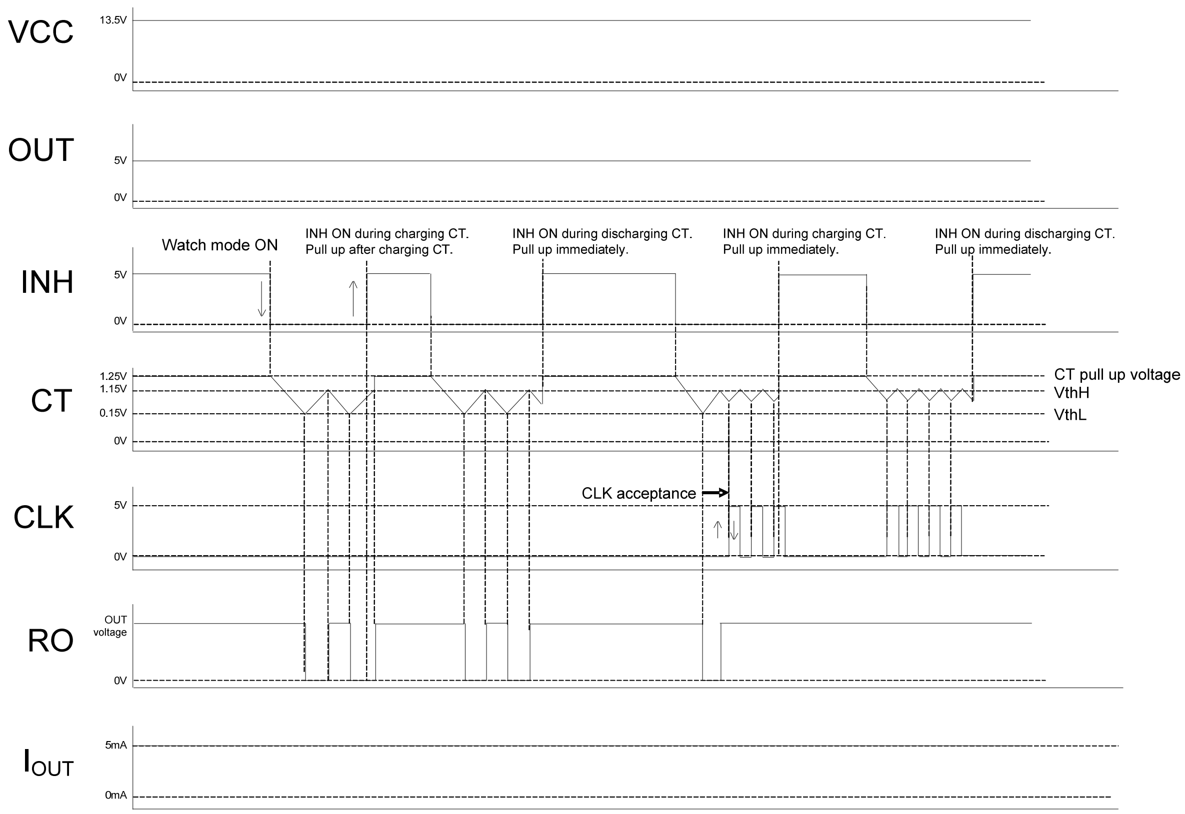
5. WDT timer ON / OFF Switch INH (Resistance Value is Typical Value)
BD3010AFV has a switch INH to turn the WDT ON / OFF



IC Internal Block Diagram

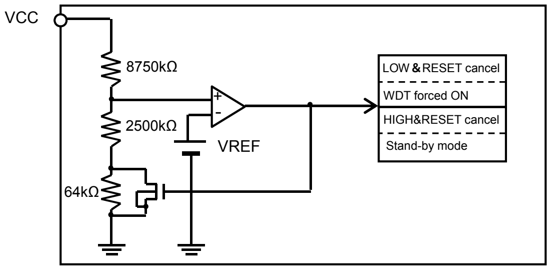
By using INH ON, CT voltage can be pulled up to internal voltage VREF_R (invalid with power ON reset)

<Timing Chart>



6. Forced Watch Mode

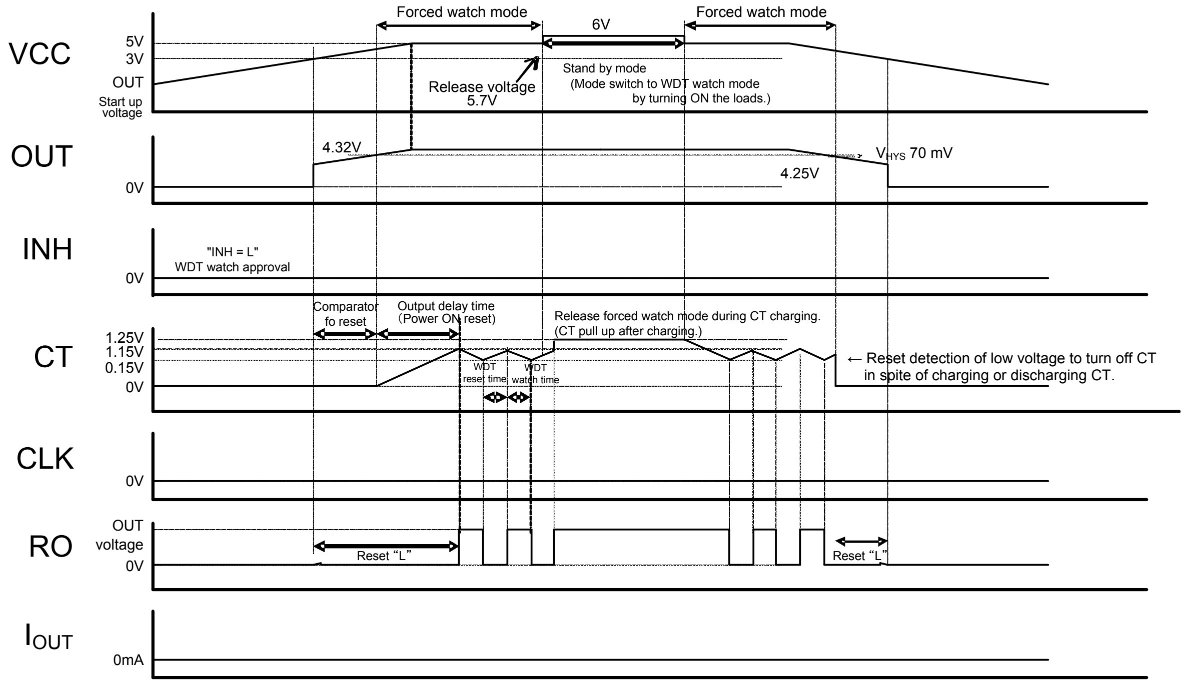
By detecting an input voltage (battery voltage) called output SAT detection, WDT can be forced to be operated.

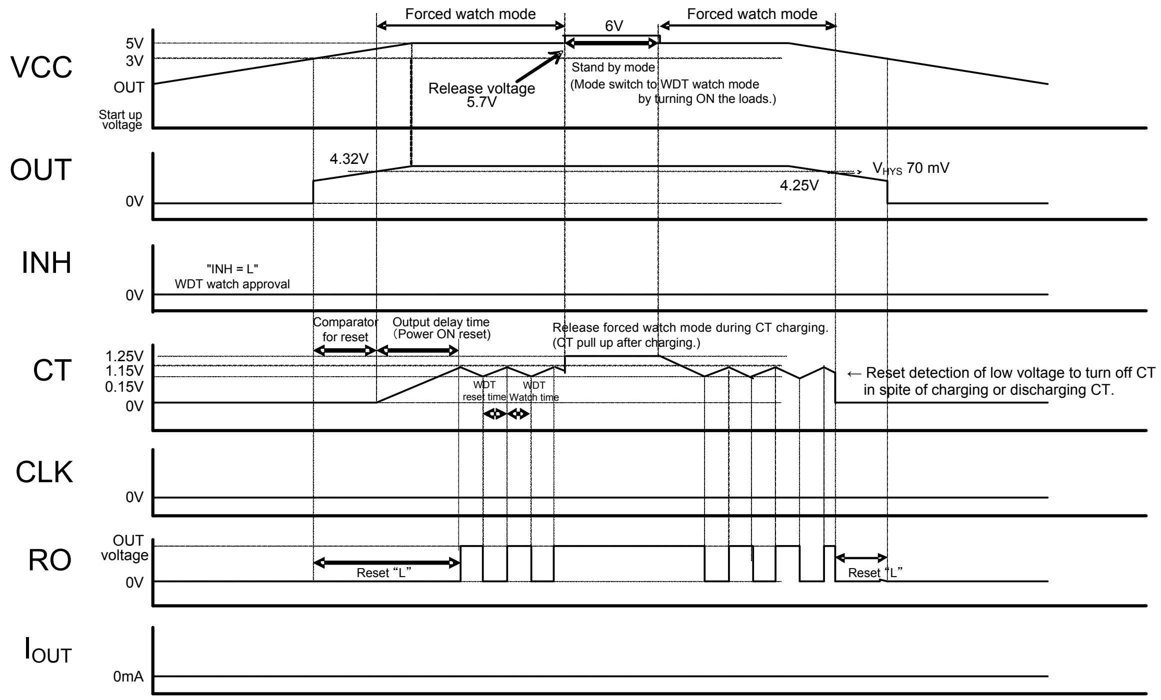


IC Internal Block Diagram

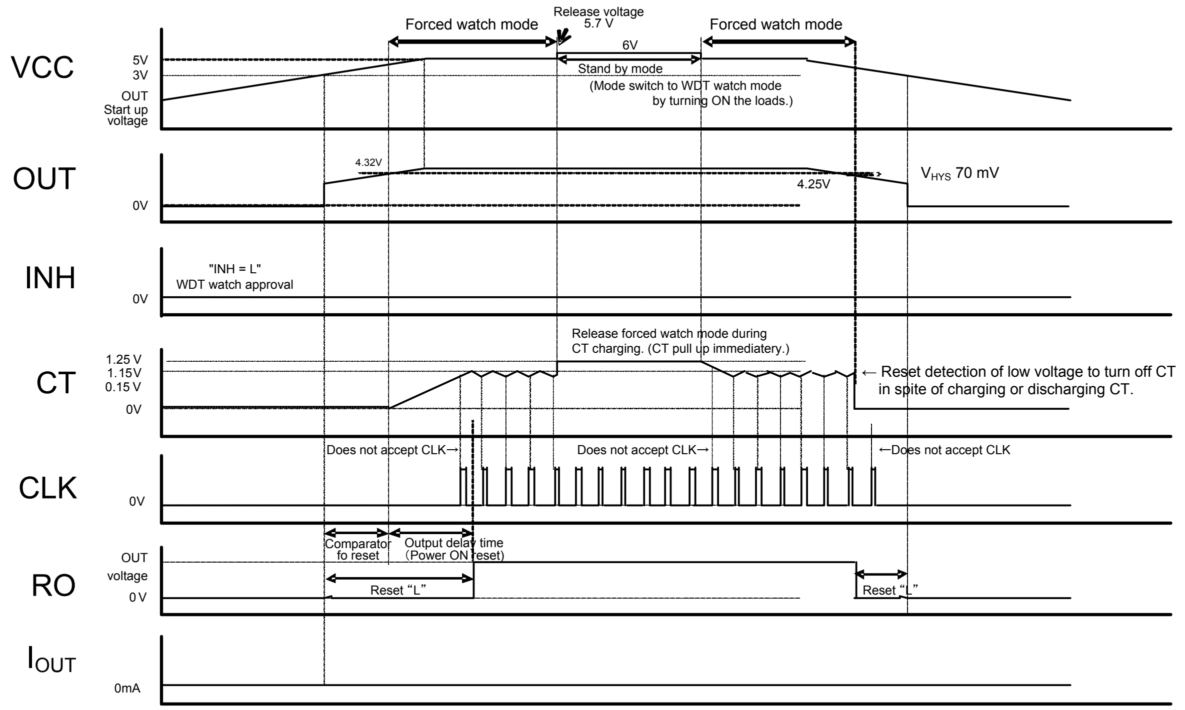
WDT will be forced ON from reset cancellation voltage to $V_{CC}\approx5.7$ V (WDT can be turned OFF by INH)

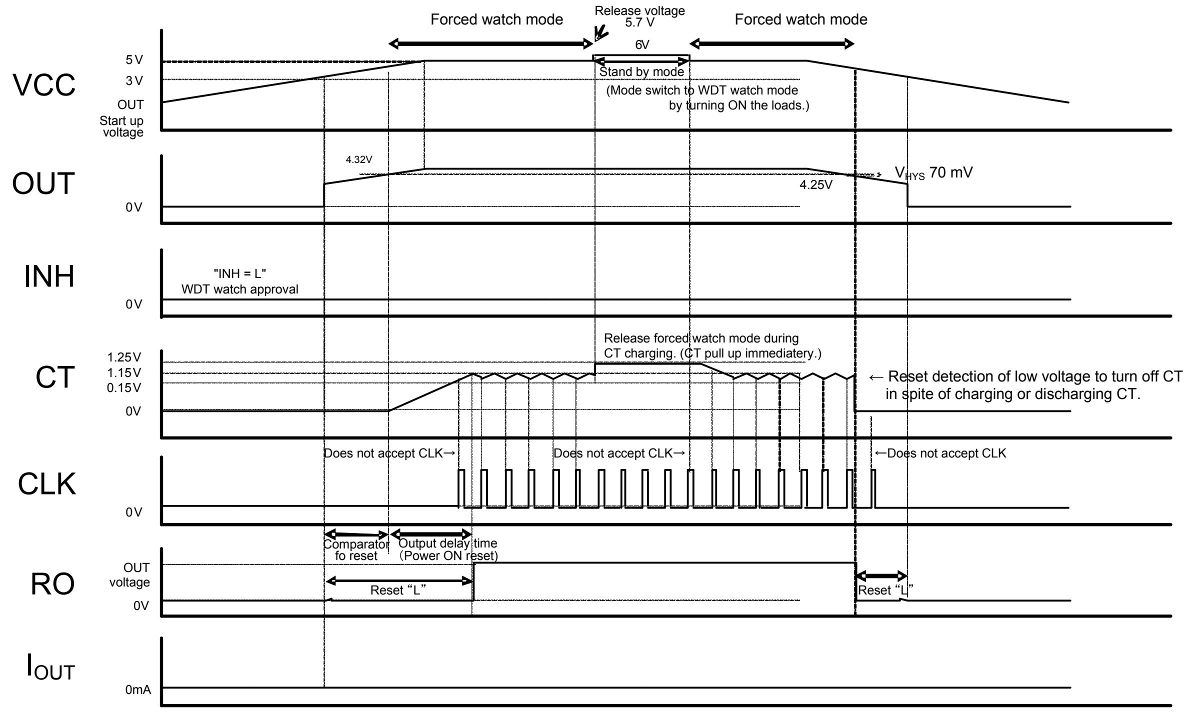
<Timing Chart including Forced Watch Mode> Note: No CLK Signal Input



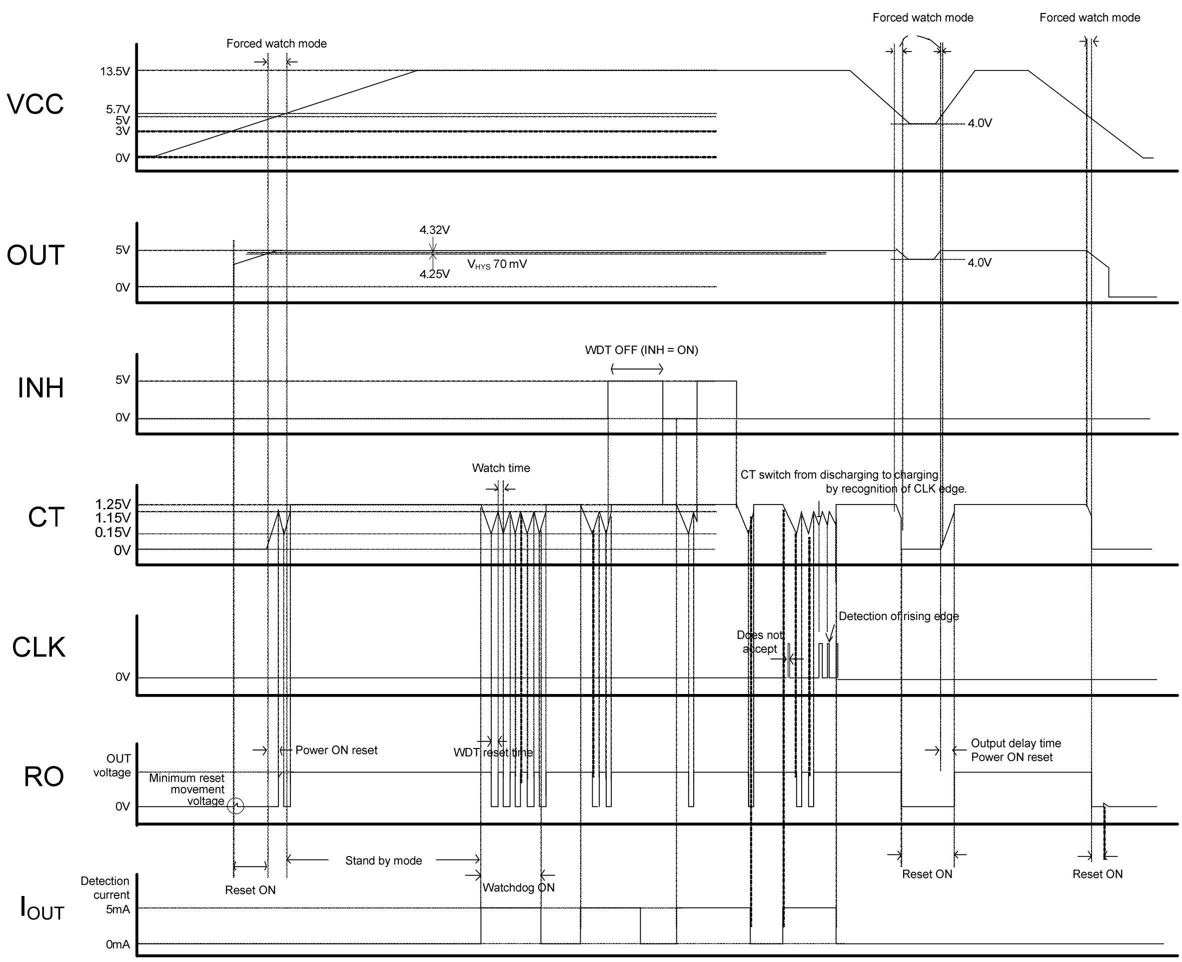


<Timing Chart including Forced Watch Mode>　Note: With CLK Signal Input





<Entire Timing Chart>



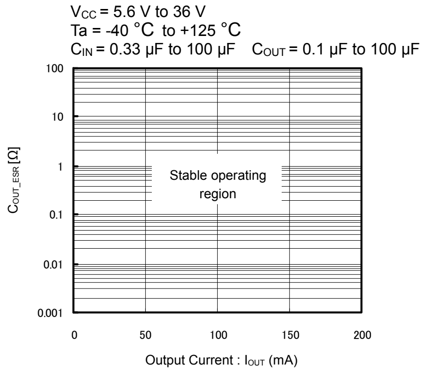
7. Pin Settings / Precautions

(1) VCC Pin

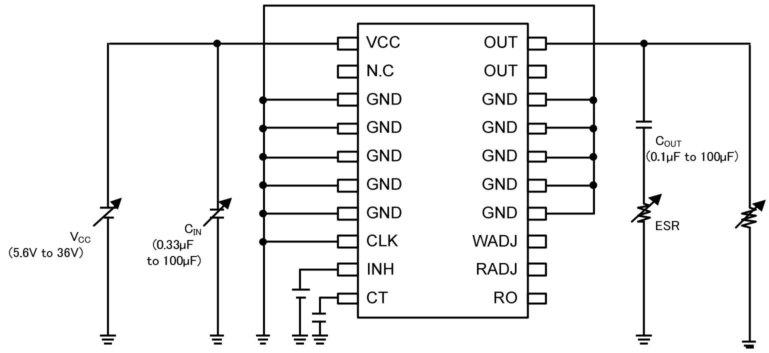
Insert a 0.33 µF to 1000 µF capacitor between the VCC and GND pins. The appropriate capacitance value varies by application. Be sure to allow a sufficient margin for input voltage levels.

(2) Output Pins

It is necessary to place capacitors between each output pin and GND to prevent oscillation on the output. Usable capacitance values range from 0.1 µF to 1000 µF. Abrupt fluctuations in input voltage and load conditions may affect the output voltage. Output capacitance values should be determined only through sufficient testing of the actual application.



C_{OUT_ESR} vs Output Current (Reference Data)



Pin Settings / Precautions (2) Measurement circuit

(3) CT Pin

Connecting a capacitance of 0.01 µF to 1µF on the CT pin is recommended.

Power Dissipation

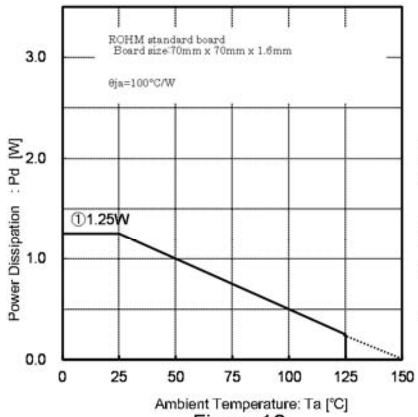


Figure 18

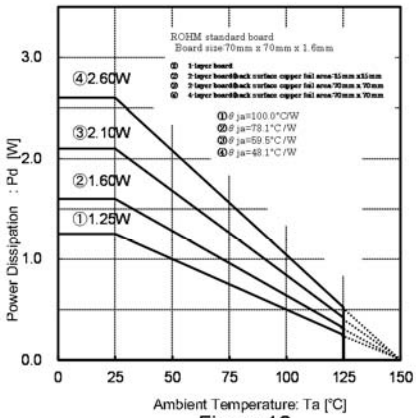


Figure 19
(Reference Data)

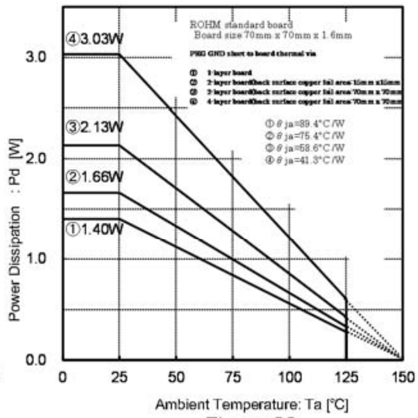


Figure 20
(Reference Data)

(Note) Reduced by 10.0mW/°C over Ta=25°C, when mounted on
70mm x 70mm x 1.6mm glass epoxy board

Refer to thermal dissipation characteristics (Figure 18 to Figure 20) for usage above Ta = 25 °C. The IC's temperature affects heavily the IC's characteristics. If it exceeds its max junction temperature (Tjmax), the chip may degrade or get destroyed. Thermal design is critical in terms of avoiding instantaneous destruction and reliability in long term usage. The IC needs to be operated below its max junction temperature (Tjmax) to avoid thermal destruction. Refer to Figure 18, Figure 19 and Figure 20 for SSOP-B20 package thermal dissipation characteristics. Operate the IC within the allowable power dissipation (Pd) when using this IC.

Power consumption Pc(W) calculation will be as below (for Figure 20④)

$$P_C = (V_{CC} - V_{OUT}) \times I_{OUT} + V_{CC} \times I_{CC2}$$

Power Dissipation Pd ≥ Pc
where:
V_{CC} is the input voltage
V_{OUT} is the output voltage
I_{OUT} is the load current
I_{CC2} is the circuit current

If load current I_{OUT} is calculated to operate within the allowable power dissipation, it will be as below, where you can find the value of the allowable max load current I_{OMAX} for the applied voltage V_{CC} of the thermal design.

$$I_{OUT} \leq \frac{Pd - V_{CC} \times I_{CC2}}{V_{CC} - V_{OUT}}$$

(Refer to Figure 2 for I_{CC2})

Example) at Ta = 85 °C, V_{CC} = 12 V, V_{OUT} = 5 V

$$I_{OUT} \leq \frac{1.578 - 12 \times I_{CC2}}{12 - 5}$$

Figure 20④: θja = 41.3 °C / W → -24.2 mW / °C
25 °C = 3.03 W → 85 °C =1.578 W

$$I_{OUT} \leq 200mA \quad (I_{CC2} = 110\mu A)$$

Refer to above and adjust the thermal design so it will be within the allowable power dissipation within the entire operation temperature range. Below is the power consumption Pc calculation when OUT is shorted to GND.

$$P_C = V_{CC} \times (I_{CC2} + I_{short})$$

where:
I_{short} is the Short current
(Refer to Figure 4. for I_{short})

I/O Equivalence Circuit

(Resistance Value is Typical Value)

<Regulator>

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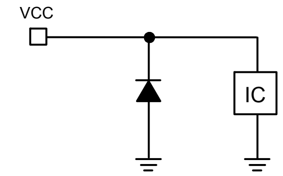
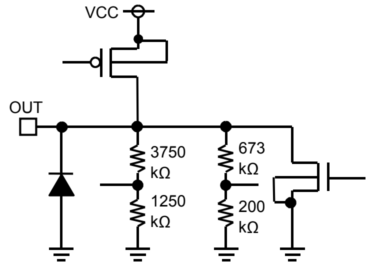
<tr><td>
</td><td>
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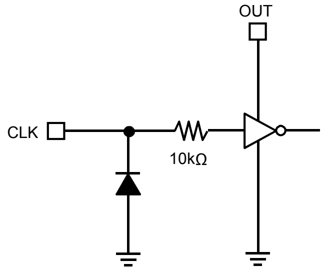
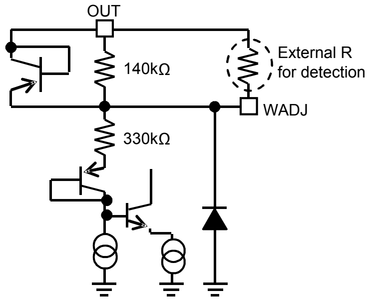
<tr><td>
</td><td>
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<Reset>

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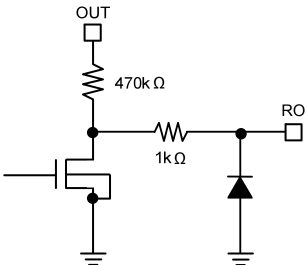
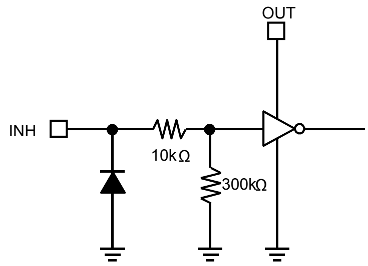
<tr><td>
</td><td>
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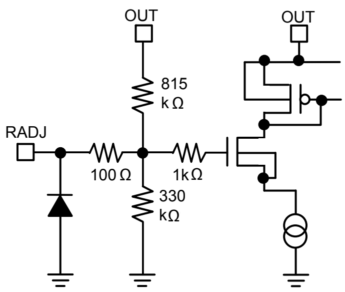
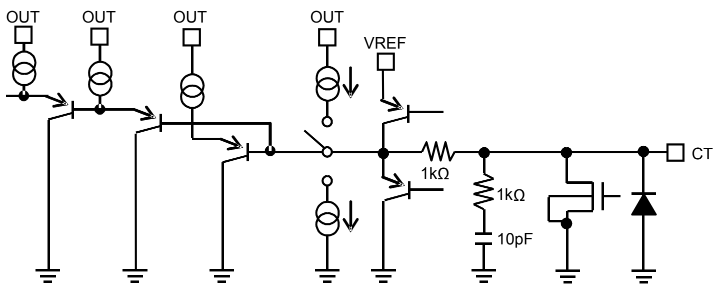
<tr><th>RADJ</th><th>CT</th></tr>
<tr><td>
</td><td>
</td></tr>
</table>

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
   Except for pins the output of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. **Regarding the Input Pin of the IC**
    This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

    When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
    When GND > Pin B, the P-N junction operates as a parasitic transistor.

    Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

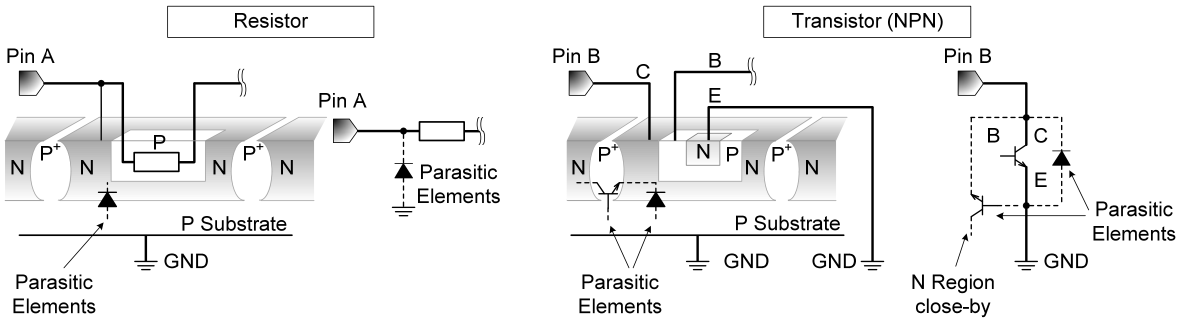


Figure 21. Example of monolithic IC structure

13. **Thermal Shutdown Circuit(TSD)**
    This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
    Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. **Over Current Protection Circuit (OCP)**
    This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

15. **Thermal Consideration**
    Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions. Consider Pc that does not exceed Pd in actual operating conditions (Pc≥Pd).

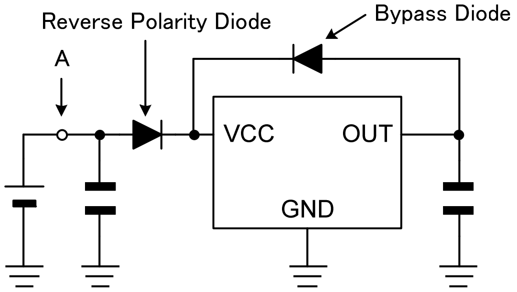
Package Power dissipation $$Pd(W) = (T_{jmax} - Ta)/\theta_{ja}$$

Power dissipation $$Pc(W) = (V_{CC} - V_{OUT}) \times I_{OUT} + V_{CC} \times I_{CC2}$$

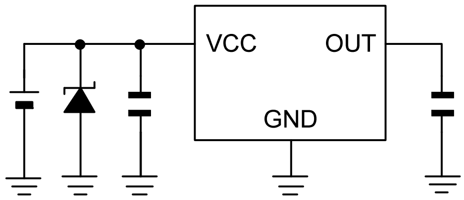
where:
$Tjmax$ is the Maximum junction temperature=150°C,
Ta is the Peripheral temperature[°C] ,
θja is the Thermal resistance of package-ambience[°C /W],
Pd is the Package Power dissipation [W],
Pc is the Power dissipation [W],
V_{CC} is the Input Voltage,
V_{OUT} is the Output Voltage,
I_{OUT} is the Load,
I_{CC2} is the Bias Current

Operational Notes – continued

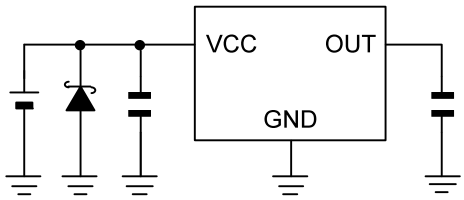
16. In some application or process testing, the voltage on the VCC or other pins may be reversed. If a large capacitor is connected between the output and ground, the current from the charged capacitor can flow to the output and possibly damage the IC. In order to avoid these problems, limiting output pin capacitance to 1000 μF or less and inserting a VCC series countercurrent prevention diode or bypass diode between the various pins and the VCC is recommended.



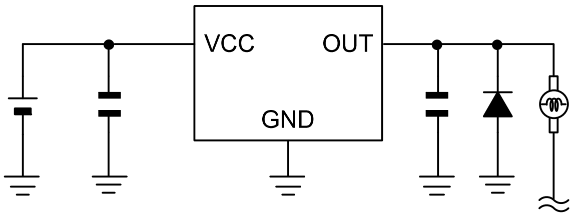
17. Positive Voltage Surges on VCC Pin
A power Zener diode should be inserted between V_{CC} and GND for protection against voltage surges of more than 50V on the VCC pin.



18. Negative Voltage Surges on VCC Pin
A schottky barrier diode should be inserted between VCC and GND for protection against voltages lower than GND on the VCC pin.



19. Output Protection Diode
Output loads with large inductive component may cause reverse current flow during startup or shutdown.
In such cases, a protection diode should be inserted on the output to protect the IC.



Ordering Information

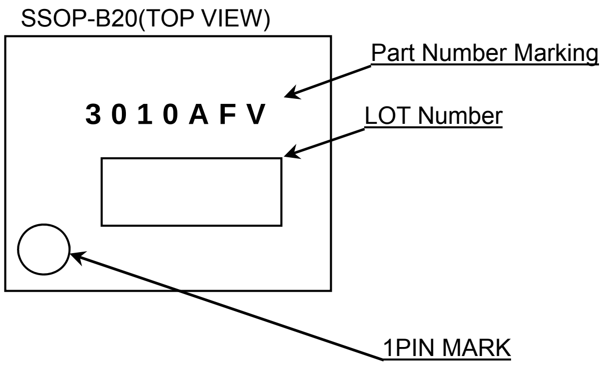
B	D	3	0	1	0	A	F	V	-	E2

Part Number

Package
FV: SSOP-B20

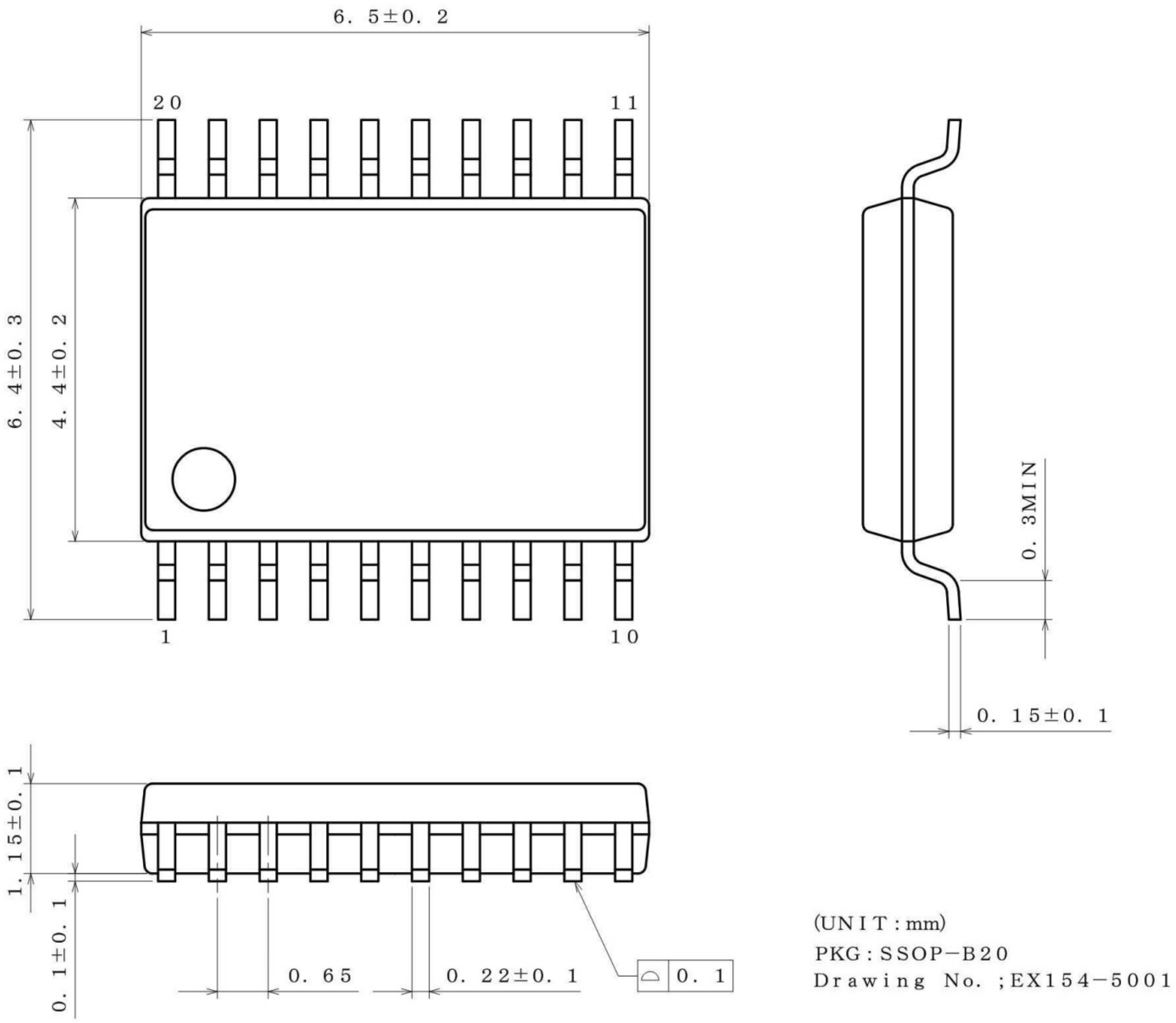
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



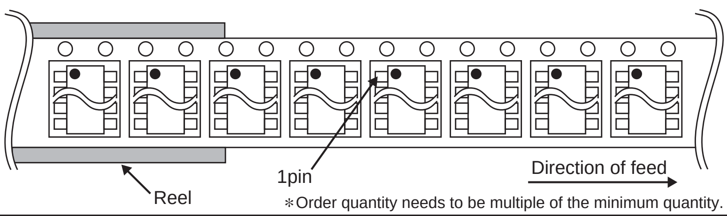
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B20



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
15.Jan.2016	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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Part Number	BD3010AFV
Package	SSOP-B20
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes