MICROCHIP

AVR® DA

Product Brief

Introduction

The AVR® DA family of microcontrollers is using the AVR® CPU with hardware multiplier, running at up to 24 MHz, with 32/64/128 KB of Flash, 4/8/16 KB of SRAM, and 512 bytes of EEPROM in 28-, 32-, 48- or 64-pin packages. The family uses the latest technologies from Microchip with a flexible and low-power architecture including Event System, accurate analog features, advanced digital peripherals and Peripheral Touch Controller (PTC).

Features

- AVR® CPU:
  - Running at up to 24 MHz
  - Single-cycle I/O access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
  - Supply voltage range: 1.8V to 5.5V
- Memories:
  - 32/64/128 KB In-system self-programmable Flash memory
  - 4/8/16 KB SRAM
  - 512B EEPROM
  - 32B of user row in nonvolatile memory that can keep data during chip-erase and be programmed while the device is locked
  - Write/erase endurance
    - Flash 10,000 cycles
    - EEPROM 100,000 cycles
  - Data retention: 40 years at 55°C
- System:
  - Power-on Reset (POR) circuit
  - Brown-out Detector (BOD)
  - Clock options
    - High-precision internal High-Frequency Oscillator with selectable frequency up to 24 MHz (OSCHF)
      - Auto-tuning for improved internal oscillator accuracy
    - Internal PLL up to 48 MHz for high-frequency operation of Timer/Counter type D (PLL)
    - 32.768 kHz ultra low-power internal oscillator (OSC32K)
    - 32.768 kHz external crystal oscillator (XOSC32K)
    - External clock input
  - Single-pin Unified Program and Debug Interface (UPDI)
  - Three sleep modes
    - Idle, with all peripherals running for immediate wake-up
    - Standby
      - Configurable operation of selected peripherals
    - Power-Down with full data retention

- Peripherals:
  - Up to two 16-bit Timer/Counter type A (TCA) with dedicated period register and three PWM channels
  - Up to five 16-bit Timer/Counter type B (TCB) with input capture and simple PWM functionality
  - One 12-bit Timer/Counter type D (TCD) optimized for power control
  - One 16-bit Real-Time Counter (RTC) running from external crystal or internal oscillator
  - Up to six USART with fractional Baud Rate Generator, auto-baud, and start-of-frame detection
  - Two Master/Slave Serial Peripheral Interface (SPI)
  - Up to two Two-Wire Interface (TWI) with dual address match
    - Independent master and slave operation (dual mode)
    - Philips I^2C compatible
    - Standard mode (Sm, 100 kHz)
    - Fast mode (Fm, 400 kHz)
    - Fast mode plus (Fm+, 1 MHz) (1)
  - Event System for CPU independent and predictable inter-peripheral signaling
  - Configurable Custom Logic (CCL) with up to six programmable Look-up Tables (LUT)
  - One 12-bit differential 130 ksps Analog-to-Digital Converter (ADC)
  - Three Analog Comparators (ACs) with window compare functions
  - One 10-bit Digital-to-Analog Converter (DAC)
  - Up to three Zero-Cross Detectors (ZCD)
  - Multiple voltage references (VREF)
    - 1.024V
    - 2.048V
    - 2.500V
    - 4.096V
  - Peripheral Touch Controller (PTC) with Driven Shield+ and Boost Mode Technologies for capacitive touch buttons, sliders, wheels and 2D surface.
    - Up to 46 self-capacitance and 529 mutual-capacitance channels
  - Automated Cyclic Redundancy Check (CRC) Flash memory scan
  - Watchdog Timer (WDT) with Window mode, with a separate on-chip oscillator
  - External interrupt on all general purpose pins
- I/O and Packages:
  - Up to 55 programmable I/O pins
  - 28-pin SPDIP, SSOP and SOIC
  - 32-pin VQFN 5x5 mm and TQFP 7x7 mm
  - 48-pin VQFN 6x6 mm and TQFP 7x7 mm
  - 64-pin VQFN 9x9 mm and TQFP 10x10 mm
- Temperature Ranges:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

Note:

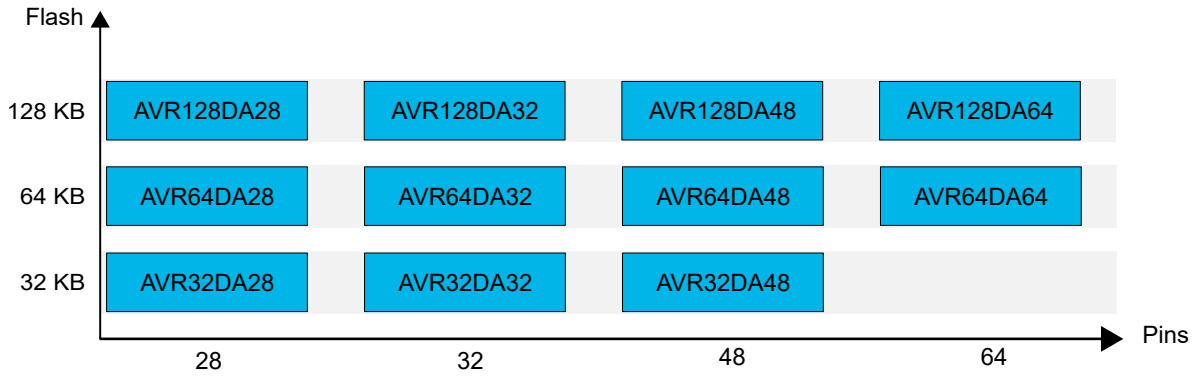
1. I^2C Fm+ is only supported for above 2.7V.

AVR® DA Family Overview

The figure below shows the AVR® DA devices, laying out pin count variants and memory sizes:

- Vertical migration is possible without code modification, as these devices are fully pin and feature compatible
- Horizontal migration to the left reduces the pin count, and therefore, the available features

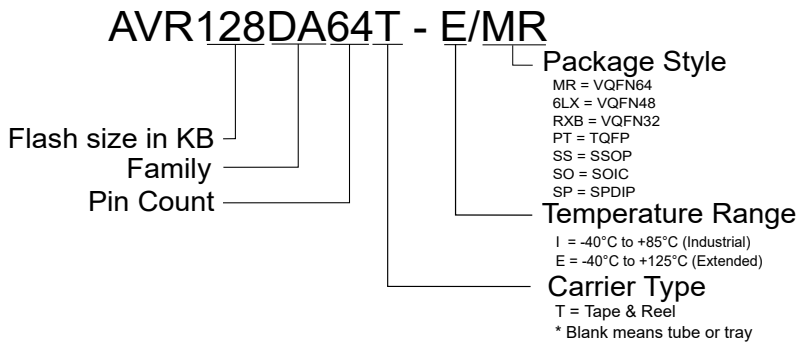
Figure 1. AVR® DA Family Overview



Devices with different Flash memory size typically also have different SRAM.

The name of a device in the AVR® DA family is decoded as follows:

Figure 2. AVR® DA Device Designations



Memory Overview

Table 1. Memory Overview

Devices	AVR32DA48 AVR32DA32 AVR32DA28	AVR64DA64 AVR64DA48 AVR64DA32 AVR64DA28	AVR128DA64 AVR128DA48 AVR128DA32 AVR128DA28
Flash memory	32 KB	64 KB	128 KB
SRAM	4 KB	8 KB	16 KB
EEPROM	512B	512B	512B
User row	32B	32B	32B

Peripheral Overview

Table 2. Peripheral Overview

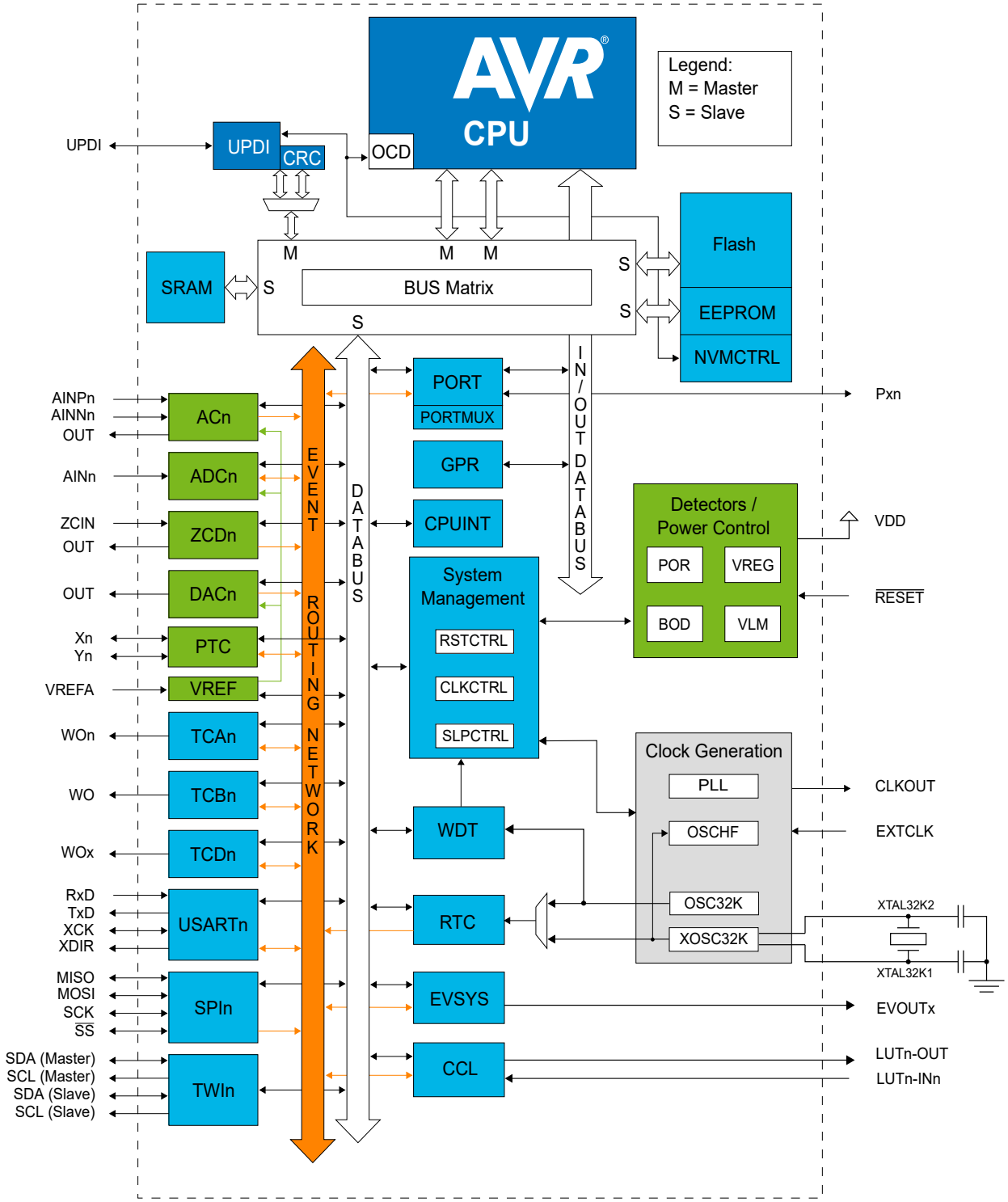
Feature	AVR128DA28 AVR64DA28 AVR32DA28	AVR128DA32 AVR64DA32 AVR32DA32	AVR128DA48 AVR64DA48 AVR32DA48	AVR128DA64 AVR64DA64
Pins	**28**	**32**	**48**	**64**
Max. frequency (MHz)	24	24	24	24
16-bit Timer/Counter type A (TCA)	1	1	2	2
16-bit Timer/Counter type B (TCB)	3	3	4	5
12-bit Timer/Counter type D (TCD)	1	1	1	1
Real-Time Counter (RTC)	1	1	1	1
USART	3	3	5	6
SPI	2	2	2	2
TWI/I^2C	1(1)	2(1)	2(1)	2(1)
12-bit Differential ADC (channels)	1 (10)	1 (14)	1 (18)	1 (22)
10-bit DAC (outputs)	1(1)	1(1)	1(1)	1(1)
Analog Comparator (AC)	3	3	3	3
Zero-Cross Detectors (ZCD)	1	1	2	3
Peripheral Touch Controller (PTC) (self-cap/mutual cap channels)	1 (18/81)	1 (22/121)	1 (32/256)	1 (46/529)
Custom Logic (LUTs)	1(4)	1(4)	1(6)	1(6)
Watchdog Timer	1	1	1	1
Event System Channels	8	8	10	10
General Purpose I/O(2)	23(2)	27(2)	41(2)	55(2)
Port	PA[7:0], PC[3:0], PD[7:0], PF[6,1,0]	PA[7:0], PC[3:0], PD[7:0],PF[6:0]	PA[7:0], PB[5:0], PC[7:0], PD[7:0], PE[3:0], PF[6:0]	PA[7:0], PB[7:0], PC[7:0], PD[7:0], PE[7:0], PF[6:0], PG[7:0]
External Interrupts	23	27	41	55
CRCSCAN	1	1	1	1
Unified Program and Debug Interface (UPDI)	1	1	1	1

Notes:

1. The TWI/I^2C can operate simultaneously as master and slave on different pins.
2. The PF6/$\overline{\text{RESET}}$ pin is input-only.

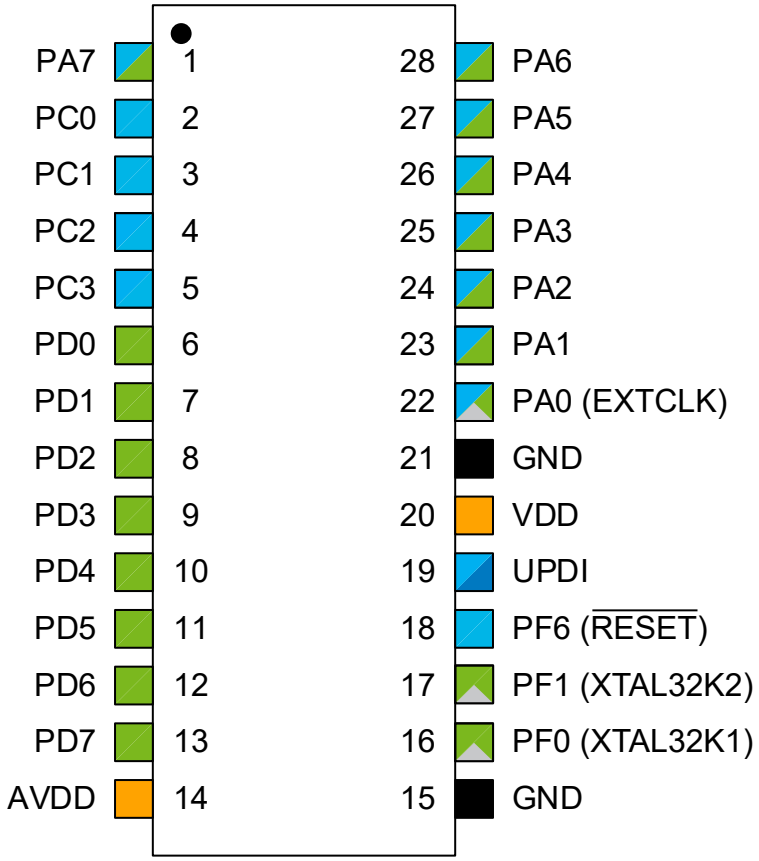
Table of Contents

1. Block Diagram



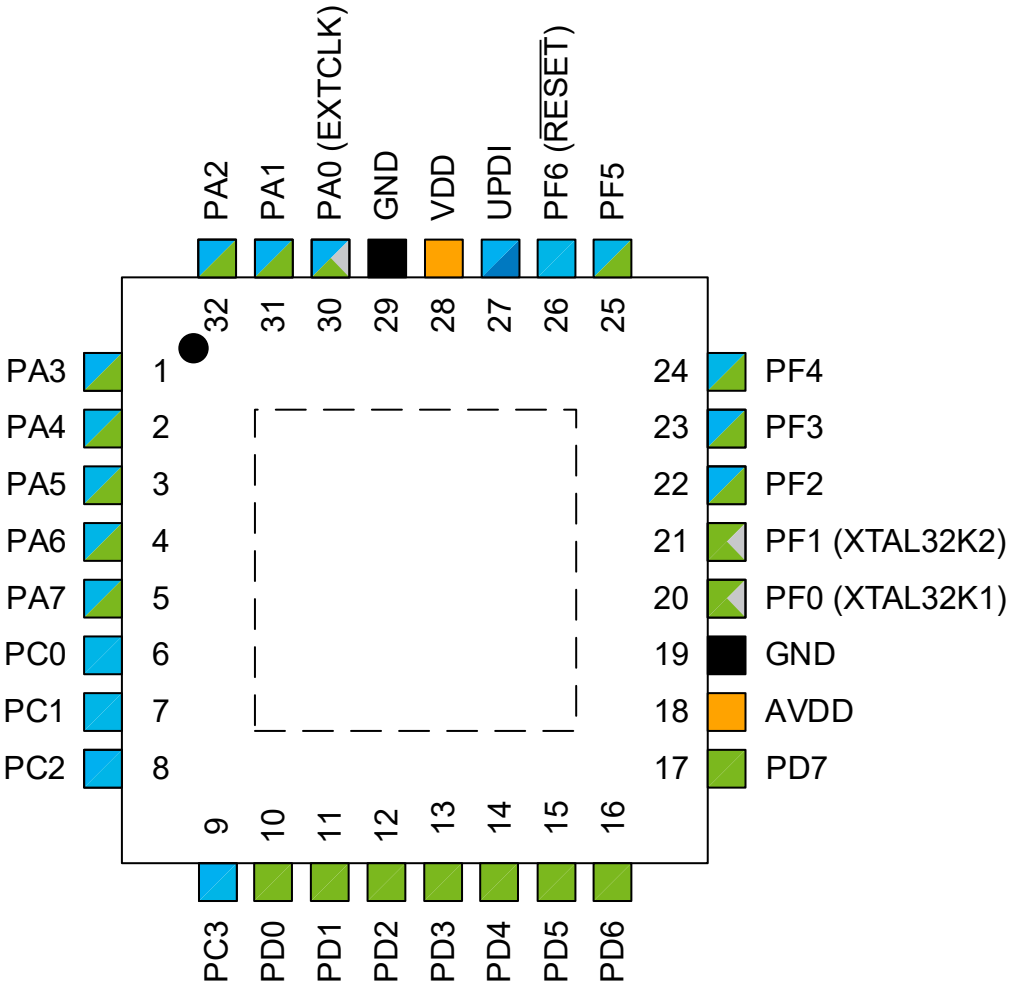
2. Pinout

2.1 28-Pin SPDIP, SSOP and SOIC



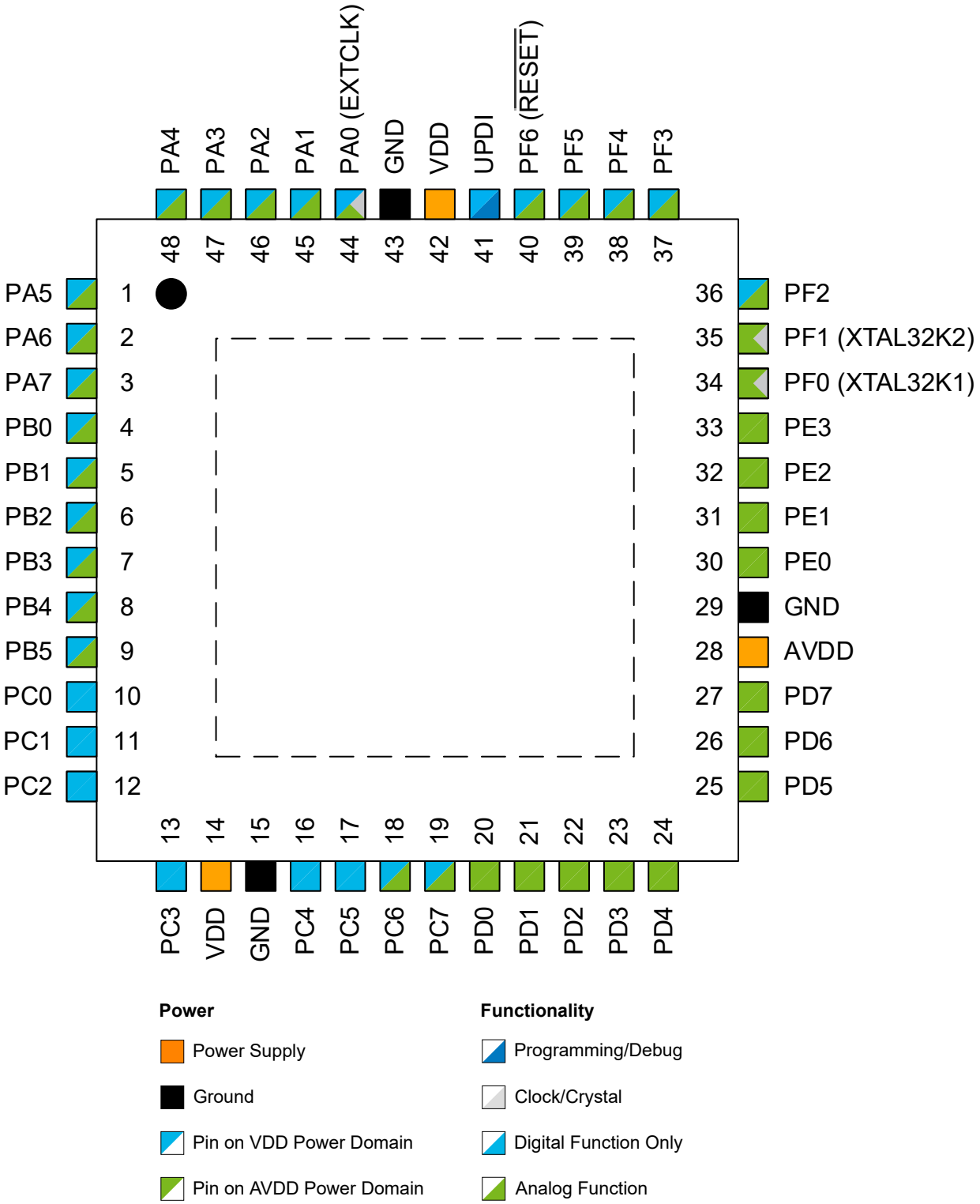
Note: For the AVR® DA Family, the VDD and AVDD are internally connected (no separate power domains).

2.2 32-Pin VQFN and TQFP



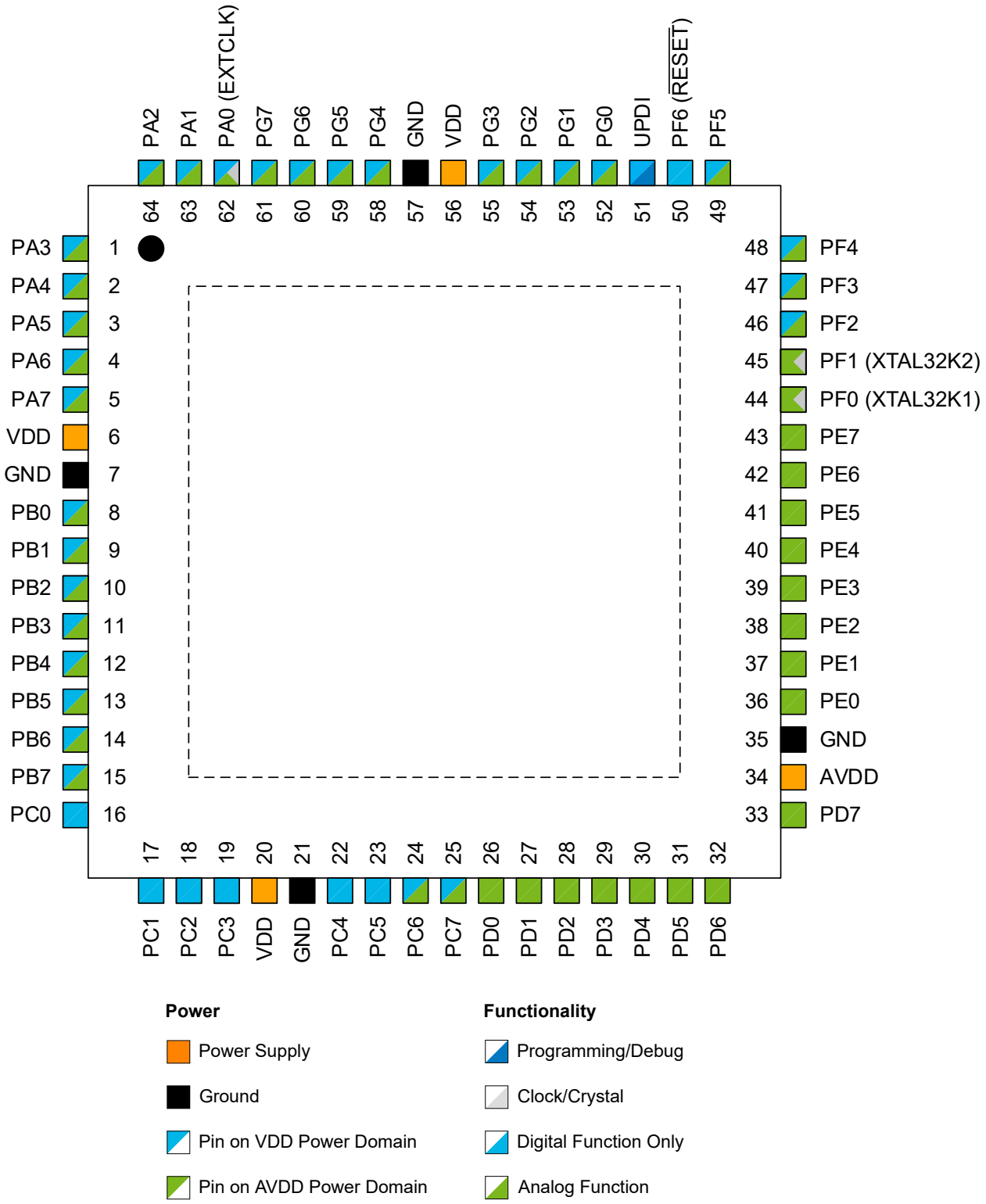
Note: For the AVR® DA Family, the VDD and AVDD are internally connected (no separate power domains).

2.3 48-Pin VQFN and TQFP



Note: For the AVR® DA Family, the VDD and AVDD are internally connected (no separate power domains).

2.4 64-Pin VQFN and TQFP



Note: For the AVR® DA Family, the VDD and AVDD are internally connected (no separate power domains).

3. I/O Multiplexing and Considerations

3.1 I/O Multiplexing

VQFN64/ TQFP64	VQFN48/ TQFP48	VQFN32/ TQFP32	SPDIP28/ SOIC28/ SSOP28	Pin name (1,2)	Special	ADC0	PTC	ACn	DAC0	ZCDn	USARTn	SPIn	TWIn(4)	TCA0	TCA1	TCBn	TCDn	EVSYS	CCL-LUTn
62	44	30	22	PA0	EXTCLK		XO/Y0				0,TxD			WO0					0,IN0
63	45	31	23	PA1			X1/Y1				0,RxD			WO1					0,IN1
64	46	32	24	PA2	TWI		X2/Y2				0,XCK		0,SDA(M)	WO2		0,WO		EVOUTA	0,IN2
1	47	1	25	PA3	TWI		X3/Y3				0,XDIR		0,SCL(M)	WO3		1,WO			0,OUT
2	48	2	26	PA4			X4/Y4				0,TxD(3)	0,MOSI		WO4			0,WOA		
3	1	3	27	PA5			X5/Y5				0,RxD(3)	0,MISO		WO5			0,WOB		
4	2	4	28	PA6			X6/Y6				0,XCK(3)	0,SCK					0,WOC		0,OUT(3)
5	3	5	1	PA7	CLKOUT		X7/Y7	0,OUT 1,OUT 2,OUT		0,OUT 1,OUT 2,OUT	0,XDIR(3)	0,$\overline{SS}$					0,WOD	EVOUTA (3)	
6				VDD															
7				GND															
8	4			PB0			X8/Y8				3,TxD			WO0(3)	WO0				4,IN0
9	5			PB1			X9/Y9				3,RxD			WO1(3)	WO1				4,IN1
10	6			PB2			X10/Y10				3,XCK		1,SDA(M)(3)	WO2(3)	WO2			EVOUTB	4,IN2
11	7			PB3			X11/Y11				3,XDIR		1,SCL(M)(3)	WO3(3)	WO3				4,OUT
12	8			PB4			X12/Y12				3,TxD(3)	1,MOSI(3)		WO4(3)	WO4	2,WO(3)	0,WOA(3)		
13	9			PB5			X13/Y13				3,RxD(3)	1,MISO(3)		WO5(3)	WO5	3,WO	0,WOB(3)		
14				PB6			X14/Y14				3,XCK(3)	1,SCK(3)	1,SDA(S)(3)				0,WOC(3)		4,OUT(3)
15				PB7			X15/Y15				3,XDIR(3)	1,$\overline{SS}$(3)	1,SCL(S)(3)				0,WOD(3)	EVOUTB (3)	
16	10	6	2	PC0							1,TxD	1,MOSI		WO0(3)		2,WO			1,IN0
17	11	7	3	PC1							1,RxD	1,MISO		WO1(3)		3,WO(3)			1,IN1
18	12	8	4	PC2	TWI						1,XCK	1,SCK	0,SDA(M)(3)	WO2(3)				EVOUTC	1,IN2
19	13	9	5	PC3	TWI						1,XDIR	1,$\overline{SS}$	0,SCL(M)(3)	WO3(3)					1,OUT
20	14			VDD															
21	15			GND															
22	16			PC4							1,TxD(3)	1,MOSI(3)		WO4(3)	WO0(3)				
23	17			PC5							1,RxD(3)	1,MISO(3)		WO5(3)	WO1(3)				
24	18			PC6				0,OUT(3) 1,OUT(3) 2,OUT(3)			1,XCK(3)	1,SCK(3)	0,SDA(S)		WO2(3)	4,WO(3)			1,OUT(3)
25	19			PC7						0,OUT(3) 1,OUT(3) 2,OUT(3)	1,XDIR(3)	1,$\overline{SS}$(3)	0,SCL(S)					EVOUTC (3)	
26	20	10	6	PD0		AIN0	X16/Y16	0,AINN1 1,AINN1 2,AINN1						WO0(3)					2,IN0
27	21	11	7	PD1		AIN1	X17/Y17			0,ZCIN				WO1(3)					2,IN1
28	22	12	8	PD2		AIN2	X18/Y18	0,AINP0 1,AINP0 2,AINP0						WO2(3)				EVOUTD	2,IN2
29	23	13	9	PD3		AIN3	X19/Y19	0,AINN0 1,AINP1						WO3(3)					2,OUT

.....continued

VQFN64/ TQFP64	VQFN48/ TQFP48	VQFN32/ TQFP32	SPDIP28/ SOIC28/ SSOP28	Pin name (1,2)	Special	ADC0	PTC	ACn	DAC0	ZCDn	USARTn	SPIn	TWIn(4)	TCA0	TCA1	TCBn	TCDn	EVSYS	CCL-LUTn
30	24	14	10	PD4		AIN4	X20/Y20	1,AINP2 2,AINP1						WO4(3)					
31	25	15	11	PD5		AIN5	X21/Y21	1,AINN0						WO5(3)					
32	26	16	12	PD6		AIN6	X22/Y22	0,AINP3 1,AINP3 2,AINP3	VOUT										2,OUT(3)
33	27	17	13	PD7	VREFA	AIN7	X23/Y23	0,AINN2 1,AINN2 2,AINN0/AINN2										EVOUTD (3)	
34	28	18	14	AVDD															
35	29	19	15	GND															
36	30			PE0		AIN8	X24/Y24	0,AINP1			4,TxD	0,MOSI(3)		WO0(3)					
37	31			PE1		AIN9	X25/Y25	2,AINP2			4,RxD	0,MISO(3)		WO1(3)					
38	32			PE2		AIN10	X26/Y26	0,AINP2			4,XCK	0,SCK(3)		WO2(3)				EVOUTE	
39	33			PE3		AIN11	X27/Y27			1,ZCIN	4,XDIR	0,$\overline{SS}$(3)		WO3(3)					
40				PE4		AIN12	X28/Y28				4,TxD(3)			WO4(3)	WO0(3)				
41				PE5		AIN13	X29/Y29				4,RxD(3)			WO5(3)	WO1(3)				
42				PE6		AIN14	X30/Y30				4,XCK(3)				WO2(3)				
43				PE7		AIN15	X31/Y31			2,ZCIN	4,XDIR(3)							EVOUTE (3)	
44	34	20	16	PF0	XTAL32K1	AIN16(6)	X32/Y32				2,TxD			WO0(3)			0,WOA(3)		3,IN0
45	35	21	17	PF1	XTAL32K2	AIN17(6)	X33/Y33				2,RxD			WO1(3)			0,WOB(3)		3,IN1
46	36	22		PF2	TWI	AIN18(6)	X34/Y34				2,XCK		1,SDA(M)	WO2 (3)			0,WOC (3)	EVOUTF	3,IN2
47	37	23		PF3	TWI	AIN19(6)	X35/Y35				2, XDIR		1,SCL(M)	WO3 (3)			0,WOD (3)		3,OUT
48	38	24		PF4		AIN20(6)	X36/Y36				2, TxD (3)			WO4 (3)		0,WO (3)			
49	39	25		PF5		AIN21(6)	X37Y37				2, RxD (3)			WO5(3)		1,WO(3)			
50	40	26	18	PF6 (5)	$\overline{RESET}$														
51	41	27	19	UPDI															
52				PG0			X40/Y40				5, TxD			WO0 (3)	WO0 (3)				5,IN0
53				PG1			X41/Y41				5,RxD			WO1(3)	WO1(3)				5,IN1
54				PG2			X42/Y42				5,XCK			WO2(3)	WO2(3)			EVOUTG	5,IN2
55				PG3			X43/Y43				5,XDIR			WO3(3)	WO3(3)	4,WO			5,OUT
56	42	28	20	VDD															
57	43	29	21	GND															
58				PG4			X44/Y44				5,TxD(3)	0,MOSI(3)		WO4(3)	WO4(3)		0,WOA(3)		
59				PG5			X45/Y45				5,RxD(3)	0,MISO(3)		WO5(3)	WO5(3)		0,WOB(3)		
60				PG6			X46/Y46				5,XCK(3)	0,SCK(3)					0,WOC(3)		5,OUT(3)
61				PG7			X47/Y47				5,XDIR(3)	0,$\overline{SS}$(3)					0,WOD(3)	EVOUTG (3)	

Notes:

1. Pins names are of type P*xn*, with *x* being the PORT instance (A, B, C, ...) and *n* the pin number. Notation for signals is PORT*x*_PIN*n*. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins P*x*2 and P*x*6 of each port have full asynchronous detection.
3. Alternate pin positions. For selecting the alternate positions refer to the *Port Multiplexer* section.
4. The TWI pins that can be used as master or slave are marked *M*. Pins with slave only are marked *S*.
5. Input-only.
6. Positive input-only.

4. Revision History

Doc. Rev.	Date	Comments
B	08/2020	Updated AVR® MCU DA (AVR-DA) to AVR® DA MCU, and AVR-DA to AVR DA, per latest trademarking
A	03/2020	Initial document release

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