AS3909/AS3910

13.56 MHz RFID Reader IC, ISO-14443 A/B

General Description

The AS3909/10 is a high performance 13.56MHz HF RFID Reader IC.

The AS3909/10 is unequalled in the domain of HF Reader ICs; it contains two differential low impedance (1.5Ω) antenna drivers.

These drivers are unmatched, which means that the IC can deliver up to 8 times the output power of a standard HF Reader IC using the same power supply voltage.

Additionally using this configuration means half of the power consumption at the same output power.

The IC has an operating voltage down to 2.4V and a low power operating mode of 5mA. This means the AS3909/10 is ideal for portable or battery powered applications.

For applications where high power is required the AS3909/10 can attain up to 700mW. This means there is no need for complex external booster circuitry.

The component count and complexity of the design is further reduced through the patented automatic modulation depth adjustment.

The analog front end (AFE) is complemented by a highly integrated data framing engine for both ISO-14443 A and B.

This includes data rates up to 848kbits with all framing and synchronization tasks on board. This enables the customer to build a complete HF RFID Reader using only a low end micro.

The AS3909/10 not only supports reader to tag communication, but sports Peer to Peer communication using the NFCIP-1 active communication mode with a data rate of 106kbps.

The IC has a SPI, which enables bi-directional communication with the external microcontroller.

Other standard and custom protocols, such as ISO -15693 or Felica can be implemented via transparent mode.

Only available in AS3910: In addition to the above mentioned advantages, AS3910 also features the ams' unique Automatic Antenna Tuning (AAT)[1] technology. With AAT, the device is optimized for application with directly driven antenna and enables the reader to retune itself to deliver maximum output at 13.56MHz, when the surroundings detunes the antenna.

For further understanding in regards to the contents of the datasheet, please refer to the Reference Guide located at the end of the document.

1. Only available in AS3910.

Figure 1:
Standard Products

Part Number	AAT	Trim Pins
AS3909	No	NC
AS3910	Yes	Connect to external trim caps as mentioned in Calibrate Antenna Resonance

Key Benefits & Features

The benefits and features of this device are listed below:

Figure 2:
Added Value of Using AS3909/10

Benefits	Features
Stable Modulation Index	Close loop adjustment of ASK modulation for accurate control of modulation depth in case of ISO-14443B protocol
Enabling Ultra Low Power Applications	Low power (3.5µA) NFC target mode
No communication holes	AM/PM demodulator
Measuring signal strength on RFI pins	Accurate RF envelope measurement (8 bit A/D)
Enables various antenna configurations	High output power at 3.3V power supply: • Up to 700mW in case regulator is externally shorted • Up to 500mW in case differential output and antenna trimming is used • Up to 125mW in case of single ended output and antenna trimming is used
Increases EMD immunity	Squelch feature which performs gain reduction to compensate for noise generated by transponder processing
Enable tuning of the Antenna LC Tank	Automatic Antenna tuning (AAT) (1)
For support of other standards and custom protocols (ISO-15693, FeliCa, ...)	Transparent mode
Enabling Inductive wakeup in combination with MCU	Amplitude and phase measurement
	Supporting 13.56 MHz and 27.12MHz Quartz oscillator with fast start-up
	Supply voltage range from 2.4V to 3.6V
	Wide temperature range: -40°C to 85°C
	32-pin QFN (5x5mm) for AS3910 and 32-pin TQFN (5x5mm) for AS3909

Note(s) and/or Footnote(s):

1. Only available in AS3910.

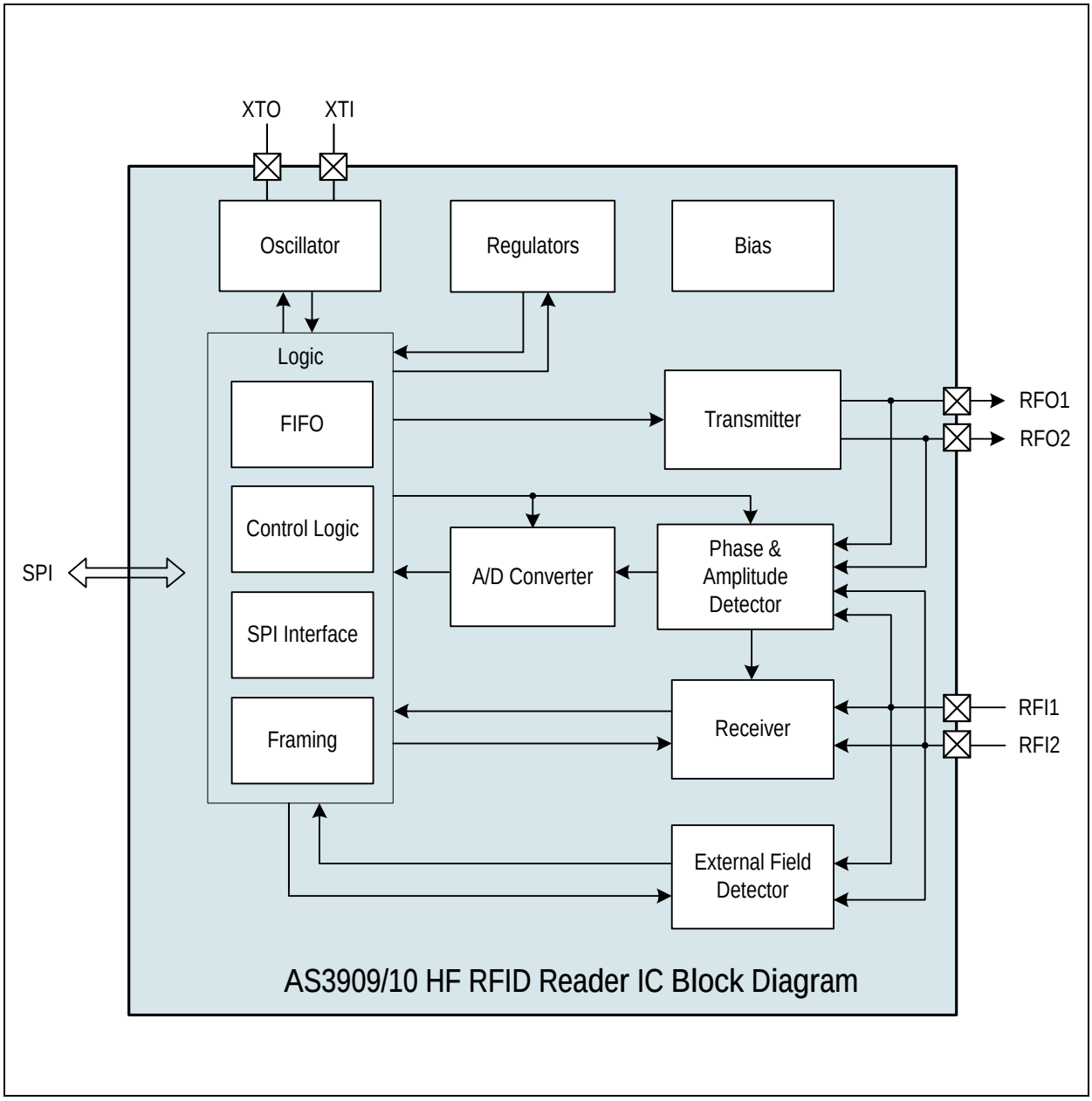
Applications

The AS3909/10 is ideal for applications where the reader antenna is directly driven (no 50Ω cable). It also includes several unique features, which make it especially suitable for low power and battery powered applications.

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 3:
AS3909/10 HF RFID Reader IC Block Diagram



Note: The main differences between AS3909 and AS3910 are elaborated in sections General Description, Pin Assignments, Detailed Description, Direct Commands, Clear and Active Receive – Use in ISO-14443B Anticollision.

Pin Assignments

The AS3909/10 pin assignments are described below.

Figure 4:
Pin Assignments (Top View)

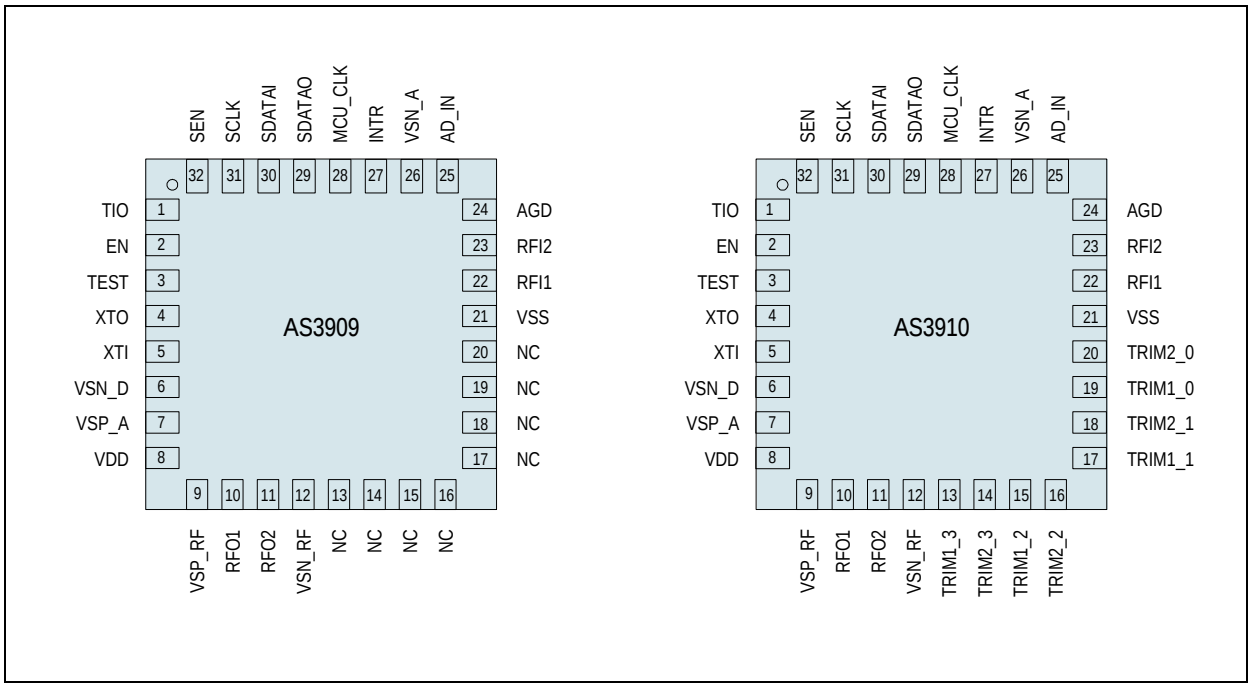


Figure 5:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	TIO	Digital bi-directional	Test IO pin
2	EN	Digital input with pull-down	Enable input
3	TEST		Test input
4	XTO	Analog output	Xtal oscillator output
5	XTI	Analog input	Xtal oscillator input
6	VSN_D	Supply	Digital ground
7	VSP_A	Analog Input / Output	Analog supply, regulator output
8	VDD	Supply	External positive supply
9	VSP_RF	Analog Input / Output	Supply, regulator output for antenna drivers
10	RFO1	Analog output	Antenna driver output
11	RFO2		
12	VSN_RF	Supply	Ground of antenna drivers

Pin Number	Pin Name	Pin Type	Description
13	NC/TRIM1_3	Analog input	AS3909: NC AS3910: Input to trim antenna resonant circuit
14	NC/TRIM2_3		
15	NC/TRIM1_2		
16	NC/TRIM2_2		
17	NC/TRIM1_1		
18	NC/TRIM2_1		
19	NC/TRIM1_0		
20	NC/TRIM2_0		
21	VSS	Supply pad	Ground, die substrate potential
22	RFI1	Analog input	Receiver input
23	RFI2		
24	AGD	Analog Input / Output	Analog reference voltage
25	AD_IN	Analog input	A/D converter input
26	VSN_A	Supply pad	Analog ground
27	INTR	Digital output	Interrupt request output
28	MCU_CLK		Microcontroller clock output
29	SDATAO	Digital Output / Tristate	Serial Peripheral Interface DATA output
30	SDATAI	Digital input	Serial Peripheral Interface DATA input
31	SCLK		Serial Peripheral Interface Clock
32	SEN		Serial Peripheral Interface Enable
Exposed Pad	VSUB	Supply	Die substrate potential, to be connected to VSS on PCB

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Comments	Min	Max	Unit
Electrical Parameters					
V_{DD}	DC supply voltage		-0.5	5	V
V_{IN}	Input pin voltage (all except TRIM pins)		-0.5	5	V
V_{INTRIM}	Input pin voltage TRIM pins		-0.5	30	V
I_{SCR}	Input current (latch up immunity)	Norm: Jedec 78	-100	100	mA
Electrostatic Discharge					
ESD		Norm: MIL 883 E method 3015 (Human Body Model)	±2		kV
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature		-55	125	°C
T_{body}	Package body temperature	Norm: IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".		260	°C
	Humidity non-condensing		5	85	%
MSL	Moisture Sensitive Level	Represents a maximum floor time of 168h	3		

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Operating Conditions

Figure 7:
Operating Conditions

Symbol	Parameter	Comments	Min	Max	Unit
V_{DD}	Positive supply voltage	In case power supply is lower than 2.6V, PSSR can not be improved using internal regulators (minimum regulated voltage is 2.4V)	2.4	3.6	V
V_{SS}	Negative supply voltage		0	0	V
T_{AMB}	Ambient Temperature		-40	85	°C
V_{TRIM}	Input pin voltage TRIM pins			30	V

DC / AC Characteristics For Digital Inputs and Outputs

Figure 8:
DC / AC Characteristics For Digital Inputs and Outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMOS Inputs: Valid for input pins EN, SEN, SDATAI, SCLK and TEST						
V_{IH}	High level input voltage		0.7 * VDD			V
V_{IL}	Low level input voltage				0.3 * VDD	V
I_{LEAK}	Input leakage current				2	µA
R_{PD}	Pull-down resistance pad EN			100		kΩ
CMOS Outputs: Valid for output pins SDATAO, INTR and MCU_CLK						
V_{OH}	High level output voltage	I_{SOURCE} = 1mA	0.9 * VDD			V
V_{OL}	Low level output voltage	I_{SINK} = 1mA			0.1 * VDD	V
C_L	Capacitive load				50	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_O	Output Resistance			250	500	Ω
SPI Timing						
T_{SENL}	SPI reset (SEN low)		100			ns
T_{SCLKL}	SCLK low		100			ns
T_{SCLKH}	SCLK high		100			ns
$T_{SENCLKR}$	SEN rising to SCLK rising	first SCLK pulse	50			ns
$T_{SENCLKF}$	SCLK falling to SEN falling	last SCLK pulse	50			ns

Electrical Specification

VDD = 3.3V, Temperature = 25ºC, unless otherwise noted.

Figure 9:
Electrical Characteristics

Symbol	Parameter	Comments	Min	Typ	Max	Unit
I_{PD}	Supply current in Power-down mode			0.3	2	µA
I_{NFC}	Supply current in Initial NFC target mode			3.5	7	µA
I_{RD}	Supply current in Ready mode	13.56 MHz Xtal used, MCU_CLK disabled		2	3	mA
I_{RA}	Supply current Receiver active	13.56 MHz Xtal used, MCU_CLK disabled		5	7	mA
I_{LP}	Supply current Receiver active, low power mode			3	5	mA
R_{RFO}	RFO1 and RFO2 driver output resistance	I_{RFO}=10mA All segments ON		1.5	4	Ω
V_{RFI}	RFI input sensitivity	f_{SUB}=848kHz (1)		0.5		mVrms
V_{RFI_LP}	RFI input sensitivity, low power receiver mode	f_{SUB}=848kHz		1.5		mVrms
R_{RFI}	RFI input resistance			10		kΩ
V_{POR}	Power on Reset Voltage		1.0	1.4	<2.4	V
V_{AGD}	AGD voltage		1.4	1.5	1.6	V
V_{AR}	Regulator drop	After execution of direct command *Adjust Regulators*		250		mV

Symbol	Parameter	Comments	Min	Typ	Max	Unit
T_{OSU}	Oscillator start-up time	13.56MHz or 27.12MHz crystal R_S=50Ω max, load capacitance according to crystal specification		0.7		ms

Note(s) and/or Footnote(s):

1. Amplitude of carrier signal at RFI inputs is 2.5Vpp, maximum amplitude is 3Vpp.

Detailed Description

Figure 10:
Minimum Configuration with Single Sided Antenna Driving

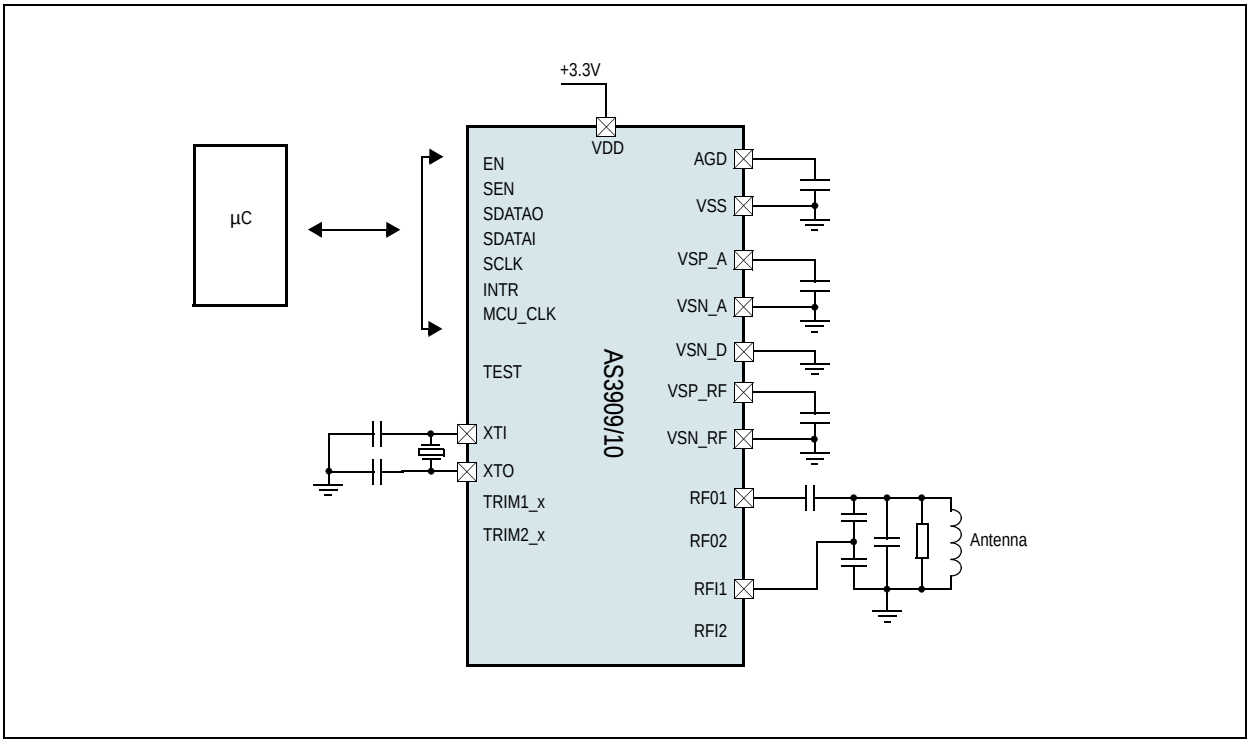
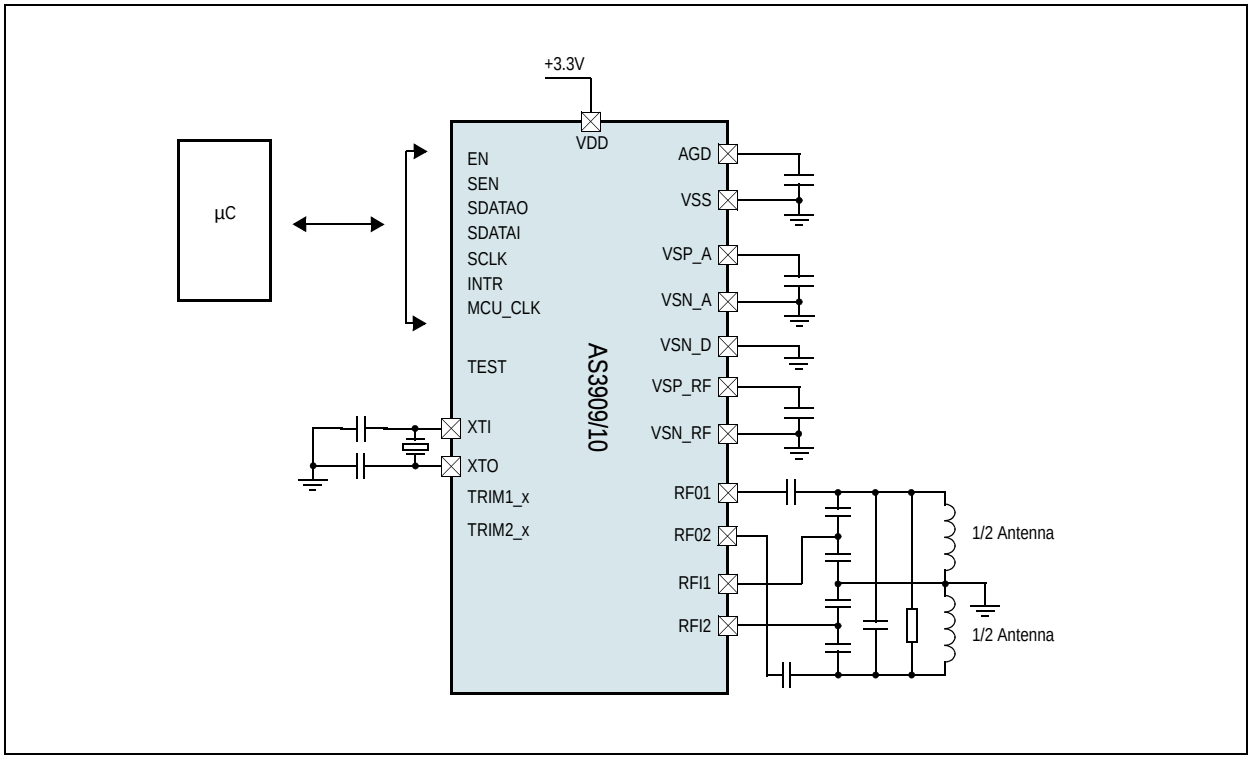


Figure 11:
Minimum Configuration with Differential Antenna Driving



Note: AAT is only available for AS3910 (hence TrimX_X is only a connectable for AS3910).

Transmitter

The Transmitter incorporates drivers, which drive external antenna through pads RFO1 and RFO2. Single sided and differential driving is possible. The transmitter block additionally contains a subblock, which modulates transmitted signal for communication reader to transponder (OOK or configurable AM modulation).

The AS3909/10 transmitter is indented to directly drive antennas (without 50Ω cable, usually antenna is on the same PCB). Operation with 50Ω cable is also possible, but in that case some of the advanced features are not possible.

Receiver

The receiver detects transponder modulation superimposed on the 13.56MHz carrier signal. The receiver chain is composed of a peak detector followed by two stages with gain and filtering function and a final digitizer stage. The filter characteristics are adjusted to optimize performance over different ISO modes and data rates (subcarrier frequencies from 212 kHz to 848 kHz are supported). The receiver chain input is the RFI1 pin; output of digitizer stage is demodulated subcarrier signal. Receiver also contains a subblock, which helps to detect the presence of external RF field in NFCIP target mode. The receiver chain incorporates several features, which enable reliable operation in challenging phase and noise conditions.

Phase and Amplitude Detector

The phase detector observes the phase difference between the transmitter output signals (RFO1 and RFO2) and the pad signals RFI1 and RFI2. The pad signals RFI1 and RFI2 are proportional to the signal on the antenna LC tank. RFI1 and RFI2 signals are also used to run the self-mixer, which generates output proportional to their amplitude. The phase detector and self mixer blocks are used for several purposes:

- Variation of RFI1 and RFI2 phase is used to perform PM demodulation
- Average phase difference between RFOx pins and RFIx pins is used to check antenna tuning and inductive wake-up via MCU
- Output of mixer is used to measure amplitude of signal present on pins RFI1 and RFI2

A/D Converter

The AS3909/10 contains a built-in A/D Converter. Its input can be multiplexed from different sources and is used in several applications (measurement of RF amplitude, calibration of modulation depth, checking of the antenna LC tank resonance,

A/D conversion of signal applied to pin AD_IN). The result of A/D conversion is stored in a register, which can be read through the SPI interface.

External Field Detector

The external field detector is a low power block, which is switched on in NFCIP target mode to detect the presence of initiator field. It is also used during the NFCIP Collision Avoidance procedure.

Quartz Crystal Oscillator

The quartz crystal oscillator can operate with 13.56MHz and 27.12MHz crystals. At start-up the transconductance of the oscillator is increased to achieve fast start-up. Since the start-up time varies depending on crystal type, temperature and other parameters, the oscillator amplitude is observed and an interrupt is sent when stable operation is reached to inform the controller that the clock signal is stable and reader field can be switched on.

It also provides a clock signal to the external microcontroller (MCU_CLK) according to setting in the control register.

Power Supply Regulators

Integrated power supply regulators ensure high power supply rejection of a complete reader system. At power up, the regulators are transparent. In case PSRR of the reader system has to be improved, then the command *Adjust Regulators* is sent. As a result of this command, the power supply level of VDD is measured in maximum load conditions and the regulated voltage reference is set 250mV below this measured level to assure a stable regulated supply. The resulting regulated voltage is stored in a register. It is also possible to define regulated voltage by writing a configuration register. In order to decouple any noise sources from different parts of IC there are two regulators integrated with separated external blocking capacitors (regulated voltage of both is the same). One regulator is for the analog blocks, the other one is for the antenna drivers. Logic and digital I/O pads are supplied directly from VDD (negative supply pin for logic and digital I/O is separated to avoid coupling of logic induced noise in the substrate). This block additionally generates a reference voltage for the analog processing (AGD - analog ground). This voltage also has an associated external buffer capacitor.

POR and Bias

This block contains the bias current and voltage generator, which provides bias currents and reference voltages to all other blocks. It also incorporates a Power on Reset (POR) circuit, which provides a reset at power-up and at low supply levels.

ISO-14443 and NFCIP Framing

This block performs ISO-14443 and NFCIP-1 106 kbps active communication framing for receive and transmit according to the selected ISO mode and data rate settings.

- In reception, it takes demodulated subcarrier signal from Receiver. It recognizes the SOF, EOF and data bits; performs parity and CRC check; organizes the received data in bytes and places them in the FIFO.
- During transmit, it operates inversely; it takes bytes from FIFO; generates parity and CRC bits; adds SOF and EOF; and performs final encoding before passing modulation signal to transmitter.
- In Transparent mode, the framing and FIFO are bypassed; the digitized subcarrier signal, which is Receiver output is directly sent to SDATAO pin; signal applied to SDATAI pin is directly used to modulate the transmitter.

FIFO

The AS3909/10 contains a 32byte FIFO. Depending on the mode, it contains either data that has been received or data that is to be transmitted.

Control Logic

The control logic contains I/O registers, which define the operation of device.

SPI Interface

A 4-wire Serial Peripheral interface (SPI) is used for communication between external microcontroller and the AS3909/10.

Application Information

Operating Modes

The AS3909/10 operating mode is defined by the content of the *Operation Control Register* (address #01).

At power up, all bits of the *Operation Control Register* are set to 0 and the AS3909/10 is in **Power-down** mode. In this mode – the AFE static power consumption is minimized, only the POR and part of bias are active, regulators are transparent and are not operating. The SPI is still functional in this mode; so all settings of ISO mode definition and configuration registers can be done.

Control bit *en* (bit 7 of *Operation Control Register*) is controlling both the oscillator and regulators. When this bit is set, the device enters in **Ready** mode. In this mode, the oscillator and regulators are enabled. An interrupt is sent to inform the microcontroller when the oscillator frequency is stable. Another possibility to enter in Ready mode is to assert EN pin high (logic OR function between bit *en* and pin EN).

Enable of Receiver and Transmitter are separated, so it is possible to operate one without switching on the other (control bits *rx_en* and *tx_en*). In some cases this may be useful, in case the reader field has to be maintained and there is no transponder response expected receiver can be switched-off to save current. Another example is NFCIP target mode in which RF field is generated by the initiator and only Receiver operates.

The receiver also has a low power mode in which its power consumption and as consequence sensitivity are reduced. This mode is entered in by setting control bit *rx_lp*.

The last control bit of the *Operation Control Register* is *nfc_t* bit. Setting of this bit is only allowed in case the NFC mode is set in the *ISO mode definition register*. Setting this bit to one, while all other *Operation Control Register* bits are set to 0, puts the AS3909/10 into **Initial NFC Target** mode. In this low power mode, only the Target Activation Detector, which will detect a presence of external RF field, is active. Once the presence of external RF field is detected, an interrupt is sent to microcontroller which will in turn switch on oscillator and receiver.

Transmitter

The Transmitter contains two identical driver blocks which are driving external antenna connected to pins RFO1 and RFO2. The driver is composed of 8 segments having binary weighted output resistance. The MSB segment typical ON resistance is 3Ω; when all segments are turned on, the output resistance is typically 1.5Ω. Usually certain segments are switched off to define AM modulated level, while they are all turned on to define the non-modulated level. It is also possible to switch off

certain segments when driving the non modulated level to reduce the amplitude of signal on the antenna and/or to reduce the antenna Q factor.

The driver impedance in increased in case of AM modulation (ISO-14443B), in case of OOK modulation (ISO-14443A) both drivers are blocked to low state. In the single driver mode (bit *sing* of configuration register 2 set to 1) only RFO1 output is driven, RFO2 output is disabled.

AM modulation and operation of the driver segments is controlled by writing AM modulation depth and antenna driver registers (see "AM Modulation Depth and Antenna Driver Registers" on page 46). Register #13 defines which segments will be used to define normal, non-modulated level. The default setting is that all segments are used. Registers #10 to #12 are used to define how the AM modulated level is set-up. It can be set-up automatically by definition of modulation depth and the direct command *Calibrate Modulation Depth* or by a direct definition of segments which are turned off during AM modulation.

Receiver

The receiver performs demodulation of the transponder subcarrier modulation which is superimposed on the 13.56 MHz carrier frequency. It performs AM or PM demodulation, band-pass filtering and digitalization of subcarrier signals, 848, 424 and 212 kHz subcarrier frequencies are supported. Additionally, it performs RSSI measurement, automatic gain control (AGC) and Squelch function.

The receiver is switched on when *Operation Control Register* bit *rx_en* is set. The operation of the receiver is additionally controlled by the signal *rx_on* which is set high when modulated signal is expected on the receiver input. This is automatically done after every Transmit command. Signal *rx_on* can be also forced high by sending direct command *Unmask Receive Data*. Signal *rx_on* is used to control features like RSSI and AGC.

AM demodulation is performed using a peak follower. Both the positive and negative peaks are tracked to suppress common mode signal. In case external demodulation is carried out the peak follower stage can be bypassed by setting bit *envi* in *Configuration Register 2*. In case of PM demodulation signal coming from the phase detector is replacing the output of peak follower.

Next stage in signal processing is the buffer amplifier followed by second order low pass filter with adjustable corner frequency. Final stage is a first order high pass filter with adjustable corner frequency. The digital signal representing transponder subcarrier modulation is produced by a window comparator.

Filter setting is done automatically when ISO mode and data rate are chosen by writing *ISO Mode Definition Register*. Setting is displayed in the *Receiver Configuration Register* (#06) and can be changed by rewriting this register. In transparent mode ISO mode register is not used and Filter selection has to be done by writing *Receiver Configuration register* (#06).

By setting the *Operation Control Register* bit *rx_lp* receiver operates in low power mode. In this mode, power consumption is lower but as consequence also receiver sensitivity is reduced (see "Electrical Characteristics" on page 7).

Gain Reduction, AGC and Squelch

The total gain of receiver chain is 160. In certain conditions it is desirable to reduce this gain. There are several features implemented in the Receiver to reduce this gain.

Automatic Gain Reduction (AGC)

AGC (automatic gain control) feature is useful in case the transponder is close to the reader. In such conditions receiver chain is in saturation and demodulation can be influenced by system noise and saturation of last gain stage. When AGC is switched on receiver gain is reduced so that the input to digitizer stage is not saturated. The AGC system comprises a window comparator which has its window three times larger than window of digitalization window comparator. When the AGC function is enabled gain is reduced until there are no transitions on its output. Such procedure assures that the input to digitalization window comparator is less than three times larger than its window.

AGC operation is controlled by the *Receiver Configuration Register* (#06) bits *agc_en* and *agc_m*. *Agc_en* bit enables AGC operation, *agc_m* defines AGC operating mode. The AGC action is started 20µs after rising edge of signal *rx_on*. In case *agc_m* bit is 0 it will operate during a complete receive period, in case it is 1 it will operate on first 8 subcarrier pulses. The AGC is reducing gain to -21dB in 7 steps of 3dB. When signal *rx_on* is low AGC is in reset.

Squelch

This feature is designed to avoid demodulation problems of transponders which produce a lot of noise during data processing which takes place when the data sent by the reader is being processed and an answer prepared. It can also be used in noisy environment. Transponder processing noise (or environment noise) may be misinterpreted as start of transponder response which results in reader decoding error. These problems are avoided by reducing receiver gain so that there are no transitions of output when noise is present. This is done by sending direct command *Squelch*.

During execution of the direct command *Squelch* the digital output of receiver (output of window comparator mentioned above) is observed. In case there are more than two transitions

on this output in 50µs time period, gain is reduced for 3dB and output is observed during next 50µs. This procedure is repeated until number of transitions in 50µs is lower or equal to 2 or until maximum gain reduction (21dB) is reached. This setting is cleared with direct command *Clear Squelch*.

Setting Gain Reduction in Receiver Configuration Register (#06)

By setting bits *rg2* to *rg0* in *Receiver Configuration Register* (#06) receiver gain can also be reduced in 7 steps of 3dB.

Actual gain reduction is combination of all three gain reduction features mentioned above (AGC, Squelch and setting gain reduction in *Receiver Configuration Register*). Actual gain reduction state can also be observed by reading the *Receiver State Display Register* (#17) bits *gr_2* to *gr_0*.

RSSI

The receiver also comprises of an RSSI block (Received Signal Strength Indicator) which measures the strength of the modulated signal that is superimposed on the 13.56MHz carrier. RSSI is a peak hold system which is started 20µs and 16 transitions of demodulated signal after rising edge of *rx_on*. It stays active while signal *rx_on* is high; while *rx_on* is low it is frozen. Result of RSSI measurements is 4 bit value which can be observed by reading *Receiver State Display Register* (#17) bits *rssi_3* to *rssi_0*. The RSSI range calculated back on RFI1 input is 280µVrms to 8.8mVrms, one LSB represents step of 2.15dB.

Since the RSSI measurement is a peak hold than the RSSI result will not follow any variations in the signal strength (the highest value will be kept). In such a case it is possible to reset RSSI bits of *Receiver State Display Register* and restart the measurement by sending direct command *Clear RSSI*.

AM and PM Demodulation

In addition to usual AM demodulation, the AS3909/10 also includes the possibility of PM demodulation. Readers which have only AM demodulation may have so called communication holes in operating volume. Communication holes are areas where transponder is not seen, they depend on transponder characteristics such as Q factor and resonant frequency variation. Usually both AM and PM modulation are present, in so called communication holes receiver input signal is only PM modulated. Choice between AM and PM demodulation is done by setting the bit *pmd* in the *Configuration Register 5* (#05); default setting is AM. As mentioned above an RSSI measurement is continually done while transponder message is being processed. By comparing RSSI value in AM and PM mode the external controller can opt for the demodulation mode in which there is more signal. PM demodulation is done by processing phase signal coming from the Phase Detector.

A/D Converter

The AS3909/10 contains an 8 bit successive approximation A/D converter. Input to A/D converter can be multiplexed from different sources to be used in several direct commands and adjustment procedures. The result of last A/D conversion is stored in a register which can be read through the SPI interface (address #0D). Typical conversion time is 12µs.

The A/D converter has two operating modes, absolute and relative.

In absolute mode the low reference is 0V and the high reference is 2V. This means that A/D converter input range is from 0 to 2V, 00 code means input is 0V or lower, FF means that input is 2V or higher, LSB is 7.8125mV.

In relative mode low reference is 1/6 of VSP and high reference is 5/6 of VSP, so the input range is from 1/6VSP to 5/6VSP. Relative mode is only used in phase measurement in which phase detector output is proportional to power supply. In all other cases absolute mode is used.

The A/D converter input can also be accessed externally. When the direct command AD Convert is sent, an A/D conversion of voltage present on pin AD_IN is performed in absolute mode, result is stored in *A/D Converter Output Register*. AD_IN pin should be left non-connected in case A/D conversion is not needed in application.

Phase and Amplitude Detector

Phase Detector

The phase detector is observing phase difference between the transmitter output signals (RFO1 and RFO2) and the pad signals RFI1 and RFI2, which are proportional to the signal on the antenna LC tank. These signals are first passed by digitizing comparators. Digitized signals are processed by a phase detector. Filter characteristics of the phase antenna are adapted to one of the two possible operation modes. For antenna tuning check, a strong low power filter is used to get average phase difference, for PM demodulation a low pass filter having 1MHz corner frequency is used to pass the subcarrier frequency.

Antenna Tuning Check

The Phase Detector output reflects phase relationship between the two inputs. The 90º phase shift (ideal antenna LC tank tuning) results in VSP/2 output voltage. In case the antenna LC tank is detuned, phase shift changes which results in different phase detector output voltage. In case of command *Check Antenna Resonance* phase detector output is applied to A/ D converter in relative mode. Output of phase detector is also observed by comparator with reference signal VSP/2. Output of this comparator is used in execution of direct command *Calibrate Antenna*.

PM Demodulation

The phase detector has low pass characteristics in case of PM demodulation. This is to allow phase demodulation of the 848 kHz subcarrier signal. The output is then fed to the Receiver.

Amplitude Detector

Signals from pads RFI1 and RFI2 are used as inputs to the self mixing stage. Output of this stage is DC voltage proportional to amplitude of signal on RFI1 and RFI2 pads. This signal is fed to A/D converter when amplitude of signal on RFI inputs has to be measured (direct commands *Measure RF and Calibrate Modulation Depth*).

External Field Detector

The External Field Detector is used in NFC mode to detect the presence of an external RF field. It is composed of two sub-blocks, Target Activation Detector and a RF Collision Avoidance Detector. Input to both blocks is the signal from the RFI1 pad. The thresholds of the two blocks can be independently set by writing the *NFCIP Field Detection Threshold Register* (#14). The outputs of both detectors are fed to a logic or gate, output of which goes to the Control logic. A low to high transition of this logic or gate output triggers an interrupt (Interrupt due to nfc event)

Target Activation Detector

This block is turned on in NFC target mode to detect the presence of an interrogator field. It is enabled by setting the *Operation Control Register* bit *nfc_t*. It is a low power block with an adjustable threshold in the range from 145mVpp and 590mVpp. This block generates an interrupt when an external field is detected and also when it disappears. With such implementation it can also be used to detect the moment when the external field disappears. This is useful to detect the moment when external NFC device (it can either an interrogator or a target) has stopped emitting an RF field since a response can only be sent afterwards. Actual state of the Target Activation Detector can be checked by reading the bit *rfp* in the *Receiver State Display Register* (#17). When this bit is set to logic one, there is a signal higher than the threshold present on the input of Target Activation Detector.

RF Collision Avoidance Detector

This block is activated during the RF Collision Avoidance sequence which is executed before every request or response in NFC active communication (Initial or Response RF Collision Avoidance). In case during the RF Collision Avoidance sequence the presence of an external field is detected, request/response is not sent, an interrupt is generated to inform the external controller about collision. During RF Collision Avoidance, the Target Activation Detector is disabled in order to have the

correct threshold when detection is made. The threshold of the RF Collision Avoidance Detector can be adjusted in the range from 50 to 1080mVpp.

Quartz Crystal Oscillator

The quartz crystal oscillator can operate with 13.56MHz and 27.12MHz crystals. The oscillator is based on an inverter stage supplied by controlled current source. A feedback loop is controlling the bias current in order to regulate amplitude on XTI pin to 1Vpp. This feedback assures reliable operation even in case of low quality crystals with Rs up to 50Ω. In order to enable a fast reader start-up an interrupt is sent when oscillator amplitude exceeds 750mVpp.

The oscillator block always provides 13.56MHz clock signal to the rest of the IC. In case of 27.12MHz crystal clock signal is internally divided by two. Divider is controlled by *Configuration Register 2* (#02) bit *osc*.

Division by two assures that 13.56 MHz signal has a duty cycle of 50% which is better for the Transmitter performance (no PW distortion). Use of 27.12MHz crystal is therefore recommended for better performance.

In case of 13.56MHz crystal, the bias current of stage which is digitizing oscillator signal is increased to assure as low PW distortion as possible.

The oscillator output is also used to drive a clock signal output pin which can be used by the external microcontroller (MCU_CLK). By setting bits in *Configuration Register 2* MCU_CLK a frequency can chosen between 13.56MHz, 6.78MHz and 3.39MHz. Any microcontroller processing generates noise which may be captured by the AS3909/10 receiver. Using MCU_CLK as the microcontroller clock source generates noise which is synchronous to the reader carrier frequency and is therefore filtered out by the receiver while using some other incoherent clock source produces noise which may generate some sideband signals captured by Receiver. Due to this fact it is recommended to use MCU_CLK as microcontroller clock source.

Power Supply, Regulators

The AS3909/10 includes two regulators which can be adjusted automatically to improve the reader PSRR. VDD is an external power supply pin. It is used to supply the logic and digital pins. One regulator is used to supply analog blocks (VSP_A), another is there just for transmitter (VSP_RF) in order to decouple transmitter current spikes from the rest of the IC. All negative power supply pins are externally connected to the same negative supply, the reason for separation is in decoupling of noise induced by voltage drops on the internal power supply lines. These pins are VSS (die substrate potential), VSN_D (negative supply of logic and digital pads), VSN_A (negative supply of analog blocks) and VSN_RF (negative supply of transmitter).

An additional regulator block provides AGD voltage (1.5V) which is used as reference potential for analog processing (analog ground).

Blocking capacitors have to be connected externally to regulator outputs and AGD pins. For pins VSP_A and VSP_RF recommended blocking capacitors are 2.2µF in parallel with 10nF, for pin AGD 1µF in parallel with 10nF is suggested.

The regulated voltage range is from 2.4V to 3.4V with step of 100mV. Both regulators are set to the same voltage. VSP_A regulator maximum capability is 20mA while maximum capability of VSP_RF regulator is 300mA. VSP_RF regulator also has a built in protection which limits current to max 300mA in normal operation and to max 500 mA in case of a short.

The regulators are operating when either the *Operating Control Register* bit *en* is set or pin EN is high. In Power-down mode the regulators are not operating, VSP_A and VSP_RF are connected to VDD through 1kΩ resistors. Connection through resistors assures smooth power up of the system and a smooth transitions from Stand-by mode to other operating modes. In case regulators were regulating or were transparent at power up a huge current would be pulled from VDD supply to charge blocking capacitors of regulated outputs which is especially problematic for battery powered systems.

At power up the regulated voltage is set to maximum voltage (3.4V).

The regulator voltage can then be set automatically or "manually". Automatic procedure is started by sending the direct command *Adjust Regulators*. In this procedure regulated voltage is set 250mV below VDD. This procedure assures that reader operates with maximum possible power while still assuring good PSRR.

Regulator operation can be controlled and observed by writing and reading two Regulator registers.

Regulator Display Register (#15) is a read only register which displays actual regulated voltage when regulator is operating. In Power-down mode its content is forced to 00.

By writing *Regulated Voltage Definition Register* (#16) user chooses between automatic and "manual" adjustment of regulated voltage. Automatic mode is chosen when bit *reg_s* is 0 (default and also recommended state). When bit *reg_s* is asserted to 1 regulated voltage is defined by bits *rege_3* to *rege_1* of the same register.

Communication to External Microcontroller

The AS3909/10 is a slave device and the external microcontroller initiates all communication. Communication is done by a 4-wire Serial Peripheral Interface (SPI). The AS3909/10 asks microcontroller for its attention by sending an interrupt (pin INTR).

In addition the microcontroller can use clock signal available on pin MCU_CLK when the oscillator is running.

The microcontroller can also drive pin EN. Putting this pin high has the same function as setting the *Operation Control Register* bit *en* (entry in Ready mode).

Serial Peripheral Interface (SPI)

For details about SPI timing refer to Figure 8.

Figure 12:
Serial Peripheral Interface (4-wire Interface) Signal Lines

Name	Signal	Signal Level	Description
SEN	Digital Input with pull down	CMOS	SPI Enable
SDATAI	Digital Input	CMOS	Serial Data input
SDATAO	Digital Output with tristate	CMOS	Serial Data output
SCLK	Digital Input	CMOS	Clock for serial communication

SPI Operation MODE Bits

When signal SEN is low, the SPI interface is in reset and SDATAO is in tristate; when it is high, SPI interface is enabled. It is recommended to keep signal SEN low whenever the SPI interface is not in use. SDATAI is sampled at the falling edge of SCLK. All communication is done in blocks of 8 bits (bytes). First two bits of first byte transmitted after low to high transition of SEN define SPI operation mode. Figure 13 defines possible modes:

Figure 13:
SPI Operation Patterns <A7-A6>

MODE	MODE Pattern (com. bits)								MODE Related Data							
	MODE		Register Address						Register Data							
	M1	M0	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
WRITE Mode	0	0	A5	A4	A3	A2	A1	A0	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
READ Mode	0	1	A5	A4	A3	A2	A1	A0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
FIFO Load	1	0	0	0	0	0	0	0	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
FIFO Read	1	0	1	1	1	1	1	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
COMMAND Mode	1	1	C5	C4	C3	C2	C1	C0								

Writing of Data to Addressable Registers (WRITE Mode)

SDATAI is sampled at the falling edge of SCLK (see Figure 14, Figure 15). A SEN LOW pulse indicates the end of the WRITE command after register has been written. Auto incrementing address is supported, which means that if after the address and first data byte some additional data bytes are sent, they are then written to addresses incremented by 1. In case the command is terminated by putting SEN low before a packet of 8 bits composing one byte is sent, writing of this register is not performed. In case the register on the defined address does not exist or it is a read only register, no write is performed. Following examples show cases of writing a single byte and writing multiple bytes with auto-incrementing address.

Figure 14:
Writing of a Single Byte (falling edge sampling)

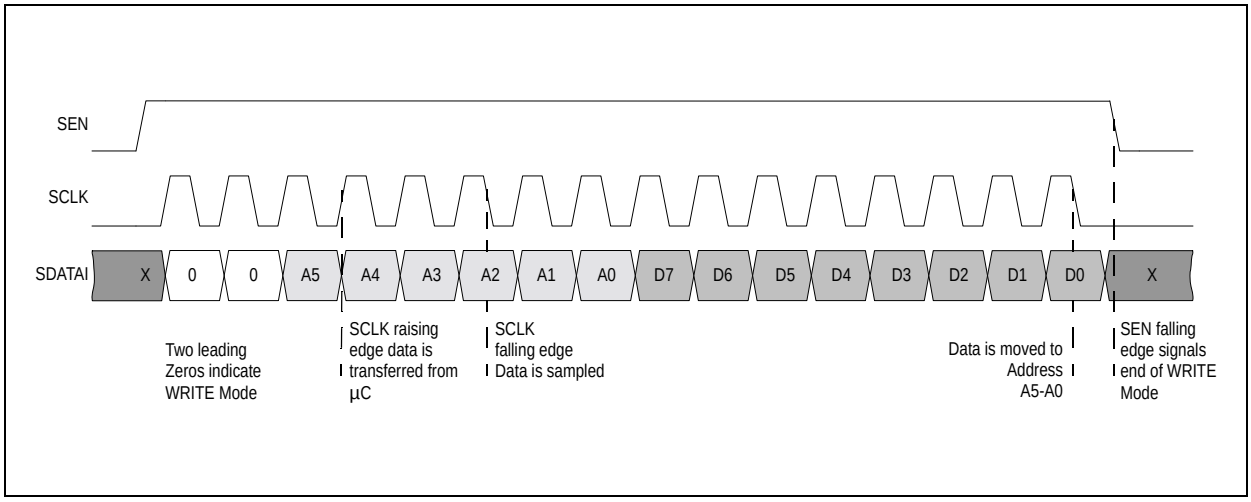
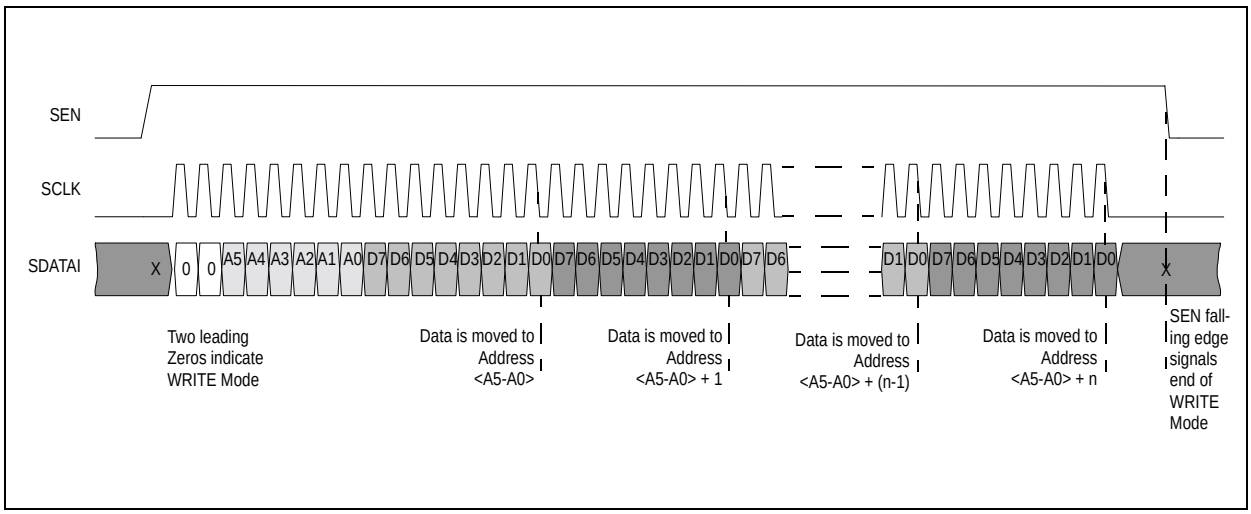


Figure 15:
Writing of Register Data with Auto-Incrementing Address



Reading of Data from Addressable Registers (READ Mode)

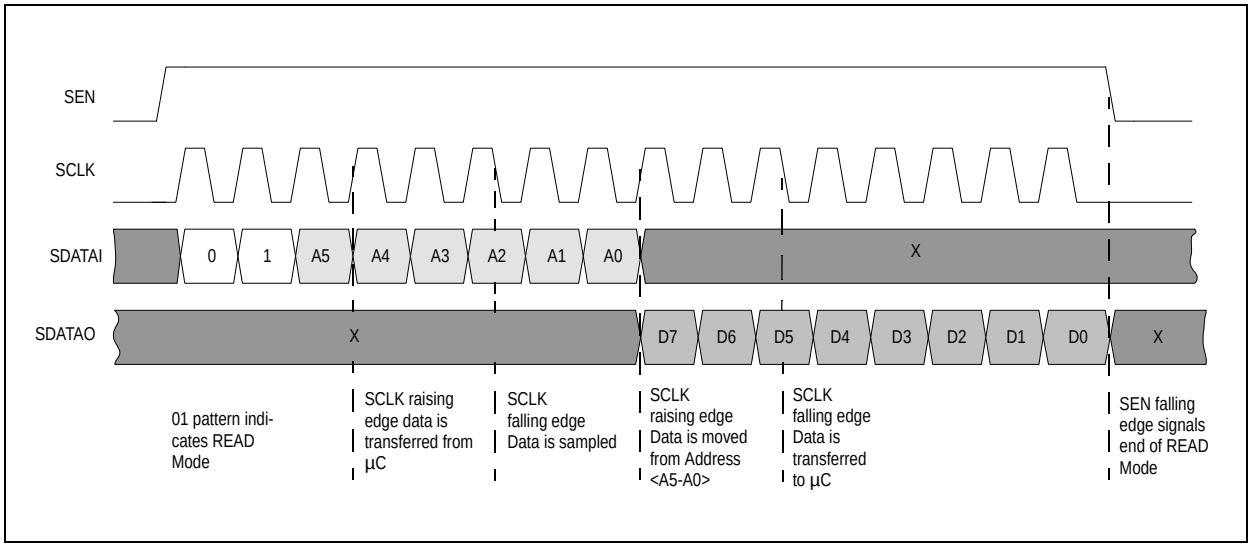
The command control Byte for a read command consists of a command code and an address. After the command code, the address of register to be read has to be provided from the MSB to the LSB. Then one or more data bytes can be transferred from the SPI slave to the master, always from the MSB to the LSB. As in case of the write command also the read command supports auto-incrementing address. To transfer bytes from consecutive addresses, SPI master has to keep the SEN signal high and the SCLK has to be active as long as data need to be read from the slave.

SDATAI is sampled at the falling edge of SCLK (like shown in the following diagrams), data to be read from the AS3909/10 internal register is driven to SDATAO pin on rising edge of SCLK and is sampled by the master (µC) at the falling edge of SCLK.

A SEN LOW pulse has to be performed after register data has been transferred in order to indicate the end of the READ command and prepare the Interface to the next command control Byte.

In case the register on defined address does not exist all 0 data is sent to SDATAO. Figure 16 illustrates an example for reading of a single byte.

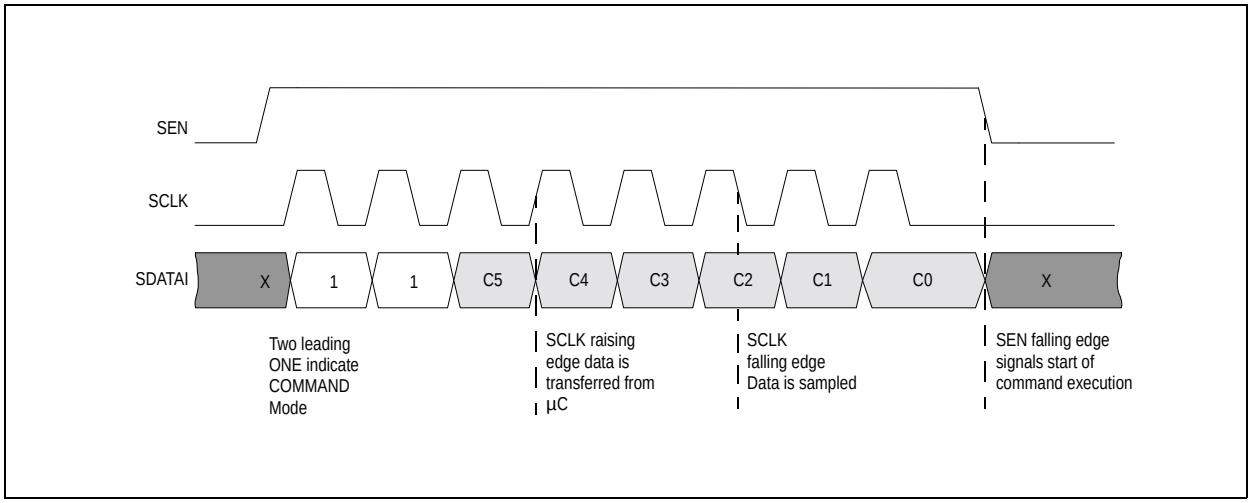
Figure 16:
Reading of a Single Register Byte



Sending Direct Commands

Direct commands have no arguments, so a single byte is sent. Command mode is entered if the SPI is started with two leading ONE. After the COMMAND mode code 11 (see Figure 20), the six bit command code is sent MSB to the LSB. The command is executed on falling edge of SEN. During the direct command execution, starting another activity over the SPI interface is not allowed.

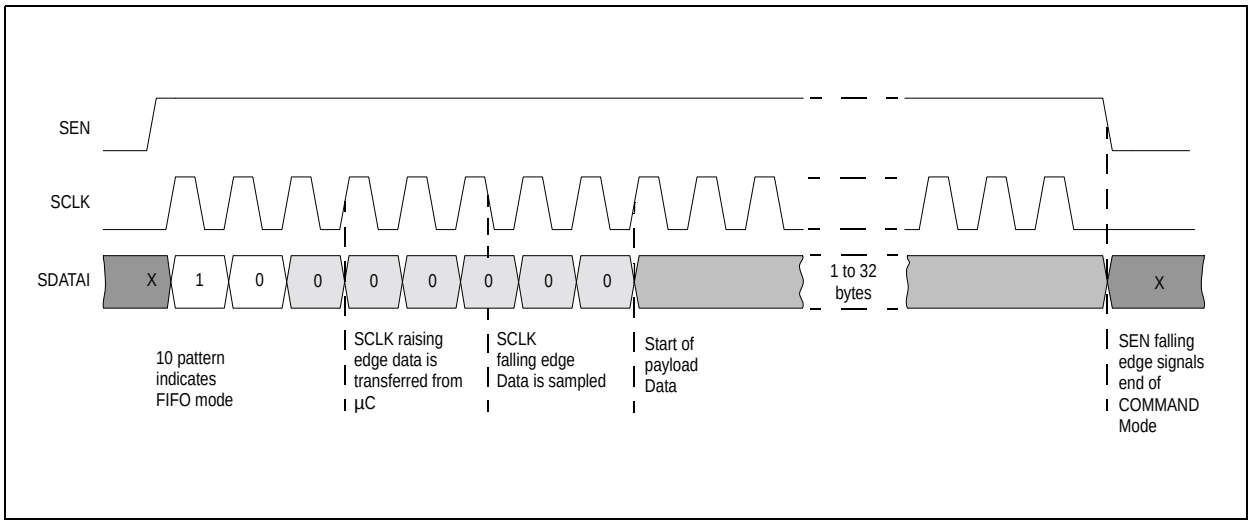
Figure 17:
Sending Direct Commands



Loading Transmitting Data into FIFO

Loading the transmitting data into the FIFO is similar to writing data into an addressable registers. Difference is that in case of loading more bytes all bytes go to the FIFO. The command mode code 10 indicates FIFO operations. In case of loading transmitting data into FIFO all bits <C5 – C0> are set to 0. Then a bit-stream, the data to be sent (1 to 32 bytes), can be transferred. In case the command is terminated by putting SEN low before a packet of 8 bits composing one byte is sent, writing of that particular byte in FIFO is not performed. Figure 18 shows how to load the Transmitting Data into the FIFO.

Figure 18:
Loading Transmitting Data into FIFO



Reading Received Data from FIFO

Reading received data from the FIFO is similar to reading data from an addressable registers. Difference is that in case of reading more bytes they all come from the FIFO. The command mode code 10 indicates FIFO operations. In case of reading the received data from the FIFO all bits

<C5 – C0> are set to 1. On the following SCLK rising edges the data from FIFO appears as in case of read data from addressable registers. In case the command is terminated by putting SEN low before a packet of 8 bits composing one byte is read that particular byte is considered unread and will be the first one read in next FIFO read operation.

Interrupt Interface

When an interrupt condition is met the source of interrupt bit is set in the *Interrupt Register* and the INTR pin transitions to high.

The microcontroller then reads the *Interrupt Register* to distinguish between different interrupt sources. After the *Interrupt Register* is read its content is reset to 0 and INTR pin signal transitions to low.

Note(s): There may be more than one *Interrupt Register* bit set in case the microcontroller did not immediately read the *Interrupt Register* after the INTR signal was set and another event causing interrupt occurred.

In case an interrupt from a certain source is not required it can be disabled by setting corresponding bit in the Mask *Interrupt Register*. In case of masking a certain interrupt source the interrupt is not produced, but the source of interrupt bit is still set in *Interrupt Register*.

After reading the *Interrupt Register* the 13.56MHz clock coming from the oscillator is used to produce a reset signal which clears it and resets INTR signal. Practically in all interrupt cases the oscillator is running when an interrupt is produced. The only exception is the interrupt in the Initial NFC Target mode where only the Target Activation Detector is operating. In this case the interrupt is cleared with first SCLK rising edge following reading of the *Interrupt Register* (an extra dummy CLK pulse during reading of the *Interrupt Register* or first SCLK pulse of the next SPI command will do the job).

Figure 19:
Serial Peripheral Interface (4-wire Interface) Signal Lines

Name	Signal	Signal Level	Description
INTR	Digital Output	CMOS	Interrupt Output pin

FIFO Water Level and FIFO Status Register

The AS3909/10 contains a 32 byte FIFO. In case of transmitting the Control logic shifts data which was previously loaded by the external microcontroller to the Framing Block and further to the Transmitter. During reception, the demodulated data is stored in the FIFO and the external microcontroller can download received data once reception was terminated.

Transmit and receive capability the AS3909/10 is not limited by of the FIFO size due to a FIFO water level interrupt system. During transmission an interrupt is sent (interrupt due to FIFO water level) when the content of data in the FIFO which still need to be sent is lower than the FIFO water level for receive. The external microcontroller can now add more data in the FIFO. The same stands for receive mode. In case the number of received bytes gets over the FIFO water level for receive an interrupt is sent to inform the external controller that data has to be downloaded from FIFO.

The external controller has to serve the FIFO faster than data is transmitted or received. A general rule is that the SCLK frequency has to be at least double than the actual data rate in receive or transmit.

There are two settings of the FIFO water level available for receive and transmit in *Configuration Register 5* (#05).

After data is received the external microcontroller needs to know how long the receive data string was before downloading data from the FIFO: This information is available in the *FIFO Status Register* (#09) which displays number of bytes in the FIFO which were not read out.

The *FIFO Status Register* also contains a FIFO overflow bit. This bit is set when during reception the external processor did not react on time and more than 32 bytes were written in FIFO. The received data is of course lost in such a case.

Direct Commands

Figure 20:
List of Direct Commands

Code	Command	Comments
000001	Set default	Puts the AS3909/10 in default state (same as after power-up)
000010	Clear	Stops all activities and clears FIFO
000100	Transmit with CRC	Starts a transmit sequence using automatic CRC generation
000101	Transmit without CRC	Starts a transmit sequence without automatic CRC generation
000110	Transmit REQA	Transmits REQA command (ISO-14443A mode only)

Code	Command	Comments
000111	Transmit WUPA	Transmits WUPA command (ISO-14443A mode only)
001000	NFC transmit with Initial RF Collision Avoidance	Equivalent to *Transmit with CRC* with additional RF Collision Avoidance
001001	NFC transmit with Response RF Collision Avoidance	Equivalent to *Transmit with CRC* with additional RF Collision Avoidance
001010	NFC transmit with Response RF Collision Avoidance with n=0	Equivalent to *Transmit with CRC* with additional RF Collision Avoidance
010000	Mask receive data	Receive after this command is ignored
010001	Unmask receive data	Receive data following this command is normally processed (this command has priority over internal mask receive timer)
010010	AD convert	A/D conversion of signal on AD_IN pin is performed, result is stored in *A/D Converter Output Register*
010011	Measure RF	RF amplitude is measured, result is stored in *A/D Converter Output Register*
010100	Squelch	Performs gain reduction based on the current noise level.
010101	Clear Squelch	Resumes gain settings which were in place before sending *Squelch* command
010110	*Adjust regulators*	Adjusts supply regulators according to the current supply voltage level
010111	Calibrate modulation depth	Starts sequence which activates the TX, measures the modulation depth and adapts it to comply with the specified modulation depth
011000	Calibrate antenna (1)	Starts the sequence to adjust parallel capacitances connected to TRIMx pins so that the antenna LC is in resonance.
011001	Check antenna resonance	Measurement of antenna LC tank resonance to determine whether calibration is needed.
011010	Clear RSSI	Clears RSSI bits and restarts the measurement
011100	Transparent mode	Enter in Transparent mode

Note(s) and/or Footnote(s):

1. Only available in AS3910.

Set Default

This direct command puts the AS3909/10 in the same state as power-up initialization. All registers are initialized to the default state. Please note that results of different calibration and adjust commands are also lost. This direct command is accepted in all operating modes.

Clear

This direct command stops all current activities (transmission or reception) and clears FIFO. It also clears Collision and *Interrupt Registers*. This command has to be sent first in a sequence preparing a transmission (except in case of direct commands *Transmit REQA* and *Transmit WUPA*).

Transmit Commands

All Transmit commands (*Transmit with CRC*, *Transmit without CRC*, *Transmit REQA* and *Transmit WUPA*) are only accepted in case the Transmitter is enabled (bit *tx_en* is set).

NFC Transmit Commands

The NFC transmit commands (*NFC transmit with Initial RF Collision Avoidance*, *NFC transmit with Response RF Collision Avoidance*, *NFC transmit with Response RF Collision Avoidance* with n=0) are used to transmit requests and responses in the NFC mode. Before actual transmission the RF Collision avoidance with Collision avoidance threshold defined in the *NFCIP Field Detection Threshold Register* is performed.

In the command NFC transmit with Response RF Collision Avoidance n is randomly set in a range from 0 to 3, while in the command NFC transmit with Response RF Collision Avoidance with n=0 it is set to 0. In case collision is detected during the RF Collision Avoidance the transmission is not done and an interrupt is sent with flag INTR due to NFC event.

The NFC transmit commands switch on and off the transmission block, setting the Operation control bit *tx_en* in the NFC mode is not allowed.

Timing of the NFC transmit commands is according to the ISO/IEC 18092 standard. For some timings the ISO/IEC 18092 specifies a range.

Figure 21:
NFC P2P Timings Implemented in AS3909/10

Symbol	Parameter	Value	Unit	Note
T_{IDT}	Initial delay time	302	µs	Initial RF Collision Avoidance
T_{RWF}	RF waiting time	37.76	µs	
T_{IRFG}	Initial guard time	5.11	ms	Initial RF Collision Avoidance
T_{ADT}	Active delay time	151	µs	Response RF Collision Avoidance
T_{ARFG}	Active guard time	84	µs	Response RF Collision Avoidance
T_{GAS}	Guard time after sending response or request	65	µs	T_{GAS} is the time during which RF field stays switched on after sending a response or request. This time is not specified in the ISO/IEC 18092.

An interrupt due to end of transmission is sent when RF field is switched off.

All NFC Transmit commands are only authorized in case the ISO mode configuration bit *nfc* is set and the oscillator and regulators are running.

Mask Receive Data and Unmask Receive Data

After the direct command *Mask Receive Data* the signal *rx_on* which enables the RSSI and AGC operation of the Receiver (see "Receiver" on page 11) is forced to low, processing of the receiver output by the framing block is disabled, all received modulation is rejected. This command is useful to block receiver and receive framing from processing the data when there is actually no input and only a noise would be processed (for example in case where a transponder processing time after receiving a command from the reader is long).

The direct command *Unmask Receive Data* is enabling normal processing of the received data (signal *rx_on* is set high to enable the RSSI and AGC operation, the framing block is enabled. A common use of this command is to enable again the receiver operation after it was disabled by the command *Mask Receive Data*.

Another possible use is in case one wants that the receive processing starts immediately after the transmit command (usually the receiver operation is enabled 40 µs after the transmission is terminated). This is accomplished by sending the *Unmask Receive Data* immediately after the end of transmission interrupt is received.

The command *Unmask Receive Data* has to be used in the NFC target mode. The sequence implemented in the AS3909/10 supposes that every action is started with a transmit command, after sending the transmit data, the receive mode is automatically entered to process the response. Such a sequence is always in place in case of the ISO-14443 reader mode and also in case of the NFCIP mode where the AS3909/10 is the initiator. In case of the NFC target mode this sequence is started by receiving the interrogator request. After the interrupt caused by the first initiator request command *Unmask Receive Data* is sent to force the AS3909/10 in receive mode.

The commands *Mask Receive Data* and *Unmask Receive Data* are only accepted when the Receiver is operating.

AD Convert

A/D conversion of signal on AD_IN pin is performed; result is stored in *A/D Converter Output Register* (see "A/D Converter" on page 11).

Duration time: 42µs max.

This command is accepted in any mode where the oscillator and regulators are running.

Measure RF

This command measures the amplitude on the RFI inputs and stores result in the *A/D Converter Output Register* (see also "A/D Converter" on page 11 and "Amplitude Detector" on page 19).

When this command is executed the output of the Amplitude detector is multiplexed to the A/D converter input (the A/D converter is in absolute mode). The Amplitude Detector conversion gain is 0.6 Vinpp/Vout. One LSB of the A/D converter output represents 13.02mVpp on the RFI inputs, a 3Vpp signal which is maximum allowed level on each of the two RFI inputs results in 1.8V output DC voltage and would produce the value of 1110 0110 on the A/D converter output.

Duration time: 42µs max.

This command is accepted in any mode where the oscillator and regulators are running.

Squelch

This direct command is intended to avoid demodulation problems of transponders which produce a lot of noise during data processing (while data sent by reader is processed and answer prepared). It can also be used in a noisy environment. The operation of this command is explained in "Squelch" on page 16.

Duration time: 500µs max

This command is only accepted when the Transmitter and Receiver are operating.

Clear Squelch

Clears the gain reduction which was established by sending *Squelch* command.

This command is accepted in any mode.

Adjust Regulators

When this command is sent the power supply level of VDD is measured in maximum load conditions and the regulated voltage reference is set 250 mV below this measured level to assure maximum possible stable regulated supply (see "Power Supply, Regulators" on page 21). Using this command increases the system PSSR.

At the beginning of execution of this command, both the receiver and transmitter are switched on to have the maximum current consumption, the regulators are set to the maximum 3.4V regulated voltage. After 300µs VSP_RF is compared to VDD, in case VSP_RF is not at least 250mV lower the regulator setting is reduced for one step (100mV) and measurement is done after 300µs. Procedure is repeated as long as VSP_RF drops 250mV below VDD of until minimum regulated voltage (2.4V) is reached.

Duration time: 5ms max

This command is accepted in any mode where the oscillator and regulators are running. This command is not accepted in case the external definition of the regulated voltage is selected in the *Regulated Voltage Definition Register* (#16, bit *reg_s* is set to H)

Calibrate Modulation Depth

Starts a patent pending sequence, which activates the transmission, measures the modulation depth and adapts it to comply with the modulation depth specified in the *Modulation Depth Definition Register* (#10). When calibration procedure is finished result is displayed in *Modulation Depth Display Register*. Please see "AM Modulation Depth Definition Using Direct Command Calibrate Modulation Depth" on page 60 for details about setting the AM modulation depth and running this command.

Duration time: 10ms max

This command is accepted in any mode where the oscillator and regulators are running.

Calibrate Antenna[2]

Sending this command starts a patent pending sequence which adjusts the parallel capacitances connected to TRIMx pins so that the antenna LC is in resonance. See "Calibrate Antenna Resonance" on page 64 for details.

Duration time: 400µs max

This command is accepted in any mode where the oscillator and regulators are running.

Check Antenna Resonance

This command measures the antenna LC tank resonance to determine whether a calibration is needed. See "Check Antenna Resonance" on page 63 for details.

Duration time: 42µs max.

This command is accepted in any mode where the oscillator and regulators are running.

Clear RSSI

The Receiver automatically clears the RSSI bits in the *Receiver State Display Register* and starts to measure the RSSI when the signal *rx_on* is asserted. Since the RSSI bits store peak value (peak-hold type) eventual variation of the receiver input signal will not be followed (this may happen in case of long message or test procedure). The direct command *Clear RSSI* clears the RSSI bits in the *Receiver State Display Register*, the RSSI measurement is restarted (in case of course *rx_on* is still high).

2. Only available in AS3910.

Transparent Mode

Enter in the Transparent mode. The Transparent mode is entered on the falling edge of signal SEN and is maintained as long as signal SEN is kept low. See "Transparent Mode" on page 66 for details about the Transparent Mode.

This command is only accepted when the Transmitter and Receiver are operating.

Registers

The 6 bit register addresses below are defined in the hexadecimal notation. The possible address range is from 00(hex) to 3F(hex). A sign # before a number is used in this document to reference a hexadecimal number.

There are two types of registers implemented in the AS3909/10: configuration registers and display registers. The configuration registers are used to configure the AS3909/10. They can be written and read through the SPI (RW). The display registers are read only (RO); they contain information about the AS3909/10 internal state which can be accessed through the SPI.

Main Registers

Figure 22:
ISO Mode Definition Register

<table>
<tr><th colspan="7">Address # 00: ISO Mode Definition Register</th><th>Type: RW</th></tr>
<tr><th>Bit</th><th>Name</th><th>Def.</th><th colspan="4">Function</th><th>Comments</th></tr>
<tr><td>7</td><td>nfc</td><td>0</td><td colspan="4">1=NFC, 0=ISO-14443</td><td>NFC means NFCIP-1,
106 kbps active communication mode</td></tr>
<tr><td>6</td><td>b_a</td><td>0</td><td colspan="4">1=ISO-14443B, 0=ISO-14443A</td><td>Applicable in case nfc=0</td></tr>
<tr><td>5</td><td>tx_rate2</td><td>0</td><td>tx_rate2</td><td>tx_rate1</td><td>tx_rate0</td><td>bit rate</td><td rowspan="8">Selects ISO-14443 data rate for transmit, Applicable in case nfc=0</td></tr>
<tr><td>4</td><td>tx_rate1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>106kb/s</td></tr>
<tr><td rowspan="5">3</td><td rowspan="5">tx_rate0</td><td rowspan="5">0</td><td>0</td><td>0</td><td>1</td><td>212kb/s</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>424kb/s</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>848kb/s</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RFU</td></tr>
<tr><td colspan="4"></td></tr>
</table>

Address # 00: ISO Mode Definition Register							Type: RW
Bit	Name	Def.	Function				Comments
2	rx_rate2	0	rx_rate2	rx_rate1	rx_rate0	bit rate	Selects ISO-14443 data rate for receive, Applicable in case nfc=0
1	rx_rate1	0	0	0	0	106kb/s	
0	rx_rate0	0	0	0	1	212kb/s	
			0	1	0	424kb/s	
			0	1	1	848kb/s	
			1	x	x	RFU	

Note: In case nfc=1, then both transmit and receive data rates are set to 106kbps independent of TX and RX setting. Default setting is set at power up and after Set Default command.

Figure 23:
Operation Control Register

Address # 01: Operation Control Register				Type: RW
Bit	Name	Def.	Function	Comments
7	en	0	en=1 enables oscillator and regulator (Ready mode)	Is internally ORed with the EN pin
6	rx_en	0	rx_en=1 enables receiver operation	
5	rx_lp	0	rx_lp=1 low power receiver operation	Receive consumption is reduced
4	tx_en	0	tx_en=1 enables RF output	
3	nfc_t	0	nfc_t =1 enables Initial NFC Target mode	At the moment RF field is detected, interrupt is sent.
2			Not used	
1				
0				

Note: Receive low power operation sacrifices the input sensitivity for low consumption. If Rx consumption is reduced from 10mA to 5mA, then a 10mA reader operation is possible. Default setting is set at power up and after Set Default command.

Configuration Registers

Figure 24:
Configuration Register 2

Address # 02: Configuration Register 2						Type: RW
Bit	**Name**	**Def.**	**Function**			**Comments**
7	sing	0	1 → only RFO1 driver will be used			Choose between single and differential driving of antenna.
6	envi	0	1 → input applied to RFI1 is envelope			RF envelope input
5	tf2	0	1 → reduces the gain for 11 dB in first stage after peak detector			When both bits are set there is 17 dB gain reduction in first stage
4	tf1	0	1 → reduces the gain for 6 dB in first stage after peak detector			
3	osc	0	0 → 13.56MHz Xtal, 1 → 27.12MHz Xtal			Selector for crystal oscillator
2	out_cl1	0	**out_cl1**	**out_cl0**	**out_cl**	Selection of clock frequency on MCU_CLK output. In case of "11", MCU_CLK output is permanently low.
1	out_cl0	0	0	0	3.39MHz	
			0	1	6.78 MHZ	
			1	0	13.56 MHZ	
			1	1	no output	
0			Not used			

Note: Default setting is set at power up and after Set Default command.

Figure 25:
Configuration Register 3

<table>
<tr><th colspan="8">Address # 03: Configuration Register 3
(ISO-14443A and NFC)</th><th>Type: RW</th></tr>
<tr><th>Bit</th><th>Name</th><th>Def.</th><th colspan="6">Function</th><th>Comments</th></tr>
<tr><td>7</td><td>crc_rx</td><td>0</td><td colspan="6">1 → receive without CRC</td><td>For ISO-14443A anticollision.
Valid only for ISO14443A mode, receive without CRC is not supported in ISO14443B mode.</td></tr>
<tr><td>6</td><td>no_par</td><td>0</td><td colspan="6">1 → no byte parity checking</td><td>When set to 1 parity bits are still detected and removed before received data is put in FIFO, but there is no check for their correctness.</td></tr>
<tr><td>5</td><td>p_len3</td><td>0</td><td>p_len3</td><td>p_len2</td><td>p_len1</td><td>p_len0</td><td>reduction</td><td rowspan="6">Modulation pulse reduction,
Defined in number of 13.56 MHz clock periods.</td></tr>
<tr><td>4</td><td>p_len2</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>3</td><td>p_len1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>74ns</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">p_len0</td><td rowspan="2">0</td><td>-
-</td><td>-
-</td><td>-
-</td><td>-
-</td><td>-
-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1106ns</td></tr>
<tr><td>1</td><td></td><td></td><td colspan="6" rowspan="2">Not used</td><td rowspan="2"></td></tr>
<tr><td>0</td><td></td><td></td></tr>
</table>

Note: Default setting is set at power up and after Set Default command.

Figure 26:
Configuration Register 4

Address # 04: Configuration Register 4 (ISO-14443B)							Type: RW
Bit	**Name**	**Def.**	**Function**				**Comments**
7	egt2	0	**egt2**	**egt1**	**egt0**	**number of EGT**	EGT time defined in number of etu
6	egt1	0	0	0	0	0	
5	egt0	0	0	0	1	1	
			- -	- -	- -	- -	
			1	1	0	6	
			1	1	1	6	
4	sof_0	0	0 → 10 etu, 1 → 11 etu				SOF, number of etu with logic 0 (10 or 11)
3	sof_1	0	0 → 2 etu, 1 → 3 etu				SOF, number of etu with logic 1 (2 or 3)
2	eof	0	0 → 10 etu, 1 → 11 etu				EOF, number of etu with logic 0 (10 or 11)
1	egt	0	0 → no EGT after last character, 1 → EGT after each character				
0			Not used				

Note: Default setting is set at power up and after Set Default command.

Figure 27:
Configuration Register 5

Address # 05: Configuration Register 5				Type: RW
Bit	**Name**	**Def.**	**Function**	**Comments**
7	pmd	0	1 → PM demodulation 0 → AM demodulation	AM/PM demodulation selection
6	am	0	0 → OOK, 1 → AM	Valid for Transparent mode. For ISO-14443 and NFC modes, modulation type is set automatically (ISO-14443A and NFC is OOK, ISO-14443B is AM see Figure 38)
5			Not used	
4				
3				
2	fifo_lr	0	0 → 28, 1 → 24	FIFO water level for receive
1	fifo_lt	0	0 → 4, 1 → 8	FIFO water level for transmit
0			Not used	

Note: Default setting is set at power up and after Set Default command.

Figure 28:
Receiver Configuration Register

Address # 06: Receiver Configuration Register								Type: RW
Bit	**Name**	**Def.**	**Function**					**Comments**
7	agc_en	0	1 → AGC is enabled					AGC operation mode
6	agc_m	0	1 → AGC operate on first eight subcarrier pulses 0 → AGC operate during complete receive period					
5	rg2	0	**rg2**	**rg1**	**rg0**	**Gain reduction**		Gain reduction in 3dB steps. From 0 to 21dB.
4	rg1	0	0	0	0	0		
3	rg0	0	0	0	1	3 dB		
			- -	- -	- -	- -		
			1	1	1	21 dB		
2	fs2	0	**fs2**	**fs1**	**fs0**	**Filter Selection**	**Comment**	Filter selection is automatically set when ISO mode or receive data rate change (Change of ISO mode definition register). After automatic preset filter, selection can be changed by writing these bits.
1	fs1	0	0	0	0	ISO-14443A 106 kb/s	Automatic preset	
0	fs0	0	0	0	1	ISO-14443B 106 kb/s	Automatic preset	
			0	1	0	ISO-14443A/ B 212 kb/s	Automatic preset	
			0	1	1	ISO-14443A/ B 424 kb/s	Automatic preset	
			1	0	0	ISO-14443A/ B 848 kb/s	Automatic preset	
			1	1	0	424/484 kHz subcarriers	No automatic preset	
			1	1	1	212 kHz	No automatic preset	
						Other combinations not supported or used for block testing purposes		

Note: Default setting is set at power up and after Set Default command, filter selection bits are preset also when ISO mode or receive data rate change.

Figure 29:
Mask Interrupt Register

Address # 07: Mask Interrupt Register				Type: RW
Bit	**Name**	**Def.**	**Function**	**Comments**
7	M_osc	0	mask INTR when oscillator frequency is stable	
6	M_nfc	0	mask INTR due to nfc event	
5	M_wl	0	mask INTR due to FIFO water level	
4	M_rxs	0	mask INTR due to end of receive	
3	M_txe	0	mask INTR due to end of transmission	
2	M_err	0	mask INTR due to error in receive data coding	
1	M_crc	0	mask INTR due to CRC error	
0	M_col	0	mask INTR due to bit collision	

Note: Default setting is set at power up and after Set Default command.

Figure 30:
Interrupt Register

Address # 08: Interrupt Register			Type: R
Bit	**Name**	**Function**	**Comments**
7	I_osc	INTR when oscillator frequency is stable	Set after enable
6	I_nfc	INTR due to nfc event	Set when nfc_t is 1 and en=0 informing that an RF field has been detected, Set when transmission could not be done due to detection of RF field during RF Collision Avoidance
5	I_wl	INTR due to FIFO water level	Set during receive, informing that FIFO is almost full and has to be read out. Set during transmit, informing that FIFO is almost empty and that additional data has to be sent.
4	I_rxs	INTR due to end of receive	
3	I_txe	INTR due to end of transmission	
2	I_err	INTR due to error in receive data coding	This includes parity error and framing error
1	I_crc	INTR due to CRC error	

Address # 08: Interrupt Register			Type: R
Bit	Name	Function	Comments
0	I_col	INTR due to bit collision	Valid only for ISO-14443A

Note: At power up and after Set Default command, content of this register is set to 0.
After Interrupt register read, its content is set to 0

Figure 31:
FIFO Status Register

Address # 09: FIFO Status Register			Type: R
Bit	Name	Function	Comments
7	fifo_b5	Number of bytes (binary coded) in the FIFO which were not read out	Valid range is from 000000 to 100000
6	fifo_b4		
5	fifo_b3		
4	fifo_b2		
3	fifo_b1		
2	fifo_b0		
1	fifo_ovr	FIFO overflow	
0	rx_act	Active receive. This bit is set to 1 when start of transponder message is detected and stays high until end of receive.	By reading this bit it can be checked whether transponder is answering. See also Application Notes (Active receive).

Note: At power up and after direct commands, Set Default and Clear content of this register is set to 0.

Figure 32:
Collision Register

Address # 0A: Collision Register (for ISO-14443A only)			Type: R
Bit	**Name**	**Function**	**Comments**
7	c_byte3	Number of full bytes before the bit collision happened	
6	c_byte2		
5	c_byte1		
4	c_byte0		
3	c_bit2	Number of bits before the collision in the byte where the collision happened	
2	c_bit1		
1	c_bit0		
0	rfu	Not used, always 0	

Note: At power up and after direct commands Set Default and Clear content of this register is set to 0.

Figure 33:
Number of Transmitted Bytes Register 0

Address # 0B: Number of Transmitted Bytes Register 0				Type: RW
Bit	**Name**	**Def.**	**Function**	**Comments**
7	ntx1	0	Number of bytes to be transmitted in one command, LSB bits	Maximum supported number of bytes is 1023
6	ntx0	0		
5	nbtx2	0	Number of bits in the split byte 000 means that all bytes all full	Applicable only to ISO-14443A bit oriented anticollision frame in case last byte is split byte
4	nbtx1	0		
3	nbtx0	0		
2			Not used	
1	frm4	0	4bit response frame	Has to be set to 1 when 4bit response frame is expected (Mifare Ultralight)
0	antcl	0	ISO-14443 anticollision frame	Has to be set to 1 when ISO-14443A bit oriented anticollision frame is sent

Note(s) and/or Footnote(s):

1. Bits frm4 and antcl are cleared after transmission is performed.
2. Default setting is set at power up and after Set Default command.

Figure 34:
Number of Transmitted Bytes Register 1

Address # 0C: Number of Transmitted Bytes Register 1				Type: RW
Bit	**Name**	**Def.**	**Function**	**Comments**
7	ntx9	0	Number of bytes to be transmitted in one command, MSB bits	Maximum supported number of bytes is 1023
6	ntx8	0		
5	ntx7	0		
4	ntx6	0		
3	ntx5	0		
2	ntx4	0		
1	ntx3	0		
0	ntx2	0		

Note: Default setting is set at power up and after Set Default command

A/D Converter Output Register

Figure 35:
A/D Output Register

Address # 0D: A/D Output Register			Type: R
Bit	**Name**	**Function**	**Comments**
7	ad7	Displays results of A/D conversion.	
6	ad6		
5	ad5		
4	ad4		
3	ad3		
2	ad2		
1	ad1		
0	ad0		

Note: At power up and after Set Default command, content of this register is set to 0.

Antenna Calibration Registers

Figure 36:
Antenna Calibration Register

Address # 0E: Antenna Calibration Register			Type: R
Bit	**Name**	**Function**	**Comments**
7	tri_3	MSB	This register stores result of *Calibrate antenna* command. LC trim switches are defined by data written in this register in case trim_s=0. A bit set to 1 indicates that corresponding transistor on TRIM1_x and TRIM2_x pin is switched on.
6	tri_2		
5	tri_1		
4	tri_0	LSB	
3	tri_err	1 → antenna calibration error	Set when *Calibrate antenna* sequence was not able to adjust resonance
2		Not used	
1			
0			

Note: At power up and after Set Default command content of this register is set to 0.

Figure 37:
External Trim Register

Address # 0F: External Trim Register				Type: RW
Bit	**Name**	**Def.**	**Function**	**Comments**
7	trim_s	0	0 → LC trim switches are defined by result of *Calibrate antenna* command 1 → LC trim switches are defined by bits tre_x written in this register	Defines source of driving switches on TRIMx pins
6	tre_3	0	MSB	LC trim switches are defined by data written in this register in case trim_s=1. A bit set to 1 switch on transistor on TRIM1_x and TRIM2_x pin.
5	tre_2	0		
4	tre_1	0		
3	tre_0	0	LSB	
2			Not used	
1				
0				

Note: Default setting is set at power up and after Set Default command.

AM Modulation Depth and Antenna Driver Registers

Figure 38:
Modulation Depth Definition Register

Address # 10: Modulation Depth Definition Register				Type: RW
Bit	**Name**	**Def.**	**Function**	**Comments**
7	am_s	0	0 → AM modulated level is defined by bits *mod5* to *mod0*. Level is adjusted automatically by Calibrate Modulation Depth command 1 → AM modulated level is defined by bits dram7 to dram0.	
6	mod5	0	MSB	See Application Notes for details about AM modulation level definition.
5	mod4	0		
4	mod3	0		
3	mod2	0		
2	mod1	0		
1	mod0		LSB	
0				

Note: Default setting is set at power up and after Set Default command.

Figure 39:
Modulation Depth Display Register

Address # 11: Modulation Depth Display Register			Type: R
Bit	**Name**	**Function**	**Comments**
7	md_7	MSB	Displays result of *Calibrate Modulation Depth* command. Antenna drivers are composed of 8 binary weighted segments. Bit md_x set to one indicates that this particular segment will be disabled during AM modulated state.
6	md_6		
5	md_5		
4	md_4		
3	md_3		
2	md_2		
1	md_1		
0	md_0	LSB	

Note: At power up and after Set Default command content of this register is set to 0.

Figure 40:
Antenna Driver AM Modulated Level Definition

Address # 12: Antenna Driver AM Modulated Level Definition				Type: RW
Bit	**Name**	**Def.**	**Function**	**Comments**
7	dram7	0	MSB	Antenna drivers are composed of 8 binary weighted segments. Setting a bit dram to 1 will disable corresponding segment during AM modulated state in case *am_s* bit is set to 1.
6	dram6	0		
5	dram5	0		
4	dram4	0		
3	dram3	0		
2	dram2	0		
1	dram1	0		
0	dram0	0	LSB	

Note: Default setting is set at power up and after Set Default command.

Figure 41:
Antenna Driver Non-Modulated Level Definition

Address # 13: Antenna Driver Non-Modulated Level Definition				Type: RW
Bit	**Name**	**Def.**	**Function**	**Comments**
7	droff7	0	MSB	Antenna drivers are composed of 8 binary weighted segments. Setting a bit droff to 1 will disable corresponding segment during normal non-modulated operation.
6	droff6	0		
5	droff5	0		
4	droff4	0		
3	droff3	0		
2	droff2	0		
1	droff1	0		
0	droff0	0	LSB	

Note: Default setting is set at power up and after Set Default command.

Figure 42:
NFCIP Field Detection Threshold

Address # 14: NFCIP Field Detection Threshold				Type: RW
Bit	**Name**	**Def.**	**Function**	**Comments**
7	trg_l3		Target activation level MSB	Threshold used to detect presence of interrogator magnetic field. See Figure 43 for threshold definition.
6	trg_l2			
5	trg_l1			
4	trg_l0		Target activation level LSB	
3	rfe_t3		Collision avoidance threshold MSB	Threshold used to detect presence of external field during collision avoidance. See Figure 44 for threshold definition.
2	rfe_t2			
1	rfe_t1			
0	rfe_t0		Collision avoidance threshold LSB	

Note: Default setting is set at power up and after Set Default command.

NFCIP Field Detection Threshold Register

Figure 43:
Target Activation Threshold as seen on RFI1 Input

trg_l3	trg_l2	trg_l1	trg_l0	Target activation threshold voltage [mVpp on RFI1]
x	0	0	0	forbidden (measurement is deactivated)
0	0	0	1	590
0	0	1	0	420
0	0	1	1	350
1	0	0	1	350
0	1	0	0	300
0	1	0	1	265
1	0	1	0	265
0	1	1	0	235
0	1	1	1	220
1	0	1	1	220

trg_l3	trg_l2	trg_l1	trg_l0	Target activation threshold voltage [mVpp on RFI1]
1	1	0	0	190
1	1	0	1	175
1	1	1	0	155
1	1	1	1	145

Figure 44:
Collision Avoidance Threshold as seen on RFI1 Input

rfe_3	rfe_2	rfe_1	rfe_0	Collision avoidance threshold voltage [mVpp on RFI1]
x	0	0	0	forbidden (measurement is deactivated)
0	0	0	1	50
0	0	1	0	67
0	0	1	1	88
0	1	0	0	120
1	0	0	1	145
0	1	0	1	172
1	0	1	0	185
0	1	1	0	240
1	0	1	1	255
1	1	0	0	340
0	1	1	1	350
1	1	0	1	480
1	1	1	0	700
1	1	1	1	1080

Regulator Registers

Figure 45:
Regulators Display Register

Address # 15: Regulators Display Register			Type: R
Bit	**Name**	**Function**	**Comments**
7	reg_3	MSB	This register displays actual regulated voltage when regulator is operating. In Power-down mode, its content is forced to 00. See Figure 47 for definition.
6	reg_2		
5	reg_1		
4	reg_0	LSB	
3		Not used	
2			
1			
0			

Note: At power up and after Set Default command, regulated voltage is set to maximum 3.4V.

Figure 46:
Regulated Voltage Definition Register

Address # 16: Regulated Voltage Definition Register				Type: RW
Bit	**Name**	**Def.**	**Function**	**Comments**
7	reg_s	0	0 → regulated voltages are defined by result of *Adjust regulators* command 1 → regulated voltages are defined by rege_x bits written in this register	Defines mode of regulator voltage setting
6	rege_3	0	MSB	External definition of regulated voltage. See Figure 47 for definition.
5	rege _2	0		
4	rege _1	0		
3	rege _0	0	LSB	
2			Not used	
1				
0				

Note: Default setting is set at power up and after Set Default command.

Figure 47:
Definition

reg_3 rege_3	reg_2 rege_2	reg_1 rege_1	reg_0 rege_0	Regulated voltage [V]
1	1	1	1	3.4
1	1	1	0	3.3
1	1	0	1	3.2
1	1	0	0	3.1
1	0	1	1	3.0
1	0	1	0	2.9
1	0	0	1	2.8
1	0	0	0	2.7
0	1	1	1	2.6
0	1	1	0	2.5
0	1	0	1	2.4
other combinations				2.4

Receiver State Display Register

Figure 48:
Receiver State Display Register

<table>
<tr><th colspan="7">Address # 17: Receiver State Display Register</th><th>Type: R</th></tr>
<tr><th>Bit</th><th>Name</th><th colspan="5">Function</th><th>Comments</th></tr>
<tr><td>7</td><td>rssi_3</td><td colspan="5">MSB</td><td rowspan="4">Stores peak value of RSSI measurement. Automatically cleared at beginning of transponder message and with Clear RSSI command.</td></tr>
<tr><td>6</td><td>rssi_2</td><td colspan="5"></td></tr>
<tr><td>5</td><td>rssi_1</td><td colspan="5"></td></tr>
<tr><td>4</td><td>rssi_0</td><td colspan="5">LSB</td></tr>
<tr><td>3</td><td>oscok/rfp</td><td colspan="5">Unlatched osc_ok flag in case nfc=0
Target activation detector output in case nfc=1</td><td></td></tr>
<tr><td rowspan="5">2</td><td rowspan="5">gr_2</td><td>gr_2</td><td>gr_1</td><td>gr_0</td><td>Gain reduction</td><td rowspan="5">Displays status of receiver gain reduction (result of AGC, gain reduction setting and Squelch command)</td></tr>
<tr><td>1</td><td>gr_1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td rowspan="3">0</td><td rowspan="3">gr_0</td><td>0</td><td>0</td><td>1</td><td>3 dB</td></tr>
<tr><td>-
-</td><td>-
-</td><td>-
-</td><td>-
-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>21 dB</td></tr>
</table>

Note: At power up and after Set Default command, content of this register is set to 0.

Figure 49:
Receive State Display Register - rssi_0 ... rssi_3 bits

rssi_3	rssi_2	rssi_1	rssi_0	Signal on RFI1 [mVrms]
0	0	0	0	0 ~ 0.28
0	0	0	1	0.28 ~ 0.35
0	0	1	0	0.35 ~ 0.45
0	0	1	1	0.45 ~ 0.57
0	1	0	0	0.57 ~ 0.74
0	1	0	1	0.74 ~ 0.95
0	1	1	0	0.95 ~ 1.21
0	1	1	1	1.21 ~ 1.56
1	0	0	0	1.56 ~ 2.00
1	0	0	1	2.00 ~ 2.55
1	0	1	0	2.55 ~ 3.27
1	0	1	1	3.27 ~ 4.20
1	1	0	0	4.20 ~ 5.37
1	1	0	1	5.37 ~ 6.88
1	1	1	0	6.88 ~ 8.80
1	1	1	1	>8.80

Typical Operating Sequence

At power up the AS3909/10 enters in the Stand-by mode. Content of all registers is set to the default state which is in most cases 0.

- First action of the microcontroller after a power-up should be to load the *ISO Mode Definition Register* and the configuration registers to configure reader operation.
- Since the regulators are by default set to the maximum 3.4V, which means that they are at supply voltages lower than 3.4V transparent, it is advised to send the direct command *Adjust Regulators* to improve the system PSRR.
- In case the LC tank trimming is implemented the direct command *Calibrate Antenna* has to be sent.
- In case the AM modulation will be used (ISO-14443B for example) setting the modulation depth in the *Modulation Depth Definition Register* and sending the command *Calibrate Modulation Depth* is suggested next.

After the sequence of events mentioned above the AS3909/10 is ready to operate.

ISO-14443 Reader Operation

First the Ready mode has to be entered by setting the *en* bit of the *Operation Control Register* (address #01 or asserting pin EN). In this mode the oscillator is started and the regulators are enabled. When the oscillator operation is stable an interrupt is sent. Before sending any command to a transponder the transmitter and receiver have to be enabled by setting the bits *rx_en* and *tx_en*.

In case REQA or WUPA has to be sent, then it is simply done by sending the appropriate direct command. Or else, the following sequence has to be followed:

1. Send the direct command *Clear*
2. Define the number of transmitted bytes in the registers 0B and 0C
3. Write the bytes to be transmitted in the FIFO
4. Send the direct command *Transmit with CRC* or *Transmit without CRC* (whichever is appropriate)
5. When all the data is transmitted, an interrupt is sent to inform the microcontroller that the transmission is finished (INTR due to end of transmission).

After the transmission is executed, the AS3909/10 receiver automatically starts to observe the RFI inputs to detect a transponder response. The RSSI and AGC (in case it is enabled) are started. The framing block processes the subcarrier signal from receiver and fills the FIFO with data. When the reception is finished and all the data is in the FIFO an interrupt is sent to the microcontroller (INTR due to end of receive), additionally

the *FIFO Status Register* displays the number of bytes in the FIFO so the microcontroller can proceeded with downloading the data.

In case there was an error or bit collision detected during reception, an interrupt with appropriate flag is sent. Microcontroller has to take appropriate action.

In case of an error it usually repeats the command; it can also check the RSSI level in the *Receiver State Display Register* and change the AM/ PM mode in case the RSSI is low.

In case of a bit collision it will consult the *Collision Register* to determine in which bit there was collision.

Transmit and Receive In Case Data Packet is Longer Than FIFO

In case a data packet is longer than FIFO the sequence explained above is modified.

Before transmit the FIFO is filled. During transmit an interrupt is sent when remaining number of bytes is lower than the water level (INTR due to FIFO water level). The microcontroller in turn adds more data in the FIFO. When all the data is transmitted an interrupt is sent to inform the microcontroller that transmission is finished.

During reception situation is similar. In case the FIFO is loaded with more data than the receive water level, an interrupt is sent and the microcontroller in turn reads the data from the FIFO (additionally to the interrupt the *FIFO Status Register* displays the number of bytes which were not read out). When reception is finished an interrupt is sent to the microcontroller (INTR due to end of receive), additionally the *FIFO Status Register* displays the number of bytes in the FIFO which are still to be read out.

NFCIP-1 Operation

Only the NFCIP-1 106 kbps active mode is supported.

For operation in this mode, the bit *nfc* has to be set in the *ISO Mode Definition Register*.

Next the *NFCIP Field Detection Threshold Register* (address #14) has to be written to define the thresholds for Target activation and RF Collision avoidance (see "External Field Detector" on page 19).

Please note that in the NFC mode the transmitter enable bit (*tx_en*) is never set in the *Operation Control Register*. The transmitter is activated automatically by the NFC transmit commands).

NFCIP Target

The AS3909/10 enters in the Initial NFC Target mode by setting the *nfc_t* bit in the *Operation Control Register*. In this low power mode only the Target Activation Detector is running.

At the moment presence of external the RF field is detected an interrupt is sent (INTR due to nfc event). The microcontroller can now activate the oscillator, regulators and receiver.

As explained in "Target Activation Detector" on page 19, the Target Activation Detector may also be used to detect the moment when initiator turns off its RF field. In case the delay time, after which the initiator turns off its field after sending its request, is known, this feature is not needed and the Target Activation Detector can be turned off by setting bit *nfc_t* low after presence of the initiator field is detected.

Next the direct command *Unmask Receive Data* has to be send to put the Receiver and control logic in the receive mode. The AS3909/10 is now ready to receive request from the initiator. Procedure during the reception is the same as in case of the ISO-14443 mode.

The target response is done in the same way as in case of the ISO-14443 transmission, only that the command which actually starts the transmission is either NFC transmit with Response RF Collision Avoidance or NFC transmit with Response RF Collision Avoidance with n=0. These two commands perform the RF Collision avoidance procedure before actually starting the transmission. In case an external RF field is detected during the RF Collision avoidance procedure an interrupt is sent (INTR due to nfc event) and the transmission is not performed.

Next the AS3909/10 expects a new request from the initiator. In case the Target Activation Detector is still enabled an interrupt will be generated when the initiator switch on its field. This is additional information for the external controller, but it is not required by the receiver. The receiver is already running, reception will be done automatically and an interrupt will be sent when reception will be completed (or when the FIFO water level will be reached in case of a long request).

NFCIP Initiator

In case the AS3909/10 is an NFCIP initiator, the microcontroller activates the oscillator and receiver and prepares everything for transmitting as in case of the ISO-14443 transmission. The transmission is actually executed by direct command *NFC Transmit with Initial RF Collision Avoidance*.

Following events are the same as described in previous chapter only that roles of the initiator and target are interchanged.

The Target Activation Detector may also be used in case of the NFCIP initiator operation to detect the moment when the target RF field turns on and off.

ISO-14443A SELECT SEQUENCE

In the 14443A select sequence the commands REQA (also WUPA), ANTICOLLISION and SELECT are used. For the commands REQA and WUPA the short frame is used, for ANTICOLLISION the bit oriented anticollision frame is used, for SELECT the standard frame is used. Transponder replies to commands REQA, WUPA and ANTICOLLISION do not contain the CRC so the configuration bit *crc_rx* of the *Configuration Register 3* (address 03) has to be set to 1 (receive without CRC) before these commands are sent.

REQA and WUPA

Sending of these two commands is simple since they are implemented as the AS3909/10 direct commands (*Transmit REQA* and *Transmit WUPA*). Procedure is the following (note that since the ATQA response does not contain a CRC the configuration bit *crc_rx* of the *Configuration Register 3* (address #03) has to be set to 1 before this procedure is started):

1. Send the direct command *Transmit REQA* (or *Transmit WUPA*)
2. When all the data is transmitted an interrupt is sent to inform the microcontroller that transmission is finished (INTR due to end of transmission)
3. When reception of the ATQA is finished and all data is in the FIFO an interrupt is sent to the microcontroller (INTR due to end of receive), additionally the *FIFO Status Register* displays number of bytes (2 bytes in case of ATQA) in the FIFO so the microcontroller can proceeded with downloading data from the FIFO.

Sending the direct command *Clear* before sending *Transmit REQA* and *Transmit WUPA* is not necessary.

ANTICOLLISION

In this command, the bit oriented anticollision frame is used. There is no CRC, neither in the command send from PCD to PICC (part 1 of the bit oriented anticollision frame), nor in the reply sent from PICC to PCD (part 2 of the bit oriented anticollision frame). Due to this configuration the bit *crc_rx* of the *Configuration Register 3* (address #03) has to be set to 1 before.

Sequence in case full bytes are transmitted (no collision during the transponder response):

1. Send the direct command *Clear*
2. Define the number of transmitted bytes for part1 of the bit oriented anticollision frame in the registers #0B and #0C. Bit 0 (antcl) of register #0B has to be additionally set to 1 to indicate that anticollision frame is sent.
3. Write the bytes to be transmitted in the FIFO
4. Send the direct command *Transmit without CRC*

5. When all the data is transmitted an interrupt is sent to inform the microcontroller that transmission is finished (INTR due to end of transmission)
6. When the reception of part2 of the bit oriented anticollision frame is finished and there was no collision detected, data is put in the FIFO and an interrupt is sent to microcontroller (INTR due to end of receive), additionally the *FIFO Status Register* displays the number of bytes in the FIFO, so the microcontroller can proceeded with downloading data from the FIFO.

Sequence in case of a split byte (no collision during transponder response):

1. Send the direct command *Clear*
2. Define the number of full bytes and the number of bits in the split byte to be transmitted in the registers #0B and #0C (bits *ntx* define the number of full bytes, bits *nbtx* in register #0B define the number of bits in the split byte). Bit 0 (antcl) of register #0B has to be additionally set to 1 to indicate that anticollision frame is sent.
3. Write the bytes to be transmitted in FIFO. Since the SPI communication is byte oriented 8 bits have to transferred also for split byte (sent last), the MSB bits of split byte which are not transmitted are don't care.
4. Send the direct command *Transmit Without CRC*
5. When all the data is transmitted an interrupt is sent to inform the microcontroller that the transmission is finished (INTR due to end of transmission)
6. When the reception of part2 of the bit oriented anticollision frame is finished and there was no collision detected, data is put in the FIFO and an interrupt is sent to the microcontroller (INTR due to end of receive), additionally the *FIFO Status Register* displays the number of bytes in the FIFO so the microcontroller can proceeded with downloading data from the FIFO. First downloaded byte contains second part of the split byte, so only the MSB part of byte which was not sent during transmit is valid.

Collision Detection

The AS3909/10 Framing block is able to detect the bit collision in case of presence of more ISO-14443A transponders. This feature is very useful during the select sequence. The collision is detected during the ANTICOLLISION command (different transponders have different UIDs); it may already be detected in the ATQA (answer to REQA or WUPA). When the bit collision is detected an interrupt is sent (INTR due to collision) and the bit at which collision occurred is indicated in the *Collision Register* (#0A). In case of anticollision frame (indicated to the AS3909/10 by bit 0 of register #0B) the bit collision position displayed in *Collision Register* is counted from beginning of anticollision frame (including the part which is transmitted).

Please note that after getting an interrupt due to a collision, the reader has to wait for the transponders to finish sending their messages before sending a new command. The end of transponder message is indicated by the End of Receive interrupt. It may also happen that the interrupt due to collision and due to end of receive are read at the same time (in case reaction to the first interrupt is slow and collision happens at the end of transponder message). *Collision Register* (#0A) can be read after receiving collision interrupt while the FIFO can only be read after receiving the End of Receive interrupt.

There is also a slight possibility that the end of message flag is just written to the *Interrupt Register* while it is being erased at the end of the *Interrupt Register* read due to the collision interrupt. In such a case there is no end of receive interrupt. In case it is not clear whether the receive logic is still processing response the Active Receive bit (*rx_act*) in *FIFO Status Register* can be consulted (See "ISO-14443B, Reduction of TR0 and TR1 and Suppression of EOF/SOF in PICC Response" on page 67 for details about Active Receive bit).

SELECT

The SELECT command uses standard frame, response to the SELECT command (SAK) contains also a CRC, so before sending this command the configuration bit *crc_rx* of *Configuration Register 3* has to be reset back to 0. Since the SELECT command contains CRC the direct command *Transmit with CRC* can be used.

Receiving 4-Bit Tag Response Frame

Mifare Ultralight tag uses 4 bit response frame to indicate ACK and NACK. The AS3909/10 framing expects that response frame is composed of bytes (except in case of anticollision frame) and it rejects a 4 bit response frame as an error (error due to receive data coding). By setting the bit 1 (frm4l) of register #0B, a 4 bit response frame is correctly processed and put in FIFO (MSB bits of first byte). In case of setting this bit a standard frame response is not processed correctly.

Response to Mifare Ultralight WRITE command is either ACK or NACK. So in case of this command bit frm4 has to be set to distinguish between the two possible 4 bit responses.

Response to READ command is either a standard frame, in case command is correctly processed, or a NACK, in case of an error. In this case the bit frm4 can not be used, interrupt due to receive data coding error should be interpreted as a NACK.

AM Modulation Depth: Definition and Calibration

The AM modulation of the transmitted carrier is used for communication reader to transponder in two configuration cases:

- The ISO-14443B mode is configured in the *ISO Mode Definition Register* (#01)
- The Transparent mode with AM modulation [direct command Transparent Mode, the bit 6(am) of the *Configuration Register 5* (#05) is set to 1]

In other cases the OOK modulation is used.

The AM modulation depth can be automatically adjusted by setting the *Modulation Depth Definition Register* (#10) and sending the direct command *Calibrate Modulation Depth*. This procedure is patent pending. There is also an alternative possibility where the command *Calibrate Modulation Depth* is not used and the modulated level is defined by writing the Antenna driver *AM Modulated Level Definition Register* (#12).

AM Modulation Depth Definition Using Direct Command Calibrate Modulation Depth

Before sending the direct command *Calibrate Modulation Depth* the *Modulation Depth Definition Register* (#10) has to be configured in the following way:

- The bit 7 (*am_s*) has to be set to 0 to chose definition by the command *Calibrate Modulation Depth*.
- The bits 6 to 1 (*mod5* to *mod0*) define target AM modulation depth.

Definition of Modulation Depth Using Bits *mod5* to *mod0*

The RFID standard documents usually define the AM modulation level in form of the modulation index. The modulation index is defined by formula (a-b)/(a+b) where 'a' is amplitude of the non-modulated carrier and 'b' is the amplitude of the modulated carrier.

The modulation index specification is different for different standards. The ISO-14443B modulation index is typically 10% with allowed range from 8% to 14%, range from 10 to 30% is defined in the ISO-15693 and 8% to 30% in the Felica™.

The bits *mod5* to *mod0* are used to calculate the amplitude of the modulated level. The non-modulated level which was before measured by the A/D converter and stored in an 8 bit register is divided by a binary number in range from 1 to 1.98. The bits *mod5* to *mod0* define binary decimals of this number.

Example: In case of the modulation index 10% the modulated level amplitude is 1.2222 times lower than the non-modulated level. 1.2222 converted to binary and truncated to 6 decimals is 1.001110. So in order to define the modulation index 10% the bits *mod5* to *mod0* have to be set to 001110.

The figure below depicts setting of the mod bits for some often used modulation indexes.

Figure 50:
Setting mod bits for Modulation Indexes

modulation index [%]	a/b [dec]	a/b [bin]	mod5……mod0
8	1,1739	1,001011	001011
10	1,2222	1,001110	001110
14	1,3256	1,010100	010100
20	1,5000	1,100000	100000
30	1,8571	1,110111	110111
33	1,9843	1,111111	111111

Execution of Direct Command Calibrate Modulation Depth

The modulation level is adjusted by increasing the RFO1 and RFO2 driver output resistance. The RFO drivers are composed of 8 binary weighted segments. Usually all these segments are turned on to define the normal, non-modulated level, there is also a possibility to increase the output resistance of the non-modulated state by writing the Antenna driver *non-modulated level definition register* (#13).

Before sending the direct command *Calibrate Modulation Depth* the oscillator and regulators have to be turned on. When the direct command *Calibrate Modulation Depth* is sent the following procedure is executed:

1. The Transmitter is turned on, non-modulated level is established
2. The amplitude of the non-modulated carrier level established on the inputs RFI1 and RFI2 is measured by the A/D converter and stored in the *A/D Converter Output Register*
3. Based on the measurement of the non-modulated level and the target modulated level defined by the bits *mod5* to *mod0* the target modulated level is calculated
4. The output driver control is taken over by the eight bit Calibrate Register with initial level defined in the *Antenna Driver Non-Modulated Level Definition Register* (#13). Content of the Calibrate Register is incremented by 1 to increase the driver resistance, the reduced amplitude is measured by the A/D converter and the result is compared to the target modulation level.
5. The procedure from previous point is repeated as long as the measured level is greater than target level.

6. When the measured level is equal or lower than the target level, actual state of the Calibrate Register is copied in the *Modulation Depth Display Register* (#11). Content of this register is used to define the AM modulated level.

Note(s): After this calibration procedure is finished, the content of *Antenna driver non-modulated level definition register* (#13) should not be changed. Modification of this register content will change the non-modulated amplitude and therefore the ration be-tween the modulated and non-modulated level will be changed.
Please also note that in case the Calibration of antenna resonant frequency in implemented command *Calibrate Antenna* has to be run before AM modulation depth adjustment.

AM Modulation Depth Definition Using Antenna Driver AM Modulated Level Definition Register (#12)

When the bit 7 (*am_s*) of the *Modulation Depth Definition Register* (#10) is set to 1 the AM modulated level is controlled by writing the Antenna Driver *AM Modulated Level Definition Register* (#12). In case setting of the modulated level is already known it is not necessary to run the calibration procedure, the modulated level can simply be defined by writing this register.

There is also a possibility to run a calibration procedure from externally using the *Antenna driver non-modulated level definition register* (#13) and the direct command *Measure RF*.

The procedure is the following:

1. Write the non-modulated level in register #13 (usually it is all 0 to have the lower possible output resistance)
2. Switch on the transmitter
3. After the settling time (10µs should be enough), send the direct command Measure RF. Read result from the *A/D Converter Output Register* (#0E)
4. Calculate the target modulated level from the target modulation index and result from the previous point
5. In the following iterations content of the register #13 is modified, the command *Measure RF* performed and result compared to the target modulated level as long as the result is not equal or close enough to the target modulated level.
6. At the end the content of the register #13 which results in the target modulated level is written in the *Antenna Driver AM Modulated Level Definition Register* (#12) while the register #13 is restored with the non-modulated level definition value.

Antenna LC Tank Resonance: Checking and Calibration

The AS3909/10 comprises the building blocks which make possible checking and adjustment of the antenna LC tank resonance frequency. The arrangement of these building blocks and associated adjustment procedure are patent pending.

The key block in the resonance frequency checking and adjustment is the Phase Detector (see "Phase Detector" on page 18). The Phase Detector is measuring the phase shift between the Transmitter output signals (RFO1 and RFO2) and the inputs RFI1 and RFI2, which are proportional to voltage on the antenna LC tank. In case of perfect tuning there is a 90° phase shift between them.

Check Antenna Resonance

In case of the perfect 90° phase shift mentioned above, the Phase Detector output results in VSP/2 output voltage. A phase shift of 1% of the carrier frequency period (3.6°) results in the output voltage change of 2% of VSP (1% phase shift results in 60mV change at VSP=3V).

During execution of the direct command *Check Antenna Resonance* the Phase Detector output is multiplexed on the input of A/ D converter which is set in relative mode. 1 LSB of the A/D conversion output represents 0.13% of carrier frequency period (0.468°). The result of A/D conversion is in case of the perfect tuning exactly in the middle of range (1000 0000 or 0111 1111).

Value higher than 1000 0000 means that phase detector output voltage is higher than VSP/2, which corresponds to case with resonance frequency higher than target 13.56 MHz. In the opposite case, when the resonance frequency is lower than target, the result of A/D conversion is lower than 0111 1111.

Execution of the command *Check Antenna Resonance* is fast and it can be used frequently to check whether system settings are correct.

Calibrate Antenna Resonance[3]

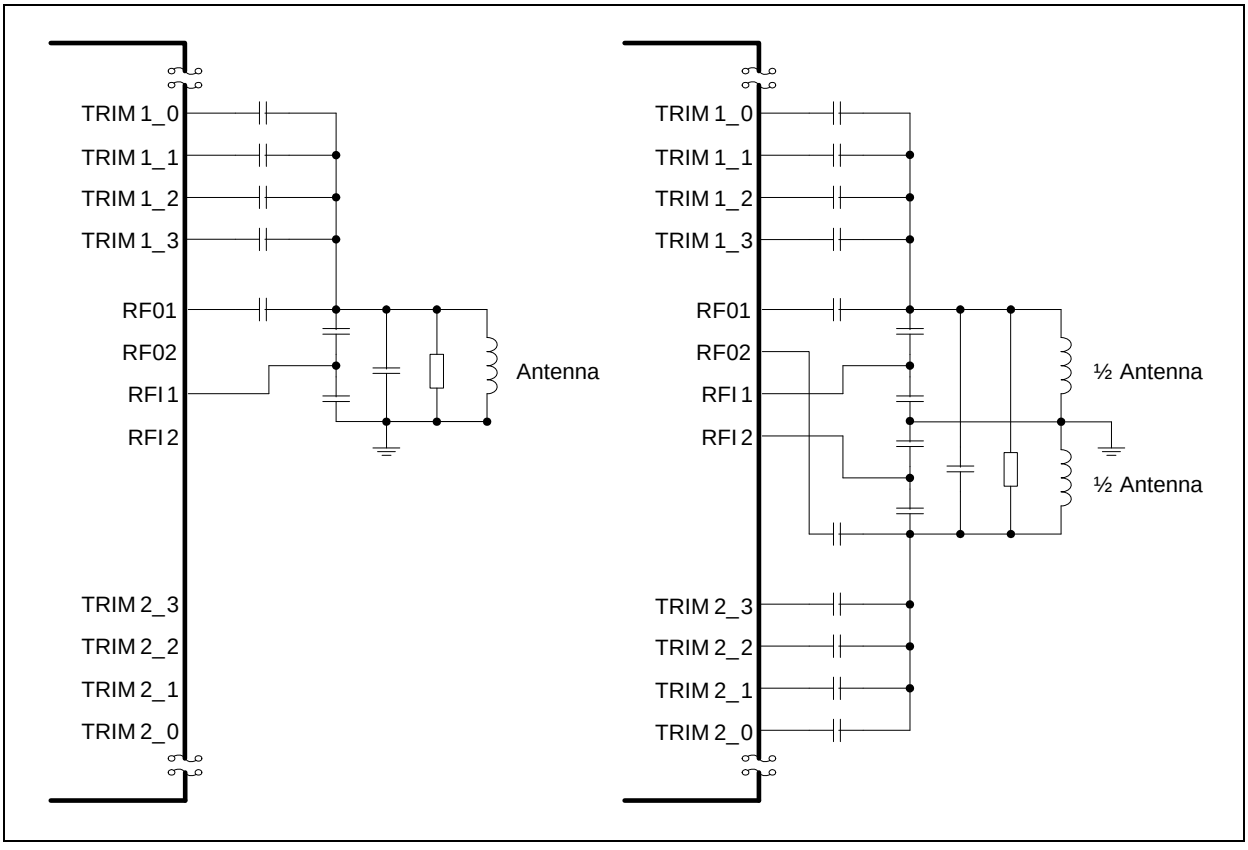
In order to implement the antenna LC tank calibration binary weighted trimming capacitors have to be connected between the two coil terminals to the pads TRIM1_3 to TRIM1_0 and TRIM2_3 to TRIM2_0. In case single driver is used only the pads TRIM1_3 to TRIM1_0 are used, pads TRIM2_3 to TRIM2_0 are left open.

Figure 51 depicts connection of the trim capacitors for both, single and differential driving. The TRIM pads contain the HVNMOS switch transistors to VSS. During trimming procedure the resonance frequency is adjusted by connecting some of the trimming capacitors to VSS and leaving others floating.

The switches of the same binary weight are driven from the same source and are both on or off (the switches TRIM1_2 and TRIM2_2 are for example both either on of off).

The breakdown voltage of the HVNMNOS switch transistors is 30V, which limits the maximum peak to peak voltage on LC tank in case trimming is used. The on resistance of TRIM1_0 and TRIM2_0 switch transistors which are meant to be connected to LSB trimming capacitor is typ 50Ω at 3V VSP, the on resistance of other pads is binary weighted (the on resistance of TRIM1_3 and TRIM2_3 is 6.25Ω).

Figure 51:
Connection of Trimming Capacitors to the Antenna LC Tank in case of Single (left) and Differential Driving (right)



3. Only available in AS3910.

Antenna Calibration Using Command Calibrate Antenna

The calibration of LC tank resonance frequency is automatically done by running the direct command *Calibrate Antenna*. During execution of this command the comparator at the output of Phase Detector is used. In case the LC tank resonance frequency is higher than the target 13.56MHz, the Phase Detector output gets higher than VSP/2 and the comparator output is high. In the opposite case, when the resonance frequency is lower, the Phase Detector output gets lower than VSP/2 and the comparator output is low.

At the beginning of the command *Calibrate Antenna* execution the switches in all TRIM pads are turned off. As consequence all the trimming capacitors are disconnected so in case the LC tank dimensioning is correct the resonance frequency has to be higher than the target and the comparator output has to be high. In case the comparator output is low at this initial state the resonance frequency is too low even when all the trimming capacitor are disconnected and adjusting of the resonance frequency is not possible. An error flag is set and execution of the command is terminated.

In case the comparator output was high at the initial state, the LSB switches (TRIM1_0 and TRIM2_0) are switched on and after 10µs state of the comparator output is checked again. This procedure is repeated until the comparator output transitions to low or until the final state with all switches turned on is reached. The switch state at which the comparator output is transitional is the one at which the LC tank is in resonance.

In case the state with all switched turned on was reached and the comparator output is still high, the resonance frequency is too high even when all the capacitors are connected and the adjusting is not possible. The error flag is set.

The result of the direct command *Calibrate Antenna* can be observed by reading the *Antenna Calibration Register* (#0E). This register displays the state of four bits representing state of the switches when resonance was reached and the error flag.

After the execution of direct command *Calibrate Antenna* the resonance can be checked by running the direct command *Check Antenna Resonance*.

Antenna Calibration Using External Trim Register

There is also a possibility to control the position of the TRIM switches by writing the *External Trim Register* (#0F). When the bit *trim_s* of this register is set to 1 position of the trim switches is controlled by bits *tre_3* to *tre_0*. Using this register and the direct command *Check Antenna Resonance* a trimming procedure may be implemented from externally.

Another possibility of external trimming procedure is using this register and the direct command *Measure RF*. In this case the resonance is adjusted by looking for operating point with the maximum amplitude.

Transparent Mode

The AS3909/10 framing supports the ISO-14443 standard. Other standard and custom 13.56MHz RFID reader protocols can be realized using the AS3909/10 AFE and framing implemented in the external microcontroller.

After sending the direct command Transparent Mode the external microcontroller directly controls the transmission modulator and gets the

Receiver output (control logic becomes “transparent”).

The Transparent Mode is entered on falling edge of signal SEN after sending the command Transparent Mode and is maintained as long as the signal SEN is kept low. Before sending the direct command Transparent Mode the Transmitter and Receiver have to be turned on, the AFE have to be configured properly.

While the AS3909/10 is in the Transparent Mode the AFE is controlled directly through SPI interface:

- The Transmitter modulation is controlled by pin SDATAI (high is modulator on)
- Signal *rx_on* is controlled by pin SCLK (high enables RSSI and AGC)
- The Receiver output is sent to pin SDATAO

By controlling the *rx_on* advanced Receiver features like the RSSI and AGC can be used.

Configuration bits related to the ISO mode, framing and FIFO are of course meaningless in Transparent Mode, all other configuration bits are respected.

For communication reader to transponder the OOK and AM modulation are supported. Type of the modulation is defined by writing the bit 6 (*am*) of the *Configuration Register 5* (#05). The direct command *Calibrate Modulation Depth* supports modulation depths up to 30%, by writing the *AM Modulated Level Definition Register* (#12) also definition of deeper am modulation is possible.

The Receiver filters support the subcarrier frequencies from 212 kHz to 848 kHz. The filter characteristics are defined by writing the bits fs2 to fs0 in the *Receiver Configuration Register* (#6).

Active Receive – Use in ISO-14443B Anticollision

Usually the microcontroller does not need information about beginning of the transponder message, it gets an interrupt once reception is finished or earlier in case the transponder message is longer than the FIFO.

In some cases the information about the fact that the receiver is already processing a message from the transponder is useful. The bit *rx_act* in the *FIFO Status Register* (address 09) provides this information. This bit is set to 1 when start of the transponder message is detected and stays high until the end of reception.

This information can be used to speed up the ISO-14443B anticollision procedure when more slots are used. In case there is no message in a certain slot the reader does not have to wait the time message ATQB takes before sending the next Slot-MARKER command, it can send it as soon as it is clear that there is no answer in that particular slot. The microcontroller can obtain this info by reading the *rx_act* flag at the time the receiver should already be processing the ATQB message. In case *rx_act* flag is set to one the receiver is processing a message and the microcontroller has to wait for the end of receive interrupt, in opposite case when the *rx_act* flag is set to zero there is no ATQB message in that particular slot and the next Slot-MARKER command can be sent immediately.

ISO-14443B, Reduction of TR0 and TR1 and Suppression of EOF/SOF in PICC Response

The ISO-14443-3 standard, chapter 7.10.3 Coding of Param 1 defines possibility to reduce the TR0 and TR1 and suppress the EOF/SOF in PICC response.

Note(s): The AS3909/10 Receiver and Framing blocks do not support the reduction of TR0 and TR1 and suppression of EOF/SOF. In case default settings of these parameters are changed, the framing block will not be able to decode the PICC response.

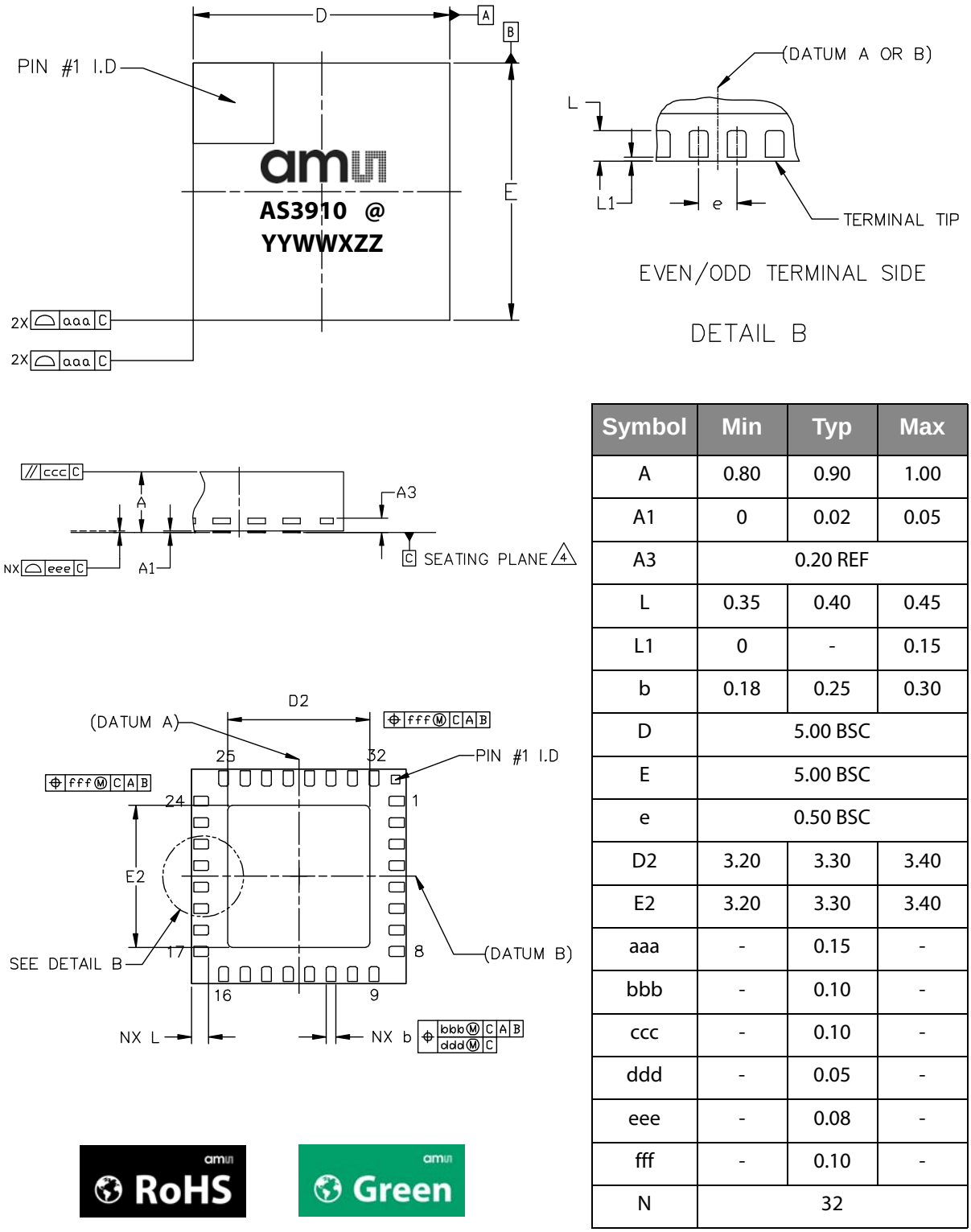
Test Pins

Pins TEST and TIO are used to test the AS3909/10. Pin TEST is a digital pin with pull down, it is used to enter the test mode, pin TIO is used in test mode as a digital IO, in normal mode it is in tristate. It is recommended to connect pin TEST to VSS and to leave pin TIO open.

Package Drawings & Markings

These devices are available in a 32-pin QFN (5x5mm) & 32-pin TQFN (5x5mm) packages.

Figure 52:
Package Drawings for AS3910 (QFN)



Symbol	Min	Typ	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
L	0.35	0.40	0.45
L1	0	-	0.15
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
D2	3.20	3.30	3.40
E2	3.20	3.30	3.40
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		32	

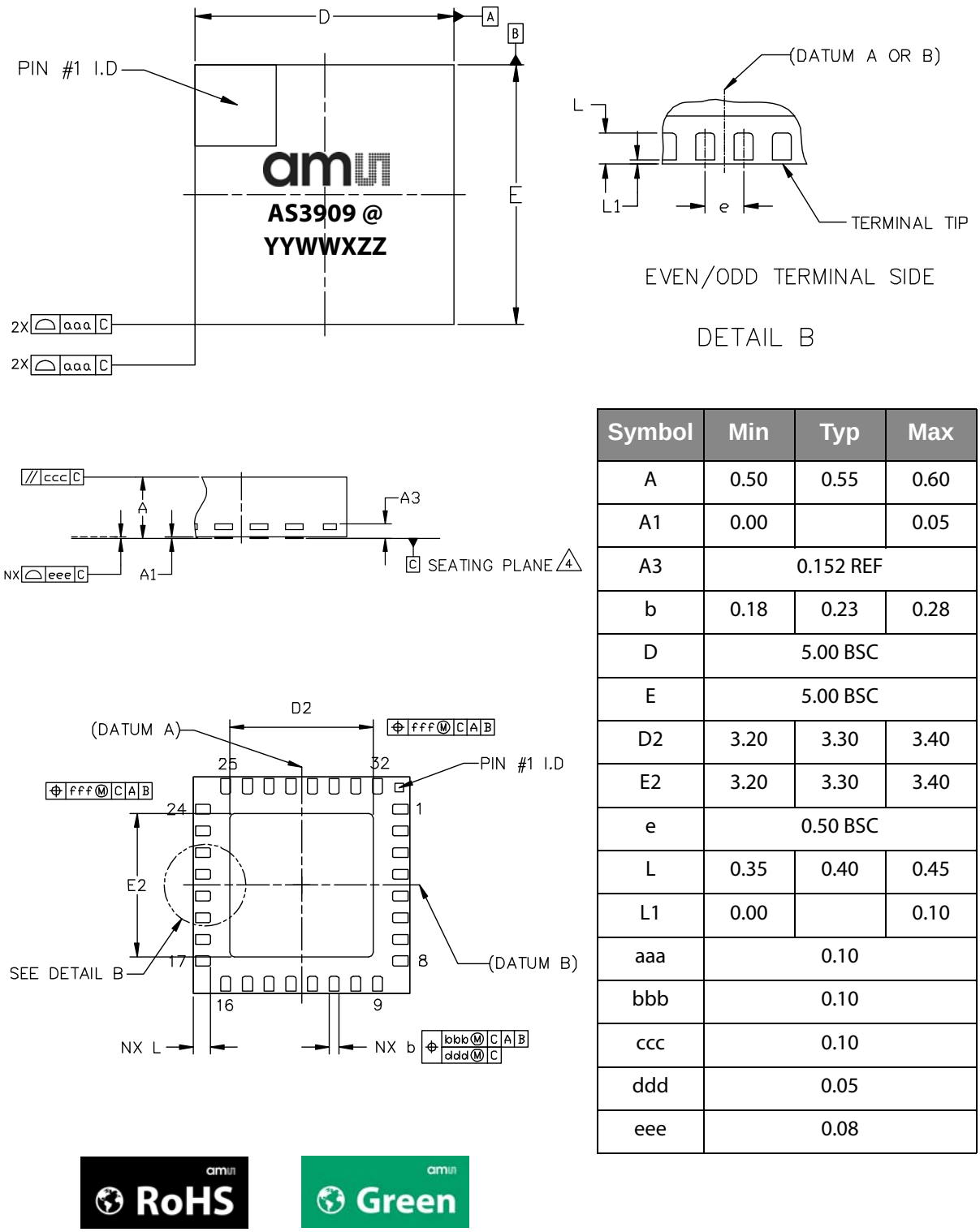
Note(s) and/or Footnote(s):

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters, angle are in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25 and 0.30mm from terminal tip.
4. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.
5. Coplanarity applies to the exposed heat slug as well as the terminal.
6. Radius on terminal is optional.
7. N is the total number of terminals.

Figure 53:
Marking YYWWXZZ

YY	WW	X	ZZ	@
Pb-free; Year	Manufacturing week	Plant Identifier	Traceability code	Sublot Identifier

Figure 54:
Package Drawings for AS3909 (TQFN)



Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00		0.05
A3		0.152 REF	
b	0.18	0.23	0.28
D		5.00 BSC	
E		5.00 BSC	
D2	3.20	3.30	3.40
E2	3.20	3.30	3.40
e		0.50 BSC	
L	0.35	0.40	0.45
L1	0.00		0.10
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Note(s) and/or Footnote(s):

1. Dimensioning & toleranceing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. angles are in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip.
4. Dimension L1 represents terminal full back from package edge up to 0.1mm is acceptable.
5. Coplanarity applies to the exposed heat slug as well as the terminal.

Figure 55:
Marking YYWWXZZ

YY	WW	X	ZZ	@
Pb-free; Year	Manufacturing week	Plant Identifier	Traceability code	Sublot Identifier

RoHS Compliant & ams Green Statement

RoHS: The term RoHS compliant means that ams products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

Important Information: The information provided in this statement represents ams knowledge and belief as of the date that it is provided. ams bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ams has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams and ams suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Ordering & Contact Information

The devices are available as the standard products shown in Figure 56.

Figure 56:
Ordering Information

Ordering Code	Description	Delivery Form	Package
AS3909-BQTT	HF RFID Reader IC	Tape & Reel	32-pin TQFN (5x5mm)
AS3910-BQFT	HF RFID Reader IC	Tape & Reel	32-pin QFN (5x5mm)

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For further information and requests, e-mail us at:
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www.ams.com/contact

Headquarters
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten
Austria, Europe

Tel: +43 (0) 3136 500 0

Website: www.ams.com

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Reference Guide