Application manual

Real Time Clock Module

RX4111CE

Product name	Product number
RX4111CE A	X1B000431000115
RX4111CE B	X1B000431000215

ETM62E Revision History

Rev. No.	Date	Page	Description
01	19.Feb.2020		Release
		8	Note is added the Metal pad of package. 5.1. External Dimensions
02	30.Sep.2021	9	V_{VLF} characteristics was added. "7. Recommended Operating Conditions"
		12	AC characteristics of V_{DD}=1.8V was updated. Note and comment was updated for SPI control. "9.2. AC characteristics"
		27	As for time of auto release of timer interruption, Symbol name was updated to tRTN2 from tRTN. "TSEL1, TSEL0 bit" tiThe symbol of tRTN was separated to tRTN1 and tRTN2.
		35	As for time of auto release of Time update interruption, Symbol name was updated to tRTN1 from tRTN. The symbol of tRTN was separated to tRTN1 and tRTN2. Auto release time of Time update interruption was corrected. 7.324ms to 7.644ms, from 7.57 ms. "14.4. Time Update Interrupt Function" "Table 37 UIE bit (Update Interrupt Enable)"
		36	"Figure 1 Time Update Interruption Timing Chart" has been revised. When UF is cleared, /INT returns to Hi-Z, Immediately.
		42	"Note in using small EDLC " is deleted. Even if using small EDLC, This note desn't need. Page42
		57	Bypass capacitor value was corrected. 0.1μF from 1.0μF. " 15.Connection example"
		60	Contacts list was updated. "Contacts"
		All	The link to index was added to the all footer.

INDEX

Low Power Real Time Clock Module with SPI-Bus Interface and Time Stamp Function

RX4111CE

- Built-in frequency adjusted 32.768 kHz crystal unit
- Interface Type : SPI-Bus 4 wire, 4 MHz Max.
- Low current consumption at backup: 100 nA Typ. / 3.0 V
- Wide operating voltage range : 1.6 V to 5.5 V
- Wide time-keeper voltage range : 1.1 V to 5.5 V
- Auto power switching function : Automatically switches to backup power supply by monitoring the V_{DD} voltage.
- Time stamp function : 8 times time-stamp,1/256 seconds with many selectable trigger.
- Time stamp memory can be used as users memory; 512 bit, 64 word x 8 bit
- Alarm interruption : Day, date, hour, minute, second
- The various functions include full calendar, seconds alarm, wake-up timer, and 32.768 kHz output
- Self monitoring function : Voltage detection, Crystal oscillation stop, etc.

1. Overview

RX4111CE is a real-time clock module with integrated 32.768 kHz crystal oscillator and SPI-Bus interface. In addition to providing a calendar (year, month, date, day, hour, minute, second), this module provides other functions including time-stamp from 1/1024 second to year, alarm, wake-up timer, time update interruption, and 32.768 kHz output. Time stamp function can record maximum of 8 events. Using the backup battery switch control function and the interface power supply input pin, RX4111CE can support various power supply circuits. All of the functions mentioned above are offered in a thin and compact 3.2 x 2.5 ceramic package which could be used in various applications requiring small footprints.

2. Block Diagram

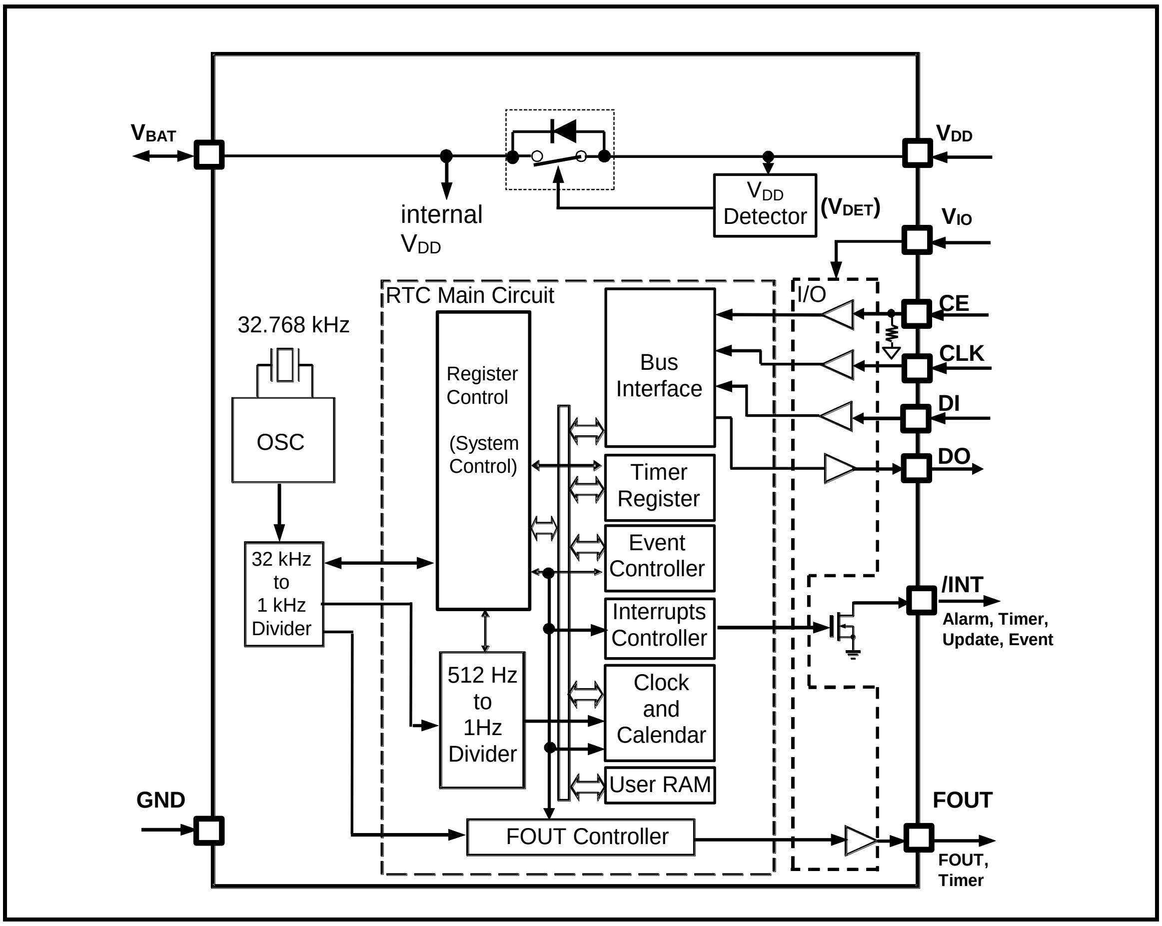


Figure 2 Block Diagram

3. Terminal Description

3.1. Terminal Connections

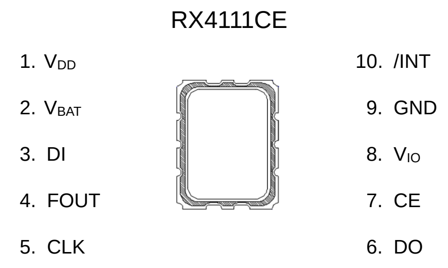


Figure 3 Package Pin Layout

3.2. Pin Functions

Table 1 Pin Description

Signal name	I/O	Function
CE	Input	Chip enables input pin (SS) Should be held high to allow access to the CPU. Incorporates a pull-down resistor
CLK	Input	Serial clock input pin (SCLK)
DI	Input	Data input pin (MOSI)
DO	Output	Data output pin (MISO)
FOUT	Output	Frequency output pin (CMOS) (frequency selection: 32.768 kHz, 1024 Hz, 1 Hz) When output is stopped, the FOUT pin is High impedance.
/INT	Open-Drain Output	This pin is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an N-ch open drain
V_{DD}	–	Power-supply pin Possible to supply different voltage from V_{IO}
V_{IO}	–	Interface power supply pin Input to supply the voltage same as a host
V_{BAT}	–	This is a power supply pin for backup battery Connect an EDLC, a secondary battery, a primary battery In the backup voltage range, supplied to IC, from this pin
GND	–	Ground pin

Note:
Be sure to connect a bypass capacitor rated at least 0.1 μF between V_{DD} and GND.
For the input terminals, it is permitted for the input to be 5.5 V regardless of the V_{IO} voltage.
For the Open-Drain pin, it is permitted for the pull-up to be 5.5 V regardless of the V_{IO} voltage.
When FOUT or INT is not used, be left open in these pins. It doesn't need pull-Up/Down resistor.

4. Connection Example

4.1. Battery Switchover Connection Examples

Note. When connecting an outside power supply or a large-sized battery to V_{BAT},
Install bypass capacitors more than 0.1 µF in a V_{BAT} terminal if necessary.
As for each of bypass-capacitor, Install nearest in each of pin as much as possible.

EX.1 V_{IO} and V_{DD} are different.

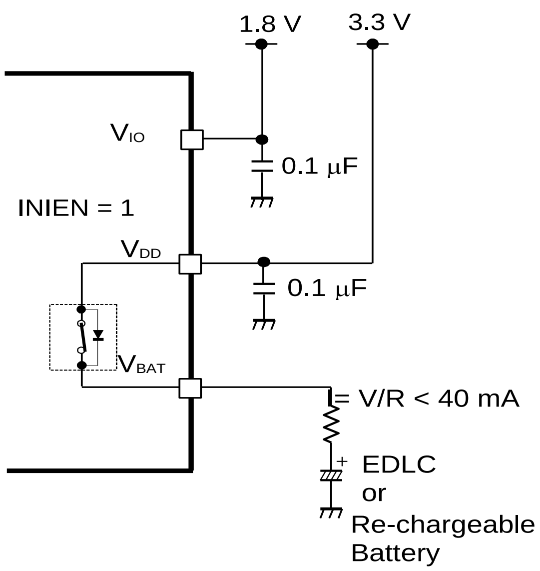


Figure 4 Circuit Ex.1

Ex.2 V_{IO} and V_{DD} are the same.

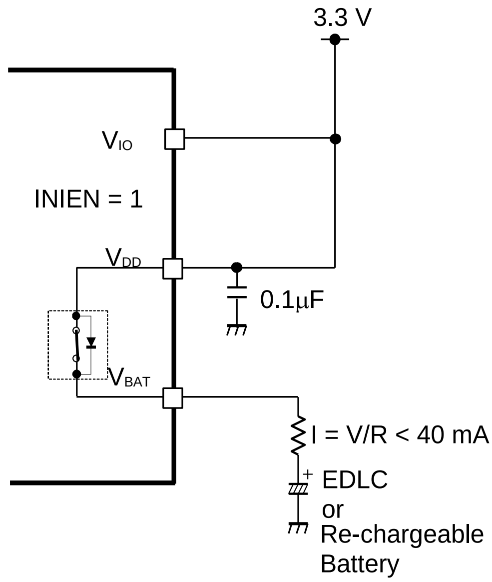


Figure 5 Circuit Ex.2

Ex.3 Connecting a Non RE-Chargeable battery

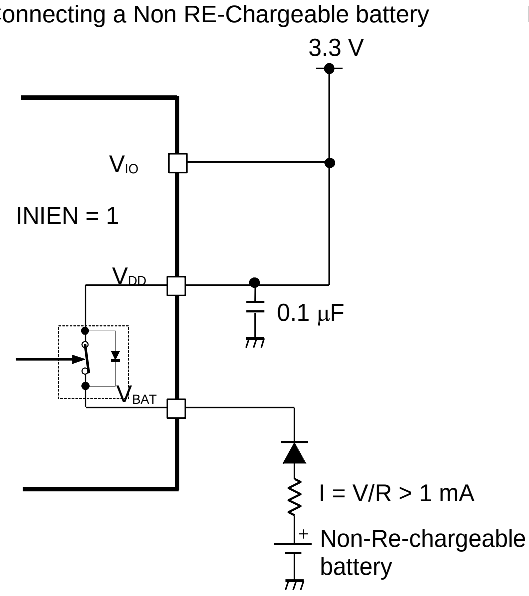


Figure 6 Circuit Ex.3

Ex.4 Not using power-switch function

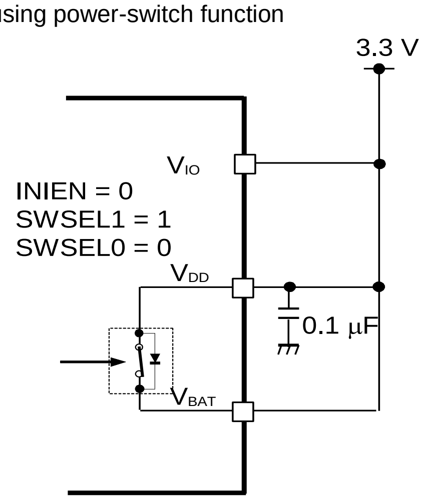


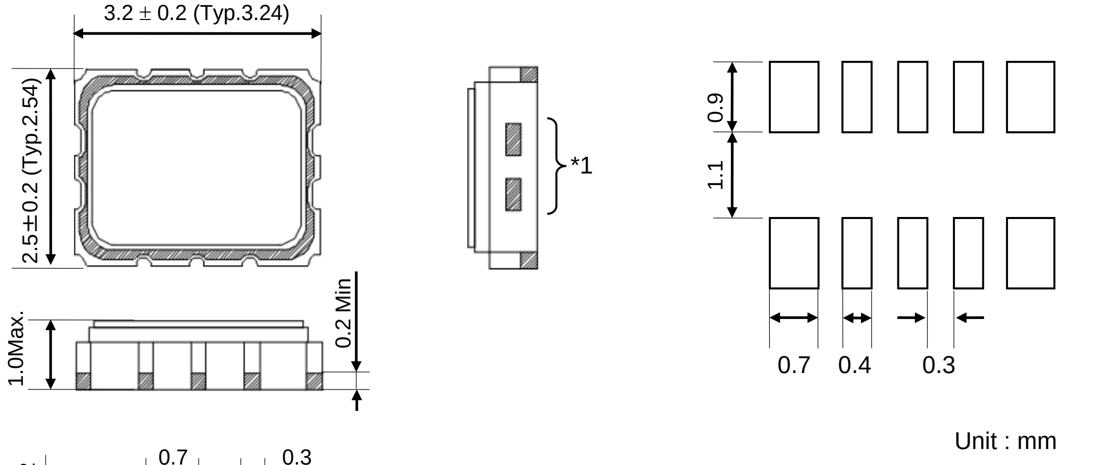
Figure 7 Circuit EX.4

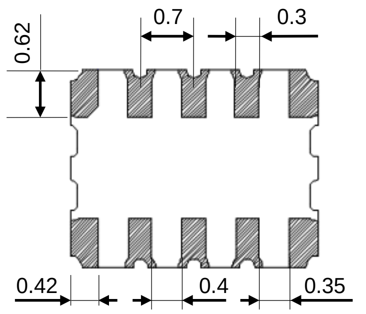
5. External Dimensions / Marking Layout

5.1. External Dimensions

RX4111CE

- External Dimensions
- Recommended soldering pattern



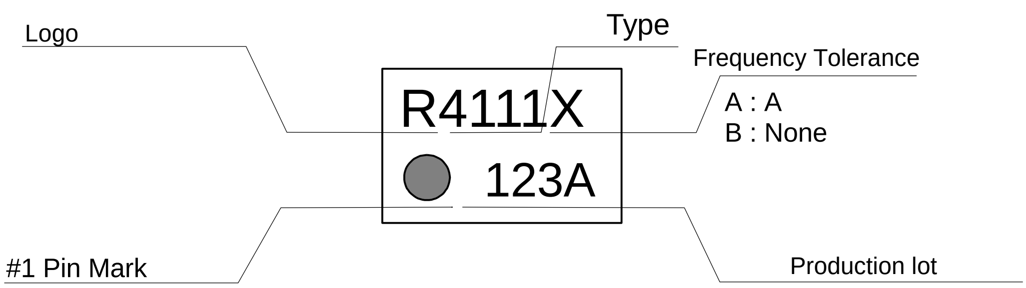


∗1. The metal pads on the short side of the 1st and 10th pins of the package are inspection pads for the crystal unit.
For stable oscillation, make sure that leakage current due to condensation or dust does not occur between these pads.
The metal pads on the short side of the 5-pin and 6-pin sides are not connected inside the RTC.

Figure 8 External dimensions

5.2. Marking Layout

RX4111CE



Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

Figure 9 Marking layout

6. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	–	–0.3 ~ +6.5	V
Backup supply voltage	V_{BAT}	–	–0.3 ~ +6.5	V
Interface supply voltage	V_{IO}	–	–0.3 ~ +6.5	V
Input voltage	V_{IN}	CE, CLK, DI	–0.3 ~ +6.5	V
Output voltage 1	V_{OUT1}	/INT	–0.3 ~ +6.5	V
Output voltage 2	V_{OUT2}	FOUT, DO	-0.3 ~ VIO+0.3	V
Storage temperature	TSTG	When stored separately, without packaging	–55 to +125	°C

7. Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Unless otherwise specified, GND = 0 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	Normal operation mode (V_{DD})	1.25	3.0	5.5	V
Interface supply voltage	VIO	VDD=1.6V ~ 5.5V	1.6	3.0	5.5	V
Clock supply voltage	V_{CLK}	Backup operation mode (V_{BAT})	V_{VLF}	3.0	5.5	V
VLF detection voltage	V_{VLF}	Low voltage detection of supply Voltage.	-	-	1.1	V
Operating temperature	T_use	No condensation	–40	+25	+85	°C

Minimum value of Clock supply voltage V_{CLK} is the lower supply voltage limit till which the RTC can assure the clock to run.
For proper initialization of the RTC RX4111 it is necessary that V_{DD} voltage exceeds 1.6V at power up.

8. Frequency Characteristics

Table 4 Frequency Characteristics

Unless otherwise specified, V_{BAT} = V_{DD} = V_{IO} = 1.6V ~ 5.5 V, Ta = -40 °C ~ +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation Frequency	fo		32.768			kHz
Frequency Tolerance	Δ f / f	Ta = +25 °C V_{DD} = 3.0 V	A : ± 11.5 *1 B : ± 23.0 *2			× 10^{-6} × 10^{-6}
Frequency/voltage characteristics	f/V	Ta = +25 °C V_{DD} = 1.1 V ~ 5.5 V	–2		+2	× 10^{-6} / V
Frequency/ Temperature characteristics	fo-Tc	Ta = –20 °C ~ +70 °C V_{DD} = 3.0 V; +25 °C reference	–120		+10	× 10^{-6}
Oscillation Start-up time	tSTA	V_{DD} = 1.6 V ~ 5.5 V			1.0	s
Aging *3	fa	Ta = +25 °C, V_{DD} = 3.0 V; First year	–5		+5	× 10^{-6} / year

*1 Equivalent to ±30 seconds per month deviation.

*2 Equivalent to ±60 seconds per month deviation.

*3 Aging stability is estimated from environmental reliability tests; expected amount of the frequency variation.
This does not intend to guarantee the product-life cycle.

9. Electrical Characteristics

9.1. DC characteristics

9.1.1. DC characteristics

Table 5 DC characteristics

Unless otherwise specified, V_{BAT} = V_{DD} = V_{IO} = 1.6 V ~ 5.5 V, Ta = -40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD}	CE = Low, FOUT = OFF, /INT = OFF, V_{DD} = V_{IO} = 3.0 V INIEN = 0b		100	450	nA
Current consumption 2	I_{32k}	CE = Low FOUT = 32.768 kHz, /INT = OFF V_{DD} = V_{IO} = 3.0 V FOUT pin CL = 15 pF INIEN = 0b		2.0	3.0	µA
Current Consumption 3	I_{BAT}	CE = Low, V_{BAT} = 3.0 V, V_{DD} = V_{IO} = 0.0 V		110	450	nA
Detection voltage of V_{DD} rise up	$+V_{DET1}$	Switch voltage of V_{DD} from V_{BAT}	1.25	1.35	1.45	V
Detection voltage of V_{DD} fall down	$-V_{DET1}$	Switch voltage of V_{BAT} from V_{DD}	1.20	1.30	1.40	V
High Input voltage	V_{IH}	CE, CLK, DI	0.8 × V_{IO}		5.5	V
Low Input voltage	V_{IL}	CE, CLK, DI	GND − 0.3		0.2 × V_{IO}	V
High Output voltage	V_{OH1}	FOUT, DO: V_{IO} = 5.0 V, I_{OH} = -1 mA	4.5		5.0	V
	V_{OH2}	FOUT, DO: V_{IO} = 3.0 V, I_{OH} = -1 mA	2.2		3.0	
	V_{OH3}	FOUT, DO: V_{IO} = 3.0 V, I_{OH} =-100 µA	2.9		3.0	
Low Output voltage	V_{OL1}	FOUT, DO: V_{IO} = 5.0 V, I_{OL} =1 mA	GND		GND+0.5	V
	V_{OL2}	FOUT, DO: V_{IO} = 3.0 V, I_{OL} = 1 mA	GND		GND+0.8	
	V_{OL3}	FOUT, DO: V_{IO} = 3.0 V, I_{OL}=100 µA	GND		GND+0.1	
	V_{OL4}	/INT: V_{IO} = 5 V, I_{OL} = 1 mA	GND		GND+0.25	V
	V_{OL5}	/INT: V_{IO} = 3 V, I_{OL} = 1 mA	GND		GND+0.4	
Input leakage current	I_{LK}	Exclude CE V_{IN} = V_{IO} or GND	−0.1		0.1	µA
	I_{LKPD}	CE, V_{IN} = GND	−0.1		0.1	
Output leakage current	I_{OZ}	FOUT, DO, Output voltage = V_{IO} or GND	−0.1		0.1	µA
V_{DD} and V_{BAT} SW = OFF leak current	I_{SW}	V_{BAT} = 3.0 V、V_{DD} = 0.0 V			50	nA
V_{BAT} and V_{DD} SW = ON resistance	I_{SWON1}	V_{DD} and V_{BAT} SW = ON ΔV=+0.1 V, V_{BAT}=5.5 V , V_{DD}=5.4 V ΔV=+0.1 V, V_{BAT}=3.0 V , V_{DD}=2.9 V R_{SWON1} = 125 Ω～750 Ω	133	-	800	µA
Input Resistance	R_{DWN}	CEpin V_{IN} = V_{IO}: V_{IO} = 5 V	75	150	300	kΩ
		CEpin V_{IN} = V_{IO}: V_{IO} = 3 V	150	300	600	

9.1.2. Chargeable Current Characteristics

Chargeable current characteristics for the re-chargeable battery depends on the ON resistance of SW and blow graphs show the voltage dependence of the charge current.
25 °C condition. Horizontal Axis: Vdif (V_{DD} -V_{BAT}), Vertical Axis: Charge current (Ichg)

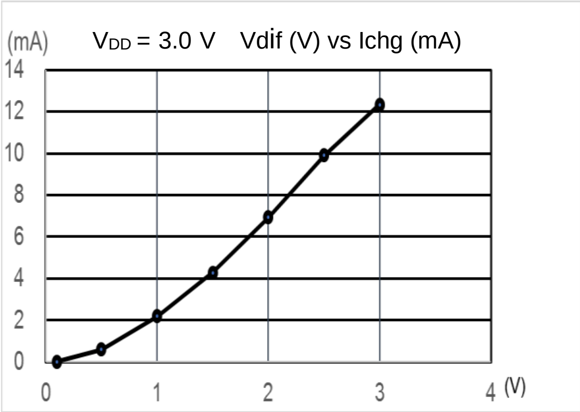


Figure 10 Chargeable current of VBAT (VDD = 3.0 V)

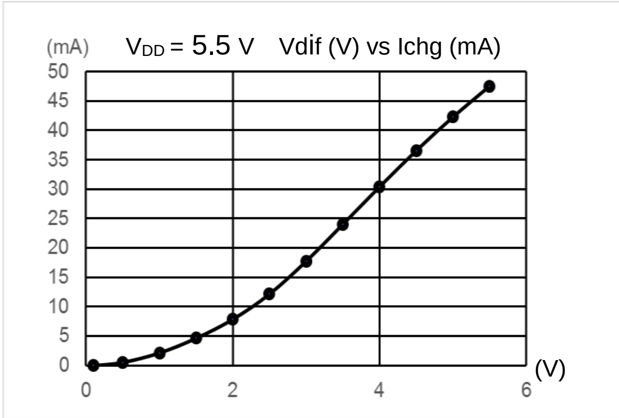


Figure 11 Chargeable Current of VBAT (VDD = 5.5V)

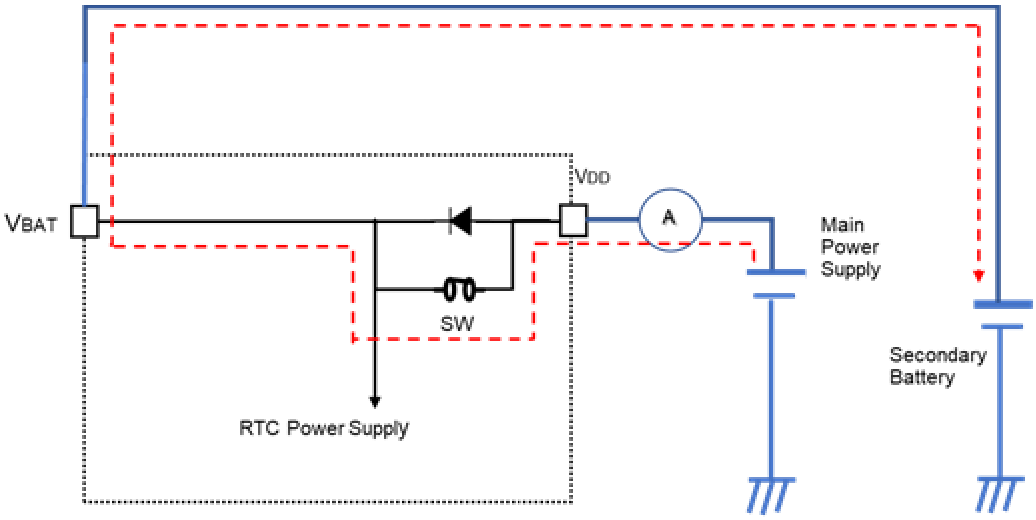


Figure 12 Circuit of charge to Re-chargeable Battery

9.1.3. Reference Value of Switching Element

Table 6 Reference value of switching element

Item	Characteristics	Condition
Current tolerance	40 mA Max.	SW = ON +25 °C
Diode Vf	0.60 V / 1 mA Typ. 0.85 V / 10 mA Typ.	V_{DD} = 3.0 V, +25 °C
Diode IR	5 nA (Max.)	VR = 5.5 V, -40 °C ~ +85 °C

Charge current into V_{BAT} should be less than 40 mA.

9.2. AC characteristics

9.2.1. AC Characteristics (1)

Table 7 AC Characteristics

Unless otherwise specified, GND = 0 V, V_{IO} = 1.6 V ~ 5.5 V, Ta = -40 °C ~ +85 °C

Item	Symbol	Condition	V_{DD} = 1.8 V ± 0.2 V		V_{DD} = 3.0 V ± 10 %		V_{DD} = 5.0 V ± 10 %		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
CLK clock cycle	t_{CLK}		1000	−	332	−	250	−	ns
CLK H pulse width	t_{WH}		450	−	166	−	125	−	ns
CLK L pulse width	t_{WL}		450	−	166	−	125	−	ns
CLK rise and fall time	t_{RF}		−	100	−	50	−	40	ns
CLK setup time	t_{CLKS}		100	−	30	−	30	−	ns
CE setup time	t_{CS}		400	−	150	−	130	−	ns
CE hold time	t_{CH}		400	−	200	−	100	−	ns
CE recovery time	t_{CR}		500	−	200	−	150	−	ns
CE rise and fall time	t_{CERF}			100	−	50	−	40	s
Write data setup time	t_{DS}		200	−	50	−	40	−	ns
Write data hold time	t_{DH}		200	−	50	−	40	−	ns
Read data delay time	t_{RD}	CL = 50 pF	0	400	−	150	−	110	ns
DO output disable time	t_{RZ}	CL = 50 pF RL = 10 kΩ	0	400	−	120	−	110	ns
DI/DO conflict avoiding time	t_{ZZ}		0	−	0	−	0	−	ns

1. Please refer to a standard of V_{IO} = 1.8 V ± 0.2 V for V_{IO} = 2.0 V ~ 2.7 V.
2. Please refer to a standard of V_{IO} = 3.0 V ± 10 % for V_{IO} = 3.3 V ~ 4.5 V.

• Timing chart

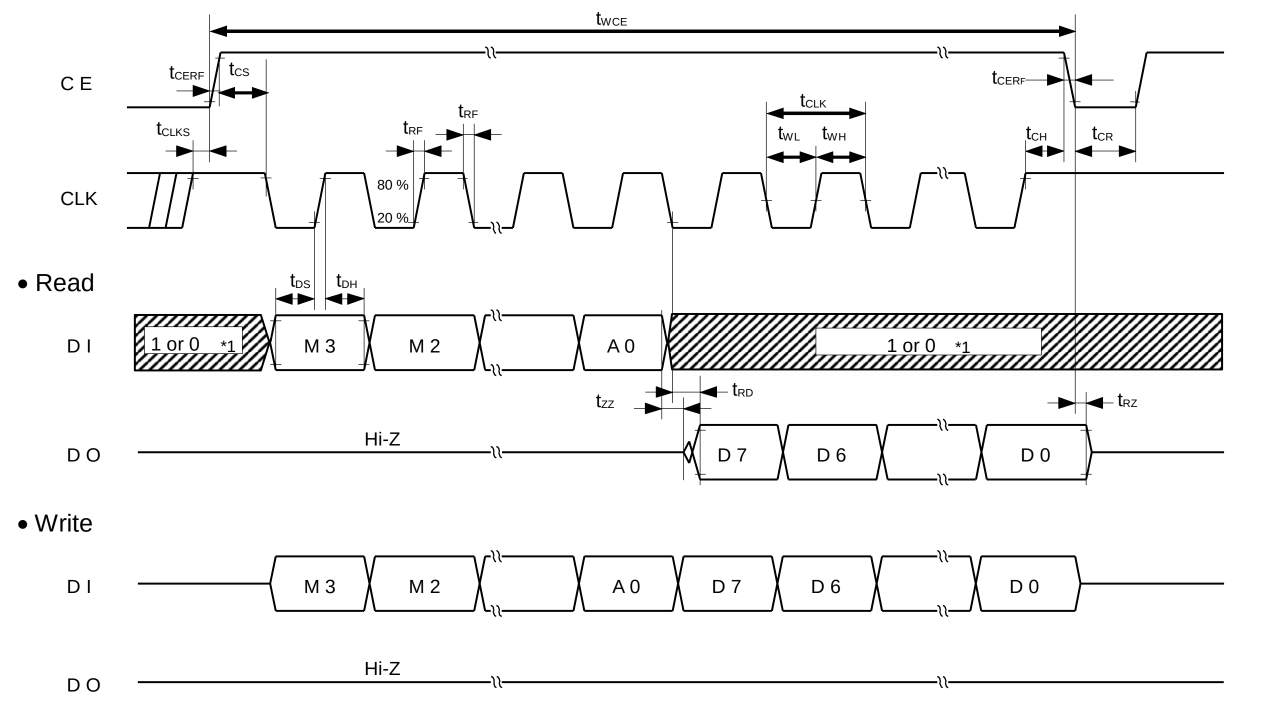


Figure 13 SPI-Bus Timing Chart

Note: When writing data, it writes the data at CLK rise after received 8 bits of data in one time.
If communication is interrupted before receiving 8 bits data, data will not be written.

*1: Even if CE is Low, DI pin is active. Don't input half voltage and don't left open DI.

9.2.2. AC Characteristics (2)

Table 8 FOUT symmetry

Unless otherwise specified, GND=0 V , V_{IO} = 1.6 V ~ 5.5 V , Ta= -40 °C ~ +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
FOUT symmetry	SYM	50 % V_{IO} Level	40		60	%

10. Interface timing when power ON / OFF

10.1. Restrictions of SPI-Bus interface in the power ON / OFF.

t_{R1} is needed for a proper power-on reset. If this power-on condition cannot be kept, it is necessary to reset the device by means of a software command.

After all power-OFF, keep VDD = VBAT = GND for more than 10 seconds for a proper power-on reset by cold start.
When cannot it, please initialize the RTC by software.

The backup period against this standard does not indicate the noise characteristics with respect to the power supply.
The backup period should be long enough (60 seconds or more).

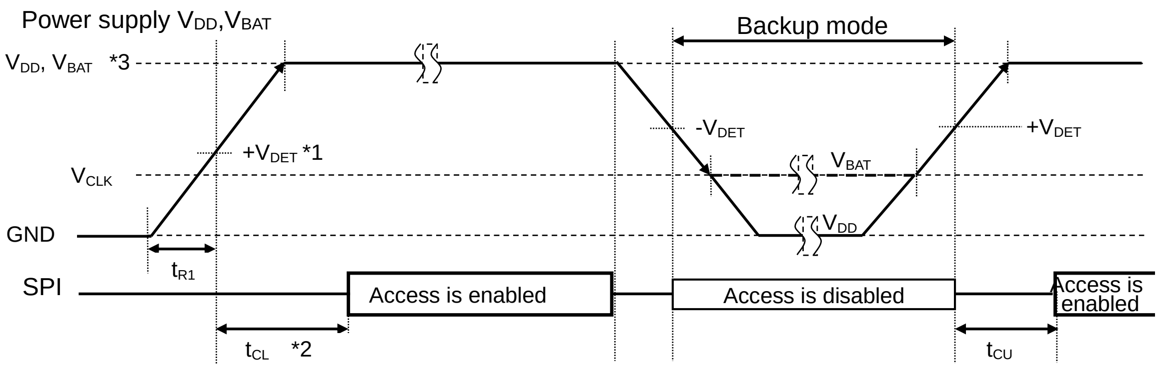


Figure 14 Power on Sequence

Table 9 Power up down characteristics

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Initial power supply rise time	t_{R1}	From GND to V_{DD} = $+V_{DET1}$	5 V	0.1	-	10	ms / V
			3 V	0.5	-	10	ms / V
Access wait time (Initial power on)	t_{CL}	After arrival to V_{DD} = 1.6 V		30	-	-	ms
Backup switchover start wait time	t_{CD}	After the access end		0	-	-	ms
Power supply fall time	t_F	From V_{DD} to V_{DD} = $-V_{DET1}$		1	-	-	ms / V
Power supply rise time (Recovery from Backup)	t_{R2}	Recovery to the operating voltage		0.1	-	-	ms / V
Access wait time (Recovery from Backup)	t_{CU}	The time from Recovery from Backup to access start		40	-	-	ms

∗1 Power-on reset is performed at the rising edge of V_{BAT} or V_{DD}.
∗2 Since the V_{DD} voltage monitoring ($+V_{DET1}$) during backup is intermittent operation (31.25 ms) , a delay occurs after V_{DD} reaches $+V_{DET1}$ until the power supply switches.
*3 For internal initialization, the V_{DD} voltage at the initial power-on must be increased to 1.6 V or more.

10.2. V_{DD} and CE Timing at Power On

When the power is turned to ON, use with CE = Low, " V_{CL} V in the diagram" as illustrated in the following timing chart.

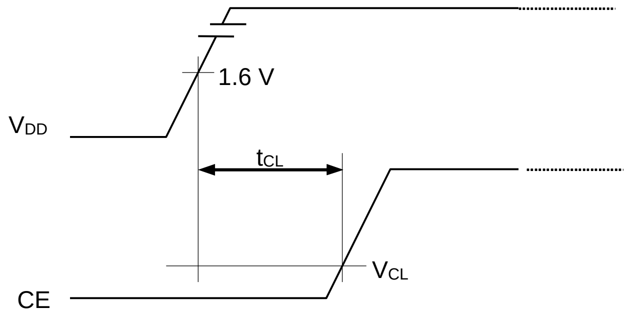


Figure 15 VDD, CE sequence

Table 10 CE Timing

Item	Symbol	Condition	Specification	Unit
CE voltage when power is turned to ON	V_{CL}	CE impressed voltage until V_{DD} = 1.6 V	0.3 Max.	V
CE = V_{CL}V time when power is turned to ON	t_{CL}	Time to maintain CE = V_{CL} until V_{DD} = 1.6 V	40 Min.	ms

10.2. Restrictions on Access Operations During Power-on Initialization and Recovery from Backup

Because most of RTC registers are synchronized with the oscillation clock of the built-in crystal oscillator, the RTC does not work normally without the integrated oscillator having stabilized. Please initialize the RTC at the time the power supply voltage returns (VLF = 1) after the oscillation has stabilized (after oscillation start time t_{STA}).
If intending to access the RTC after the main supply voltage returns, please note following points:

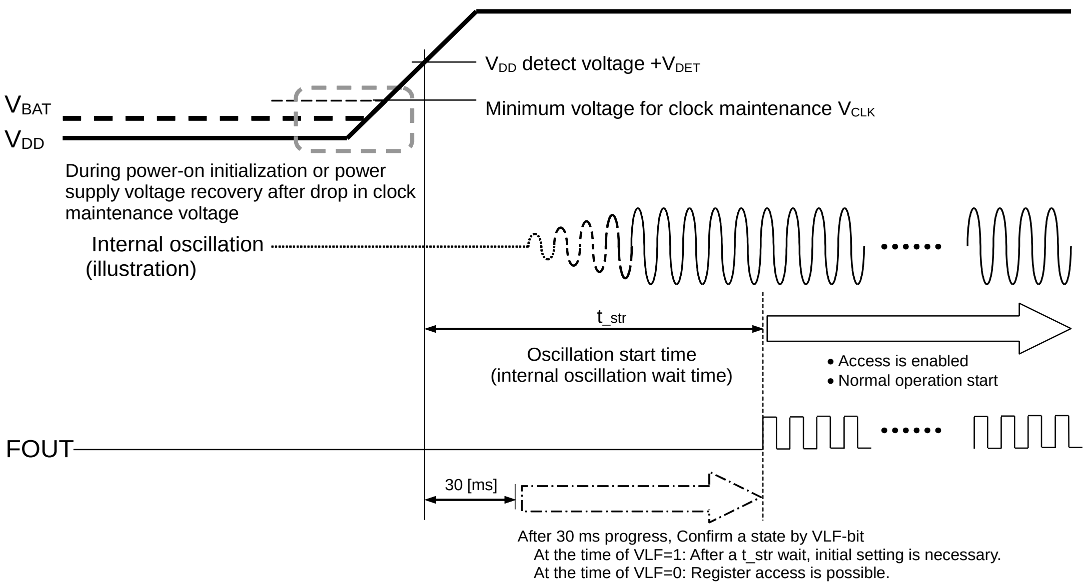


Figure 16 Oscillation start time chart (Power initial supply)

- Recovery from Backup

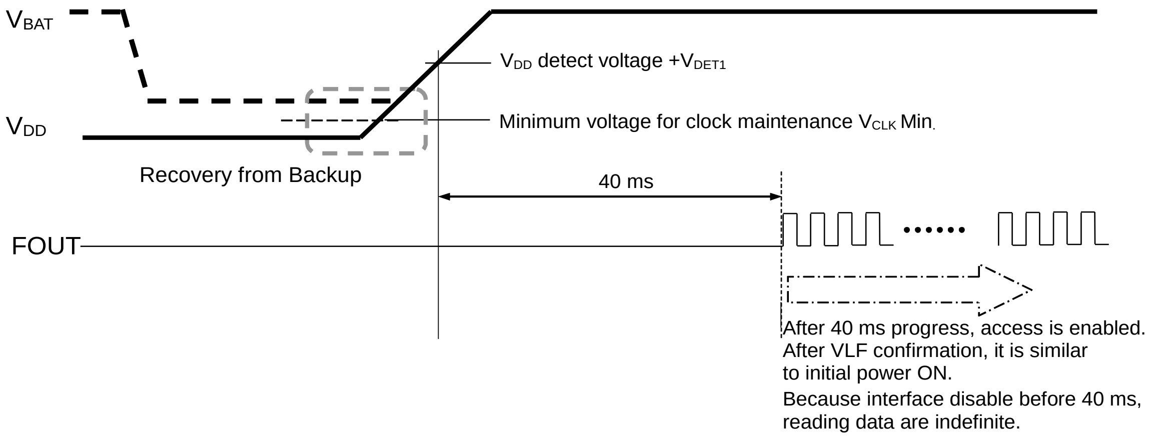


Figure 17 Recovery from Backup

10.3. Reset by Software

Software sequence for generating Power-on-reset

1) Power ON
2) Wait more than 40 ms. *1
3) Dummy readout *2
4) Confirm VLF-bit = 1.
5) Write 00h Address: Bank3 - 2h INIEN = 0b
6) Write 80h Address: Bank3 - Fh TEST = 1 *3
7) Write 6Ch Address: Bank5 - 0h
8) Write 03h Address: Bank5 - 1h
9) Write 10h Address: Bank5 - 2h
10) Write 20h Address: Bank5 - 3h
11) Wait more than 2 ms. TEST-bit is reset automatically. *4

*1 *1 When 40 ms waiting time is so long time in your system, an another method.
Jump to step3 from step1.
At step4, when VLF is 1, write 0 to VLF. While VLF is 1, repeat reset to VLF and verify VLF is 0.
If VLF is cleared to 0, jump to step5. In this method, it have possibility this sequence is short than 40 ms.
After 40 ms, when VLF doesn't reset to 0, go to step5.

*2 *2 Dummy reading. Any address is acceptable.

*3 *3 Should be execute this command even if VLF is 0. Even if VLF is 1, it available after step5.

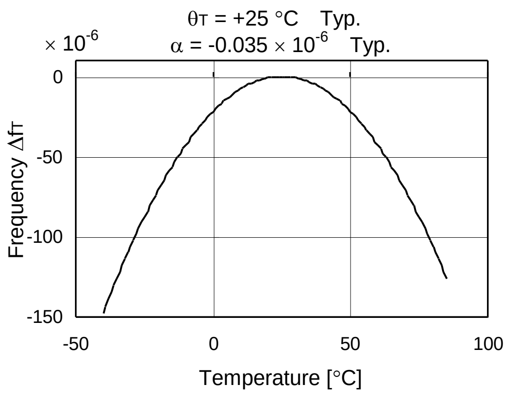
*4 *4 2ms wait is needed for RESET completion.

Note: Except using this RESET sequence, never write 1 to a TEST- bit.

11. Reference information

11.1. Reference Data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

   $\Delta f_T = \alpha \ (\theta_T - \theta_X)^2$

   - Δf_T : Frequency deviation in any temperature
   - α [1 / °C²] : Coefficient of secondary temperature $(-0.035 \pm 0.005) \times 10^{-6}$ / °C²
   - θ_T [°C] : Ultimate temperature (+25 ± 5 °C)
   - θ_X [°C] : Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

   $\Delta f/f = \Delta f/f_o + \Delta f_T + \Delta f_V$

   - $\Delta f/f$: Clock accuracy (stable frequency) in any temperature and voltage.
   - $\Delta f/f_o$: Frequency precision
   - Δf_T : Frequency deviation in any temperature.
   - Δf_V : Frequency deviation in any voltage.

3. How to find the date difference

   Date Difference = $\Delta f/f \times 86400$ (Sec)

   * For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

Figure 18 Frequency vs Temperature characteristics

There is a tool on our web that makes it easy to calculate the time error due to temperature. Please come to this *"Link"*

12. Application notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins. Also, avoid placing any device that generates high level of electronic noise near this module.

(3) Voltage levels of input pins

When the voltage of out of the input voltage specifications range input into an input terminal constantly, a penetration electric current occurs. Thus, current consumption increases very much. This causes Latch-up, and there is the case that, as a result, a built-in IC is destroyed. Please use an input terminal according to input voltage specifications.

(4) Handling of unused pins

Disposal of unused input terminals. When an input terminal is open state, it causes increase of a consumption electric current and the behavior that are instability. Please connect an unused input terminal to VIO or GND.

2) Notes on packaging

(1) Soldering heat resistance.

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. The reflow conditions within our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

(6) Installation of charged battery.

When a charged backup battery is installed by soldering, battery connection terminal of this device should connect to GND, beforehand.

13. Overview of Functions and Registers

Note: The initialization of the register is necessary about the unused function.

13.1. Overview of Functions

1) Clock functions

This function is used to set and read out second, minute, hour, day, month, last two digits of the year, and date data. Any two-digit year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099. It corresponds to the writing of 60 seconds for leap second correction.

2) Wake-up Timer Interrupt Function

The Wake-up timer interrupt function generates an interrupt event periodically at any Wake-up set between 244.14 µs and 32 years.
When an interrupt event is generated, the /INT pin goes to low level and 1 is set to the TF bit to report that an event has occurred.
It can use Wake-up timer interrupt function as Long-Timer or Wake up timer.
This function measures the operation time on the main power supply and the operation time on the backup power supply and can automatically sum them up.

3) Alarm Interrupt Function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, minute, and second settings. When an interrupt event occurs, the AF bit value is set to 1 and the /INT pin goes to low level to indicate that an event has occurred.

4) Voltage Drop Detection Function

This is a function to detect a drop in V_{DD} voltage.
It is possible to judge whether the timekeeping contents are valid, such as when the initial power is turned on or when the power supply voltage drops.
When a voltage drop is detected, the device enters the initial state (reset state) by the power-on reset function.

5) Frequency Stop Detection Function

This flag bit indicates the retained status of clock operations or internal data. Its value changes from 0 to 1 when data loss might have occurred due to a low supply voltage.

6) Clock Output Function

A clock with the same frequency (32.768 kHz) as the built-in crystal resonator can be output from the FOUT pin. Output could also be 1 Hz, or 1024 Hz.

7) Time Stamp Function

Data can be recorded from 1/10024 second digit to year digit.

8) User RAM

RAM register is read/write accessible for any data.
Built-in 8bit × 64word (512bit) RAM
When not use Timestamp function, it can use for users memory.

13.2. Register Table

The target register is selected and accessed with the first 4-bit mode setting code of communication.

Table 11 SPI-Bus 4bits Registers

Mode	Bank1	Bank2	Bank3	Bank4	Bank5	Bank6	Bank7
Read	9h	Ah	Bh	Ch	Dh	Eh	Fh
Write	1h	2h	3h	4h	5h	6h	7h

13.2.1. Register Table

Table 12 Register Table 1

Bank1 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0h	SEC	z	40	20	10	8	4	2	1
1h	MIN	z	40	20	10	8	4	2	1
2h	HOUR	z	z	20	10	8	4	2	1
3h	WEEK	z	6	5	4	3	2	1	0
4h	DAY	z	z	20	10	8	4	2	1
5h	MONTH	z	z	z	10	8	4	2	1
6h	YEAR	80	40	20	10	8	4	2	1
7h	MIN Alarm	AE	40	20	10	8	4	2	1
8h	HOUR Alarm	AE	●	20	10	8	4	2	1
9h	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		●	20	10	8	4	2	1
Ah	Timer Counter 0	128	64	32	16	8	4	2	1
Bh	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
Ch	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536
Dh	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	▲	TSEL1	TSEL0
Eh	Flag Register	POR	z	UF	TF	AF	EVF	VLF	XST
Fh	Control Register	z	z	UIE	TIE	AIE	EIE	z	STOP

Bank2 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0h	Time Stamp 1/1024S	-	-	-	-	-	-	1/512	1/1024
1h	Time Stamp 1/256S	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256
2h	Time Stamp SEC	z	40	20	10	8	4	2	1
3h	Time Stamp MIN	z	40	20	10	8	4	2	1
4h	Time Stamp HOUR	z	z	20	10	8	4	2	1
5h	Time Stamp WEEK	z	6	5	4	3	2	1	0
6h	Time Stamp DAY	z	z	20	10	8	4	2	1
7h	Time Stamp MONTH	z	z	z	10	8	4	2	1
8h	Time Stamp YEAR	80	40	20	10	8	4	2	1
9h	Status Stamp	z	z	●	●	VDET	z	XST	z
Ah	No Function	z	z	z	z	z	z	z	z
Bh	Over Write Control	▲	No Function					OVW	-
Ch	SEC Alarm	AE	40	20	10	8	4	2	1
Dh	Timer Control	z	z	z	z	TBKON	TBKE	TMPIN	TSTP
Eh	Time Stamp control 0	z	z	z	z	z	z	z	COMTG
Fh	Command Trigger	z	z	z	z	z	z	z	z

Table 13 Register Table 2

Bank3 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0h	No Function	z	z	z	z	z	z	z	z
1h	No Function	z	z	z	z	z	z	z	z
2h	Power Switch Control	▲	INIEN	z	z	SWSEL1	SWSEL0	SMPT1	SMPT0
3h	No Function	z	•	z	z	•	z	•	z
4h	Time Stamp Control 1	z	z	z	z	z	EISEL	TSCLR	TSRAM
5h	Time Stamp Control 2	•	z	z	z	▲	EVDET	▲	EXST
6h	Time Stamp Control 3	z	z	z	TSFUL	TSEMP	TSDA2	TSDA1	TSDA0
7h	No Function	z	z	z	•	z	z	z	•
8h to Dh	No Function	z	z	z	z	z	z	z	z
Eh	No Function	-	-	-	-	-	-	-	-
Fh	TEST	TEST	z	z	z	z	z	z	z

Bank4,5,6,7 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0h	Time stamp 1/256S	1	2	4	8	16	32	64	128
1h	Time Stamp SEC	•	40	20	10	8	4	2	1
2h	Time Stamp MIN	•	40	20	10	8	4	2	1
3h	Time Stamp HOUR	•	•	20	10	8	4	2	1
4h	Time Stamp DAY	•	•	20	10	8	4	2	1
5h	Time Stamp MONTH	•	•	•	10	8	4	2	1
6h	Time Stamp YEAR	80	40	20	10	8	4	2	1
7h	Status stamp	•	•	•	•	VDET	•	XST	•
8h	Time stamp 1/256S	1	2	4	8	16	32	64	128
9h	Time Stamp SEC	•	40	20	10	8	4	2	1
Ah	Time Stamp MIN	•	40	20	10	8	4	2	1
Bh	Time Stamp HOUR	•	•	20	10	8	4	2	1
Ch	Time Stamp DAY	•	•	20	10	8	4	2	1
Dh	Time Stamp MONTH	•	•	•	10	8	4	2	1
Eh	Time Stamp YEAR	80	40	20	10	8	4	2	1
Fh	Status stamp	•	•	•	•	VDET	•	XST	•

After the initial power-up (from 0 V) or in case the VLF bit returns 1, make sure to initialize all registers, before using the RTC.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect. Week data is not need care.
The TEST bit is used by the manufacturer for testing. Be sure to write 0 by initializing before using the RTC. Afterward, be sure to set 0 when writing
Any bit marked with “z” should be used with a value of 0 after initialization. Writing 1 is ignored.
Any bit marked with “•” is a RAM bit that can be used to read or write any data.
Write ‘0’ to the “-“’ mark when writing. The read value is undefined. Please mask the corresponding bit after reading it.
The above table shows only the user registers. Due to functional reasons, RTC has different registers not mentioned above table which are programmed by the manufacturer. Please make sure to only access above mentioned user registers.
Writing operation is ignored at any bit marked “No Function”.
"▲" mark bits are must be cleared to 0. Afterward, be kept in 0, anytime. When writes 1 to "▲", it has possibility of current consumption is increased.

13.2.2. Register Initial value, And Read/Write Operation Table

This value is initialized by power-on reset.

X : Undefined 0 or 1
Initialization by register writing is needed. It is not necessary to initialize time stamp data area.
0 : Reset state.
1 : Set state.

Table 14 Register Initial Value 1

Bank 1 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0h	SEC	**0**	X	X	X	X	X	X	X
1h	MIN	**0**	X	X	X	X	X	X	X
2h	HOUR	**0**	**0**	X	X	X	X	X	X
3h	WEEK	**0**	X	X	X	X	X	X	X
4h	DAY	**0**	**0**	X	X	X	X	X	X
5h	MONTH	**0**	**0**	**0**	X	X	X	X	X
6h	YEAR	X	X	X	X	X	X	X	X
7h	MIN Alarm	**1**	X	X	X	X	X	X	X
8h	HOUR Alarm	**1**	X	X	X	X	X	X	X
9h	WEEK Alarm	**1**	X	X	X	X	X	X	X
	DAY Alarm		X	X	X	X	X	X	X
Ah	Timer Counter 0	X	X	X	X	X	X	X	X
Bh	Timer Counter 1	X	X	X	X	X	X	X	X
Ch	Timer Counter 2	X	X	X	X	X	X	X	X
Dh	Extension Register	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Eh	Flag Register	**1**	**0**	**0**	**0**	**0**	**0**	**1**	X
Fh	Control Register	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bank 2 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0h	Time Stamp 1/1024S	**0**	**0**	**0**	**0**	X	X	X	X
1h	Time Stamp 1/256S	X	X	X	X	X	X	X	X
2h	Time Stamp SEC	**0**	X	X	X	X	X	X	X
3h	Time Stamp MIN	**0**	X	X	X	X	X	X	X
4h	Time Stamp HOUR	**0**	**0**	X	X	X	X	X	X
5h	Time Stamp WEEK	**0**	X	X	X	X	X	X	X
6h	Time Stamp DAY	**0**	**0**	X	X	X	X	X	X
7h	Time Stamp MONTH	**0**	**0**	**0**	X	X	X	X	X
8h	Time Stamp YEAR	X	X	X	X	X	X	X	X
9h	Status Stamp	**0**	**0**	X	X	X	**0**	X	**0**
Ah	No Function	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bh	Over Write Control	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Ch	SEC Alarm	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Dh	Timer Control	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Eh	Time Stamp control 0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Fh	Command Trigger	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Table 15 Register Initial Value 2

Bank 3 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0h	No Function	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
1h	No Function	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
2h	Power Switch Control	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
3h	No Function	**0**	X	**0**	**0**	**0**	**0**	**0**	**0**
4h	Time Stamp Control 1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
5h	Time Stamp Control 2	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
6h	Time Stamp Control 3	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**
7h	No Function	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
8h to Dh	No Function	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Eh	No Function	X	X	X	X	X	X	X	X
Fh	TEST	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bank4,5,6,7 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0h	Time stamp 1/256S	X	X	X	X	X	X	X	X
1h	Time Stamp SEC	X	X	X	X	X	X	X	X
2h	Time Stamp MIN	X	X	X	X	X	X	X	X
3h	Time Stamp HOUR	X	X	X	X	X	X	X	X
7h	Time Stamp DAY	X	X	X	X	X	X	X	X
5h	Time Stamp MONTH	X	X	X	X	X	X	X	X
6h	Time Stamp YEAR	X	X	X	X	X	X	X	X
7h	Status stamp	X	X	X	X	X	X	X	X
8h	Time stamp 1/256S	X	X	X	X	X	X	X	X
7h	Time Stamp SEC	X	X	X	X	X	X	X	X
Ah	Time Stamp MIN	X	X	X	X	X	X	X	X
Bh	Time Stamp HOUR	X	X	X	X	X	X	X	X
Ch	Time Stamp DAY	X	X	X	X	X	X	X	X
Dh	Time Stamp MONTH	X	X	X	X	X	X	X	X
Eh	Time Stamp YEAR	X	X	X	X	X	X	X	X
Fh	Status stamp	X	X	X	X	X	X	X	X

X : Undefined 0 or 1
0 : Reset state.
1 : Set state.

13.3. Description Of Registers

13.3.1. Clock and Calendar Counter (Bank1 - 1h ~ 6h)

This is counter registers from a second to a year.
Please refer to [14.1 Clock calendar explanation] for details.

13.3.2. Timer Setting and Timer Counter Register (Bank1 - Ah ~ Ch)

This register is used to set the default (preset) value for the counter.
To use the Wake-up timer interrupt function, TE, TF, TIE, TSEL1, TSEL0, TBKON, TBKE, TSTP, TMPIN bits are set and used. When the Wake-up timer interrupt function is not being used, the Wake-up timer control register can be used as a RAM register. In such cases, stop the Wakeup timer function by writing 0 to the TE and TIE bits.
Please refer to [14.2. Wakeup Timer Interrupt Function] for the details.

13.3.3. Alarm Registers (Bank1 – 7h ~ 9h, Bank2 - Ch)

The alarm interrupt function is used, along with the AE, AF, and WADA bits, to set alarms for specified date, day, hour, minute, and second values.
Please refer to [14.3. Alarm Interrupt Function] for the details.

13.3.4. Function-Related Register (Bank1 - 1Dh ~ 1Fh)

1) FSEL1, FSEL0 bit
A combination of the FSEL1 and FSEL0 bits are used to select the frequency to be output.
If customer does not use this function, FESL1, FSEL0 should be set to 1.
Please refer to 14.6 FOUT Function

2) USEL, UF, UIE bit
This bit is used to specify either “second update” or “minute update” as the update generation timing of the time update interrupt function.
If customer does not use this function, USEL, UIE should be reset to 0. UF do not care.”.
Please refer to [14.4. Update interrupt function] for the details.

3) TE, TF, TIE, TSEL1, TSEL0, TSTP, TBKON, TBKE, TMPIN bit
These bits are used to control operation of the wake-up timer interrupt function.
If customer does not use this function, (TE, TIE, TSTP, TMPIN) should be (0,0,0,0), TSEL1, TSEL0(1,0). TF do not care.
Please refer to [14.2 Wake-up timer interrupt function] for the details.

4) WADA, AF, AIE bit
These bits are used to control operation of the alarm interrupt function.
If customer does not use this function, WADA should be 1, AIE 0. AF do not care.
Please refer to [14.3. Alarm interrupt function] for the details.

5) ETS, EVF, EIE bit
These bits are used to control operation of the time stamp function.
If customer does not use this function, ETS, EIE should be reset to 0. EVF do not care.
Please refer to [14.8. Time Stamp function] for the details.

6) VLF, POR, XST bit
These bits are used to detect RTC inner status and recording.
Ex. During power on resetting, lower voltage detection makes VLF bit 1.
Please refer to [14.5. RTC inner status detection function] for the details.

7) STOP bit
This bit is to stop a timekeeping operation. In the case of “STOP bit = 1”:
All the update of timekeeping (year, month, day, week, hour, minute, second, 1/128 s, 1/512 s) operation and the calendar operation stops. With it, an update interrupt event does not occur at an alarm interrupt and the time stamp data is to be stopping condition.
(Please refer to 14.8.5)
The part of the fixed-cycle timer interrupt function stops.
A count stops the source clock setting of the timer in case of “64 Hz, 1 Hz, 1 min, 1 h”.
(In case of 4096 Hz, it does not stop.)
The effect of STOP bit to FOUT functions.
When STOP = 1, 32.768 kHz and 1024 Hz output is possible. But 1 Hz output is disabled.
Switchover function cannot work in order that the V_{DD} voltage drop detection stops even if a main power supply falls.

13.3.5. Power Switching Circuit-Related Register Bank3 02h

1) INIEN bit
   This bit sets power switching operation and SPI-Bus communication stop at backup
2) SMPT1, SMPT0 bit
   This bit sets the intermittent operation active time of the voltage monitoring circuit of the built-in MOS switch.
3) SWSEL1, SWSEL0 bit
   When not using the power switching function, this bit sets the built-in MOS switch.

13.3.6. Time stamp-related register

Please refer to [13.8. Time stamp function] for the details.

1) Time stamp and status record register (Bank2 - 0h ~ 9h; Bank4, 5, 6, 7 - 0h ~ Fh)
   This register records time stamp data from 1/1000 second digit to Year digit and internal state when an event occurs.
2) Command trigger Time stamp control register (Bank2 - Eh ~ Fh)
   This register is used when triggering time stamp using SPI-Bus communication access.
3) Time stamp trigger control register (Bank3 - 5h)
   This register is used to perform time stamp trigger.

13.3.7. RAM registers (Bank4, 5, 6, 7)

This RAM register is read/write accessible for any data in the range from 0h to Fh.

14. How to use

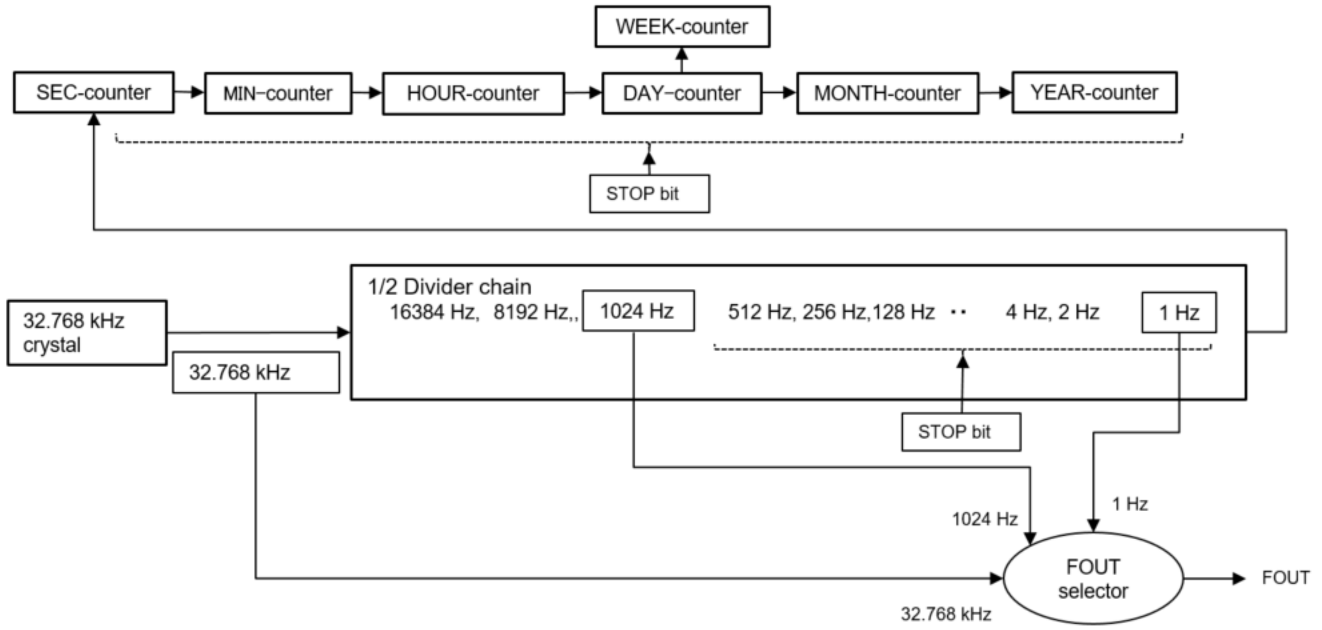


Figure 19 Basic Function 32.768 kHz oscillation, counter, FOUT

14.1. Clock Calendar Explanation

At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end. Therefore, it recommends that the access to a clock calendar has continuous access by the auto increment function. When reading the current time, do not use the STOP bit (STOP = 0).

Setting example: Sun, 29-Feb-88 17:39:45 (leap year)

Table 16 Time Calendar setting Ex.

Bank1 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0h	SEC	0	1	0	0	0	1	0	1
1h	MIN	0	0	1	1	1	0	0	1
2h	HOUR	0	0	0	1	0	1	1	1
3h	WEEK	0	0	0	0	0	0	0	1
4h	DAY	0	0	1	0	1	0	0	1
5h	MONTH	0	0	0	0	0	0	1	0
6h	YEAR	1	0	0	0	1	0	0	0

Note
With caution that writing non-existent time data may interfere with normal operation of the clock counter
Time starts at the moment of STOP bit operation (1 to 0 timing)

14.1.1. Clock Counter

1) [SEC], [MIN] register
These registers are 60-base BCD counters. When update signals were generated from a lower counter, a upper counter is one incremented. At the timing when the lower register changes from 59 to 00, carry is generated to the higher register and thus incremented.
When writing is performed to [SEC] register, Internal-count-down-chain less than one second (512 Hz ~ 1 Hz) is cleared to 0.

2) [HOUR] register
This register is a 24-base BCD counter (24-hour format). These registers are incremented at the timing when carry is generated from a lower register.

3) Leap second adjustment
For leap second adjustment, user can write “60” into SEC counter, after 1 second SEC counter is to be set “00”.
Normally second counter counts up “59” to “00”.

14.1.2. Week Counter

The day (of the week) is indicated by 7 bits, bit 0 to bit 6.
The day data values are counted as: Day 01h → Day 02h → Day 04h → Day 08h → Day 10h → Day 20h → Day 40h → Day 01h → Day 02h, etc.
It is incremented when carry is generated from the HOUR register. This register does not generate carry to a higher register.
Since this register is not connected with the YEAR, MONTH and DAY registers, it needs to be set again with the matching day of the week if any of the YEAR, MONTH or DAY registers have been changed.
When not use Week data, It is not necessary for Week register to be initialized.
Do not set 1 to more than one day at the same time.

Table 17 Week Register

Day	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Data [h]
Sunday	0	0	0	0	0	0	0	**1**	01 h
Monday	0	0	0	0	0	0	**1**	0	02 h
Tuesday	0	0	0	0	0	**1**	0	0	04 h
Wednesday	0	0	0	0	**1**	0	0	0	08 h
Thursday	0	0	0	**1**	0	0	0	0	10 h
Friday	0	0	**1**	0	0	0	0	0	20 h
Saturday	0	**1**	0	0	0	0	0	0	40 h

Do not set 1 to more than one day at the same time.

14.1.3. Calendar Counter

1) [DAY], [MONTH] resister
The DAY register is a variable (between 28-base and 31-base) BCD counter that is influenced by the month and the leap year. The MONTH register is 12-base BCD counter. when carry is generated from a lower register.

Table 18 DAY, MONTH Register

		Jan.	Feb.	Mar	Apr.	May	June	July	Aug.	Sep.	Oct.	Nov.	Dec.
Days	Normal year	31	28	31	30	31	30	31	31	30	31	30	31
	Leap year		29										

2) [YEAR] register
This register is a BCD counter for years 00 to 99.
The leap year is automatically determined and influences the DAY register.
This RTC processes following years as leap years: 00,04,08,12, 96.
User software correction is needed in the years 2100, 2200, 2300 as they are common years.

Definition of leap years
Leap year: year divisible by 4, year divisible by 400
Ex. 2000, 2004, 2008, 2012, 2096, 2400, 2800,
Common year: year indivisible by 4, year divisible by 100
Ex. 2001, 2002, 2003, 2005, 2099, 2100, 2200, 2300, 2500,,

14.2. Wake-up Timer Interrupt Function

The Wake-up timer interrupt function generates an interrupt event periodically at any Wake-up set between 244.14 µs and 31.9 years. It can be paused and can also be used as an accumulate timer.
tRTN2 after the interrupt occurs, the /INT status is automatically released (/INT status changes from low-level to Hi-z).

14.2.1. Related Registers For Function Of Wake-up Timer Interrupt Function

Table 19 Wake-up Timer Interrupt Register

Bank1 Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
A	Timer Counter 0	128	64	32	16	8	4	2	1
B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
C	Timer Counter 2	8388608	4194304	2097152	1048576	524288	262144	131072	65536
D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	▲	TSEL1	TSEL0
E	Flag Register	POR	z	UF	TF	AF	EVF	VLF	XST
F	Control Register	z	z	UIE	TIE	AIE	EIE	z	STOP
Bank2-D	Timer Control	z	z	z	z	TBKON	TBKE	TMPIN	TSTP

Before setting the operation, clear the TE bit to 0.
When the Wake-up timer function is not being used, the Wake-up Timer Counter0,1 register can be used as a RAM register. In such cases, stop the Wake-up timer function by writing 0 to the TE and TIE bits.

1) Down counter for Wake-up timer (Timer Counter 2, 1, 0)

This register is used to set the default (preset) value for the counter. Any count value from 1 to 16777216 can be set. Be sure to write 0 to the TE bit before writing the preset value.

When TE=0, read out data of timer counter is default (Preset) value. When TE = 1, read out data of timer counter is just counting value. But, when access to timer counter data, counting value is not held.
Therefore, for example, perform twice read access to obtain right data, and a way to adopt the case that two data accorded is necessary.

2) TSEL1, TSEL0 bit

The combination of these three bits is used to set the countdown period (source clock) for this function.

Table 20 TSEL bit Source Clock Select

TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock	Auto release time tRTN2 Min.
0	0	4096 Hz /Once per 244.14 µs	122 µs
0	1	64 Hz /Once per 15.625 ms	7.813 ms
1	0	1 Hz /Once per second	7.813 ms
1	1	1/60 Hz /Once per minute	7.813 ms

1) The /INT pin's Auto reset time (tRTN2) varies as shown above according to the source clock setting.
2) The first countdown shortens than a source clock.
When selected 4096 Hz / 64 Hz / 1 Hz as a source clock, one period of error occurs at the maximum.
When selected 1/60 Hz, 1 Hz of error occurs at the maximum.

The example of the error of the first countdown: A preset value is 04h.

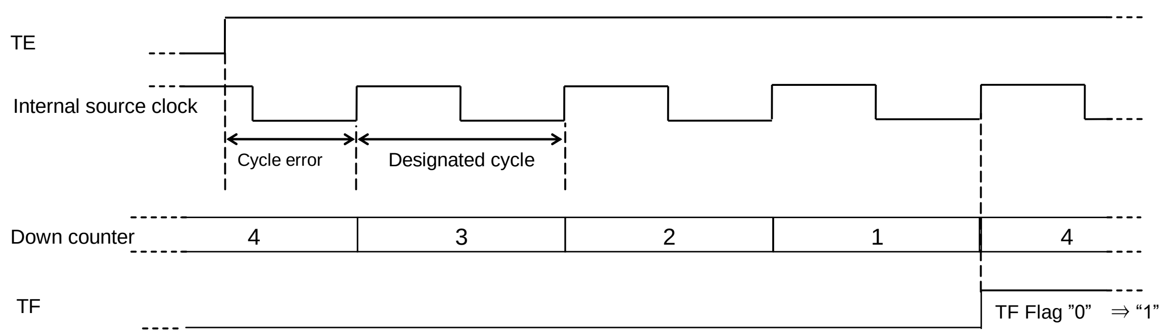


Figure 20 Wake-up Timer Initial Sequence (cycle error)

Block diagram of Inside counter of wake-up Timer.

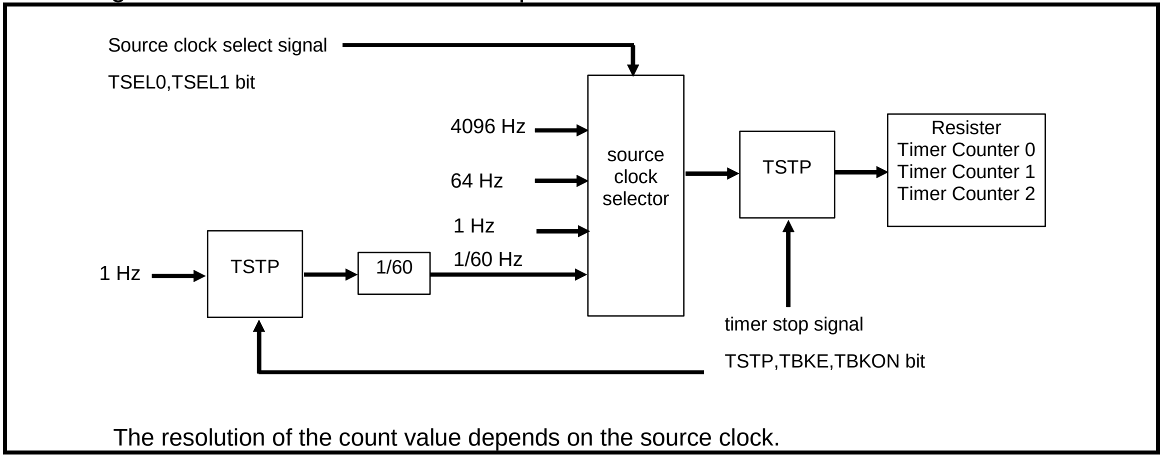


Figure 21 Wake-up Timer Block Diagram (timer source)

3) TE bit (Timer Enable)

When TE bit is 0, the default (preset) can be checked by reading this register.

Table 21 TE bit (Timer Enable)

TE	Data	Description
Write	0	Stops Wake-up timer interrupt function. Timer load the preset value and stop.
	1	Starts Wake-up timer interrupt function. The countdown that starts when the TE bit value changes from 0 to 1 always begins from the preset value.

4) TF bit (Timer Flag)

This is a flag bit that retains the result when a Wake-up timer interrupt event is detected.

Table 22 TF bit (Timer Flag)

TF	Data	Description
Write	0	The TF bit is cleared to zero to prepare for the next status detection
	1	Invalid. writing a 1 will be ignored
Read	0	–Wake-up timer interrupt events are not detected.
	1	Wake-up timer interrupt events are detected. (Result is retained until this bit is cleared to zero.)

5) TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the /INT pin when a Wake-up timer interrupt event has occurred.

Table 23 TIE bit (Timer Interrupt Enable)

TIE	Data	Description
Write	0	1) The Wake-up Timer interrupt signal is not output. 2) The time wake-up Timer interrupt signal during output is immediately released. Note. as for INT-pin, Alarm, Wake-up Timer and Time update interrupts are output as OR.
	1	When a Wake-up timer interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-z to low).

6) TBKON, TBKE bit

This function selects the operation time with the main power supply or the operation time with the backup power supply. The count value is added.

Table 24 TBKON, TBKE (Timer Backup ON, Timer Backup/Normal Enable)

operation	TBKE	TBKON	Description
Write	0	X	This setting counts normal mode and backup mode.
	1	0	This setting counts it at time of normal mode (V_{DD} operation)
		1	This setting counts it at time of backup mode (V_{BAT} operation)

7) TMPIN bit

The timer interrupt output can be assigned to the /INT or FOUT pin. Since it is an OR output with the FOUT setting, please set the FOUT output setting to FSEL 1, 0 = (1, 1) and OFF the frequency output function.

Table 25 TMPIN bit (Timer PIN)

TMPIN	Data	Description
Write	0	Assign output to / INT pin
	1	Assign output to FOUT pin

8) TSTP bit (Timer Stop)

This bit is used to stop Wake-up timer count down.

Table 26 TSTP bit (Timer STOP)

TE	STOP	TBKE	TSTP	Description
1	0	0	0	Writing a 0 to this bit cancels stop status (restarts timer counts down). The reopening value of the countdown is a stopping value
			1	Count stops.
		1	X	TSTP is invalid. and the countdown doesn't stop even if set in TSTP = 1.
	1	X	X	The count stops at the time of the setting of 64 Hz, 1 Hz,1/60 Hz.
0	X	X	X	It doesn't start counting

14.2.2. Wake-up Timer Start Timing

The timer source clock selects bits (TSEL1, TSEL0) are also fixed at the rising edge of CLK.
The timer countdown starts after the data is fixed at the rising edge of CLK of the 8th data bit (D0).

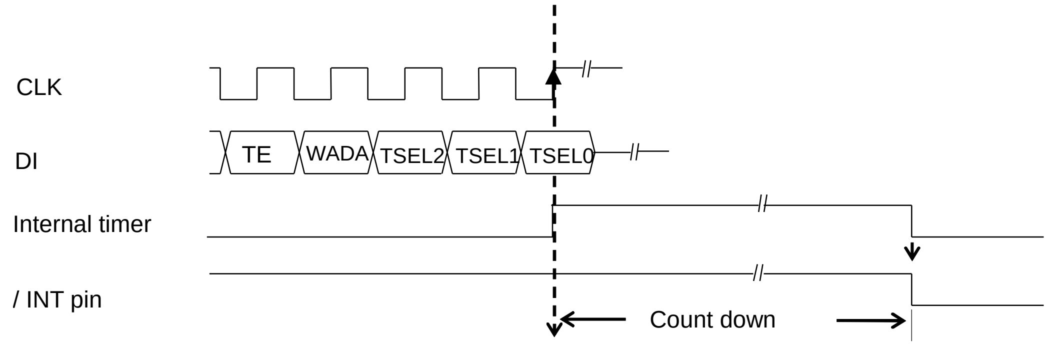


Figure 22 Wake-up Timer Start Sequence

14.2.3. Interruption period of wake-up Timer.

The combination of the source clock settings and Wake-up timer countdown value sets interrupt interval, as shown in the following examples.

Table 27 Wake-up Timer Interrupt Cycles

Timer Counter setting 1 ~ 16777216	Source clock			
	4096 Hz TSEL1, 0 = 0, 0	64 Hz TSEL1, 0 = 0, 1	1 Hz TSEL1, 0 = 1, 0	1/60 Hz TSEL1, 0 = 1, 0
0	–	–	–	–
1	244.14 μs	15.625 ms	1 s	1 min
:	:	:	:	:
410	100.10 ms	6.406 s	410 s	410 min
:	:	:	:	:
3840	0.9375 s	60.000 s	3840 s	3840 min
:	:	:	:	:
4096	1.0000 s	64.000 s	4096 s	4096 min
:	:	:	:	:
16777216	1.13 h	72.81 h	4660 h	31.9 Year

When the all counter value is set to 0b, the timer will not work.

14.2.4. Diagram of Wake-up Timer Interrupt Function

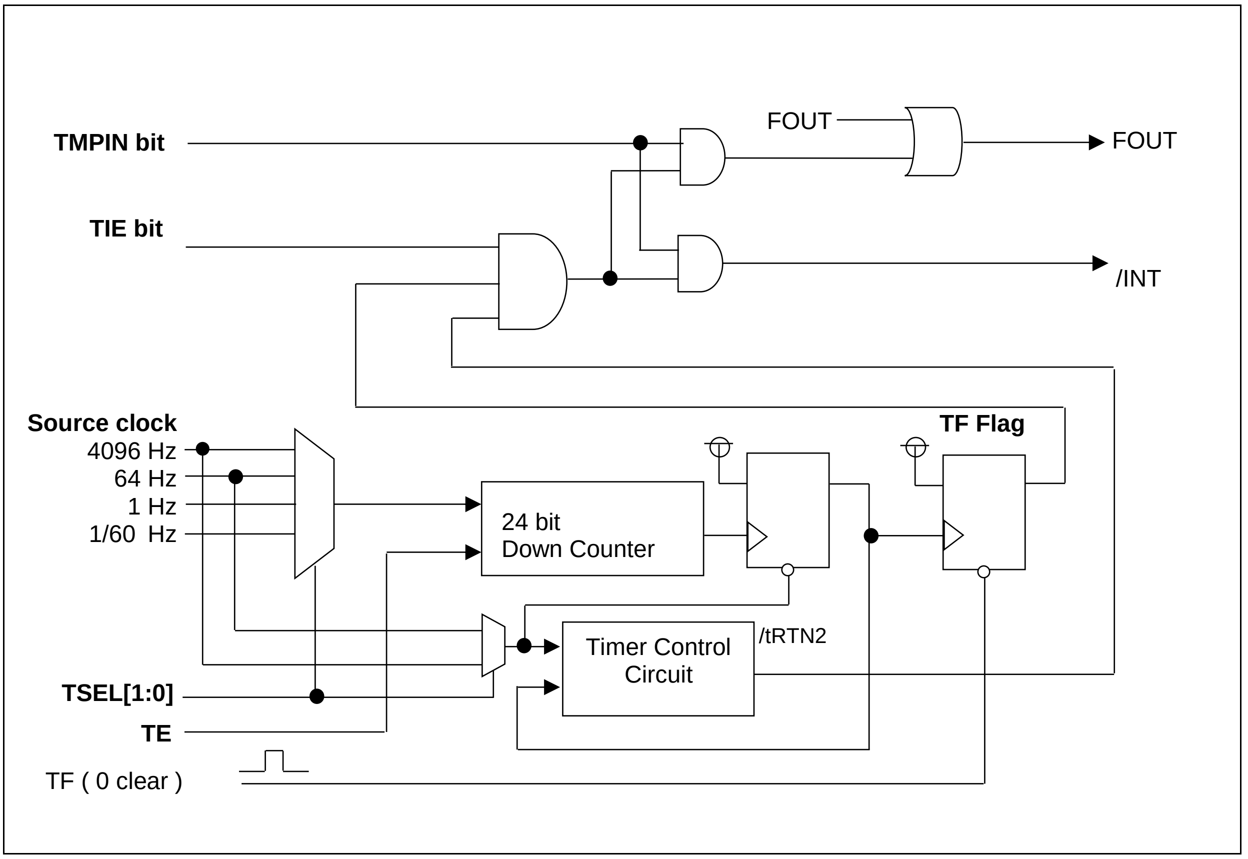


Figure 23 Wake-up Timer Block Diagram

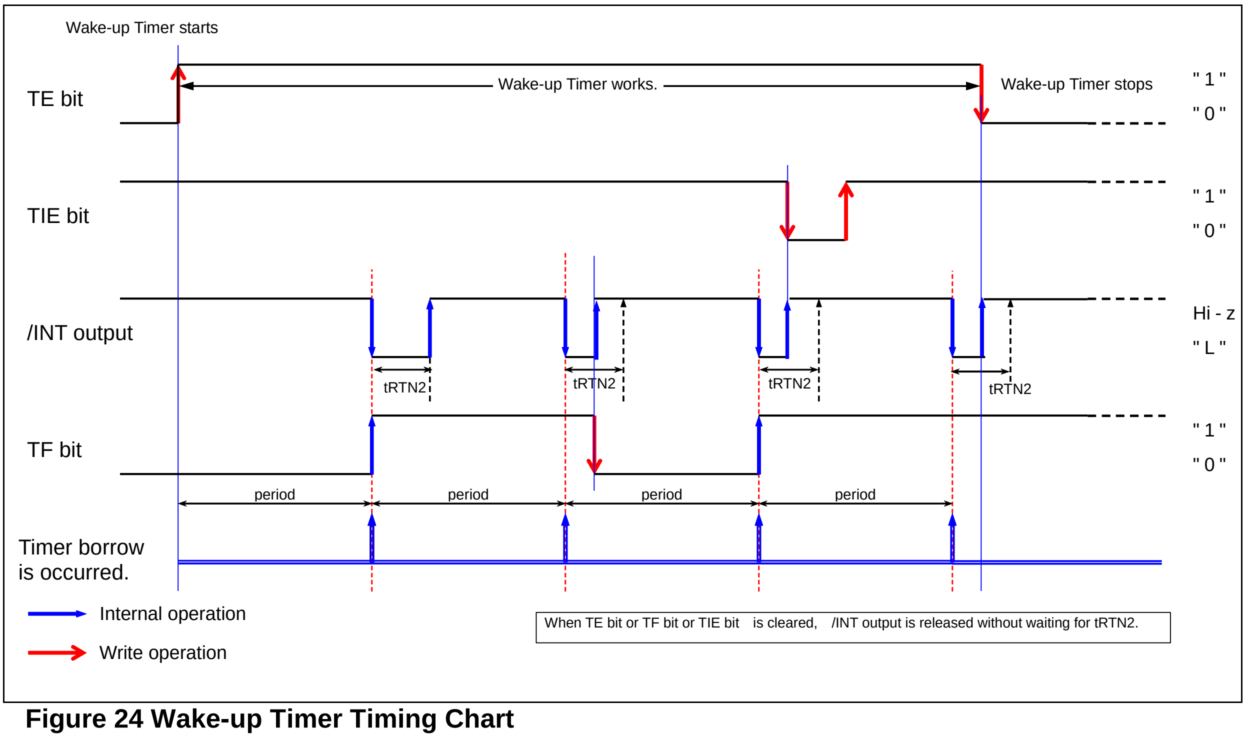


Figure 24 Wake-up Timer Timing Chart

After the interruption occurs when the count value changes from 1h to 0h, the counter automatically reloads the preset value and again starts to count down. (Repeated operation)

The countdown that starts when the TE bit value changes from 0 to 1 always begins from the preset value.

14.3. Alarm Interrupt Function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, minute, and second settings. When an interrupt event occurs, the AF bit value is set to 1 and the /INT pin goes to low level to indicate that an event has occurred.
/INT= Low output when occurs alarm interruption event is not cancelled automatically unless giving intentional cancellation and /INT = Low are maintained.

14.3.1. Related Registers for Alarm Interrupt Functions.

Table 28 Alarm Interrupt Registers

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Bank2 - C	SEC Alarm	**AE**	40	20	10	8	4	2	1
Bank1 - 7	MIN Alarm	**AE**	40	20	10	8	4	2	1
8	HOUR Alarm	**AE**	•	20	10	8	4	2	1
9	WEEK Alarm	**AE**	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
D	Extension Register	FSEL1	FSEL0	USEL	TE	**WADA**	•	TSEL1	TSEL0
E	Flag Register	POR	z	UF	TF	**AF**	EVF	VLF	XST
F	Control Register	z	z	UIE	TIE	**AIE**	EIE	z	STOP

Before entering settings for operations, it is recommended to first set the AIE bit to 0 in order to avoid inadvertent hardware interrupt at setting.

When the STOP bit value is 1 alarm interrupt events do not occur.

When the alarm interrupt function is not being used, the Alarm registers can be used as a RAM register. In such cases, be sure to write 0 to the AIE bit. When the AIE bit value is 1 and the Alarm registers is being used as a RAM register, /INT may be changed to low level unintentionally.

1) Alarm registers

The second, minute, hour, day and date when an alarm interrupt event will occur is set using this register and the WADA bit.
In the WEEK alarm /Day alarm register, the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

In case “AE” bit of register 9h is set to 1, the day will be ignored, and an interrupt occurs ones the actual time matches the seconds, minutes and hour setting of the alarm register.
(Example) Write 80h (AE = 1) to the WEEK Alarm / DAY Alarm register (Reg - 9h):
Only the hour, minute and second settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets.
As a result, alarm occurs if only the hour, minute and second values match the alarm data.
If all 4 AE bit values are 1 the week/date and time settings are ignored, and an alarm interrupt event will occur once per second.
The alarm does not occur even if it is set the same as the current time. Occurs at the next time match.

2) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

Table 29 WADA bit (Week Alarm / Day Alarm Select)

WADA	Data	Description
Write	0	Sets WEEK as target of alarm function
	1	Sets DAY as target of alarm function

3) AF bit (Alarm Flag)

When this flag bit value is already set to 0, occurrence of an alarm interrupt event changes it to 1. When this flag bit value is 1, its value is retained until a 0 is written to it.

Table 30 AF bit (Alarm Flag)

AF	Data	Description
Write	0	Clearing this bit to zero enables /INT low output to be canceled (/INT remains Hi-z) when an alarm interrupt event has occurred.
	1	Invalid (writing a 1 will be ignored)
Read	0	Alarm interrupt events are not detected.
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

4) AIE bit (Alarm Interrupt Enable)

This bit is used to control output of interrupt signals from the /INT pin when an Alarm interrupt event has occurred.

Table 31 AIE bit (Alarm Interrupt Enable)

AIE	Data	Description
Write	0	1) The Alarm interrupt signal is not output. 2) The Alarm interrupt signal during output is immediately released. Note. as for INT-pin, Alarm, Wake-up Timer and Time update interrupts are output as OR.
	1	When an Alarm interrupt event occurs, an interrupt signal is generated (/INT status changes from Hi-z to low).

The AIE bit is only output control of the /INT pin. It is necessary to clear an AF flag to cancel alarm.

14.3.2. Examples Of Alarm Settings

1) Example of alarm settings when "Week" has been specified (and WADA bit = 0)

Table 32 Alarm Setting Ex1.

Week is specified WADA bit = 0	Week Alarm								HOUR Alarm	MIN Alarm	SEC Alarm
	bit 7 AE	bit 6 S	bit 5 F	bit 4 T	bit 3 W	bit 2 T	bit 1 M	bit 0 S			
Monday through Friday, at 7:00 AM Second value is ignored. Alarm repeatedly generate for 1 minute at set time.	0	0	1	1	1	1	1	0	07h	00h	AE bit 1
Every Saturday and Sunday, for 30m00s each hour Hour value is ignored	0	1	0	0	0	0	0	1	AE bit 1	30h	00h
Every day, at 6:59:30 PM	0	1	1	1	1	1	1	1	18h	59h	30h
	1	X	X	X	X	X	X	X			

X: Don't care

2) Example of alarm settings when "Day" has been specified (and WADA bit = 1)

Table 33 Alarm Setting Ex2.

Day is specified WADA bit = 1	Day Alarm								HOUR Alarm	MIN Alarm	SEC Alarm
	bit 7 AE	bit 6 •	bit 5 20	bit 4 10	bit 3 08	bit 2 04	bit 1 02	bit 0 01			
First of each month, at 7:00 AM Second value is ignored. Alarm repeatedly generate for 1 minute at set time.	0	0	0	0	0	0	0	1	07h	AE bit 1	AE bit 1
15th of each month, for 30m00s each hour. Hour value is ignored	0	0	0	1	0	1	0	1	AE bit 1	30h	00h
Every day, at 6:59:30 PM	1	X	X	X	X	X	X	X	18h	59h	30h

X: Don't care

14.3.3. Diagram Of Alarm Interrupt Function

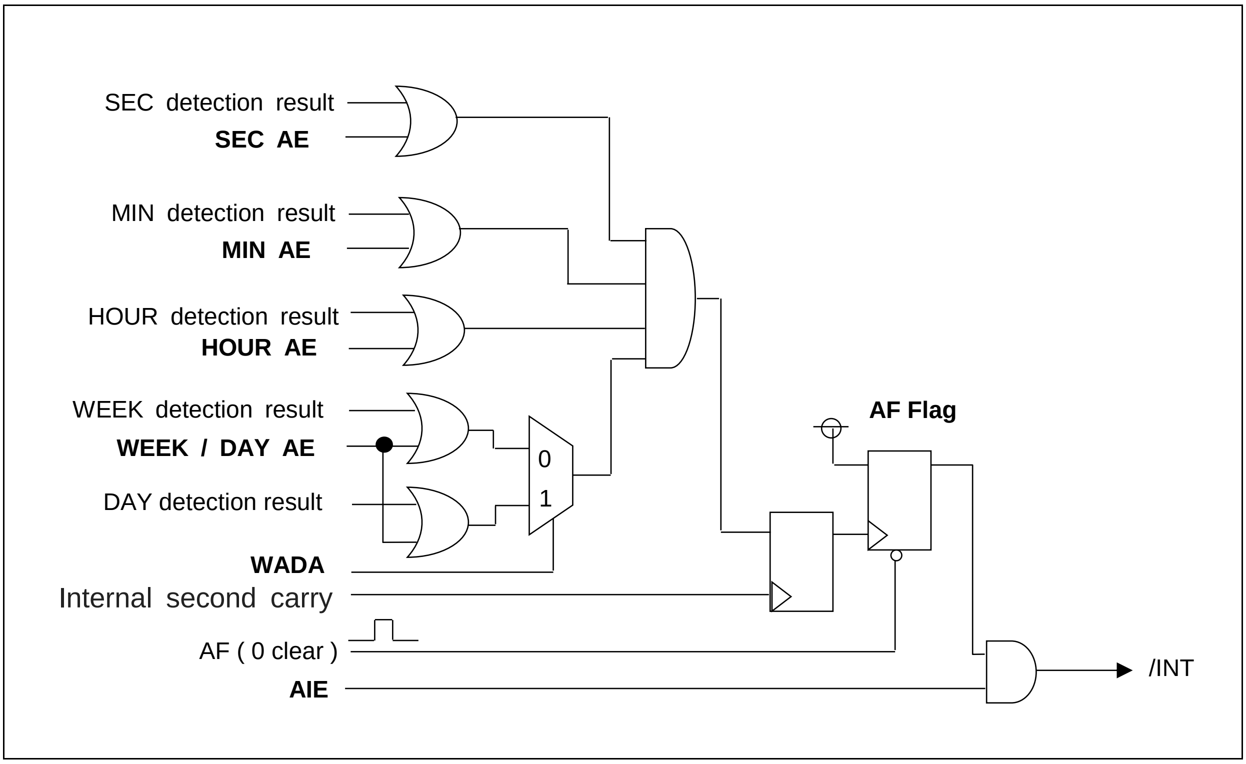


Figure 25 Alarm Interrupt Black Diagram

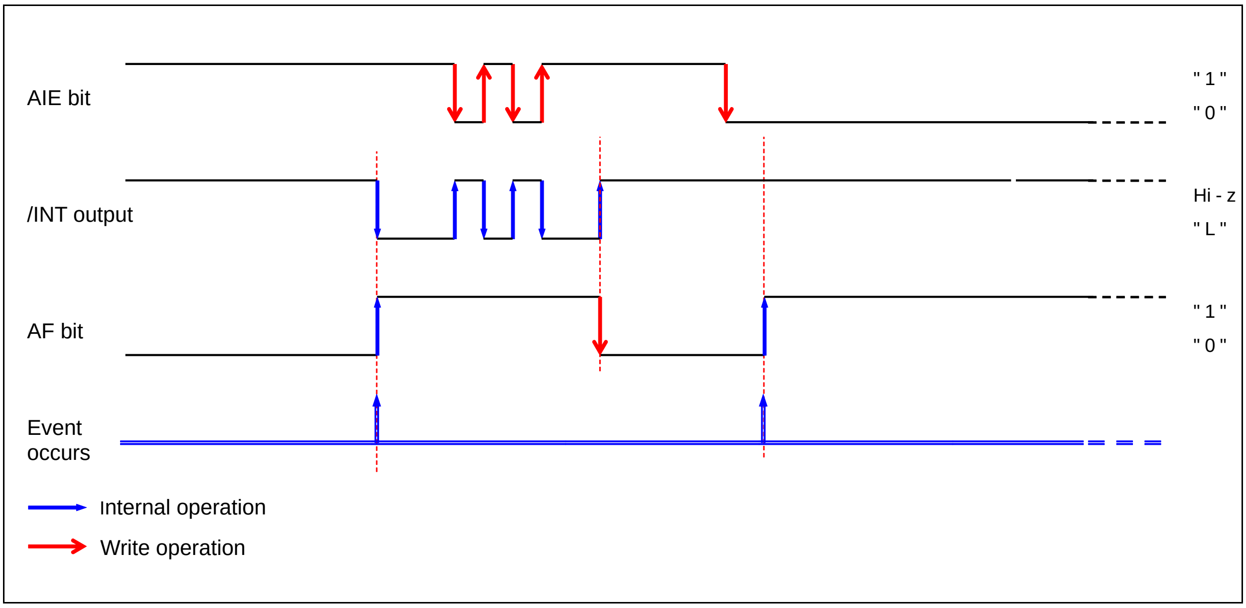


Figure 26 Alarm Interrupt Timing Chart

14.4. Time Update Interrupt Function

The interrupt of time updating is generated at the seconds update or the minutes update.
This interruption output is released to Hi-Z from active Low automatically.
This auto released time (tRTN1) is 7.324 ms to 7.644 ms, from time updating.

14.4.1. Related Registers For Time Update Interrupt Functions.

Table 34 Time Update Interrupt Registers

Bank1 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Dh	Extension Register	FSEL1	FSEL0	**USEL**	TE	WADA	▲	TSEL1	TSEL0
Eh	Flag Register	POR	z	**UF**	TF	AF	EVF	VLF	XST
Fh	Control Register	z	z	**UIE**	TIE	AIE	EIE	z	STOP

Before entering settings for operations, it is recommended to first set the UIE bit to 0 in order to avoid inadvertent hardware interrupt at setting.
When the STOP bit value is 1 time update interrupt events do not occur.
Although the time update interrupt function cannot be fully stopped, if 0 is written to the UIE bit, the time update interrupt function can be prevented from changing the /INT pin status to low.

1) USEL bit (Update Interrupt Select)

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

Table 35 USEL bit (Update Interrupt Select)

USEL	Data	Description
Write	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

2) UF bit (Update Flag)

This flag bit value changes from 0 to 1 when a time update interrupt event occurs.

Table 36 UF bit (Update Flag)

UF	Data	Description
Write	0	When UF bit clears to 0, /INT output returns to Hi-Z immediately.
	1	Invalid (writing a 1 will be ignored
Read	0	Time update interrupt events are not detected.
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

3) UIE bit (Update Interrupt Enable)

This bit selects whether to generate an interrupt signal or to not generate it.

Table 37 UIE bit (Update Interrupt Enable)

UIE	Data	Description
Write / Read	0	1) The interrupt signal due to time update is not output. 2) The time update interruption signal is immediately stopped. Note. as for INT-pin, alarm, timer and time update interrupts are output as OR.
	1	When a time update occurs, an interrupt signal is generated. /INT status changes from Hi-z to Low. 7.324 ms to 7.644 ms after the interrupt occurs, the active Low is automatically released. /INT status changes from Low to Hi-Z.(tRTN1)

14.4.2. Time Update Interrupt Function Diagram

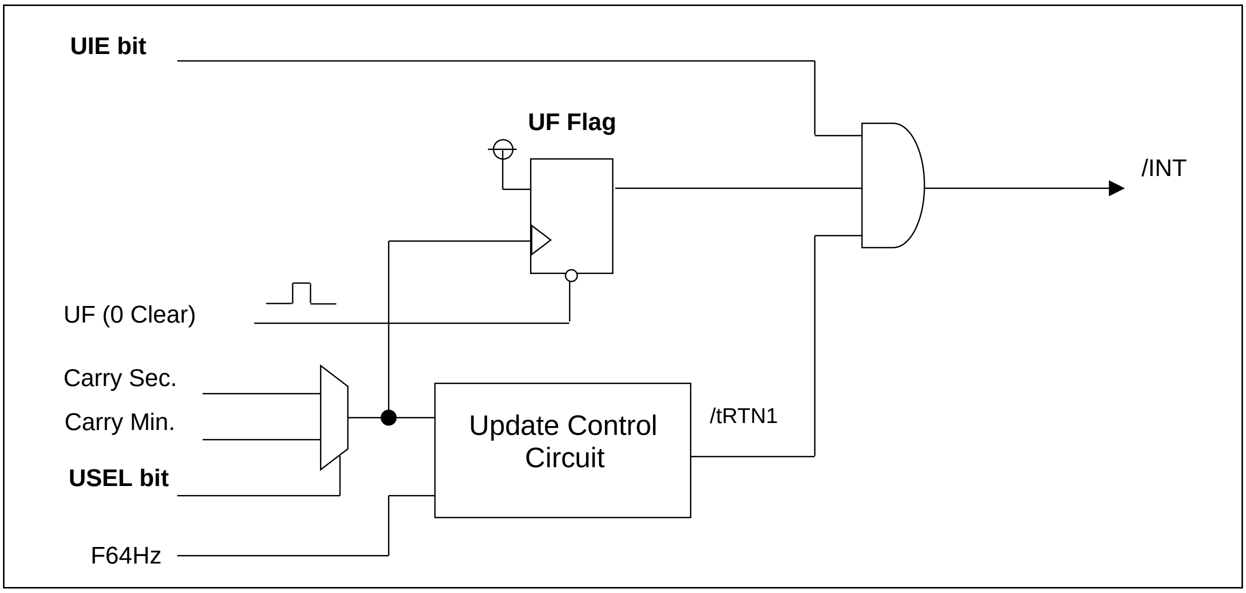


Figure 27 Time Update Interrupt Block Diagram

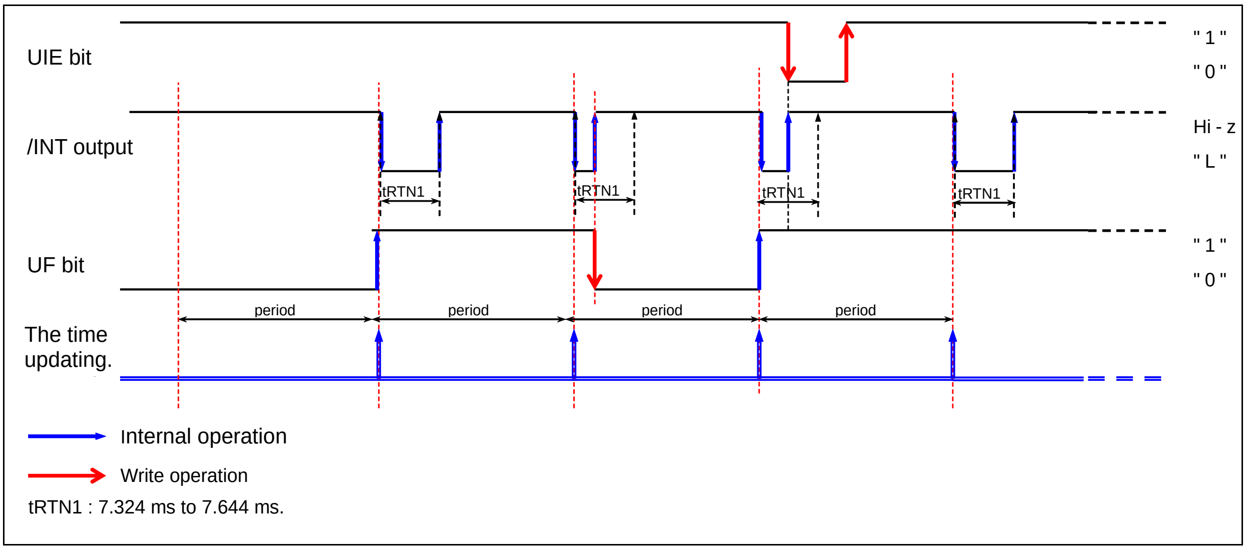


Figure 28 Time Update Interruption Timing Chart

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14.5. Status Monitoring Function

It is a flag bit that detects the state of this product and holds the result. 3 kinds of status changes.
- Power ON Reset
- VLF bit is set
- XST bit is set.

14.5.1. Related Registers For Status Monitoring.

Table 38 RTC Status Monitor Register

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Bank1 - E	Flag Register	**POR**	**z**	UF	TF	AF	EVF	**VLF**	**XST**

1) POR bit

Detects Power-on Reset (POR) occurred.

Table 39 POR bit (Power ON Reset)

POR	Data	Description
Write	0	Clear for next detection.
	1	Ignored.
Read	0	POR was not detected.
	1	POR was detected. (The result is retained until this bit is cleared to zero.) The default value of the register is set by power-on reset.

2) VLF bit

VLF are set from POR or XST.

Table 40 VLF bit (Voltage Low Flag)

VLF	Data	Description
Write	0	Clear for the next detection.
	1	Ignored
Read	0	VLF was not detected.
	1	POR or XST was detected. (The result is retained until this bit is cleared to zero.) It is used for judgment of initialization of an RTC.

3) XST bit

When an oscillation of crystal is stopped, it is set.

Table 41 XST bit (Crystal Oscillation Stop)

XST	Data	Description
Write	0	Clear for the next detection.
	1	Ignored.
Read	0	XST was not detected.
	1	Crystal oscillation stop was detected. (The result is retained until this bit is cleared to zero.)

This bit is not initialized in power-on reset.

14.6. FOUT Function [Clock Output Function]

The clock signal can be output via the FOUT pin. Output is stopped upon detection of the voltage drop below When the output of an FOUT terminal was stopped, a FOUT shifts to Hi-z

14.6.1. FOUT Control Register

Table 42 FOUT Register (Frequency OUT)

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Bank1 - D	Extension Register	**FSEL1**	**FSEL0**	USEL	TE	WADA	▲	TSEL1	TSEL0

14.6.2. FOUT Function Table

1) FSEL1, FSEL0 bit

Table 43 FSEL Register (Frequency Select)

FSEL1	FSEL0	TMPIN	Output
0	0	x	32768 Hz Output
0	1	0	1024 Hz Output
1	0		1 Hz Output
1	1	x	OFF

x: don't care

Timer interrupt output can be assigned to the FOUT pin, so when using frequency output, set TMPIN = 0 and set the timer interrupt to the /INT pin.
At the time of the initial power-on, 0 is set to FSEL1, FSEL0.

Note: effect of STOP bit to FOUT functions.
When STOP = 1, 32768 Hz and 1024 Hz output is possible. But 1 Hz output is disabled.

14.7. Battery Backup Switchover Function

14.7.1. Description of Battery Backup Switchover Function

This function can detect voltage drop of V_{DD} and switchover power supply from V_{DD} to V_{BAT}. This function circuit comprises the comparator detector "VDET" which detect the power down of the main power source "V_{DD}", and built-in MOS switch (SW) and a diode located between the main power-source pin "V_{DD}" and the backup power supply pin "V_{BAT}". Refer to Figure 28.
By switching SW according to the result of the supply-voltage detection of V_{DET1}, the RTC power supply is changed from V_{DD}. Also, the diode protects reverse current from V_{BAT} to V_{DD}.

There are two modes depend on power supply status.
1) Normal mode: RTC power supply from V_{DD}
2) Backup mode: RTC power supply from V_{BAT}

During backup mode, FOUT becomes Hi-Z status, SPI-Bus is inactive, signal lines are floating.
When the VLF bit detects 0 → 1, the default value of backup battery switchover function related registers is set.

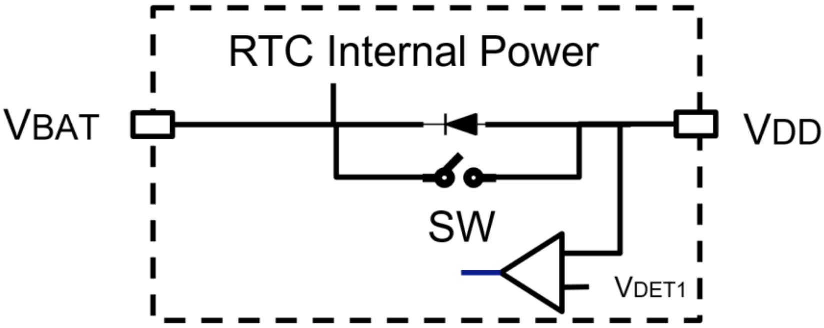


Figure 29 Battery Backup Switchover Function Block Diagram

14.7.2. Related Register of Battery Backup Switchover Function

Table 44 Battery backup switchover function related register

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Bank3 - 2	Power Switch Control	▲	INIEN	z	z	SWSEL1	SWSEL0	SMPT1	SMPT0

1) INIEN bit
Control of MOS-Switchover function ON/OFF.

Table 45 INIEN bit (Initial Enable)

INIEN	Data	Description
Write / Read	0	MOS switchover control function: OFF Default setting.
	1	MOS switchover control function: ON If V_{DD} voltage drop is detected SPI-Bus communication is switched OFF and signals are floating.

2) SW status

Table 46 SW status

State	SW	Description
Power supplied from V_{BAT} first then V_{DD} supply	OFF	Power supplied diode OR of V_{DD} and V_{BAT}.
Power supplied from V_{DD} first then V_{BAT} supply	OFF	Power supplied from V_{DD} via diode first then Power supplied diode OR of V_{DD} and V_{BAT}.
Battery backup switchover function: ON INIEN bit = 1	ON	V_{DD} = ON: Normal mode
	OFF	V_{DD} = OFF: Backup mode

3) SWSEL1, SWSEL0 bit

When user set INIEN to 0, it is locked status of a built-in MOS switch

Table 47 INIEN, SWSEL combination

INIEN	SWSEL1	SWSEL0	SW	SPI disable control	comment
0	0	1	OFF	OFF	Default
	1	0	ON	OFF	Battery backup switchover function: OFF
	0	0	OFF	OFF	Do not select this combination
	1	1	OFF	OFF	Do not select this combination
1	1	1	OFF	ON	SPI-Bus interface: ON
	Other than (1,1)		Auto control	ON	Battery backup switchover function: ON

When using a non-re-chargeable battery, it is necessary to install a charge protection diode externally.

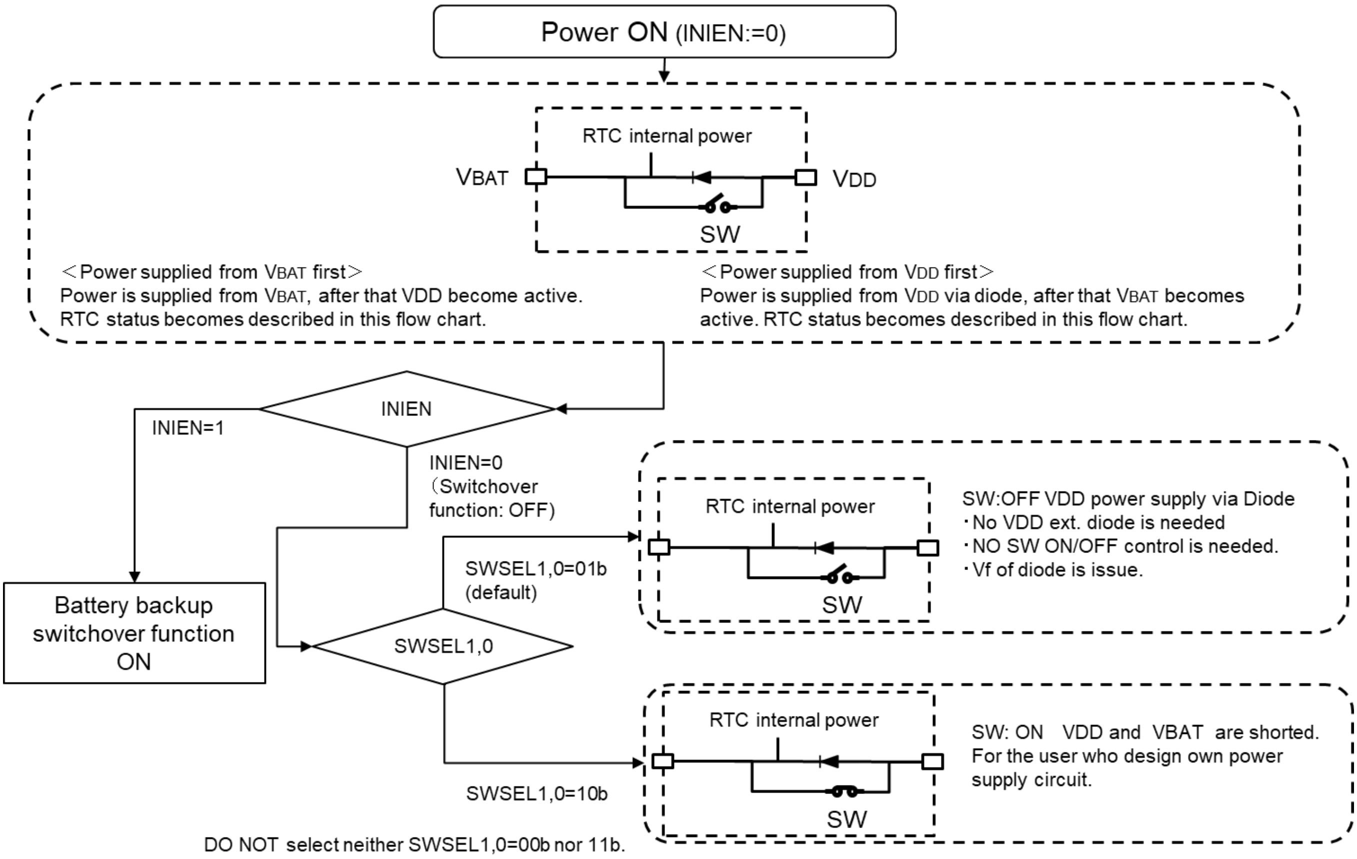


Figure 30 Battery backup switchover control (Initial power on)

Voltage detection intermittent timing

Table 48 The timing of VDET1

Power supply	V_{DD} (INIEN=1)	V_{DD} (INIEN=0)	V_{BAT} (Backup mode)
V_{DET1} detection	Always ON	Stopped	Once per 31.25 ms

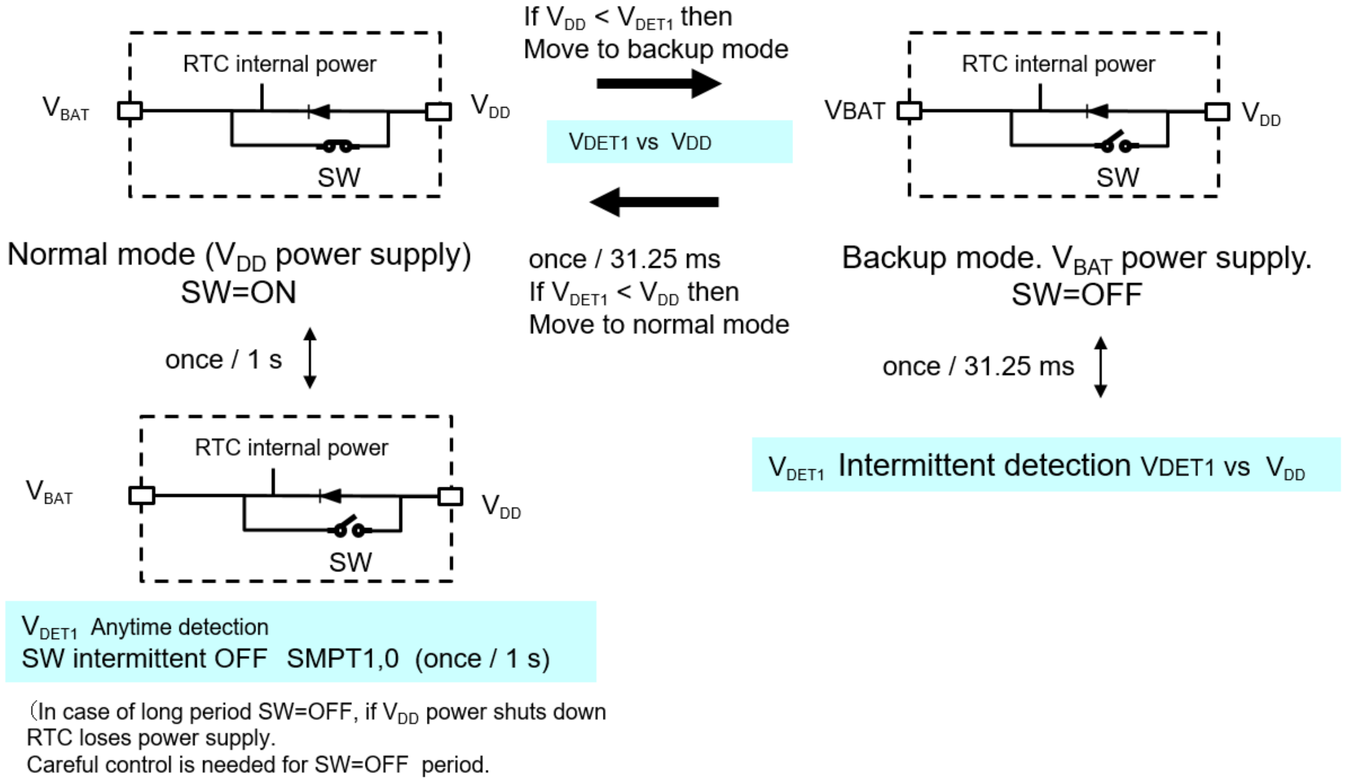


Figure 31 Battery backup switchover control (INIEN:1)

4) SMPT1, SMPT0 bit

7) V_{DD} voltage detection register SMPT1, SMPT0 bit Battery switchover functions managed by V_{DD} voltage low detection ($-V_{DET1}$).
This detection is checking voltage anytime with setting SW1(V_{DD}- ~ V_{BAT}) ON/OFF intermittently.
These two bits control SW1 OFF period and user can check much precision voltage by preventing reverse current from V_{BAT} to V_{DD} when main V_{DD} shuts down.
V_{DD} voltage low detection ($-V_{DET1}$) is active anytime, so lower voltage detection moves RTC into backup mode immediately regardless SW1 OFF time.
These SW1 OFF occur every second.

Refer to Figure 31

Table 49 SMPT bit (sample time)

SMPT1	SMPT 0	SW OFF time
0	0	Always ON
0	1	2 ms
1	0	128 ms
1	1	256 ms

Once per a Second.

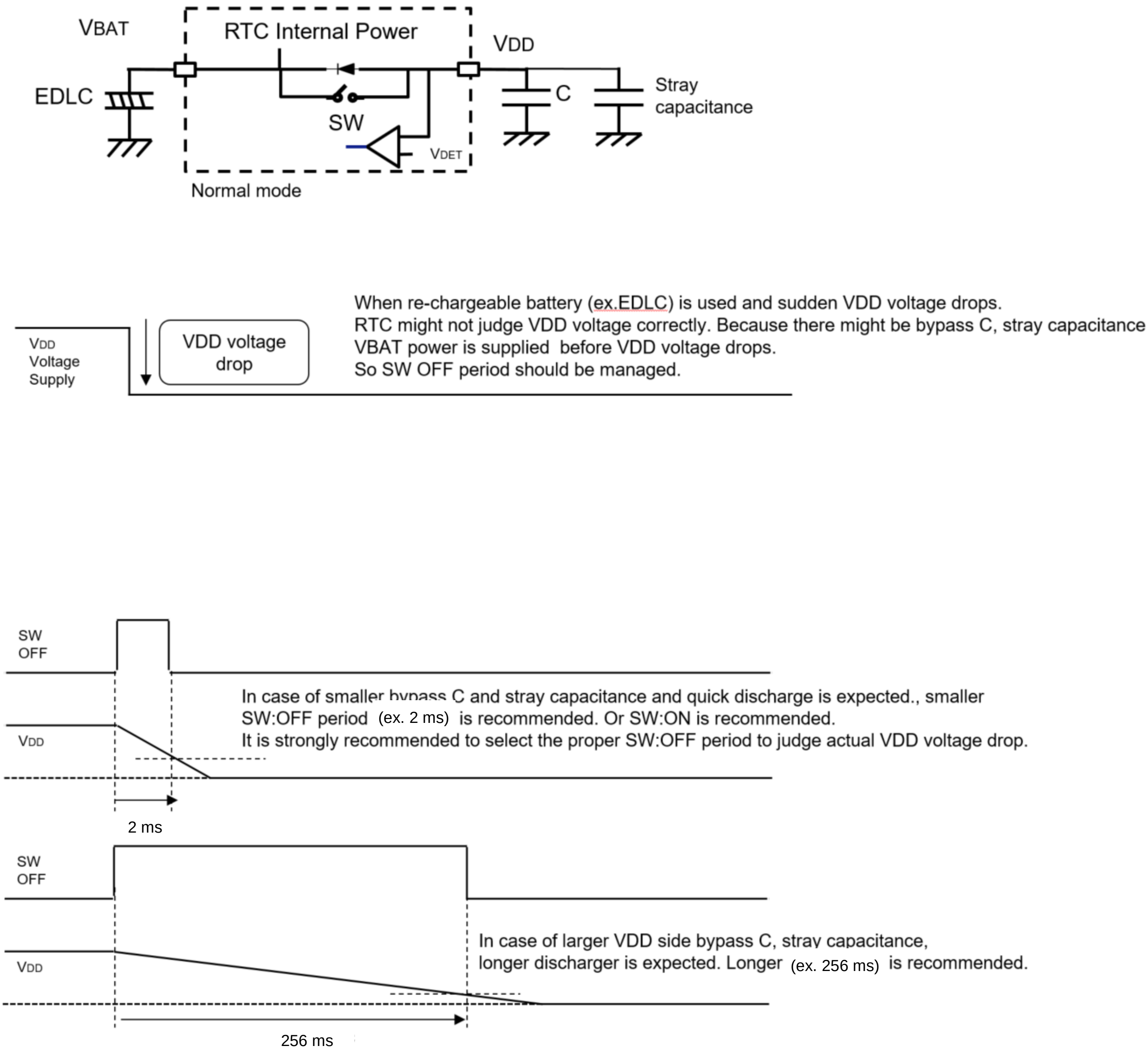


Figure 32 VDD voltage detection SW OFF intermittent operation

14.8. Time Stamp Function

14.8.1. Description Of Time Stamp Function

Time stamp function is executed by two kinds of event.

1) Command trigger of SPI-Bus communication by Bank2 Fh reading.
2) RTC self monitoring warning.

The time stamp records maximum 8-events. Also interrupt output is available with /INT pin. This time stamp function works even in backup mode and records time data from 1/256 s to year.

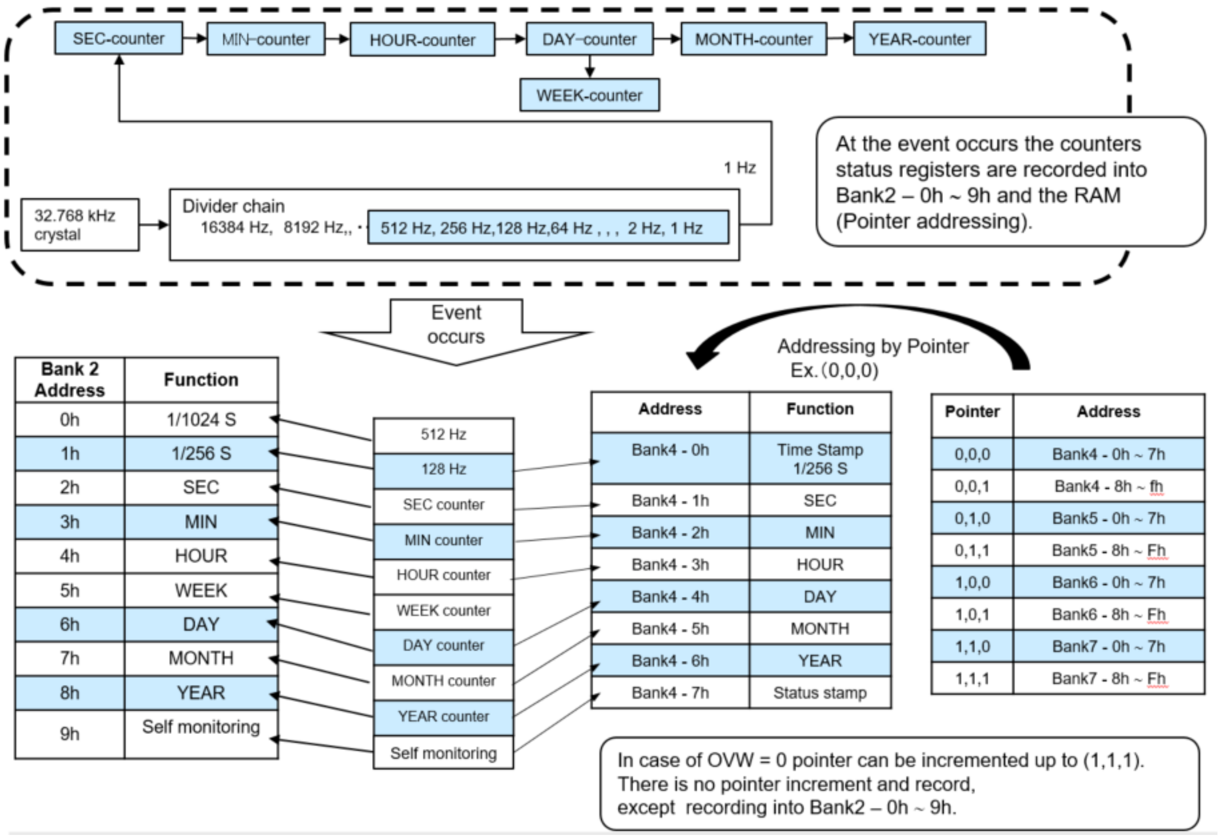


Figure 33 Time Stamp function

14.8.2. Related Registers For Time Stamp Functions.

Table 50 Time Stamp function registers

Address [h]	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Bank1- D	Extension Register	FSEL1	FSEL0	USEL	TE	WADA	▲	TSEL1	TSEL0
Bank1 E	Flag Register	POR	○	UF	TF	AF	**EVF**	VLF	XST
Bank1 F	Control Register	**z**	**z**	UIE	TIE	AIE	EIE	**z**	STOP
Bank2 B	Over Write Control	▲	No Function					OVW	-
Bank2-E	Time Stamp control 0	**z**	**z**	**z**	**z**	**z**	**z**	**z**	COMTG
Bank2-F	Command Trigger	**z**	**z**	**z**	**z**	**z**	**z**	**z**	**z**
Bank3- 4	Time Stamp Control 1	**z**	**z**	**z**	**z**	**z**	**EISEL**	**TSCLR**	**TSRAM**
Bank3-5	Time Stamp Control 2	●	**z**	**z**	**z**	▲	**EVDET**	▲	**EXST**
Bank3-6	Time Stamp Control 3	**z**	**z**	**z**	**TSFUL**	**TSEMP**	**TSAD2**	**TSAD1**	**TSAD0**

51) EVF bit (Event Flag)

When event occurs, a Time stamp is performed, and EVF is set.

Table 51 EVF bit (Event Flag)

EVF	Data	Description
Write	0	When /INT is outputting Low, it is canceled. It is released to Hi-Z.
	1	Ignored
Read	0	Specified interrupt events are not detected.
	1	Event occasion is detected. (The result is retained until this bit is cleared to zero.)

Note: EVF is not set by SPI-Bus command trigger

2) EIE bit (Event Interrupt Enable)

Control of /INT interrupt output when an event occurs (EVF, " 0 " → " 1 ") .

Table 52 EIE bit (Event Interrupt Enable)

EIE	Data	Description
Write	0	1) When an event interrupt event occurs, an interrupt signal is not generated (/INT status remains Hi-z) 2) When an event interrupt event occurs, the interrupt signal is canceled. (/INT status changes from low to Hi-z)
	1	When an event interrupt occurs, an interrupt signal is generated (/INT status changes from Hi-z to low)

3) OVW bit (Over Write)

Control of overwriting of Time stamp record

Table 53 OVW bit (Over Write)

OVW	Data	Description
Write	0	The recording is stopped with 8-time stamps, and it is not overwritten.
	1	Overwrite available

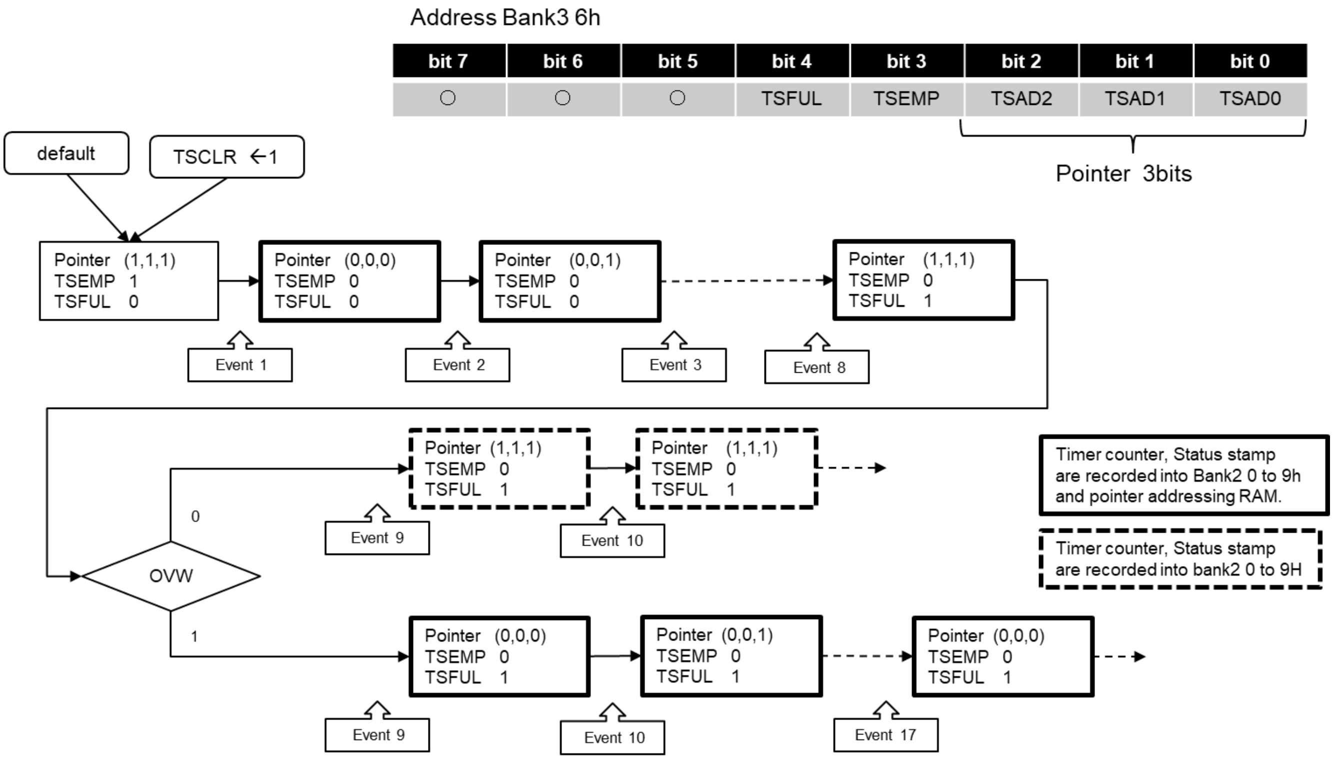


Figure 34 OVW, pointer operation

14.8.3. Time Stamp function triggered by SPI Access

1) COMTG bit (Command Trigger) Time stamp by SPI-Bus access.
Note: EVF is not set by SPI-Bus command trigger. Therefore, Time stamp interruption doesn't occur.
This function was prepared for to read time data of sub seconds from Year without contradiction.

Table 54 COMTG bit (Command Trigger)

COMTG	Data	Description
Write	0	Time stamp by SPI-Bus is disabled.
	1	Time stamp by SPI-Bus available When a reading command to Bank2 address Fh is transmitted by SPI-Bus, the time is recorded by Bank2 address 0h to 9h. The read value of Bank2 address Fh is 0h.

2) Time stamp Timing

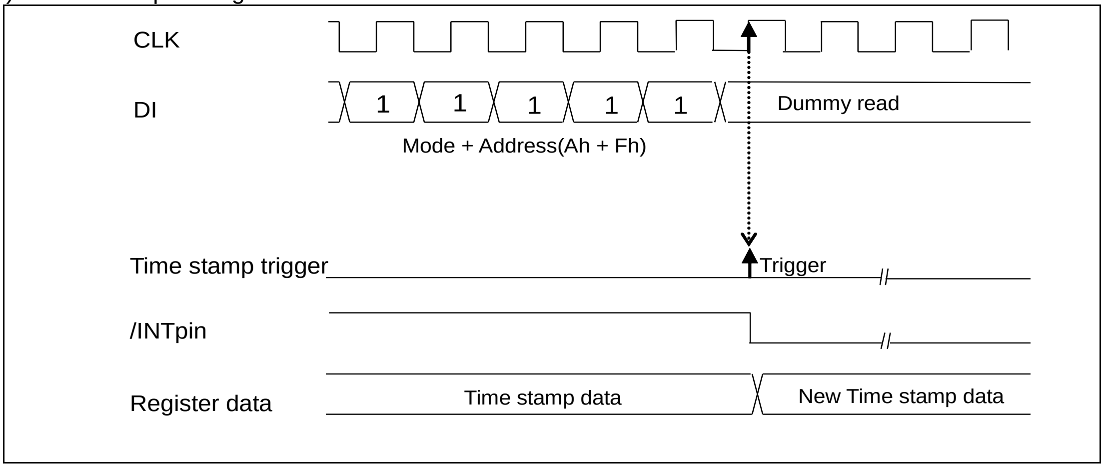
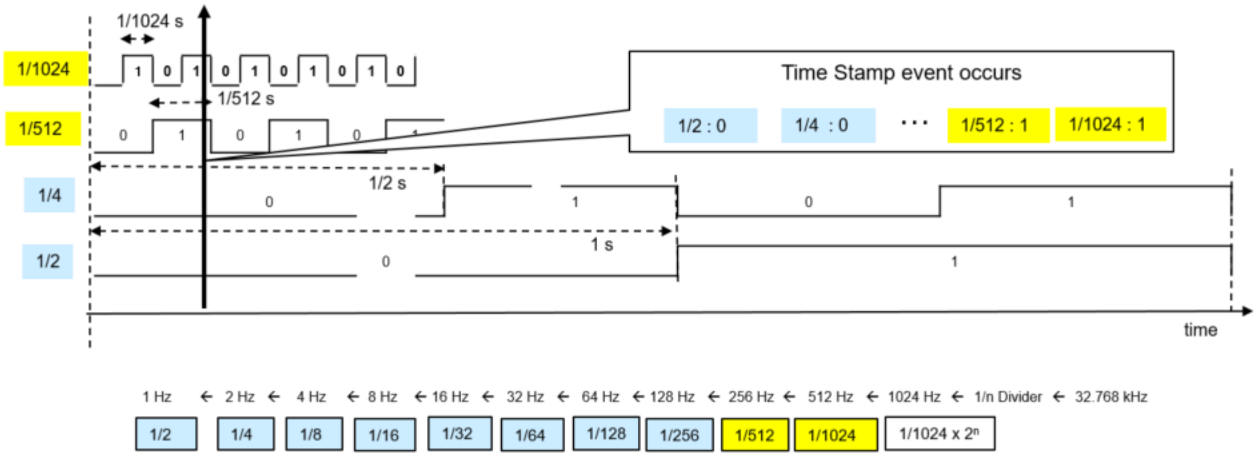


Figure 35 Time Stamp SPI-Bus record timing

14.8.4. Time Stamp Record Register.

When an event is detected, the following data is recorded .
Multiple access time stamp data is available. Refer to Figure 33.



address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Bnak2 0h	--	--	--	--	--	--	1/512	1/1024
Bank2 1h	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Pointer addressing	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

Figure 36 Time stamp recording registers

Table 55 Time Stamp Record Register

Bank2 Address	Function	Time stamp data
0h	Time Stamp 1/1024S	256Hz,512Hz.
1h	Time Stamp 1/128S	1Hz~256Hz
2h	Time Stamp SEC	Seconds
3h	Time Stamp MIN	Minutes
4h	Time Stamp HOUR	Hours
5h	Time Stamp WEEK	Day
6h	Time Stamp DAY	Date
7h	Time Stamp MONTH	Month
8h	Time Stamp YEAR	Years
9h	Status Stamp	RTC Internal status (VDET, XST)

Status stamp register

Table 56 Status Stamp

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Bank2 – 9h	Status Stamp	z	z	•	•	VDET	z	XST	z

Table 57 Time Stamp RAM control registers

Bank3 Address [h]	Function	bit 7	bit 6		bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4	Time Stamp Control 1	z	z		z	z	z	EISEL	TSCLR	TSRAM
5	Time Stamp Control 2	•	z		z	z	▲	EVDET	▲	EXST
6	Time Stamp Control 3	z	z		z	TSFUL	TSEMP	TSDA2	TSDA1	TSDA0

14.8.5. RTC Self Monitoring Time stamp Function

1) VDET bit (Time Stamp VDET)
Comparison result of V_{DD} and V_{DET1}

Table 58 VDET bit (VDET)

VDET	Data	Description
Read	0	$V_{DD} > V_{DET1}$, Normal mode (V_{DD} supply)
	1	$V_{DD} < V_{DET1}$, Backup mode (V_{BAT} supply)

2) XST bit (Time stamp Crystal Oscillation Stop)
Status record of crystal oscillation

Table 59 XST bit (Crystal Oscillation Stop)

XST	Data	Description
Read	0	Crystal oscillation is normal.
	1	Crystal oscillation stopped or temporarily stopped. XST detects more than 10ms stopped.

The time stamp cannot be recorded at the moment of oscillation stop. It is recorded at the moment the oscillation restores.

3) EVDET bit (Enable VDET)
Enable/Disable control of time stamp VDET

Table 60 EDVET bit (Enable VDET)

EVDET	Data	Description
Write	0	No time stamp even VDET is detected.
	1	Time stamp by VDET detection.

4) EXST bit (Enable Time stamp Crystal Oscillation Stop)
Enable/Disable control of time stamp XST

Table 61 EXST bit

EXST	Data	Description
Read	0	No time stamp even Crystal oscillation stops.
	1	Time stamp by Crystal oscillation stop detection.

14.8.6. Time Stamp Record Register

When an event is detected, the following data is recorded.

Table 62 Time Stamp RAM control registers

Bank3 Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
4h	Time Stamp Control 1	z	z	z	z	z	EISEL	TSCLR	TSRAM
5h	Time Stamp Control 2	•	z	z	z	▲	EVDET	▲	EXST

6h	Time Stamp Control 3	z	z	z	TSFUL	TSEMP	TSDA2	TSDA1	TSDA0

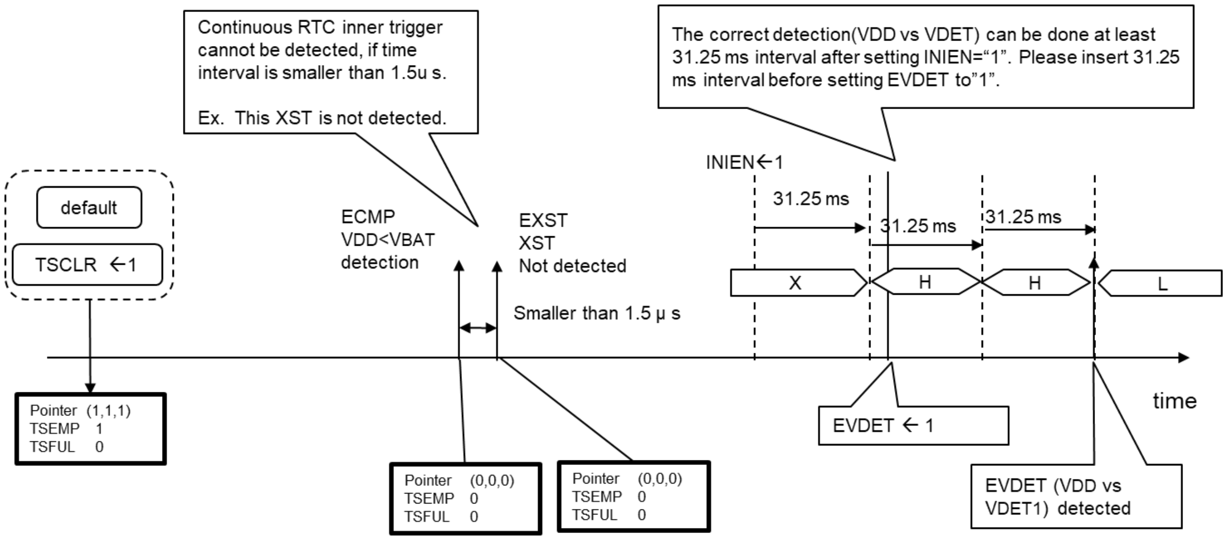


Figure 37 Careful timing process for VDET, XST time stamp

14.8.7. Multiple Time Stamp

By using following registers, user can record time stamp maximum 8-times.
Multiple timestamp related register
Multiple time stamp operation is possible by setting the following registers.
1/1024 seconds and WEEK information are not recorded in the recording area of Bank4 ~ Bank7.

1) TSRAM bit (Time Stamp RAM)
Selection of time stamp recording area or USER RAM.

Table 63 TSRAM bit (Time Stamp RAM)

TSRAM	Data	Description
Write	0	It can read and write as USER RAM. Time stamp data is recorded only at addresses Bank2 0h to 8h.
	1	Bank4 to Bank7 is used as the time stamp recording area. To clear the time stamp data, write 0 directly to the recording area by SPI-Bus access.

When TSRAM = 1, the first time stamp is recorded in both Bank2 0h ~ 8h and Bank4 0h ~ 7h.

	pointer	Address (h)	Bit7 ~ bit0
Time Stamp Events 3-times	0,0,0	Bank4 0~7h	Time stamp data 1
	0,0,1	Bank4 8~Fh	Time stamp data 2
	0,1,0	Bank5 0~Fh	Time stamp data 3
	0,1,1	Bank5 8~Fh	
	1,0,0	Bank6 0~7h	
	1,0,1	Bank6 8~Fh	
USER RAM 2bytes use	1,1,0	Bank7 0~Fh	Data xx
	1,1,1	Bank7 8~Fh	Data yy

Figure 38 Mixed usage of USER RAM and Time stamp RAM

2) TSCLR bit (Time Stamp Clear)
Initialization of Bank3 6h

Table 64 TSCLR bit

TSCLR	Data	Description
Write	0	No operation
	1	Initialize Bank3 6h. TSEMP: 1, TSFUL: 0, TSAD2,1,0: (1,1,1)

EISEL bit (Enable Interrupt Select)
Enable/Disable control of interrupt is output when 8-time stamp data becomes full.

Table 65 EISEL bit (Event Interrupt Select)

EISEL	Data	Description
Write	0	Each event makes interrupt output respectively from /INT.
	1	In case of 8-time stamp full recording, interrupt output from /INT.

Even SPI-Bus command trigger is executed, it makes no interrupt output.

1) TSFUL bit (Time Stamp Full)
8-time stamp data area full recording

Table 66 TSFUL bit

TSFUL	Data	Description
Read	0	Time stamp RAM area is not full.
	1	8 times of time stamp recording area is fully recorded.

2) TSEMP bit (Time Stamp Empty)
No recording date in RAM.

Table 67 Time Stamp Empty bit

TSEMP	Data	Description
Read	0	There is some data.
	1	There is no data.

TSAD2, TSAD1, TSAD0 bit (Time Stamp Address pointer)
The latest address pointer time stamped recorded in RAM

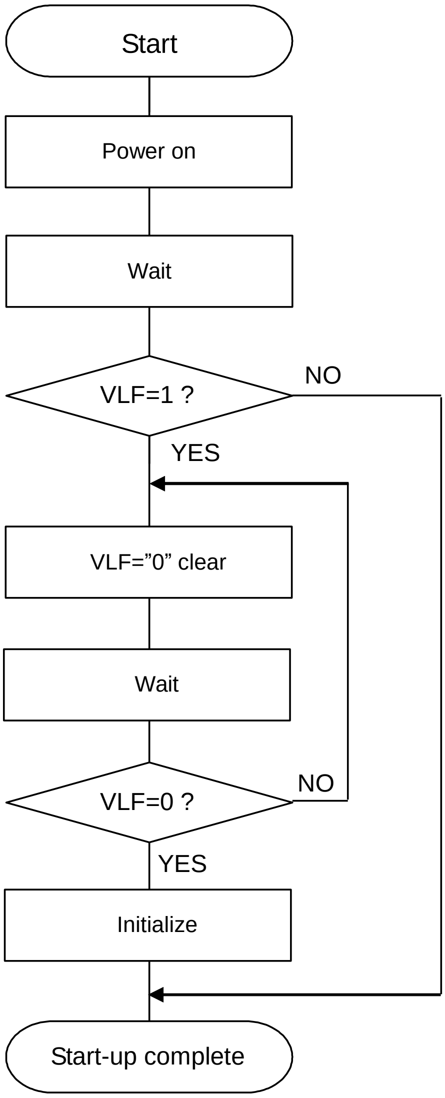
Table 68 TSAD bit

TSAD2, 1, 0	TSAD2	TSAD1	TSAD0	Address pointer
Read	0	0	0	Bank4 0h - 7h
	0	0	1	Bank4 8h - Fh
	0	1	0	Bank5 0h - 7h
	0	1	1	Bank5 8h - Fh
	1	0	0	Bank6 0h - 7h
	1	0	1	Bank6 8h - Fh
	1	1	0	Bank7 0h - 7h
	1	1	1	Bank7 8h - Fh, default

14.9. Flow Chart

The following flow-chart is one example, but it is not necessarily applicable for every use-case and not necessarily the most effective process for individual applications.

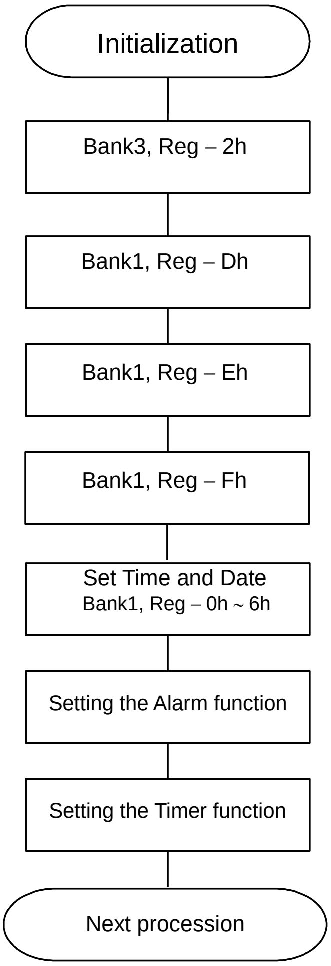
1) In Initial power on



- Wait time of 40 ms is necessary at least.
- Whether it is a return from the state of the backup is confirmed.
- VLF can not be cleared to "0" until internal oscillation starts.
- Please set waiting time depending on load of a system optionally.
  It takes about 200 ms from Power ON to oscillation start.

Figure 39 Flow1

2) Initialize



- Set the Battery backup switchover function.

- Set TE bit to "0".
- Set FSEL1, 0 bit optionally.

- Clear various flags to "0".
  * VLF and XST retain the state of "1" even if "0" is cleared until oscillation starts.

- Set AIE, TIE, UIE bit to "0 " to prevent unprepared interruption output.

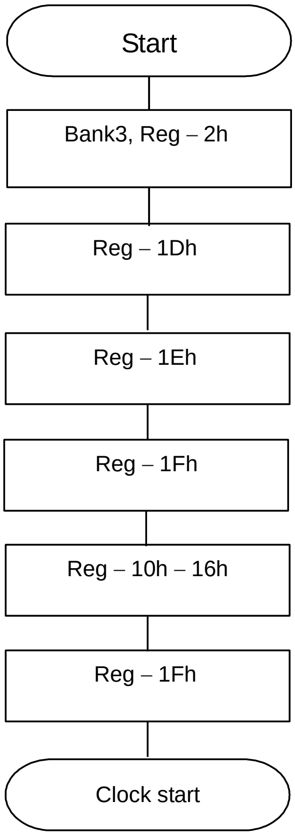
- Set the time and date.
  * Setting the present time concerned, please refer to item of [Clock and calendar writing] .

- Set the Alarm interrupt function.
  When the alarm interrupt function is not being used, the Alarm registers can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.
- Set the Wakeup Timer function.
  When the fixed-cycle timer function is not being used, the Timer Counter register can be used as a RAM register. In such cases, stop the fixed-cycle timer function by writing "0" to the TE and TIE bits.

* When initialization is finished, be sure to set STOP bit to "0".

Figure 40 Flow2

Example 2. Initialization example when using only clock function.

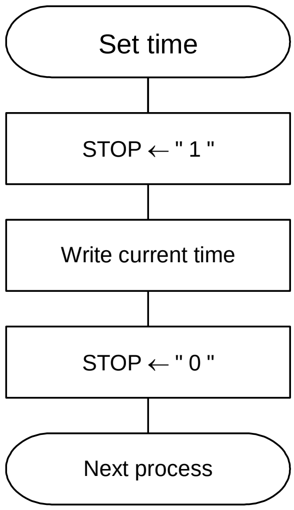


- Write value 04 h (when using primary battery)
- When using a capacitor or a rechargeable battery not requiring charge control Write 0C h. Adjust the setting of SMPTSEL1,0 when the power switching is difficult with the default values 00b.
- Write value 00 h
- Write value 00 h
  ∗State of VLF=1 is held even if it 0 clear until oscillation start.
  When initialize it without waiting for an oscillation start, Clear VLF bit after an oscillation
- Write value 00 h
  ∗ To use the STOP bit, set it to 01 h and stop counting until the time is set.
- Setting the current time
- Write 00h
  It is unnecessary when not using the STOP bit.

∗ When initialization is finished, be sure to set STOP bit to “0”.

Figure 41 Flow3

3) The setting of the clock and calendar



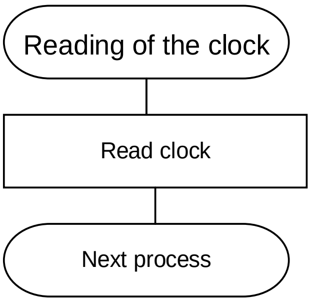
- Set STOP bit to “1” to prevent time update in time setting.
- Write information of [year / month /date [day of the week] hour: minute: second] which is necessary to set (or reset).
  In case of initialization, please initialize all data.
- Cancel STOP bit to “0” and start (restart) clock movement.
  Clock is started when set STOP bit to “0”.

∗ It is able to set time even if not combined use of STOP bit.
If do not use the STOP bit, RTC will start counting from the point of writing second. Even when batch writing is performed from [seconds] to [year], the counter below second will be reset by the acknowledge following [s], clocking will start from that point.

∗ When STOP = 1, please be aware that the functions such as the voltage detection function stop.

Figure 42 Flow4

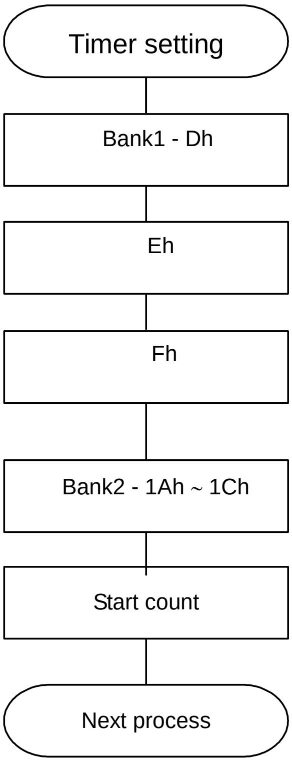
4) The reading of the clock and calendar



- Please complete access within 0.95 seconds
  The STOP bit holds "0".
  (It causes the clock delay to set STOP bit to "1")
- At the time of a communication start, the Clock & Calendar data are fixed (hold the carry operation), and it is automatically revised at the time of the communication end.
- The access to a clock calendar recommends to have access to continuation by a auto increment function.

Figure 43 Flow5

5) Setting example of the Wake-up timer interrupt function



- Clear TE bit to "0" to stop timer-interrupt function.
- The countdown period is fixed by the combination of the TSEL1, TSEL0 bit.
- Clear TF bit to "0" to cancel last timer interrupt output (/INT output).
- Set the / INT output at event occurrence by setting the TIE bit.
- Set initial value of down counter.
- Set TE bit to "1" to start timer interrupt function.
  When start timers interrupt function, please surely set/reset
  2) initial value of down counter in advance.

∗1 Countdown is suspended with TSTP, " 0 " → " 1 " and countdown is performed again with TSTP, " 1 " → " 0 "

∗2 When you want to restart from a pre-set value, please set a TE bit to "1" again after setting a TE bit to "0".

Figure 44 Flow6

6) Setting example of the Alarm interrupt function

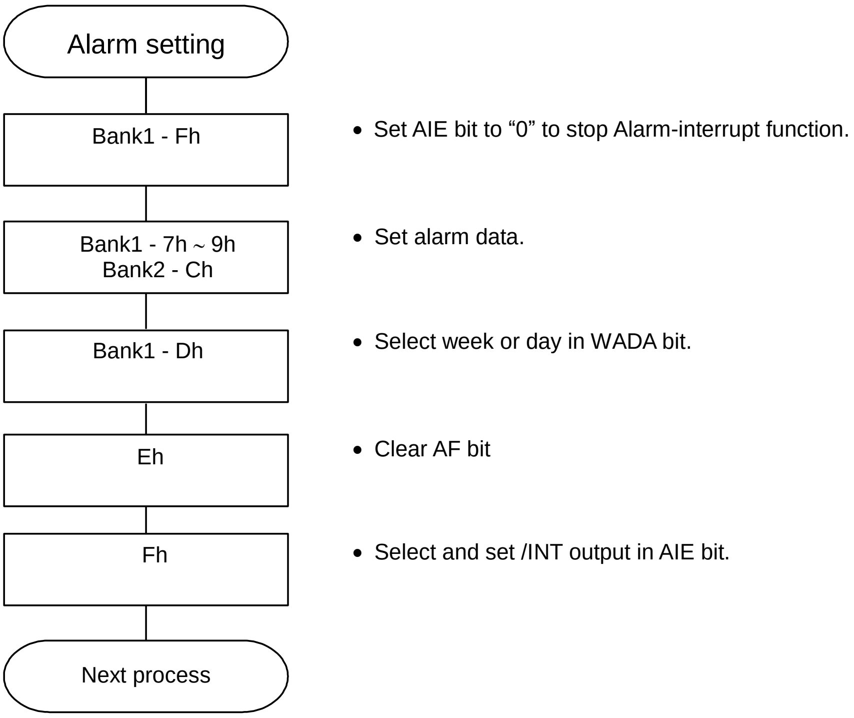
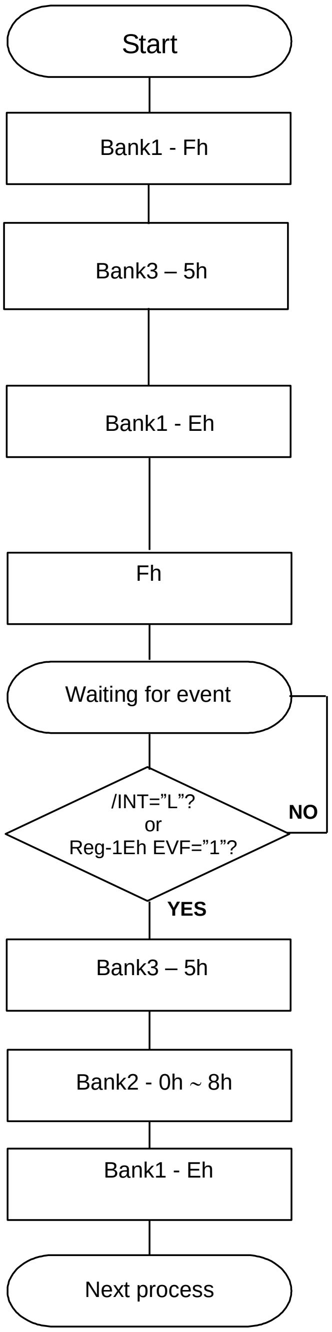


Figure 45 Flow7

7) One shot timestamp function setting example



- Clear EIE bit to 0.
- Set EVDET or EXST to 1.
- Clear EVF. to 0.
- Set EIE to 1.
- When an event occurs, the EVF bit changes to "1", and an interrupt occurs from the /INT pin.
- Clear EVDET and EXST to "0" to disable the time stamp function. Do not generate time stamps while reading time stamp data.
- Read the time stamp data.
- Clear EVF to "0".

Figure 46 Flow8

14.10. Reading/Writing Data via the SPI-Bus Interface

For both read and write, first set up chip condition (internally CE="H") to CE="H", then specify the 4-bits address, and finally read or write in 8-bits units. Both read and write use MSB-first. In continuous operation, objected address is auto incremented. Auto incrementing of the address is cyclic, so address "F" is followed by address 0.

14.10.1 Write / Read and Bank Select

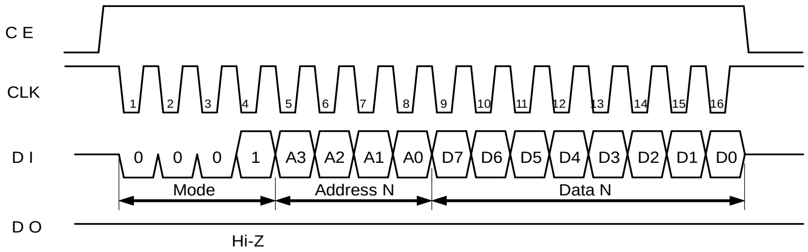
R/W and Register bank are specified by the four bits mode setting code.

Mode	Bank1	Bank2	Bank3	Bank6
Read	9h	Ah	Bh	Eh
Write	1h	2h	3h	6h

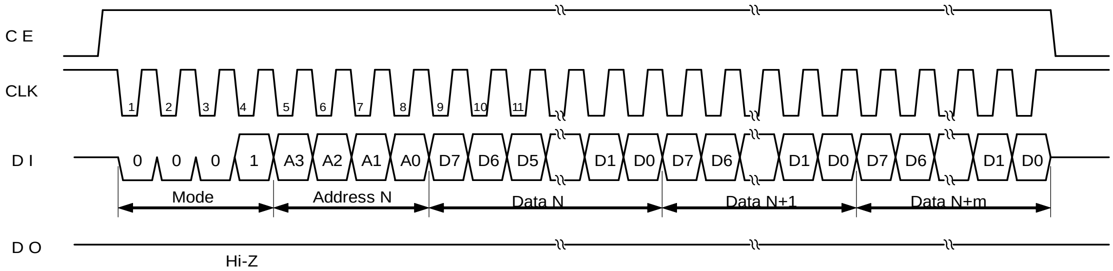
Bank5 and Bank6 are for software reset

14.10.2 Write of Data

1) One-shot writing



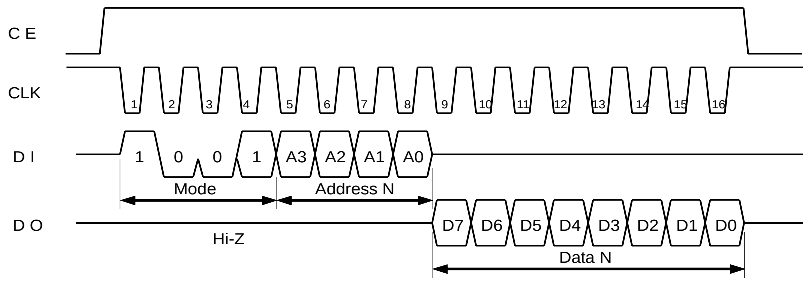
2) Continuous writing



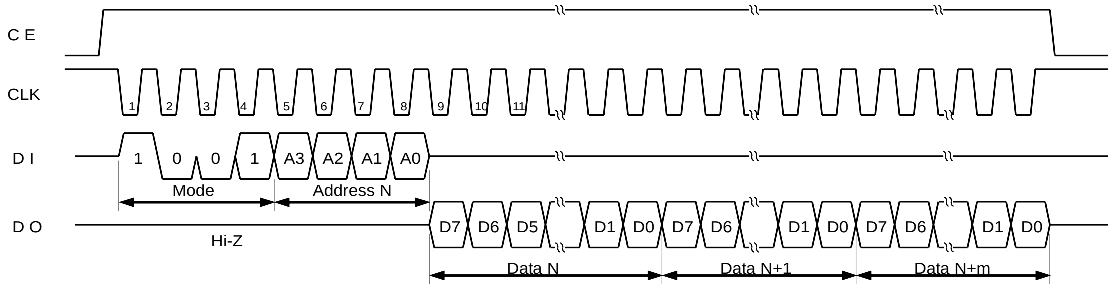
When writing data, the data needs to be entered in 8-bits units.
If the input of data in 8-bits unit is not completed before CE input falls, the 8-bits data will not be written properly at the time CE input falls.

14.10.3 Read of Data

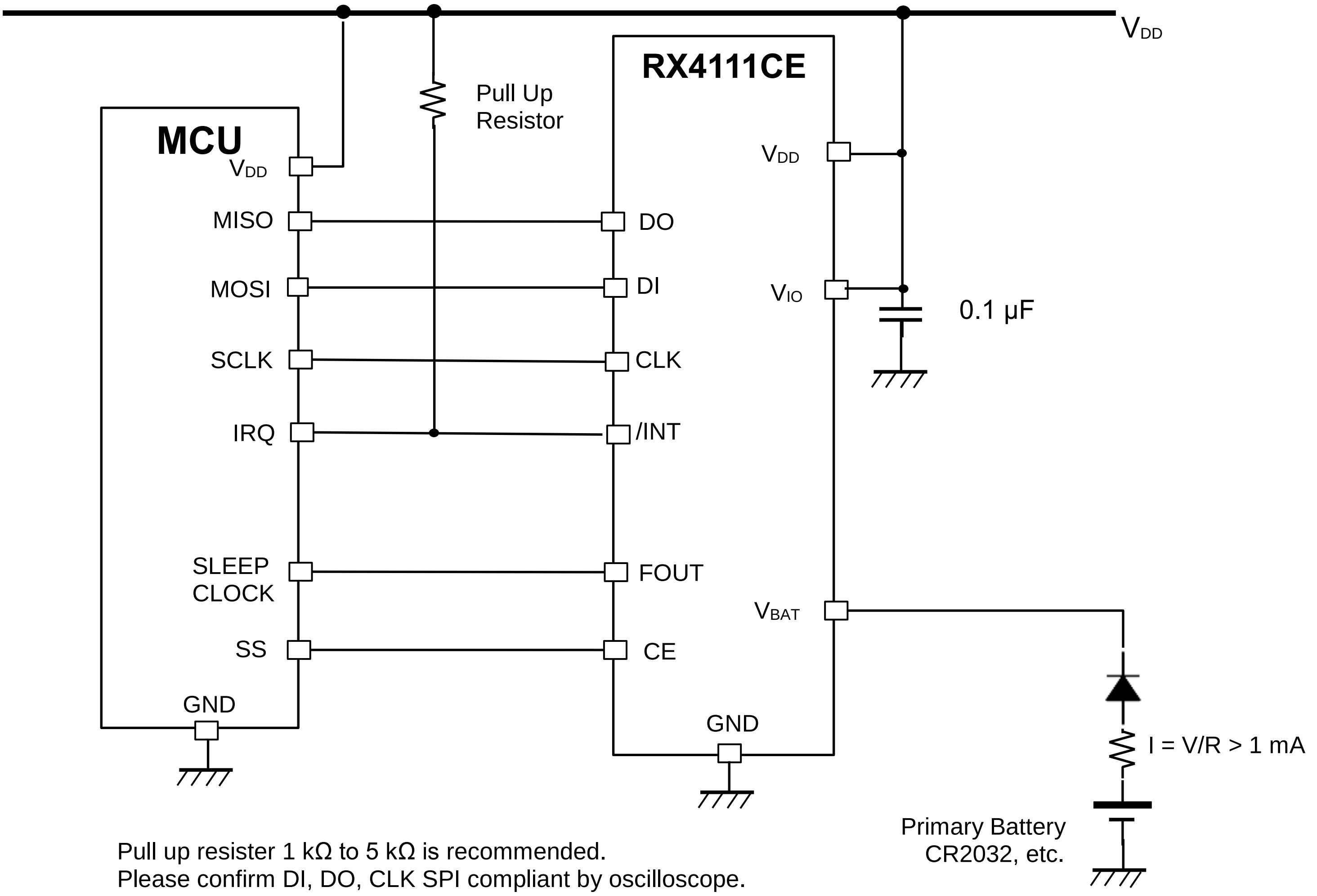
1) One-shot reading



2) Continuous reading



15. Connection example



Pull up resister 1 kΩ to 5 kΩ is recommended.
Please confirm DI, DO, CLK SPI compliant by oscilloscope.
Please set 0.1 µF bypass capacitor near RTC pin.

Figure 47 Typical MCU connection example

16.Tables

17.Figures

Application Manual
Real Time Clock Module
RX4111CE

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