Wireless LAN Module　MBH7WLZ16　Datasheet

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FUJITSU COMPONENT LIMITED

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1. Introduction

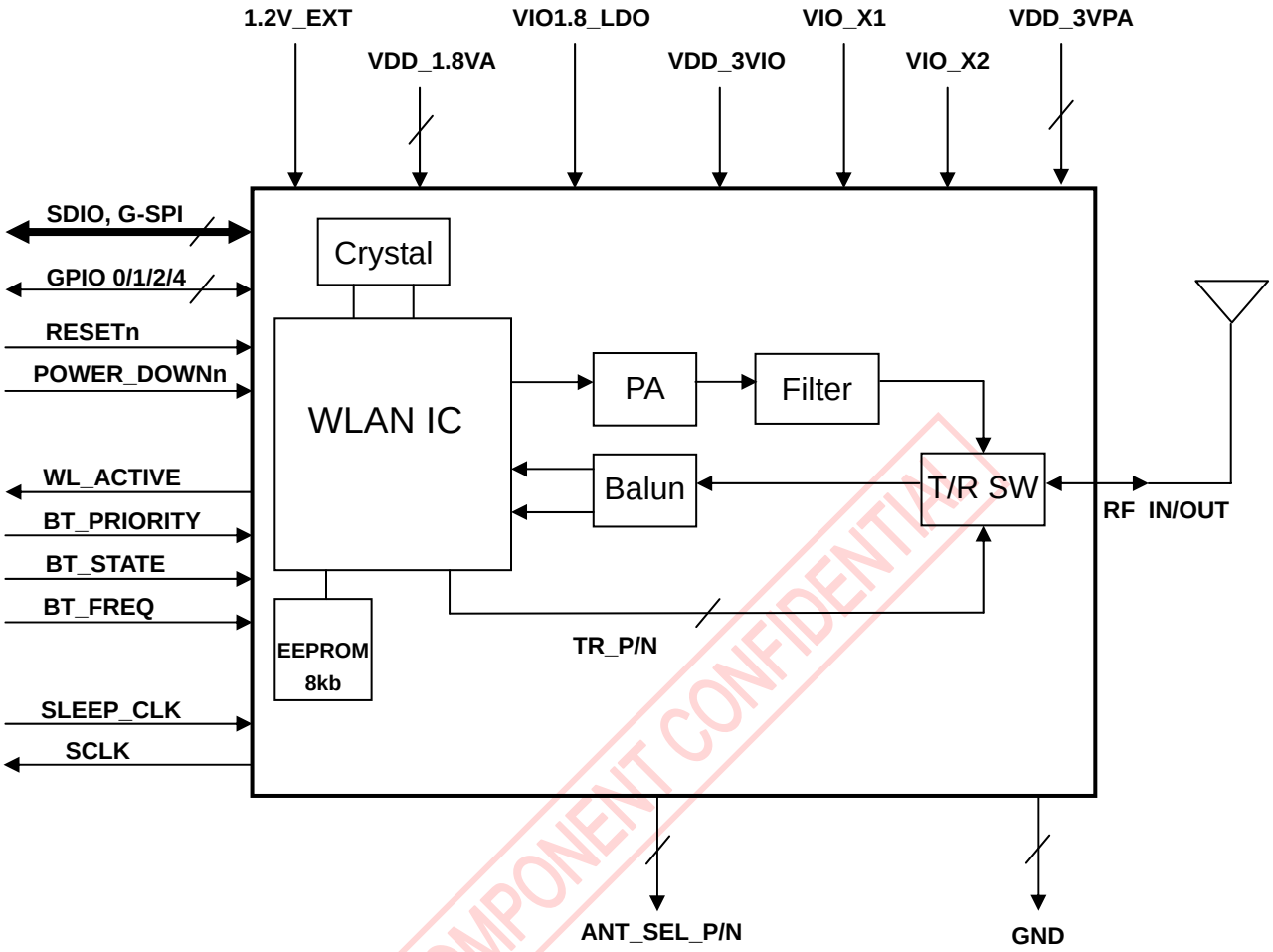
This document applies to the Wireless LAN module MBH7WLZ16.

2. Features

MBH7WLZ16 is a microminiaturized Wireless LAN module conforming to the IEEE standard 802.11/802.11b/802.11g, and transmits and receives in the 2.4 GHz ISM band.
MBH7WLZ16 has the following features:

- IEEE standard 802.11/802.11b/802.11g Compliant
- Frequency Range: 2400 – 2497 MHz
  (1 – 13 channel (IEEE802.11/11b/11g), 14 channel (IEEE802.11/11b) ISM band)
- Modulation Technique: Direct Sequence Spread Spectrum (CCK, DQPSK, DBPSK)
  Orthogonal Frequency Division Multiplexing (64QAM, 16QAM, DQPSK, DBPSK)
- Transmission Rate: 1 Mbps, 2 Mbps (802.11), 5.5 Mbps, 11 Mbps (802.11b)
  6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, 54 Mbps (802.11g)
- Host Interface: SDIO
  Generic SPI (G-SPI)
- Security: 64/128-bit WEP, WPA (TKIP), WPA2 (AES-CCMP)
- QoS (Quality of Service) support
- Bluetooth Coexistence support
- Surface mount, 60pin LGA type (Compatible with Pb-free solder processing)
- RoHS Compliant
- Miniaturized package: 8.5 x 8.5 x 1.2 mm
- Antenna port: Single Antenna port
- Built-in Crystal Oscillator
- Low power consumption

3. Block Diagram



4. Pin Description and Power

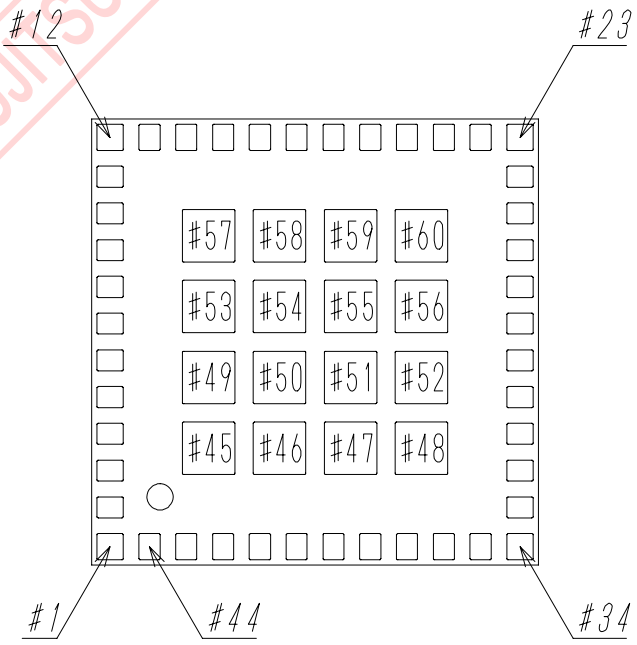
4-1. Pin Description

<table>
<tr><th>Name</th><th>No.</th><th>I/O</th><th>Description</th></tr>
<tr><td>SPI_SDI/
SD_CMD</td><td>18</td><td>I/O</td><td>G-SPI mode: G-SPI Data Input
SDIO 4-bit mode: Command/Response
SDIO 1-bit mode: Command Line
SDIO SPI mode: Data Input</td></tr>
<tr><td>SPI_CLK/
SD_CLK</td><td>19</td><td>I/O</td><td>G-SPI mode: G-SPI Clock Input
SDIO 4-bit mode: Clock Input
SDIO 1-bit mode: Clock Input
SDIO SPI mode: Clock Input</td></tr>
<tr><td>SPI_SCSn/
SD_DAT0</td><td>17</td><td>I/O</td><td>G-SPI mode: G-SPI Chip Select Input (active low)
SDIO 4-bit mode: Data Line Bit [0]
SDIO 1-bit mode: Data Line
SDIO SPI mode: Data Output</td></tr>
<tr><td>SPI_SDO/
SD_DAT1</td><td>16</td><td>I/O</td><td>G-SPI mode: G-SPI Data Output
SDIO 4-bit mode: Data Line Bit [1]
SDIO 1-bit mode: Interrupt
SDIO SPI mode: Reserved</td></tr>
<tr><td>SPI_SINTn/
SD_DAT2</td><td>15</td><td>I/O</td><td>G-SPI mode: G-SPI Interrupt Output (active low)
SDIO 4-bit mode: Data Line Bit [2] or Read Wait (optional)
SDIO 1-bit mode: Read Wait (optional)
SDIO SPI mode: Reserved</td></tr>
<tr><td>SD_DAT3</td><td>14</td><td>I/O</td><td>SDIO 4-bit mode: Data Line Bit [3]
SDIO 1-bit mode: Reserved
SDIO SPI mode: Card Select (active low)</td></tr>
<tr><td>GPIO[0]/
SLEEPn</td><td>11</td><td>I/O</td><td rowspan="4">General Purpose Input/Output (Internal pull-up)
These pins are asynchronous to internal clocks. Several of these pins can be selected to perform alternate functions such as an LED controller.
When not used, these pins should be left floating.
Notes:
• GPIO[0]: SLEEPn. This pin drives low during power down sleep mode.
• GPIO[1]: LED output (strap pin). Transmit power or receive ready LED.
• GPIO[4]: WLAN MAC wake-up input / Interrupt input</td></tr>
<tr><td>GPIO[1]/
LED</td><td>21</td><td>I/O</td></tr>
<tr><td>GPIO[2]</td><td>39</td><td>I/O</td></tr>
<tr><td>GPIO[4]/
Module_wake_up</td><td>20</td><td>I/O</td></tr>
<tr><td>WL_ACTIVE</td><td>40</td><td>O</td><td>Bluetooth WLAN Active
2-Wire BCA Mode:
When high, WLAN is transmitting or receiving packets.
3-Wire BCA Mode:
0 = Bluetooth device allowed to transmit
1 = Bluetooth device not allowed to transmit
This pin drives low when POWER_DOWNn is asserted.
In WLAN Sleep mode, all I/O PADs are powered down. This pad must stay at a low state even in power down mode.</td></tr>
<tr><td>BT_PRIORITY</td><td>42</td><td>I</td><td>Bluetooth Priority
2-Wire BCA Mode:
When high, Bluetooth is transmitting or receiving high priority packets.
3-Wire BCA Mode:
When high, Bluetooth is transmitting or receiving packets.</td></tr>
<tr><td>BT_STATE</td><td>41</td><td>I</td><td>Bluetooth State
0 = normal priority, Rx
1 = high priority, Tx
Priority is signaled after BT_PRIORITY has been asserted. After priority signaling, BT_STATE indicates the Tx/Rx mode of Bluetooth radio.</td></tr>
<tr><td>BT_FREQ</td><td>43</td><td>I</td><td>4-Wire BCA Mode:
Bluetooth Frequency
Asserted (logic high) when the Bluetooth transceiver hops into the restricted channels defined by the coexistence mechanism.
2-Wire, 3-Wire BCA Mode:
Tied to ground (GND)</td></tr>
<tr><td>ANT_SEL_P</td><td>37</td><td>O</td><td>Differential Antenna Select Positive Output
Provides the antenna select positive control signal.
Default value is 1.
Also used as RF switch control for single Bluetooth/WLAN antenna configurations.
<table>
<tr><th>ANT_SEL_N</th><th>ANT_SEL_P</th><th>For antenna diversity</th><th>For single BT/WLAN antenna</th></tr>
<tr><td>0</td><td>0</td><td>---</td><td>---</td></tr>
<tr><td>0</td><td>1</td><td>Antenna 1</td><td>Bluetooth</td></tr>
<tr><td>1</td><td>0</td><td>Antenna 0</td><td>WLAN</td></tr>
<tr><td>1</td><td>1</td><td>---</td><td>---</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>ANT_SEL_N</td><td>36</td><td>O</td><td>Differential Antenna Select Negative Output
Provides the antenna select negative control signal.
Default value is 0.
Also used as RF switch control for single Bluetooth/WLAN antenna configurations.
<table>
<tr><th>ANT_SEL_N</th><th>ANT_SEL_P</th><th>For antenna diversity</th><th>For single BT/WLAN antenna</th></tr>
<tr><td>0</td><td>0</td><td>---</td><td>---</td></tr>
<tr><td>0</td><td>1</td><td>Antenna 1</td><td>Bluetooth</td></tr>
<tr><td>1</td><td>0</td><td>Antenna 0</td><td>WLAN</td></tr>
<tr><td>1</td><td>1</td><td>---</td><td>---</td></tr>
</table></td></tr>
<tr><td>RESETn</td><td>8</td><td>I</td><td>Reset (active low, Internal pull-up)</td></tr>
<tr><td>POWER_DOWNn</td><td>7</td><td>I</td><td>Full power down (active low, Internal pull-up)
0 = full power down mode
1 = normal mode
Connect to power down pin of host or 1.8V.</td></tr>
<tr><td>SLEEP_CLK</td><td>9</td><td>I</td><td>Clock Input for External Sleep Clock
NOTE: SLEEP_CLK is used by the WLAN and Bluetooth MAC. The input clock frequency is typically 32 kHz/32.768 kHz/3.2 kHz. The Bluetooth radio chip supply 3.2 kHz. The WLAN requires 32 kHz.</td></tr>
<tr><td>SCLK</td><td>24</td><td>O</td><td>Serial Interface Clock (Internal pull-up)
Serial interface clock output for power management device programming interface control.</td></tr>
<tr><td>RF_IN/OUT</td><td>3</td><td>RF</td><td>Antenna port, 50Ω</td></tr>
<tr><td>1.2V_EXT</td><td>22</td><td>Power</td><td>1.2V Digital Power Supply</td></tr>
<tr><td>VDD_1.8VA_1</td><td>5</td><td>Power</td><td>1.8V Analog Power Supply</td></tr>
<tr><td>VDD_1.8VA_2</td><td>6</td><td>Power</td><td>1.8V Analog Power Supply</td></tr>
<tr><td>VIO1.8_LDO</td><td>29</td><td>Power</td><td>1.8V Digital I/O and Internal Voltage Regulator Power Supply</td></tr>
<tr><td>VDD_3VIO</td><td>27</td><td>Power</td><td>3.0V Digital I/O Power Supply</td></tr>
<tr><td>VIO_X1</td><td>13</td><td>Power</td><td>1.8V/3.3V Host Supply</td></tr>
<tr><td>VIO_X2</td><td>26</td><td>Power</td><td>1.8V/3.3V Digital Power Supply</td></tr>
<tr><td>VDD_3VPA_1</td><td>32</td><td>Power</td><td>3.0V Power Supply for PA</td></tr>
<tr><td>VDD_3VPA_2</td><td>31</td><td>Power</td><td>3.0V Power Supply for PA</td></tr>
<tr><td>GND</td><td>1,2,4,10, 12,23,25,28, 30,33,34,35 38,44,45,46, 47,48,49,50, 51,52,53,54, 55,56,57,58, 59,60</td><td>Ground</td><td>Ground</td></tr>
</table>

I/O Type:

I: Digital Input, O: Digital Output, I/O: Digital Input/Output



Pin Assignment (Bottom View)

4-2. Power

MBH7WLZ16 requires the following supply voltages:

- **1.2V_EXT** — 1.2V Digital Core Power Supply (1.2V Supply can be derived from the Internal Voltage Regulator.)
- **VDD_1.8VA_1, VDD_1.8VA_2** — 1.8V Analog Power Supply
- **VIO1.8_LDO** — 1.8V Digital I/O and Internal Voltage Regulator Power Supply
- **VIO_X1** — 1.8V/3.3V Host Power Supply
- **VIO_X2** — 1.8V/3.3V Digital Power Supply
- **VDD_3VIO** — 3.0V Digital I/O Power Supply
- **VDD_3VPA_1, VDD_3VPA_2** — 3.0V PA Power Supply

The following table lists the pins operating from each voltage supply.

No.	Name	No.	Name	No.	Name	No.	Name
VIO_X1		**VIO_X2**		**VDD_3VIO**		**VIO1.8_LDO**	
7	POWER_DOWNn	24	SCLK	36	ANT_SEL_N	40	WL_ACTIVE
8	RESETn			37	ANT_SEL_P	41	BT_STATE
9	SLEEP_CLK					42	BT_PRIORITY
11	GPIO[0]/SLEEPn					43	BT_FREQ
14	SD_DAT3						
15	SPI_SINTn/SD_DAT2						
16	SPI_SDO/SD_DAT1						
17	SPI_SCSn/SD_DAT0						
18	SPI_SDI/SD_CMD						
19	SPI_CLK/SD_CLK						
20	GPIO[4]/Module_wake_up						
21	GPIO[1]/LED						
39	GPIO[2]						

5. Electrical Characteristics

5-1. General Specification

Network Standard	IEEE standard 802.11/802.11b/802.11g Compliant
Interface	Secure Digital Input/Output (SDIO) Generic SPI (G-SPI)
Frequency Band	2400 ~ 2497 MHz (ISM band) (IEEE802.11b: Channel 1 ~ 14, IEEE802.11g: Channel 1 ~ 13)
Data Transfer Mode	Direct Sequence Spread Spectrum (DSSS) Orthogonal Frequency Division Multiplexing (OFDM)
Modulation Techniques	CCK (11 Mbps, 5.5 Mbps), DQPSK (2 Mbps), DBPSK (1 Mbps) OFDM-64QAM (54 Mbps, 48 Mbps), OFDM-16QAM (36 Mbps, 24 Mbps) OFDM-DQPSK (18 Mbps, 12 Mbps), OFDM-DBPSK (9 Mbps, 6 Mbps)
Media Access Protocol	CSMA/CA (Carrier Sense Multiple Access with Collision Avoidance)
Access Method	Ad-Hoc mode, Infrastructure mode

5-2. Absolute Maximum Rating

Symbol	Parameter	Min	Typ	Max	Unit
1.2V_EXT	Power Supply Voltage with respect to GND	---	1.2	1.35	V
VDD_1.8VA_1, VDD_1.8VA_2	Power Supply Voltage with respect to GND	---	1.8	2.3	V
VIO1.8_LDO	Power Supply Voltage with respect to GND	---	1.8	2.3	V
VDD_3VIO	Power Supply Voltage with respect to GND	---	3.0	3.5	V
VIO_X1	Power Supply Voltage with respect to GND	---	1.8	2.3	V
		---	3.3	4.2	V
VIO_X2	Power Supply Voltage with respect to GND	---	1.8	2.3	V
		---	3.3	4.2	V
VDD_3VPA_1, VDD_3VPA_2	Power Supply Voltage with respect to GND	---	3.3	5.0	V
$T_{STORAGE}$	Storage Temperature	-40	+25	+105	°C

5-3. Recommendable Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
1.2V_EXT	1.2V digital power supply	1.08	1.2	1.32	V
VDD_1.8VA_1, VDD_1.8VA_2	1.8V analog I/O power supply	1.7	1.8	1.9	V
VIO1.8_LDO	1.8V internal voltage regulator power supply	1.62	1.8	1.98	V
VDD_3VIO	3.0V digital I/O power supply	2.95	3.0	3.3	V
VIO_X1	Host interface digital I/O power supply	1.62	1.8	1.98	V
		2.97	3.3	3.63	V
VIO_X2	1.8V digital I/O power supply	1.62	1.8	1.98	V
		2.97	3.3	3.63	V
VDD_3VPA_1, VDD_3VPA_2	3.0V PA power supply	3.0	3.3	3.6	V
T_A	Ambient operating temperature	-20	+25	+70	°C

5-4. DC Electricals – Digital 3V Pads (VDD_3VIO)

Symbol	Parameter	Min	Typ	Max	Unit
V_{30}	Power supply voltage (VDD_3VIO)	2.95	3.0	3.3	V
V_{IH}	Input high voltage	2.0	---	V_{30}+0.3	V
V_{IL}	Input low voltage	-0.3	---	0.6	V
V_{HYS}	Input hysteresis	250	---	---	mV
V_{OH}	Output high voltage	2.3	---	---	V
V_{OL}	Output low voltage	---	---	0.4	V

5-5. DC Electricals – Digital 1.8V/3V Pads (VIO_X1, VIO_X2)

Symbol	Parameter	Mode	Condition	Min	Typ	Max	Unit
V_{18}	Power supply voltage (VIO_X1, VIO_X2)	1.8V	---	1.62	1.8	1.98	V
V_{33}	Power supply voltage (VIO_X1, VIO_X2)	3.3V	---	2.97	3.3	3.63	V
V_{IH}	Input high voltage	1.8V	---	1.2	---	V_{18}+0.3	V
		3.3V	---	2.0	---	V_{33}+0.3	V
V_{IL}	Input low voltage	1.8V	---	-0.3	---	0.6	V
		3.3V	---	-0.3	---	1	
V_{HYS}	Input hysteresis	1.8V	---	250	---	---	mV
		3.3V	---	300	---	---	mV
V_{OH}	Output high voltage	1.8V	SR[1] = Slew Rate[2] **SR I_{OH}(max)** 3 16 mA 2 16 mA 1 5 mA 0 5 mA	1.22	---	---	V
		3.3V	SR = Slew Rate **SR I_{OH}(max)** 3 16.5 mA 2 16.5 mA 1 5.5 mA 0 5.5 mA	2.57	---	---	V
V_{OL}	Output low voltage	1.8V	SR = Slew Rate[3] **SR I_{OL}(max)** 3 23 mA 2 15.5 mA 1 7.5 mA 0 7.5 mA	---	---	0.4	V
		3.3V	SR = Slew Rate **SR I_{OL}(max)** 3 23.5 mA 2 15.5 mA 1 7.5 mA 0 7.5 mA	---	---	0.4	V
I_pullup[4]	---	---	---	16	22	29	µA
I_pulldown	---	---	---	12	23	33	µA
I_pullup_weak	---	---	---	---	---	10	µA
I_pulldown_weak	---	---	---	---	---	10	µA

1. Slew rate that controls the output drive strength and rise/fall time of the pad.
2. I_{OH} is the maximum current draw to maintain a minimum V_{OH} level.
3. I_{OL} is the maximum sink current to maintain a maximum V_{OL} level.
4. There are two types of pull-up/pull-down pads—regular and weak. Each pad type (regular and weak) has different internal resistor values.

5-6. Power Supply Configurations

For flexibility, MBH7WLZ16 integrates an internal voltage regulator. The 1.2V_EXT supply can be derived from this regulator.
The following table lists the connections of the VIO1.8_LDO and 1.2V_EXT power supplies in various applications.

Configuration	VIO1.8_LDO	1.2V_EXT
Internal voltage regulator with/without Bluetooth coexistence interface	Connected	Not Connected
External 1.2V supply with/without Bluetooth coexistence interface	Connected	Connected

5-7. Power Sequence

Figure 5-1 shows the power up sequence of MBH7WLZ16.

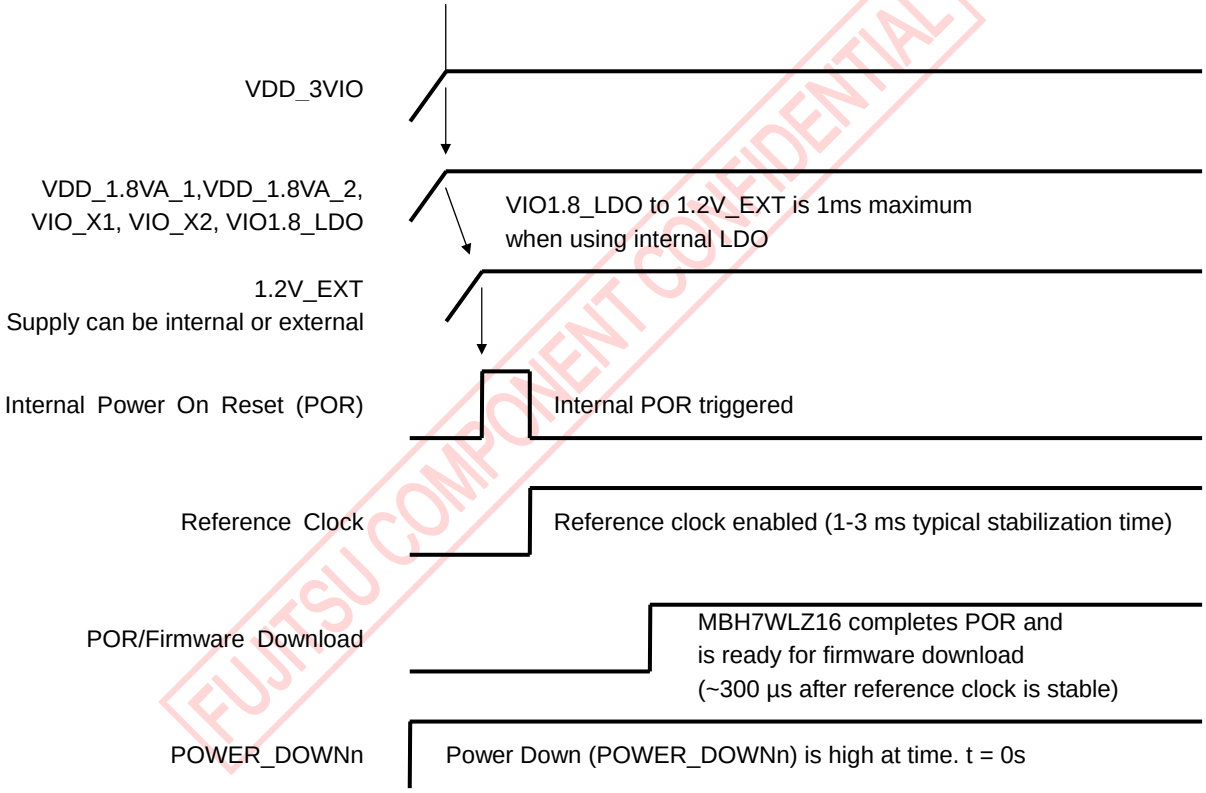


Figure 5-1 Power Up Timing Sequence

5-8. Power Management

The following table lists the state of the functional pins when in power down mode.

No.	Tri-State (Floating)	No.	Output Low	No.	Output High
9	SLEEP_CLK	11	GPIO[0]/SLEEPn	37	ANT_SEL_P
14	SD_DAT3	24	SCLK		
15	SPI_SINTn/SD_DAT2	36	ANT_SEL_N		
16	SPI_SDO/SD_DAT1	39	GPIO[2]		
17	SPI_SCSn/SD_DAT0	40	WL_ACTIVE		
18	SPI_SDI/SD_CMD				
19	SPI_CLK/SD_CLK				
20	GPIO[4]/Module_wake_up				
21	GPIO[1]/LED				
41	BT_STATE				
42	BT_PRIORITY				
43	BT_FREQ				

5-9. Reset Configuration

MBH7WLZ16 is reset to its default operating state under the following conditions:

- Power-on reset
- Software/Firmware reset

5-9-1. Internal Reset

MBH7WLZ16 is reset and the internal CPU begins the boot sequence when any of the following internal reset events occurs:

- MBH7WLZ16 receives power and the 1.2V supply rises (this triggers the internal POR circuit)
- Internal CPU issues a software reset
- Host driver issues a soft reset
- Watchdog timer expires (used for debug purpose only)

5-9-2. External Reset

MBH7WLZ16 is reset and the internal CPU begins the boot sequence when the RESETn input pin transitions from low to high.

5-9-3. Calibration

MBH7WLZ16 performs calibration when the device is powered up. In addition, calibration is also performed under the following operating conditions:

- Exiting receive mode
- Exiting transmit mode
- Change of channel frequency

5-10. RF Specification*[1]

Items		Condition	Min	Typ	Max	Unit
Transmit power levels	Channel 1-13	54 Mbps (64QAM) 48 Mbps (64QAM)	-	12.0	-	dBm
		36 Mbps (16QAM) 24 Mbps (16QAM) 18 Mbps (DQPSK) 12 Mbps (DQPSK) 9 Mbps (DBPSK) 6 Mbps (DBPSK)	-	15.0	-	dBm
		11 Mbps (CCK) 5.5Mbps (CCK) 2 Mbps (DQPSK) 1 Mbps (DBPSK)	-	16.0	-	dBm
	Channel 14	11 Mbps (CCK) 5.5Mbps (CCK) 2 Mbps (DQPSK) 1 Mbps (DBPSK)	-	8.0	-	dBm
802.11b Transmit spectrum mask	1st Side Lobe	1 Mbps (DBPSK)	-	-	-30	dBr
	2nd Side Lobe		-	-	-50	dBr
802.11g Transmit spectrum mask	11 MHz offset	6 Mbps (DBPSK)	-	-	-20	dBr
	20 MHz offset		-	-	-28	dBr
	30 MHz offset		-	-	-40	dBr
Transmit center frequency tolerance		54 Mbps (64QAM)	-25	-	25	ppm
Symbol clock frequency tolerance		54 Mbps (64QAM)	-25	-	25	ppm
Transmit power-on ramp		11 Mbps (CCK)	-	-	2	µs
Transmit power-down ramp		11 Mbps (CCK)	-	-	2	µs
RF carrier suppression		2 Mbps (DQPSK)	15	-	-	dB
EVM (Peak)		11 Mbps (CCK)	-	10	35	%
		1 Mbps (DBPSK)	-	8	35	%
EVM (RMS)		54 Mbps (64QAM)	-	-31	-25	dB
		6 Mbps (DBPSK)	-	-28	-5	dB
Receiver minimum input level sensitivity		54 Mbps (64QAM)	-	-74	-65	dBm
		6 Mbps (DBPSK)	-	-90	-82	dBm
		11 Mbps (CCK)	-	-89	-76	dBm
		1 Mbps (DBPSK)	-	-92	-85	dBm
Receiver maximum input level		54 Mbps (64QAM)	-20	-	-	dBm
		11 Mbps (CCK)	-10	-	-	dBm
Receiver adjacent channel rejection		54 Mbps (64QAM)	-1	-	-	dB
		11 Mbps (CCK)	35	-	-	dB

*1) Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

6. Host Interface

MBH7WLZ16 connects several host interface bus units to the internal bus of the device. The connection of each host interface bus unit to the internal bus is multiplexed with the other host interface bus units. MBH7WLZ16 allows only one host interface unit to be active at a time.
MBH7WLZ16 supports the following host interfaces:

- SDIO interface
- G-SPI interface

6-1. SDIO Interface

MBH7WLZ16 supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the WLAN device. The SDIO interface contains interface circuitry between an external SDIO bus and the internal shared bus.
MBH7WLZ16 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in MBH7WLZ16 through the use of BARs and a DMA engine.
The SDIO device interface main features include:

- Internal memory used for CIS
- Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer mode at the full clock range of 0 to 50 MHz
- Special Interrupt register for information exchange
- Allows module to interrupt host

The SDIO interface pins are powered from the VIO_X1 voltage supply.

6-1-1. SDIO Command List

All mandatory SDIO commands are supported for both SDIO and SPI modes. SDIO mode commands are shown in Table 6-1. SPI mode commands are shown in Table 6-2.

Table 6-1 SDIO Mode, SDIO Commands

Command	Command Name	Description
CMD0	GO_IDLE_STATE	Used to change from SDIO to SPI mode
CMD3	SEND_RELATIVE_ADDR	SDIO Host asks for RCA
CMD5	IO_SEND_OP_COND	SDIO Host asks for and sets operation voltage
CMD7	SELECT/DESELECT_CARD	Sets SDIO target device to command state or back to standby
CMD15	GO_INACTIVE_STATE	Sets SDIO target device to inactive state
CMD52	IO_RW_DIRECT	Used to read/write host register and CIS table
CMD53	IO_RW_EXTENDED	Used to read/write data from/to SQU memory

Table 6-2 SPI Mode, SDIO Commands

Command	Command Name	Description
CMD0	GO_IDLE_STATE	Used to change from SDIO to SPI mode
CMD5	IO_SEND_OP_COND	Used in initialization state
CMD52	IO_RW_DIRECT	Used to read/write host register and CIS table
CMD53	IO_RW_EXTENDED	Used to read/write data from/to SQU memory
CMD58	CRC_ON_OFF	SPI only. Enable/disable CRC

6-1-2. Power-Up Initialization

The power-up transaction sequences for SDIO and SPI modes are as follows:

6-1-2-1. SDIO Mode Power-Up Transaction Sequence

(1) CMD5 (arg = 0)
(2) SDIO Card response with OCR
(3) CMD5 from host to set operation voltage using OCR
(4) SDIO Card response with IORDY = 1 and MP = 0 (not SD memory, not combo card)
(5) CMD3 and CMD7 to set in one active mode
(6) CMD15 to put the card inactive

6-1-2-2. SPI Mode Power-Up Transaction Sequence

(1) CMD0 + CS = LOW
(2) CMD5 (arg = 0)
(3) SDIO Card response with OCR
(4) CMD5 from host to set operation voltage using OCR
(5) CMD15 to put the card inactive

6-1-3. Operation Sequence

Table 6-3 lists the registers used to program the operation sequence. See the SDIO Registers section of the separate Host Interface Registers document for register programming information.

Table 6-3 SDIO Registers

Register	Offset
Host Interrupt	0x107
Card Status	0x120

Operation transaction sequences are as follows:

6-1-3-1. SDIO Host Reads CIS Table Sequence

(1) Check Card Status, Offset 0x120[2]. It is set by Card after CIS table is initialized.
(2) HOST reads CIS Table using Function 0 address 8030_807F and function 1 address 8080_80FF.

6-1-3-2. SDIO Host Downloads Packet

(1) Card sets Card Status, Offset 0x120[0].
(2) Host Polls Dnld_Card_Rdy and IO_Ready.
(3) Host starts CMD53 block mode using function 1 with IO port address. CMD53 write clears Dnld_Card_Rdy.
(4) Host sends the data in terms of predefined blocks. If BUSY, host delays the next block.
(5) After CMD53 write completes, an interrupt CardInt is sent to firmware.
(6) Firmware checks Host Interrupt Status, Offset 0x107[2] and Host Interrupt Status, Offset 0x107[0] registers. If Dnld_CRC_Err = 1, this packet has CRC error. If Dnld_Restart = 1, firmware ignores this packet.
(7) Back to the first step.

6-1-3-3. SDIO Host Uploads Packet

(1) Card sets Card Status, Offset 0x120[1].
(2) Upld_Card_Rdy triggers an interrupt to SDIO HOST in the interrupt period.
(3) SDIO HOST read to clear INT or write 0 to clear the interrupt.
(4) SDIO HOST checks Upld_Card_Rdy and IO_Ready.
(5) HOST starts CMD53 read using function 1 with IO address with infinite block number or defined block number. CMD53 clears Upld_Card_Rdy bit.
(6) After Host receives all data, HOST writes Abort using CMD52.
(7) This terminate read operation. Card gets an interrupt with abort and with packet read, is complete.
(8) Firmware reads interrupt, clears interrupt.
(9) Firmware reads Host Interrupt Status, Offset 0x107[1]. If it is set by HOST, Firmware prepares to reissue this packet.
(10) Back to the first step.

The SDIO HOST checks IO_READY before starting a new CMD53. The SDIO target device can take a new SDIO HOST command only after the SDIO target device internal state machine is set back to IO_READY state. Otherwise, the new CMD53 is ignored.

6-1-4. SDIO Timing

SDIO Timing specifications are shown in the followings.

Table 6-4 SDIO Timing Data

Symbol	Items	Condition	Min	Typ	Max	Unit
fPP	CLK Frequency	-	0	-	50	MHz
tWL	CLK Low Time	-	11.1	-	-	ns
tWH	CLK High Time	-	11.1	-	-	ns
tISU	Input Setup Time	-	5	-	-	ns
tIH	Input Hold Time	-	5	-	-	ns
tODLY	Output Delay Time	-	0	-	15	ns

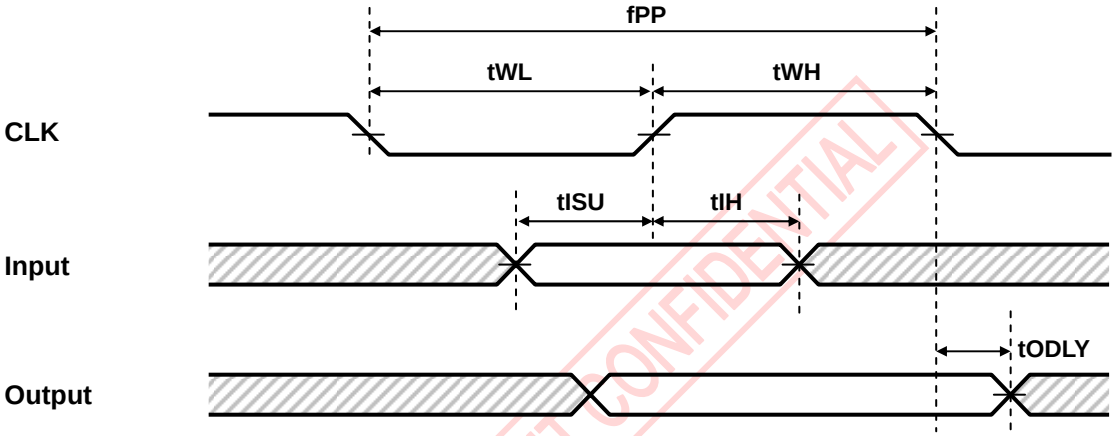


Figure 6-1 SDIO Timing Diagram

Note: The SDIO-SPI CS signal timing is identical to all other SDIO inputs.

6-2. G-SPI Interface

MBH7WLZ16 supports a generic, half-duplex, DMA-assisted SPI host interface (G-SPI) that allows a host controller using a generic SPI bus protocol to access the WLAN device. The G-SPI interface contains interface circuitry between an external SPI bus and the internal shared bus.
The MBH7WLZ16 acts as the device on the SPI bus. The host unit can access the G-SPI registers directly and can access shared memory in MBH7WLZ16 through the use of BARs and DMA engine.
The SPI unit supports generic SPI interface protocols as detailed in the following sections. The design is capable of 50MHz operation. The interface supports the following functionally.

- SPI unit bus device operation.
- SPI unit register read / write.
- Interrupt generation to internal CPU.
- Interrupt generation to the SPI unit host.
- DMA to internal memories
- Wake interrupt to the Power Management Unit

MBH7WLZ16 G-SPI interface pins are powered from the VIO_X1 voltage supply.

6-2-1. G-SPI Interface Functional Description

The G-SPI supports a variety of simple address/data protocols over a standard G-SPI physical bus. The protocols supported are differentiated by the number of address bits and data ordering.
Each transaction is initiated by assertion of the active low signal SCSn. Following the assertion of SCSn, the SDI input is latched with every positive edge of SCLK. When data is output, it is clocked out with the negative edge of SCLK. The clock input SCLK is low at the start and completion of a transaction.

6-2-1-1. Transaction Delays

The first block of data to be transferred is from host to the device. This block of data contains an address and read/write control. The MSB of the address is low for read operations and high for write operations.

6-2-1-1-1. Write Transaction Delay

For write transactions, the data phase of a transaction immediately follows the address phase of the transaction. There is no need to extend the low time of the clock between address and data or for the host to clock any dummy cycles.

6-2-1-1-2. Read Transaction Delay

There is a delay required between the end of the address phase on the bus and the start of the data phase of the transaction. This delay is shown as TDRR (time delay read register) and TDRP (time delay read port). This delay represents the time delay required for the device to prepare valid data to return to the host.
This delay can be created in two different ways.
First, the read transaction delay is created by the host clocking a known number of dummy clock cycles to the device. The number of dummy clock cycles is specified in the Delay Read Register. There are two parameters in this parameter:

- Register read access
- Port read access

This mode is selected by setting the Delay Mode bit to 1 in the SPU Bus Mode, Offset 0x70[2].
Second, the delay is created by the host holding the clock signal low for a minimum period of time between the address and data phases. This mode is selected by setting the Delay Mode bit to 0 in the SPU Bus Mode, Offset 0x70[2].
During the data phase of a transaction, the host continues to provide clock pulse and either drives data on the SDI input or read data from the SDO output.

6-2-1-2. Data Transfer

The host always accesses configuration registers in the G-SPI unit. To access internal memory space, some registers are defined as Port registers. When Port registers are accessed, the device reads or writes from internal memory space using the corresponding Base Address Register (BAR) and DMA engine.
Every transfer between host and device is a burst transfer (single address followed by multiple data). A transfer is terminated by the host after reading or writing the desired amount of data by de-asserting the SCSn input.

6-2-1-2-1. Port Register Access

When the host system reads Port Registers, there is no limit to the burst length (other than the limit imposed by the valid address range of the internal bus). When the host system writes to Port Registers, the only condition on burst length is that the length be a multiple number of DWORDS.
Port Registers (I/O Port, Command Port, Data Port) are used to access internal 32-bit memory space and are always accessed on 32-bit boundaries. Each of these port registers has a corresponding BAR for reads and writes (acting as a pointer to the starting physical address location). Internal memory is also accessed only on 32-bit boundaries. This is accomplished by programming the corresponding BAR with 32-bit aligned values. During these accesses, the lower 16 bits are always presented on the bus first.

6-2-1-2-1-1. Port Register Write Data

Write data to a Port Register is packed into sequential 32-bit memory locations starting at the location of the corresponding BAR. When reading from the Data and Command Ports of the device, the DMA engine continues to fill the FIFO whenever there is room for eight DWORDs (32-bits) of data. When writing data to the device, the de-assertion of SCSn input causes a flush to the write FIFO.

6-2-1-2-1-2. Port Register Read Data

When reading data from the I/O Port of the device, it is selectable whether the DMA engine performs a single read or burst reads. Burst reads are treated like Data and Command Port reads. Single reads cause the DMA engine to perform a single DWORD access on the internal bus. A single read transaction must be terminated following the first or second 16-bit block of returned data.

6-2-1-2-2. Configuration Register Access

When the host system accesses registers other than the Port Registers, the burst length must be limited to one 16-bit data transfer, or two 16-bit data transfers if the address is on a DWORD boundary. When a unit on the internal bus accesses G-SPI interface registers, the access must be a single DWORD access or smaller.
G-SPI interface registers, with the exception of Port Registers, can be read from or written to on 16-bit boundaries. Transactions can be terminated after a single 16-bit word is read or written.

6-2-1-3. G-SPI Clock Frequency

The G-SPI clock frequency must not be greater than 2.5 times the internal bus clock frequency.

6-2-1-4. Data Formats

There are a total of 16 valid data formats. The following nine data formats (shown below) are valid.

- All four data read formats in which the clock signal remains low during the delay between the address and data phase
- All four data write formats
- One data read format in which the clock signal toggles for a fixed number of cycles during the delay between the address and data phase

For each of the transaction types (read and write) there are two address lengths, either 8-bit or 16-bit. There are two data orderings for each address length.

Figure 6-2 through Figure 6-5 show the read data format when the Delay Method register control is 0. In this case, the 'tdr(r/p)' values represent a time delay between the last address bit in a given transaction and the first data bit for that same transaction. There are two different time delay values, reading from a G-SPI interface configuration register and reading from a G-SPI interface port register. Once the time delay value specified by the type of transaction has expired, valid data can be clocked from the device. The clock signal SCLK should remain low in Delay Method is 1, the data format is similar to the figures bellow with the exception that there are a fixed number of clock cycles between the address and data phase.

6-2-1-4-1. Programmable Clock Cycle Delay

6-2-1-4-1-1. Read Data Formats

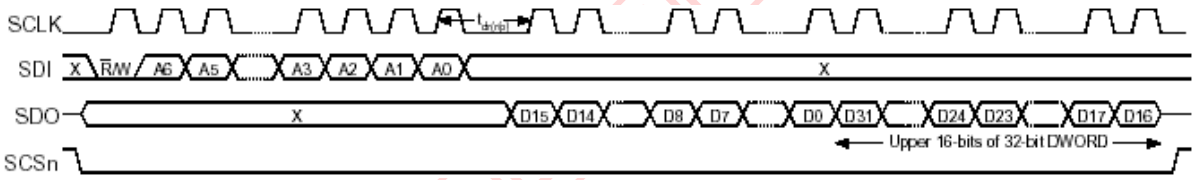


Figure 6-2 Read Data Format 1 – 8-bit Address, 16-bit Data

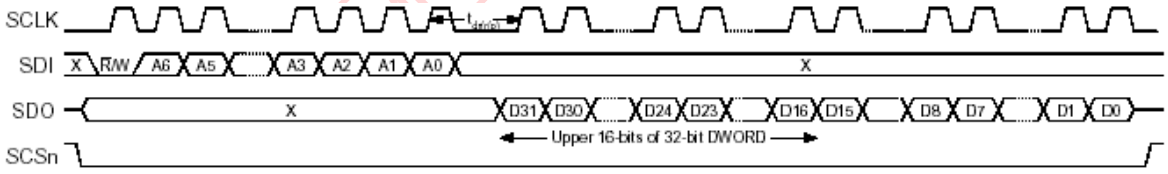


Figure 6-3 Read Data Format 2 – 8-bit Address, 32-bit Data (32-bit aligned address)

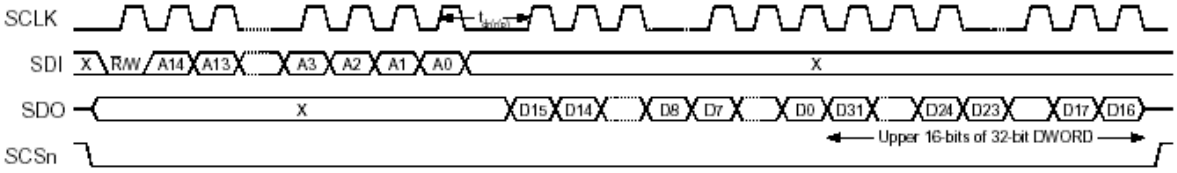


Figure 6-4 Read Data Format 3 – 16-bit Address, 16-bit data

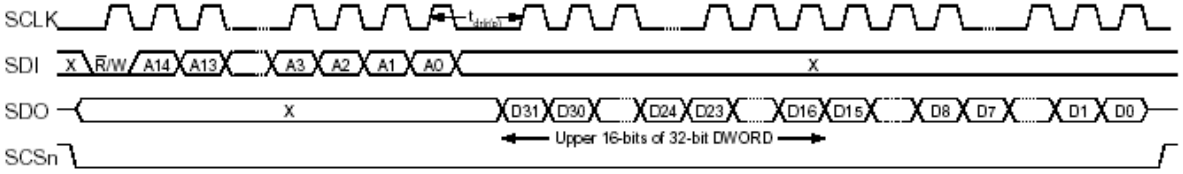


Figure 6-5 Read Data Format 4 – 16-bit Address, 32-bit Data (32-bit aligned address)

6-2-1-4-1-2. Write Data Formats

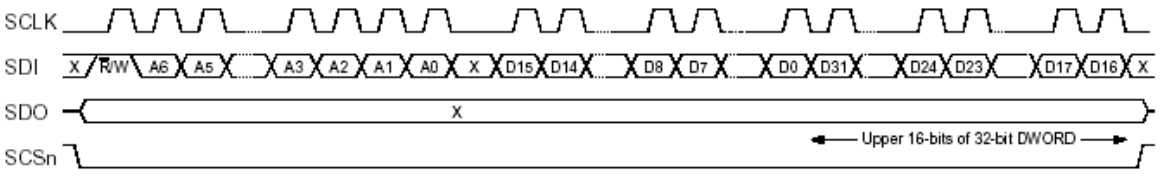


Figure 6-6 Write Data Format 1 – 8-bit Address, 16-bit Data

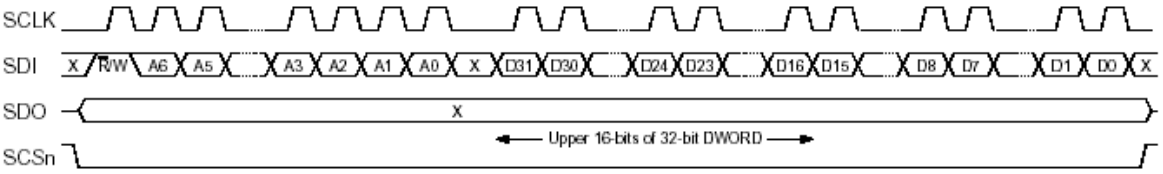


Figure 6-7 Write Data Format 2 – 8-bit Address, 32-bit Data (32-bit aligned address)

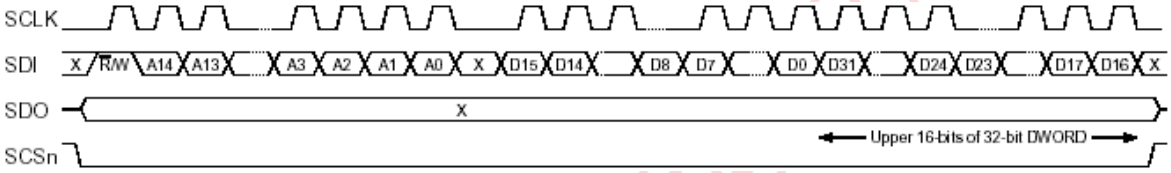


Figure 6-8 Write Data Format 3 – 16-bit Address, 16-bit Data

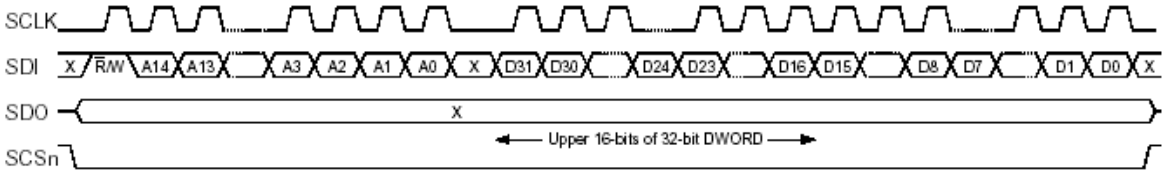


Figure 6-9 Write Data Format 4 – 16-bit Address, 32-bit Data (32-bit aligned address)

6-2-1-4-2. Fixed Clock Cycle Delay

6-2-1-4-2-1. Example Read Data Format

Figure 6-10 shows an example of one of the read data formats with a fixed clock cycle delay.

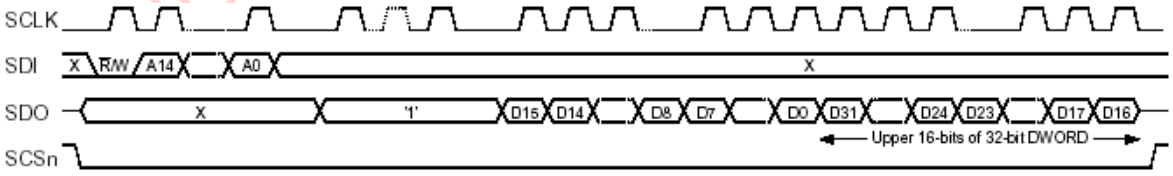


Figure 6-10 Read Data Format – 16-bit Address, 16-bit Data (fixed clock delay)

6-2-1-5. Example Transactions

The tables and figures below show some example host transactions on the G-SPI interface bus. Table 6-5 and Table 6-6 show memory ranges and data for G-SPI interface register space and internal memory space.
From the Host System, G-SPI interface registers can be accessed on 16-bit boundaries with the exception of the Port Registers. From the internal bus, registers are always accessed on 32-bit boundaries.
Table 6-5 shows a portion of the G-SPI interface configuration register space. Register addresses are shown from both the Host System and the internal bus. Example data which is used in Figure 6-11, is shown stored in the registers.
Table 6-6 shows a portion of the SQU memory on the internal bus, along with example data used in Figure 6-11.
For these examples, it is assumed all base address registers contain the value 0xC000_1000. Address and data values in the example figures are in hexidecimal.

An “x” represents an undefined (don’t care) value. A “z” re presents a high impedance state.

Table 6-5 G-SPI Interface Register Memory Space

Bits		**Bits**		**Internal Address**
31	**16**	**15**	**0**	
Address from Host (and stored data)				
0x0042		0x0040		0x8000 0040
0x0046		0x0044		0x8000 0044
0x004A		0x0048		0x8000 0048
0x004E		0x004C		0x8000 004C
0x0052		0x0050		0x8000 0050
0x0056		0x0054		0x8000 0054
0x005A		0x0058		0x8000 0058
0x005E		0x005C		0x8000 005C

Table 6-6 Internal SQU memory Space

Bits		**Bits**		**Internal Address**
31	**16**	**15**	**0**	
Stored Data				
0x1002		0x1000		0x8000 1000
0x1006		0x1004		0x8000 1004
0x100A		0x1008		0x8000 1008
0x100E		0x100C		0x8000 100C
0x1012		0x1010		0x8000 1010
0x1016		0x1014		0x8000 1014
0x101A		0x1018		0x8000 1018
0x101E		0x101C		0x8000 101C

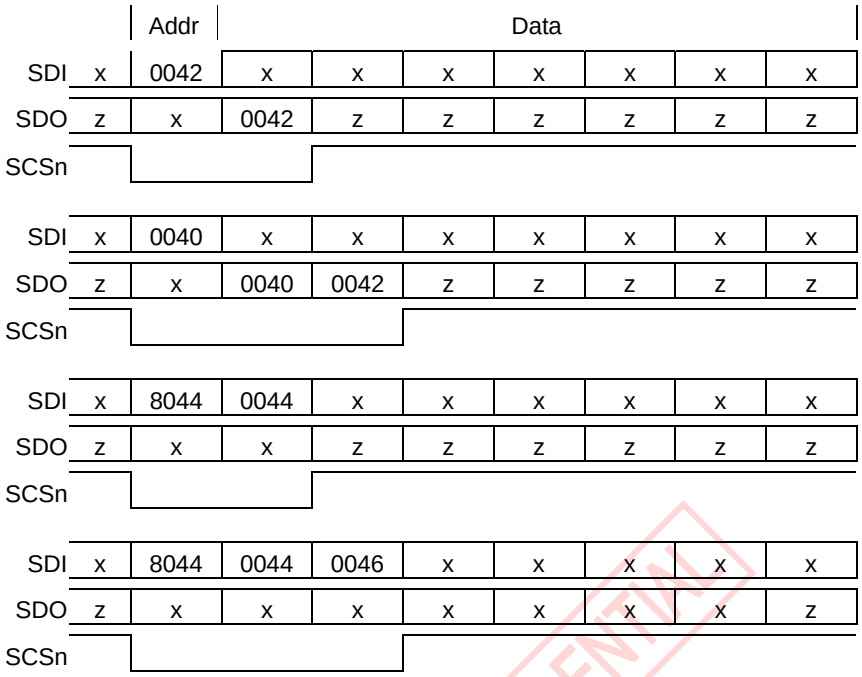


Figure 6-11 Example Bus Transactions to Register Space – 16-bit Address and 16-bit Data

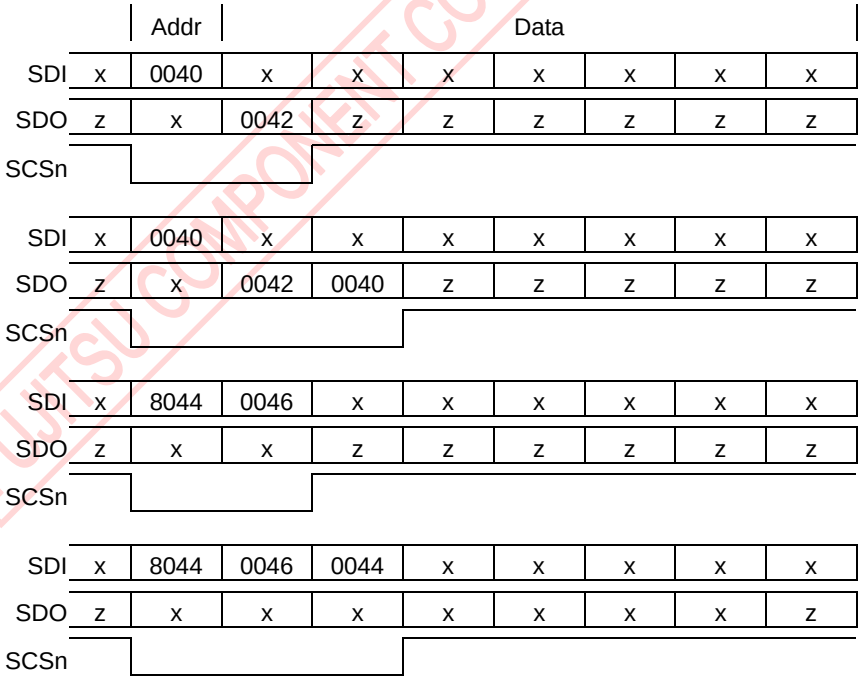


Figure 6-12 Example Bus Transactions to Register Space – Data Formats 7 and 11

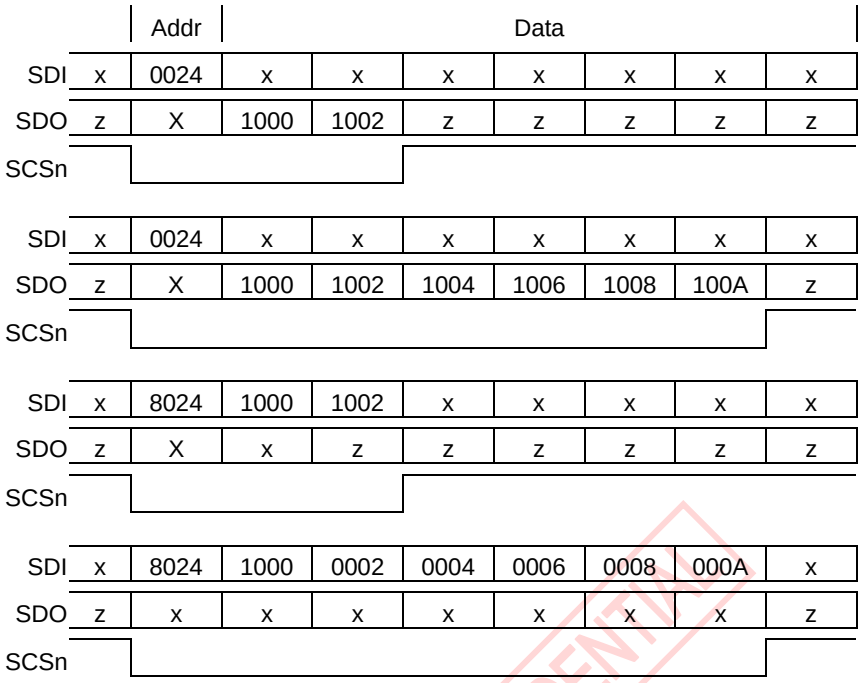


Figure 6-13 Example Bus Transactions to Internal Memory

6-2-2. G-SPI Timing

G-SPI Timing specifications are shown in the followings.

Table 6-7 G-SPI Timing Data

Symbol	Parameter	Min	Typ	Max	Unit
T1	Clock Period	20	---	---	ns
T2	Clock High	5	---	---	ns
T3	Clock Low	9	---	---	ns
T4	Clock Rise Time	---	---	1	ns
T5	Clock Fall Time	---	---	1	ns
T6	SDI Hold Time	2.5	---	---	ns
T7	SDI Setup Time	2.5	---	---	ns
T8	SDIO Hold Time	5	---	---	ns
T9	SDIO Setup Time	1	---	---	ns
T10	SCSn Fall to Clock	5	---	---	ns
T11	Clock to SCSn Rise	0	---	---	ns
T12	SCSn Rise to SCSn Fall	400	---	---	ns

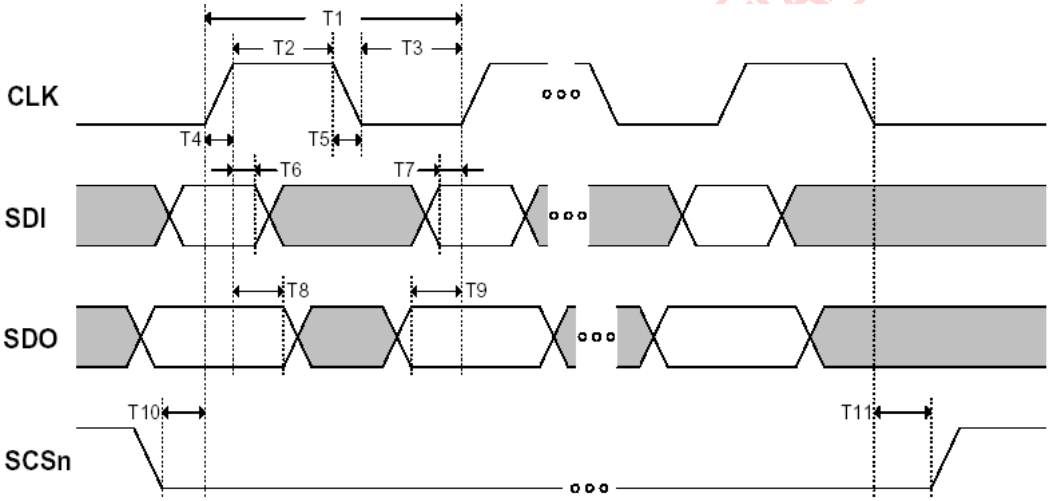


Figure 6-14 G-SPI Transaction Timing

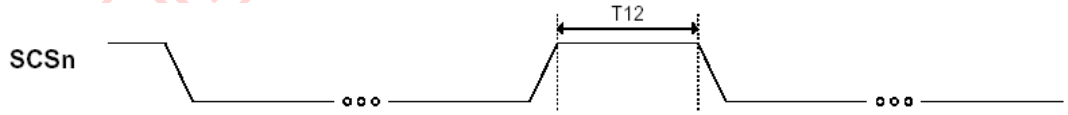


Figure 6-15 G-SPI Inter-Transaction Timing

7. Bluetooth Coexistence

MBH7WLZ16 supports coexistence capability with co-located Bluetooth devices.
There are three Bluetooth Coexistence Arbitration (BCA) units in MBH7WLZ16:

- 2-Wire Bluetooth Coexistence Arbitration (2WBCA) scheme
- 3-Wire Bluetooth Coexistence Arbitration (3WBCA) scheme
- 4-Wire Bluetooth Coexistence Arbitration (4WBCA) scheme

Only one of the BCA units can be used at a time. In addition, MBH7WLZ16 contains a Switch Module (SM) that controls antenna switching for both single antenna and dual antenna applications.

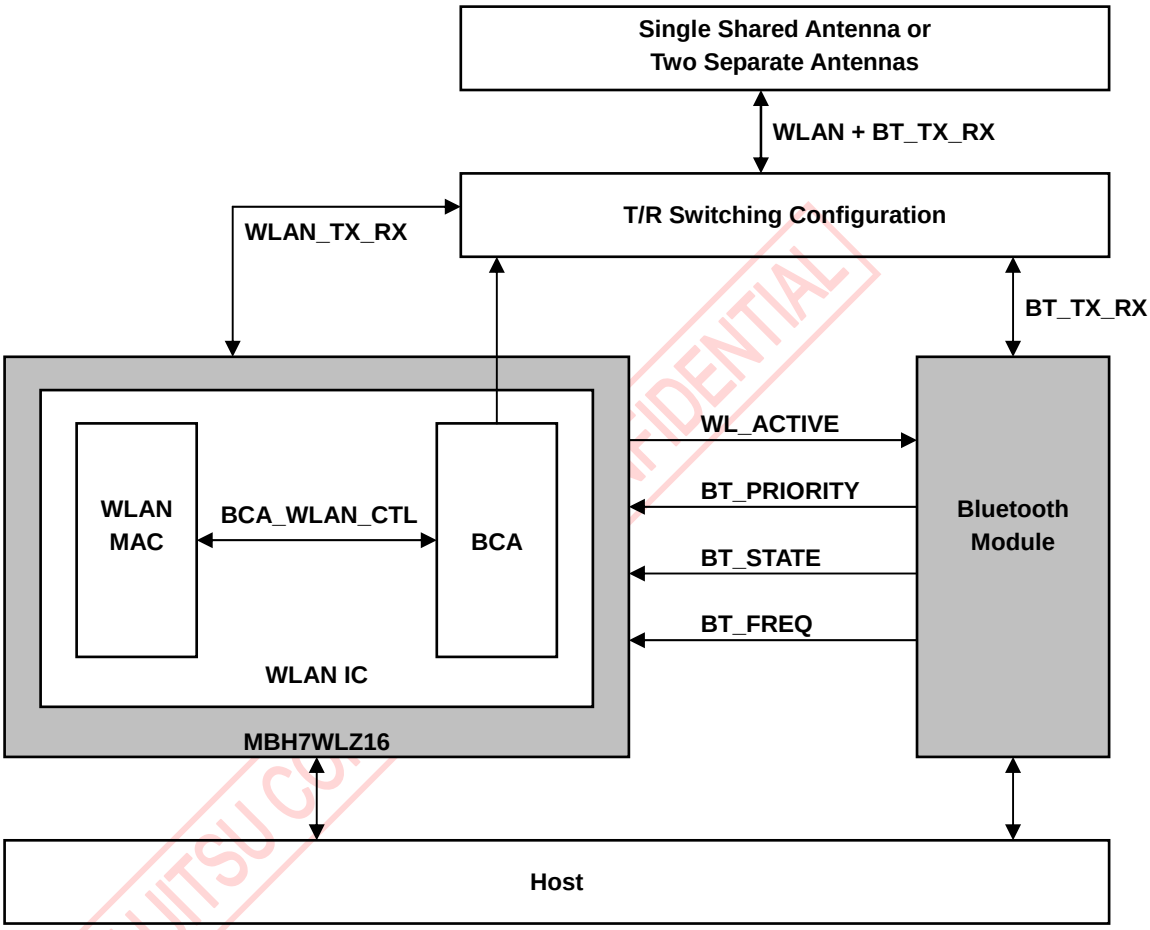


Figure 7-1 Bluetooth Top Block Diagram

7-1. System Level Configuration

Hardware configurability enables the following system-level configuration options:

- Bluetooth v1.1 or Bluetooth v1.2 Adaptive Frequency Hopping (AFH)
- QoS-aware 2-wire coexistence signaling interface or 4-wire coexistence signaling interface
- Single shared antenna or dual antenna
  - For single antenna system, dual 2-port T/R switching configuration
- Configurable timing on coexistence signaling interface and switch control interface
- Future-proofed firmware programmable and system-configurable QoS classification and prioritization

7-2. WLAN/Bluetooth Channel Information Exchange

Since Bluetooth and 802.11b/g WLAN use the same 2.4 GHz frequency band, each can cause interference with the other. The level of interference depends on the respective frequency channel used by Bluetooth and WLAN (other factors can impact interference, like Tx power and Rx sensitivity of the device).
In a system with both Bluetooth and WLAN, the common host receives information about WLAN channel usage and passes this information to the Bluetooth device. For Bluetooth v1.2 devices with AFH enabled, the Bluetooth device can block channel usage that overlaps the WLAN channel in use.
When the Bluetooth device avoids all channels used by the WLAN, the impact of interference is greatly reduced, but not completely eliminated. For Bluetooth v1.1 devices, the Bluetooth device cannot block WLAN channel usage and an active BCA scheme at the MAC levels is required. The BCA scheme can also be used with Bluetooth v1.2 devices to further reduce the impact of interference to a minimum.

7-2-1. Dual/Single Antenna Support

All the arbitration units support dual and single antenna configurations.

7-2-1-1. Dual Antenna Configuration

In dual antenna configurations, both WLAN and Bluetooth have their own dedicated antennas. In this case, the BCA allows simultaneous WLAN and Bluetooth transactions, resulting in higher WLAN/Bluetooth network performance. Figure 7-2 shows the Dual Antenna Configuration.

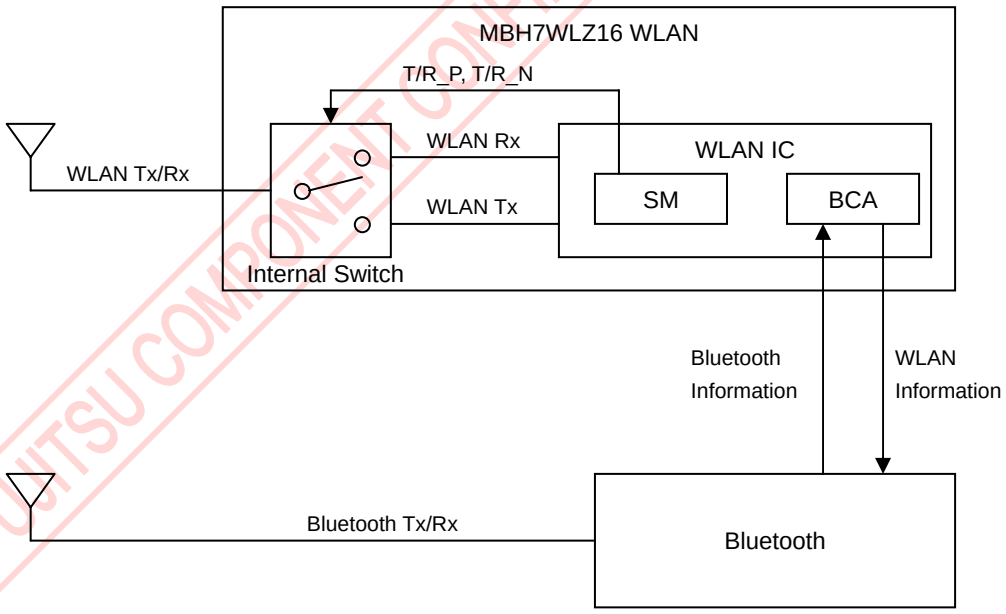


Figure 7-2 Dual Antenna Configuration

7-2-1-2. Single Antenna Configuration

In single antenna configurations, both WLAN and Bluetooth share one antenna. In this case, the BCA must ensure that only one device is allowed to use the antenna. A single antenna configuration has an advantage of lower cost and board space saving, compared to the dual antenna configuration.
The external RF switch for the single antenna needs additional control signals for switch control. This is accomplished by Switch Module (SM) logic in MBH7WLZ16. Figure 7-3 shows the Single Antenna Configuration with 2-way switch.

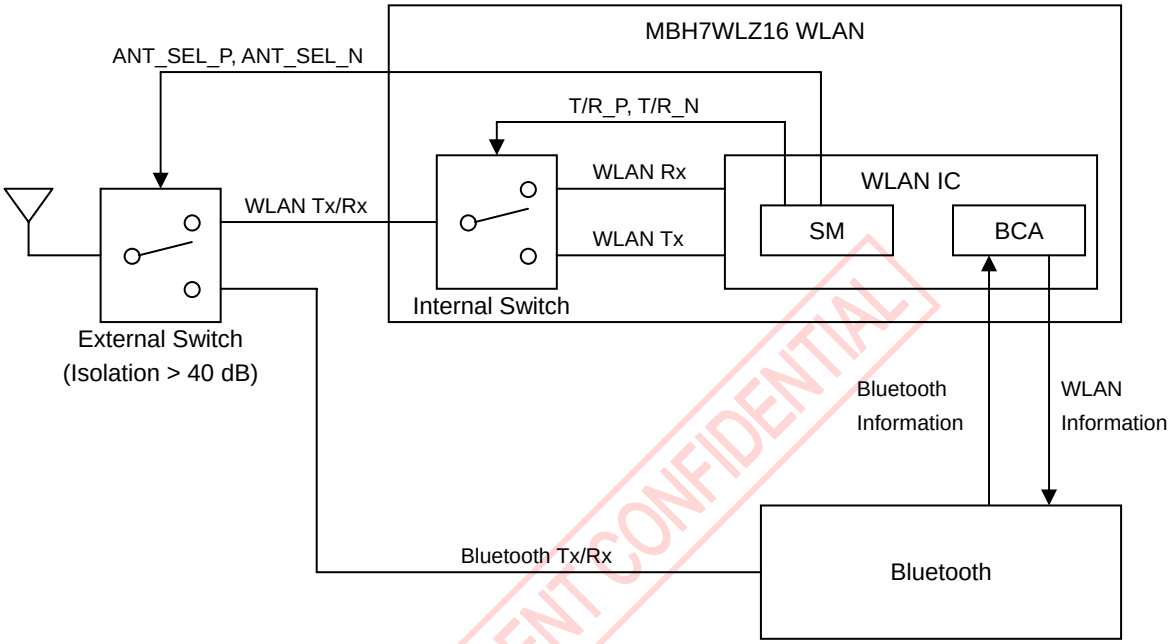


Figure 7-3 Single Antenna Configuration with 2-way Switch

7-3. 2-Wire BCA

The 2WBCA interface decides which device has primary access to the shared wireless medium according to the 2WBCA coexistence scheme. The 2WBCA interface makes its decision based on input signals from the Bluetooth device, input signals from the 802.11 MAC device, and MAC register settings. The input signals from the 802.11 and Bluetooth device report activity or priority for their respective devices. The 2WBCA interface module compares any conflicting traffic based on a programmable table in the MAC registers.

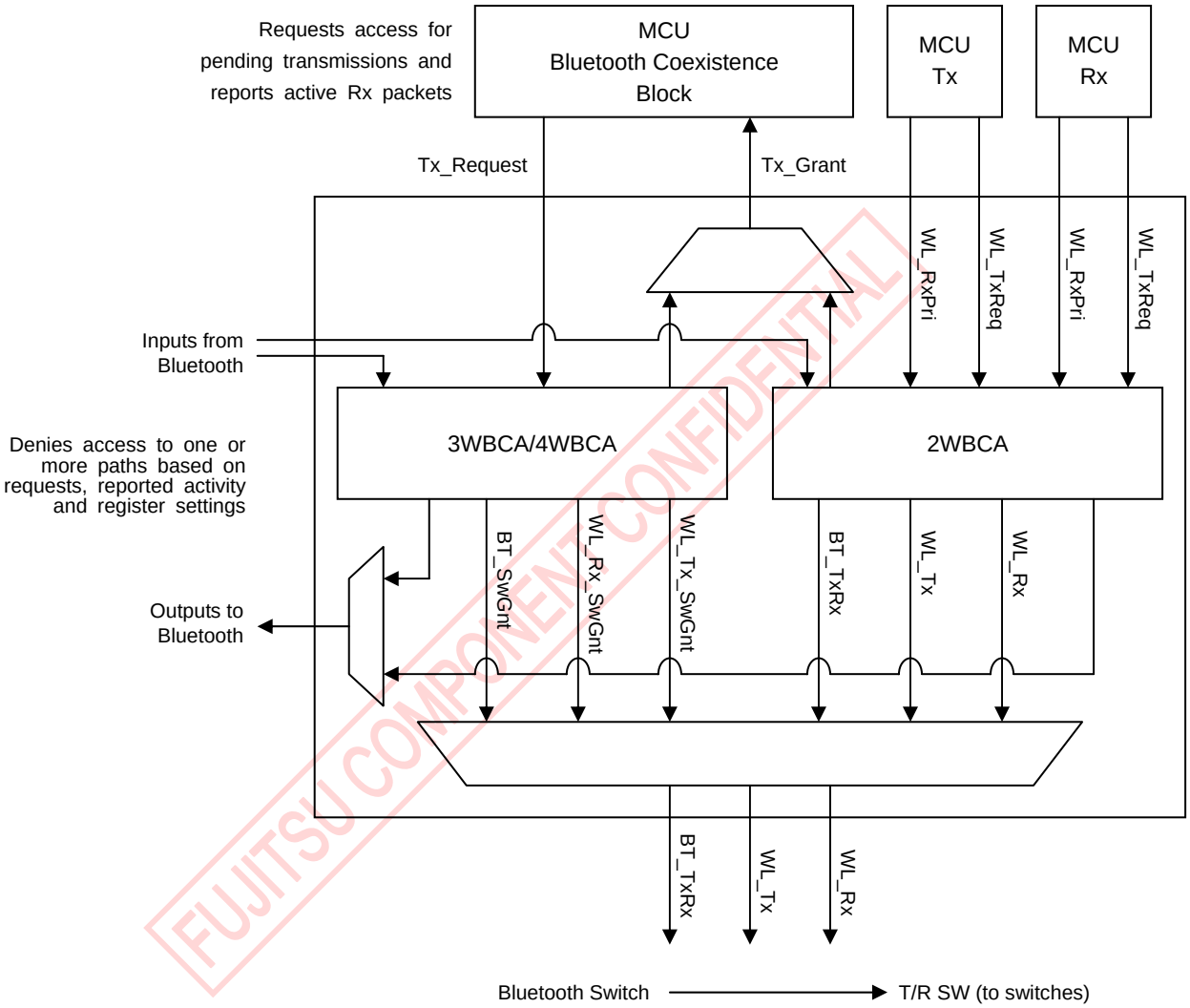


Figure 7-4 2WBCA Block Diagram

7-3-1. 2-Wire BCA Arbitration Tables

The arbitration scheme is as follows:

- WLAN high-priority packets have priority over all Bluetooth packets. Bluetooth high-priority packets have priority over WLAN low-priority packets.
- When the Bluetooth priority signal is asserted, the arbiter checks if the WLAN has a Tx or Rx request. If the WLAN requests during this time, the arbiter makes an arbitration decision based on the arbiter decision table. Typically, for the Bluetooth device, once the arbiter allows it to transmit, the Bluetooth does not stop transmitting until the transmitting packet completes. For this reason, if a higher priority WLAN request enters while the Bluetooth is transmitting, the arbiter allows the Bluetooth to complete transmission before granting access to the WLAN.
- For WLAN requests, the arbiter has no WLAN arbitration window, but the arbiter may stop the WLAN while the WLAN is in the middle of packet transmission. Since there is no WLAN arbitration window, the WLAN is granted access immediately if there is no Bluetooth request at that time. Except for WLAN high-priority packets, there is no guarantee that WLAN can transmit or receive (for single antenna case) the entire packet. The arbiter can stop the WLAN from transmitting or receiving (for single antenna case) in the middle of the packet if there is a new Bluetooth request, and the new arbiter decision is in favor of the Bluetooth packet. This approach optimizes the performance of Bluetooth voice applications, at the expense of WLAN performance.

Table 7-1 Single Antenna Default Arbitration Table

WLAN Tx Request	WLAN Tx Priority	WLAN Rx Request	WLAN Rx Priority	Bluetooth Priority	Result
0	0	1	0	1	Stop Low Priority WLAN Rx High Priority Bluetooth OK
0	0	1	1	1	High Priority WLAN Rx OK Stop High Priority Bluetooth
1	0	0	0	1	Stop Low Priority WLAN Tx High Priority Bluetooth OK
1	1	0	0	1	High Priority WLAN Tx OK Stop High Priority Bluetooth

Table 7-2 Dual Antenna Default Arbitration Table

WLAN Tx Request	WLAN Tx Priority	WLAN Rx Request	WLAN Rx Priority	Bluetooth Priority	Result
0	0	1	0	1	Low Priority WLAN Rx OK High Priority Bluetooth OK
0	0	1	1	1	High Priority WLAN Rx OK High Priority Bluetooth OK
1	0	0	0	1	Stop Low Priority WLAN Tx High Priority Bluetooth OK
1	1	0	0	1	High Priority WLAN Tx OK Stop High Priority Bluetooth

7-4. 3-Wire BCA and 4-Wire BCA

The 3WBCA and 4WBCA units operate the same, except that the 4WBCA includes an additional input signal to specify to the SoC whether the Bluetooth device is using a channel that overlaps with the WLAN channel.
The 4WBCA coexistence framework is based on the IEEE 802.15.2 recommended practice Packet Traffic Arbitration (PTA) scheme. This scheme is recommended for next generation mobile phones. The PTA logic in the WLAN block assumes the Bluetooth and WLAN have separate antenna (i.e. Bluetooth and WLAN can receive simultaneously, and the PTA logic has no control on the Bluetooth/WLAN receive path).

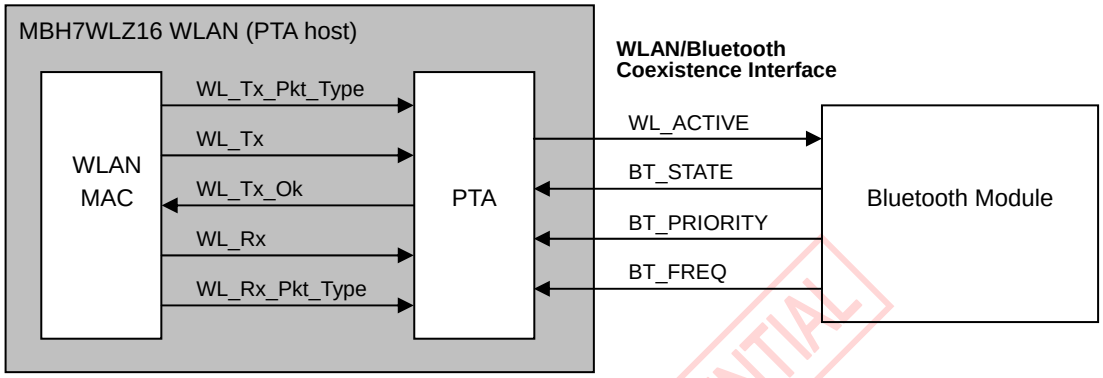


Figure 7-5 4WBCA High-Level Block Diagram

7-4-1. Packet Classification

WLAN packet information includes the 6-bit Pkt_Type (apply to either WLAN Tx or Rx packets). The arbitration unit has two 64-bit programmable masks (WL_Tx_Pri_Mask and WL_Rx_Pri_Mask) to mask off all the low-priority packet types. The remaining unmasked packet types are considered high-priority packet types (firmware puts 0 on the WL_Pri_Mask corresponding to the packet type that has low-priority). By default, only WLAN ACK packet types have a 1 in the mask.

{WL_Tx_Pkt_Type, WL_Tx_Pri_Mask} –> WL_Tx_Pri
{WL_Rx_Pkt_Type, WL_Rx_Pri_Mask} –> WL_Rx_Pri

7-4-2. Arbitration

The WLAN MAC includes a flexible packet level arbitration scheme between the WLAN and Bluetooth. An arbiter inside the arbitration block decides whether WLAN or Bluetooth can transmit.

{WL_Pri, WL_Tx_Rx, BT_Pri, BT_Tx_Rx} –> Arb_Decision

Table 7-3 shows the default Arb_Decision, which is geared towards performance optimization for both WLAN and Bluetooth, based on coexistence test results. Arb_Decision is controlled by two sets of 32-bit firmware-programmable registers for flexibility during performance turning.

Decisions made by the arbitration scheme use the following inputs and register controls:

- Classification of each type of WLAN packet as high priority or low priority
- Recognition of each Bluetooth request as a request to transmit or receive high or low priority
- Selection of which traffic type has higher priority: high priority WLAN or high priority Bluetooth
- Selection of which traffic type has higher priority: low priority WLAN or low priority Bluetooth

7-4-2-1. Arbitration Scheme

The arbitration scheme is as follows (default behavior shown):

- WLAN high-priority packets have priority over all Bluetooth packets. Bluetooth high-priority packets have priority over WLAN low-priority packets.
- If AFH is enabled in the Bluetooth device and sufficient guard-band outside the WLAN operating frequency is preserved, the Bluetooth device uses the OutOfBand (OOB) channel with respect to the WLAN device. Otherwise, the Bluetooth device uses the InBand (IB) and OOB channels with respect to the WLAN device. Firmware controls the arbiter for Bluetooth IB versus OOB by programming the arbitration mode configuration register.
- For the co-located devices running in dual antenna configuration:
  - WLAN Tx and Bluetooth Tx in OOB situation have little interference impact on each other.
  - WLAN Tx and Bluetooth Tx in IB situation have a sizable interference impact on each other. Therefore, the arbiter decision table allows either WLAN or Bluetooth Tx, based on their relative packet priorities.
  - WLAN Tx and Bluetooth Rx (both OOB and IB) have sizable interference impacts on Bluetooth Rx. Therefore, the decision table stops WLAN Tx when Bluetooth Rx is prioritized over WLAN Tx.
  - WLAN Rx and Bluetooth Tx (both OOB and IB) have sizable interference impacts on WLAN Rx. Therefore, the decision table stops Bluetooth Tx when WLAN Rx is prioritized over Bluetooth Tx.
- For Bluetooth requests, the arbiter has a Bluetooth arbitration window of approximately 75µs after assertion of the signal indicating the start of Bluetooth Tx/Rx high-priority packets. During the Bluetooth arbitration window, the arbiter checks if the WLAN has a Tx or Rx request. If the WLAN requests during the arbitration window, the arbiter makes an arbitration decision based on the arbiter decision table. Typically, for the Bluetooth device, once the arbiter allows it to transmit, the Bluetooth does not stop transmitting until the transmitting packet completes. For single antenna mode, if a higher priority WLAN request enters while the Bluetooth transaction is on going, the arbiter requests the SM to stop Bluetooth immediately and allow the WLAN to use the antenna.
- For WLAN requests, the arbiter has no WLAN arbitration window, but the arbiter may stop the WLAN while the WLAN is in the middle of packet transmission. Since there is no WLAN arbitration window, the WLAN is granted access immediately if there is no Bluetooth request at that time. Except for WLAN high-priority packets, there is no guarantee that WLAN can transmit or receive the entire packet (for single antenna case). The arbiter can stop the WLAN from transmitting or receiving (for single antenna case) in the middle of the packet if there is a new Bluetooth request, and the new arbiter decision is in favor of the Bluetooth packet. This approach optimizes the performance of Bluetooth voice application, but at the expense of WLAN performance.

  A configurable register bit (MCU Modes, Offset 0x5F0[15], in the WLAN MAC Registers section of the separate Network Registers document) prevents WLAN Tx/Rx requests to the arbiter when Bluetooth transactions have already started, even if the WLAN has a higher priority packet than Bluetooth. This mode is enabled by default (i.e., stop WLAN Tx/Rx requests while Bluetooth is in transaction).

7-4-2-2. Arbiter Decision Tables

7-4-2-2-1. Dual Antenna System Configuration

Table 7-3 Arbiter Decision Table (BT_FREQ_OOB Bit =1, always InBand)

Name	Value									
WLAN Priority 0 = low 1 = high	1	1	1	X	0	0	0	0	0	0
WLAN Tx_Rx 0 = Rx 1 = Tx	1	1	0	0	1	1	0	0	1	1
Bluetooth Priority 0 = low 1 = high	X	X	X	X	0	1	0	1	0	1
Bluetooth Tx_Rx 0 = Rx 1 = Tx	0	1	1	0	0	0	1	1	1	1
Arbiter Decision (WL_Arb_TxOk_Cfg; BT_Arb_TxOk_Cfg registers)	WLAN Tx OK BT Rx OK	WLAN Tx OK BT Tx stop	WLAN Rx OK BT Tx stop	WLAN Rx OK BT Rx OK	WLAN Tx OK BT Rx OK	WLAN Tx stop BT Rx OK	WLAN Rx OK BT Tx stop	WLAN Rx OK BT Tx OK	WLAN Tx OK BT Tx stop	WLAN Tx stop BT Tx OK

Table 7-4 Arbiter Decision Table, Bluetooth v1.2 Device (BT_FREQ_OOB Bit = 0, Always OutOfBand)

Name	Value									
WLAN Priority 0 = low 1 = high	1	1	1	X	0	0	0	0	0	0
WLAN Tx_Rx 0 = Rx 1 = Tx	1	1	0	0	1	1	0	0	1	1
Bluetooth Priority 0 = low 1 = high	X	X	X	X	0	1	0	1	0	1
Bluetooth Tx_Rx 0 = Rx 1 = Tx	0	1	1	0	0	0	1	1	1	1
Arbiter Decision (WL_Arb_TxOk_Cfg; BT_Arb_TxOk_Cfg registers)	WLAN Tx OK BT Rx OK	WLAN Tx OK BT Tx stop	WLAN Rx OK BT Tx stop	WLAN Rx OK BT Rx OK	WLAN Tx OK BT Rx OK	WLAN Tx stop BT Rx OK	WLAN Rx OK BT Tx stop	WLAN Rx OK BT Tx OK	WLAN Tx OK BT Tx stop	WLAN Tx stop BT Tx OK

7-4-2-2-2. Single Antenna System Configuration

For a single antenna system, WLAN and Bluetooth priority solely determines the arbiter decision. The result of this is that direction of data flow (Rx versus Tx) is ignored by the arbiter.
For this scheme, WLAN high-priority packets have priority over all Bluetooth packets by default. Bluetooth high-priority packets have priority over WLAN low-priority packets.
In this mode, the arbiter must generate three output signals (WL_Tx_SwGnt, WL_Rx_SwGnt, BT_SwGnt) to the SM. The SM controls the select signals to the external switch. The outputs to the SM follow the timing of the original request signals. The arbiter does not insert additional delay to compensate for any latency requirement required by the BBU/RF/external switch.

Table 7-5 Arbiter Decision Table, Bluetooth v1.2/v1.1 Device

Name	Value			
WLAN Priority 0 = low 1 = high	0	0	1	1
Bluetooth Priority 0 = low 1 = high	0	1	0	1
Arbiter Decision (SWL_Arb_TxOk_Cfg)	WLAN Tx/Rx OK Bluetooth Tx/Rx stop	WLAN Tx/Rx stop Bluetooth Tx/Rx OK	WLAN Tx/Rx OK Bluetooth Tx/Rx stop	WLAN Tx/Rx OK Bluetooth Tx/Rx stop

7-4-2-2-3. Arbitration Table Variables

Table 7-6 Arbitration Decision Variables

Variable	Description
WLAN_TX_RX	WLAN Tx/Rx Timeslot 0 = WLAN requests to receive, or the WLAN is in the middle of receiving a packet 1 = WLAN requests to transmit, or the WLAN is in the middle of transmitting a packet
BT_TX_RX	Bluetooth Tx/Rx Timeslot 0 = next Bluetooth timeslot is receive timeslot, or Bluetooth is in the middle of receiving a packet 1 = next Bluetooth timeslot is transmit timeslot, or Bluetooth is in the middle of transmitting a packet
Sleep Mode	Arbiter asserts WL_ACTIVE and Bluetooth device is always allowed to transmit when the WLAN module is in sleep mode.
Custom Coexistence Behavior	WLAN transaction decision and Bluetooth transaction decision outputs of the arbiter shown in Table 7-5 are generated from user-configurable vectors. The system designer can then overwrite the default values in the vectors and implement custom coexistence behavior. (See BT BCA WLAN TxOk Configuration, Offset 0x5DC, BT BCA Bluetooth TxOk Configuration, Offset 0x5E0 for Dual Antenna mode, and BT Configuration (3WBCA and 4WBCA), Offset 0x5A0 for Single Antenna mode in the WLAN MAC Registers section of the separate Network Registers document.)

7-4-2-3. WLAN Association Process

During the WLAN association process, the WLAN needs to have higher priority than the Bluetooth (this way also applies to Bluetooth voice). In this case, firmware can disable all Bluetooth traffic by programming 0x0 to BT_Arb_TxOk_Cfg, and can enable all WLAN traffic by programming 0xFFFFFFFF to WL_Arb_TxOk_Cfg. After the WLAN finishes the association process, firmware restores regular settings to the above two registers.

7-4-2-4. WLAN Sleep Duration

When the WLAN enters sleep mode, the arbiter always grants to Bluetooth. However, it is possible that when the WLAN first exits sleep mode, there is an ongoing Bluetooth transaction. The first WLAN Tx transaction may have higher priority than Bluetooth, and WLAN might Tx in the middle of a Bluetooth packet.

7-4-2-5. I/O Description

Table 7-7 I/O Description

Name	Type	Description
WLAN Coexistence Interface		
WL_ACTIVE	O	Bluetooth WLAN Active **2-Wire BCA Mode:** When high, WLAN is transmitting or receiving packets. **3-Wire BCA Mode:** 0 = Bluetooth device allowed to transmit 1 = Bluetooth device not allowed to transmit Once asserted, WL_ACTIVE stays asserted until the Bluetooth device completes the transmission. Once allowed to transmit, Bluetooth device cannot stop in the middle of packet. If asserted during Bluetooth transmission (so that the Tx has not been started), the Bluetooth module must not activate the transmitter during the rest of the Tx period.
BT_PRIORITY	I	Bluetooth Priority **2-Wire BCA Mode:** When high, Bluetooth is transmitting or receiving high priority packets. **3-Wire BCA Mode:** When high, Bluetooth is transmitting or receiving packets. Asserted 1 during local Bluetooth Rx and Tx slots.
BT_STATE	I	Bluetooth State 0 = normal priority, Rx 1 = high priority, Tx Priority is signaled after BT_PRIORITY has been asserted. After priority signaling, BT_STATE indicates the Tx/Rx mode of Bluetooth radio.
BT_FREQ	I	Bluetooth Hopping Frequency 0 = no frequency conflict between WLAN and next Bluetooth hopping frequency 1 = frequency conflict between WLAN and next Bluetooth hopping frequency Asserted (logic high) when the Bluetooth transceiver hops into the restricted channels defined by the coexistence mechanism.
BCA-WLAN-SM Interface (for Single Antenna Mode Only)		
WL_Tx_SwGnt	O	WLAN Tx Single Antenna Use 0 = BCA does not grant WL_Tx single antenna use 1 = BCA grants WL_Tx single antenna use The three grant outputs are always one-hot. When all grants de-assert, no request is coming from Bluetooth and WLAN.
WL_Rx_SwGnt	O	WLAN Rx Single Antenna Use 0 = BCA does not grant WL_Rx single antenna use 1 = BCA grants WL_Rx single antenna use The three grant outputs are always one-hot. When all grants de-assert, no request is coming from Bluetooth and WLAN.
BT_SwGnt	O	WL_SwGnt Single Antenna Use 0 = BCA does not grant WL_SwGnt single antenna use 1 = BCA grants WL_SwGnt single antenna use The three grant outputs are always one-hot. When all grants de-assert, no request is coming from Bluetooth and WLAN.

7-5. Switch Module

The switch module (SM) generates the switch control signals to the RF switch. The outputs are set by three input signals from the arbitration module and registers settings. The switch module is not responsible for requesting access to the medium, reporting WLAN or Bluetooth activity, nor for deciding who has access to the medium. The SM should be used primarily in single antenna mode. In two antenna mode, the arbitration logic will stop WLAN transmissions that could collide. In both antenna configurations, if none of the three transceiver paths is selected then the SM can give the antenna control signals (T/R_P, T/R_N, ANT_SEL_P/N) are independently set for each possible access condition (Bluetooth has access, WLAN Tx has access, WLAN Rx has access).

7-5-1. Switch Module Input Ports and States

Table 7-8 SM Input Ports and States

WL_Tx	WL_Rx	BT_TxRx	Result
0	0	0	Bluetooth has antenna (may be sent to WL_Rx or alternate)
0	0	1	Bluetooth has antenna
0	1	0	WL_Rx has antenna
0	1	1	Bluetooth has antenna (programmable)*1
1	0	0	WL_Tx has antenna
1	0	1	WL_Tx has antenna (programmable)*1
1	1	0	WL_Tx has antenna (programmable)*1
1	1	1	WL_Tx has antenna (programmable)*1

*1. More than one device is selected. The BCA unit will not generate this condition.

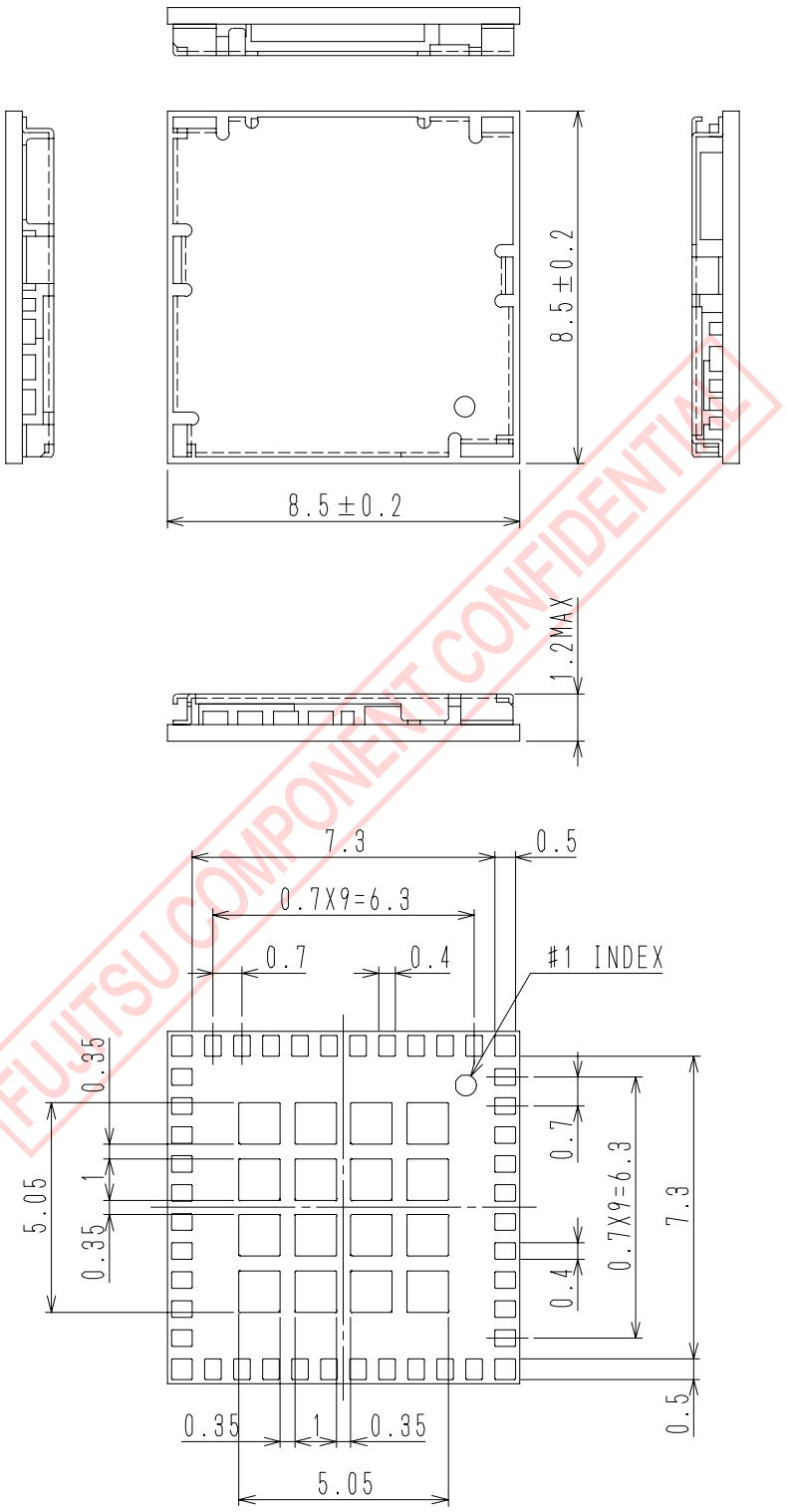
7-5-2. Switch Module Port List

Table 7-9 SM Port List

Module Port Name	I/O	Description
WLAN Tx	Input	Input signal to the switch module indicating the 802.11 transmit path should have access to the RF components. If WLAN Tx is asserted, neither WLAN Rx nor Bluetooth Tx/Rx should be asserted in single antenna mode. This signal comes from the arbitration engine.
WLAN Rx	Input	Input signal to the switch module indicating the 802.11 receive path should have access to the RF components. If WLAN Rx is asserted, neither WLAN Tx nor Bluetooth Tx/Rx should be asserted in single antenna mode. This signal comes from the arbitration engine.
Bluetooth Tx/Rx	Input	Input signal to the switch module indicating the Bluetooth device should have access to the RF components. If Bluetooth Tx/Rx is asserted, neither WLAN Tx nor WLAN Rx should be asserted in single antenna mode. This signal comes from the arbitration engine. Not used if the device is in dual antenna mode.
TR Switch P	Output	Output signal to one of the switch controllers. Value depends on who has access to the RF components and programmable registers. If BP_TR_SW is asserted, T/R_P is driven with this value.
TR Switch N	Output	Output signal to one of the switch controllers. Value depends on who has access to the RF components and programmable registers. If BP_TR_SW is asserted, T/R_N is driven with this value.
TR Switch 2P	Output	Output signal to the baseband. If BBU ANT_SEL is asserted, BBU drives the ANT_SEL_P pin with this value.
TR Switch 2N	Output	Output signal to the baseband. If BBU ANT_SEL is asserted, BBU drives the ANT_SEL_N pin with this value.

8. Mechanical Characteristics

8-1. Appearance and Dimensions

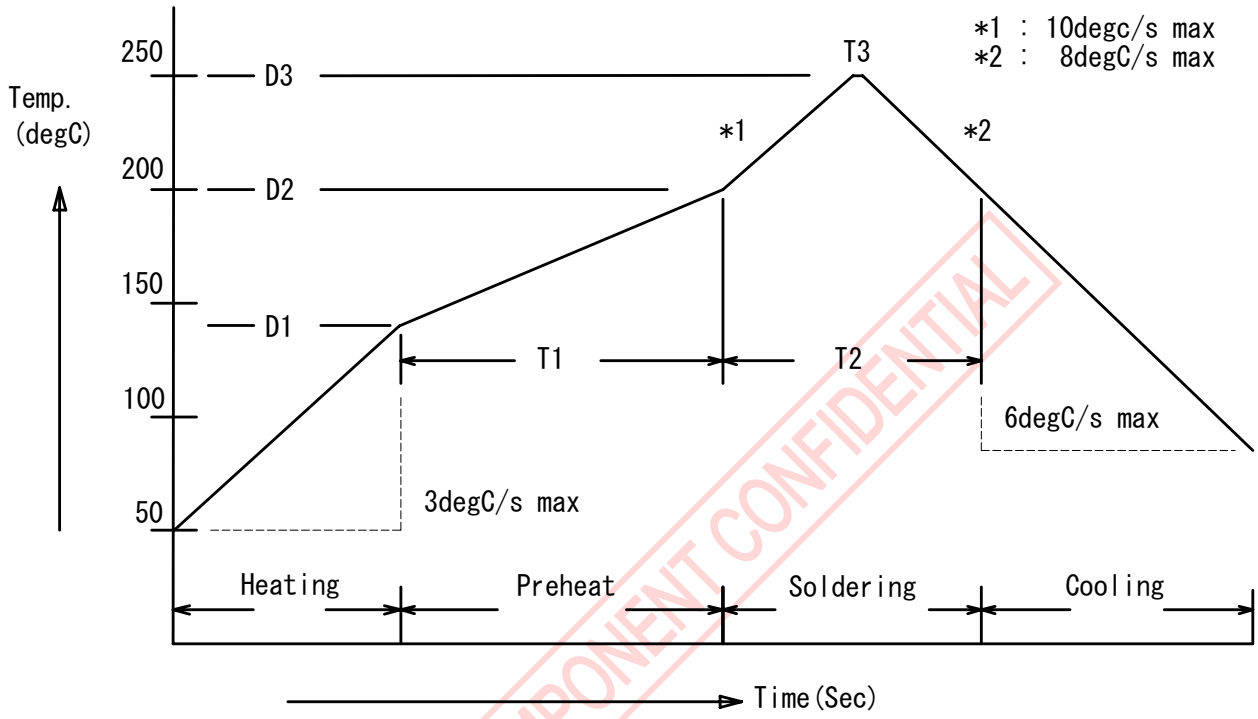


Unit: mm

8-2. Moisture Sensitivity Level

IPC/JEDEC Standard J-STD-020D: Level 3
In case of keeping except above condition, be sure to apply baking.
Baking Method: Ta = 60 °C, over 24 h

8-3. Recommended Reflow Profile



Note: * Reflow soldering is recommended two times maximum.

* If your soldering conditions are different from our recommendation, consult with us.

No.	Item	Temperature	Time (sec)
1	Pre-heart	D1 : 140 ~ D2 : 200	T1 : 60 ~ 120
2	Soldering	D2 ≥ 200	T2 : 80 max
3	Peak-Temp.	D3 : 250 max	T3 : 10 max

Reflow-Profile