CIPOS™ Maxi IPM

IM818 Series application note

About this document

Scope and purpose

The scope of this application note is to describe the IM818 product group of CIPOS™ Maxi family and the basic requirements for operating the products in a recommended mode. This is related to the integrated components, such as IGBT, diode or gate driver IC, as well as to the design of the necessary external circuitry, such as bootstrap or interfacing.

Intended audience

Power electronics engineers who want to design reliable and efficient CIPOS™ Maxi IPM applications.

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1 Scope

The scope of this application note is to describe the product group of IM818 and the basic requirements for operating the products in a recommended mode. This is related to the integrated components, such as IGBT or gate driver IC, as well as to the design of the necessary external circuitry, such as bootstrap or interfacing. Integrating discrete power semiconductors and gate driver ICs into one package allows design engineers to reduce the time and effort spent on design. To meet the strong demand for small size and higher power density, Infineon Technologies has developed a new family of highly integrated intelligent power modules that contain nearly all of the semiconductor components required to drive electronically controlled variable-speed electric motors. They incorporate a three-phase inverter power stage with an SOI gate driver and Infineon's leading-edge 1200 V TRENCHSTOP™ IGBT and Emitter Controlled-Diode.

The application note concerns the following products:

IM818-SCC

IM818-MCC

IM818 is a product group of CIPOS™ Maxi IPM family, which are designed for motor drives in commercial applications, such as fan drives, active filters for HVAC (heating, ventlating, and air-conditioning) systems, low power General Purpose Inverter (GPI), and pumps applications as well.

1.1 Product line-up

Table 1 Line-up of IM818 product

Part Number	Rating		Topologies	Package	Isolation voltage [Vrms]	Main applications
	Current [A]	Voltage [V]				
IM818-SCC	5	1200	3ϕ Bridge open emitter	Fully molded Dual In-Line(DIL) module with Direct Copper Bond(DCB) substrate	2500 Vrms/60 Hz (sinusoidal, 1 min. All pins shorted – heatsink)	Active filter for aircons, fans and pumps
IM818-MCC	10					

1.2 Nomenclature

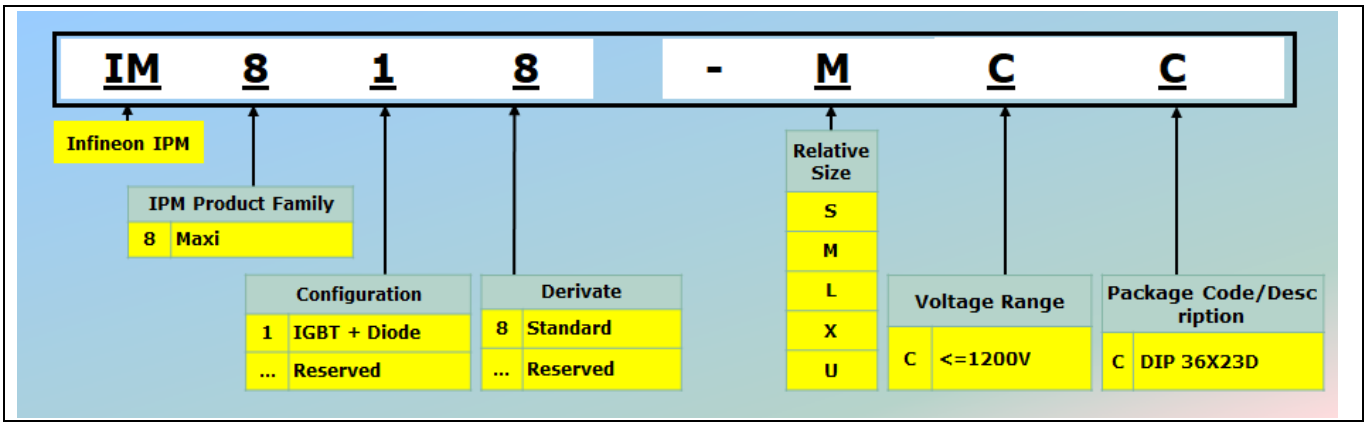


Figure 1 IM818 product group nomenclature

2 Internal components and package technology

2.1 Power transistor technology

2.1.1 1200 V TRENCHSTP™ IGBT4

Infineon Technologies introduced TRENCHSTOP™ IGBT4 technology in 2006 [1]. Infineon's TRENCHSTOP™ IGBT4 technology has led to significant improvements in the static as well as dynamic performance of the device, due to the combination of trenchstop-cell and fieldstop concept. The combination of IGBT with soft recovery Emitter Controlled-Diodes further minimizes the turn-on losses. Highest efficiency is reached due to the best compromise between switching and conduction losses. These technologies continue to possess the well-known robustness properties of Infineon's IGBTs, such as short-circuit withstand capability and maximum junction temperature.

2.1.2 1200 V Emitter Controlled-Diode

The Emitter Controlled-Diode uses Infineon's unique fast-recovery diode technology. The ultrathin wafer and field-stop technology makes the Emitter Controlled-Diode from Infineon ideally suited for consumer industry applications, as it lowers the turn-on losses of the IGBT with soft recovery.

2.2 Control IC - 1200 V 6-channel gate driver IC

The basic feature of this technology is the separation of the active silicon from the base material by means of a buried silicon oxide layer. The buried silicon oxide provides an insulation barrier between the active layer and silicon substrate and hence reduces the parasitic capacitance tremendously. Moreover, this insulation barrier disables leakage or latch-up currents between adjacent devices. This also prevents the latch-up effect even in case of high dv/dt switching under elevated temperature, and hence provides improved robustness. Besides the thin-film SOI technology provides additional benefits like lower power consumption and higher immunity to radioactive radiation or cosmic rays [2]. A monolithic single control IC for all 6 IGBTs provides further advantages, such as bootstrap circuitry, matched propagation delay times, built-in deadtime, cross conduction prevention, and all 6 IGBTs turn-off under fault situations like under-voltage lockout or over-current.

2.3 Thermistor

In IM818, the thermistor is integrated in the internal PCB. It is connected between the VTH and VSS pins. A circuit proposal using the thermistor for over-temperature protection is discussed in Section 5.5.

Table 2 Raw data of the thermistor used in IM818

T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]	T [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tol [%]
-40	2662.292	2962.540	3262.789	10.1	45	34.520	36.508	38.496	5.4
-35	1925.308	2133.692	2342.076	9.8	50	28.400	29.972	31.545	5.2
-30	1407.191	1553.414	1699.637	9.4	55	23.485	24.735	25.985	5.1
-25	1038.949	1142.63	1246.312	9.1	60	19.517	20.515	21.514	4.9
-20	774.497	848.747	922.997	8.7	65	16.296	17.097	17.898	4.7
-15	582.690	636.369	690.048	8.4	70	13.670	14.315	14.960	4.5
-10	442.252	481.410	520.568	8.1	75	11.517	12.039	12.561	4.3
-5	338.491	367.303	396.114	7.8	80	9.745	10.169	10.593	4.2

0	261.164	282.537	303.910	7.6	85	8.279	8.625	8.971	4.0
5	203.056	219.036	235.016	7.3	90	7.062	7.345	7.628	3.9
10	159.044	171.081	183.118	7.0	95	6.046	6.279	6.511	3.7
15	125.454	134.586	143.717	6.8	100	5.199	5.388	5.576	3.5
20	99.630	106.605	113.580	6.5	105	4.468	4.640	4.811	3.7
25	79.638	85.000	90.362	6.3	110	3.856	4.009	4.163	3.8
30	64.055	68.203	72.352	6.1	115	3.338	3.477	3.615	4.0
35	51.831	55.059	58.287	5.9	120	2.900	3.024	3.149	4.1
40	42.182	44.708	47.235	5.7	125	2.527	2.639	2.751	4.2

2.4 Package technology

The IM818 offers the smallest size while providing high power density up to 1200 V, 10 A by employing IGBTs and diodes with 6-channel gate driver ICs. It contains all the power components such as the IGBTs and diodes, and isolates them from each other and from the heat sink. All low power components such as the gate driver IC and thermistor are assembled on a PCB.

The electric insulation is provided by the DCB itself, which is simultaneously the thermal contact to the heat sink. In order to further decrease the thermal impedance, the internal lead frame design is optimized [3]. Figure 2 shows the external view and internal structure of IM818 package.

The two dummy pins on the package side which fix the inner PCB have no connection with the internal circuit, which means that the dummy pins have no electrical function and are isolated in the package.

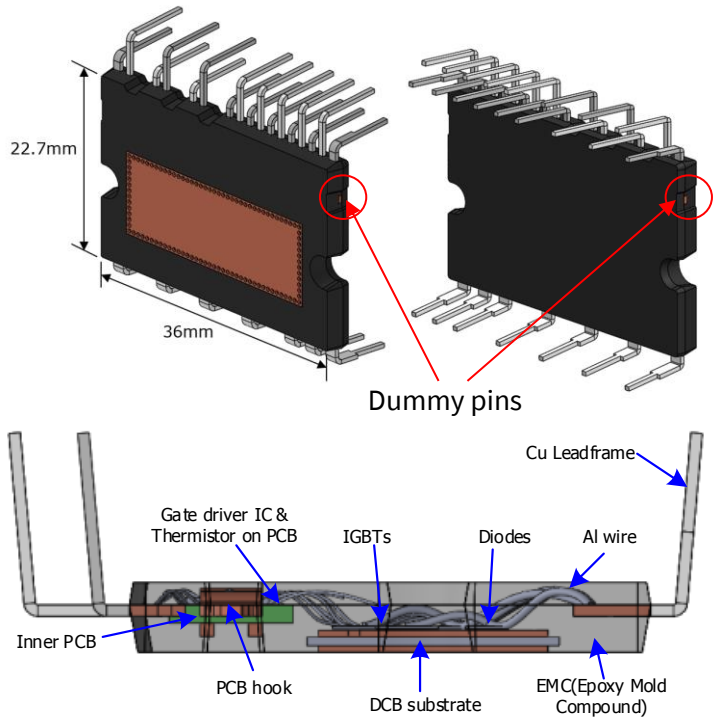


Figure 2 External view and internal structure of IM818 packages(DIP 36x23D)

3 Product overview

3.1 Internal circuit and features

Figure 3 illustrates the internal block diagram of the IM818. It consists of a three-phase inverter circuit and a gate driver IC with control functions. The detailed features and integrated functions of IM818 are described as follows.

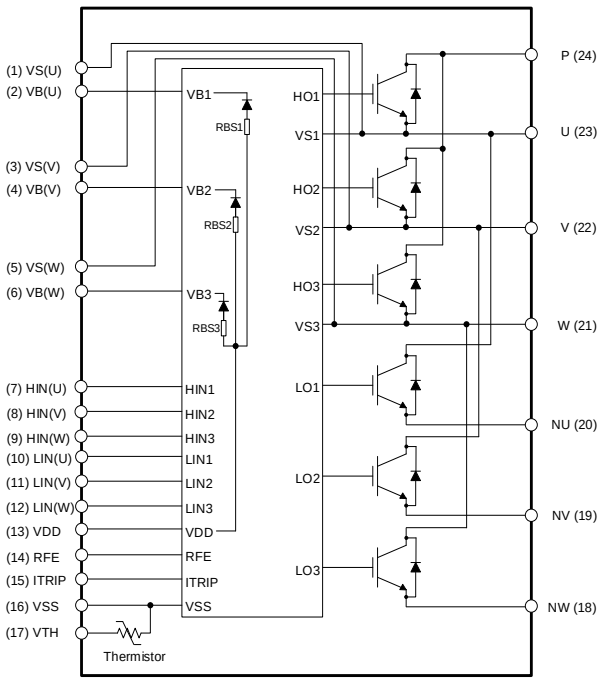


Figure 3 Internal circuit (3-phase inverter with open emitter)

Features

- 1200 V/5 A, 10 A rating in one physical package size (mechanical layouts are identical)
- Fully isolated DIL molded module with DCB substrate
- 1200 V TRENCHSTOP™ IGBT4 with anti-parallel diode(1200 V Emitter Controlled-Diode)
- Rugged 1200 V SOI gate driver technology with stability against transient and negative voltage
- Integrated bootstrap functionality
- Matched delay times of all channels/built-in deadtime
- Lead-free terminal plating; RoHS compliant

Functions

- Over-current shutdown
- Built-in, UL-certified NTC thermistor for temperature monitoring
- Under-voltage lockout at all channels
- Low-side emitter pins accessible for current monitoring
- Cross-conduction prevention
- All six switches turn off during protection
- Programmable fault clear timing and enable input

3.2 Maximum electrical ratings

Table 3 Detail description of absolute maximum ratings (IM818-MCC)

Item	Symbol	Rating	Description
Max. blocking voltage	V_{CES}	1200 V	The sustained collector-emitter voltage of internal IGBTs
DC collector current	I_C	±16 A	The allowable IGBT DC collector current at Tc = 25°C.
		±10 A	The allowable IGBT DC collector current at Tc = 80°C.
Junction temperature	T_J	-40 ~ 150°C	Considering temperature ripple on the power chips, the maximum junction temperature rating of the IPM is 150°C.
Operating case temperature range	T_C	-40 ~ 125°C	T_C (case temperature) is defined as the temperature of the package surface underneath the specified power chip. Please mount a temperature sensor on a heat-sink surface at the defined position in Figure 4, so as to get accurate temperature information.

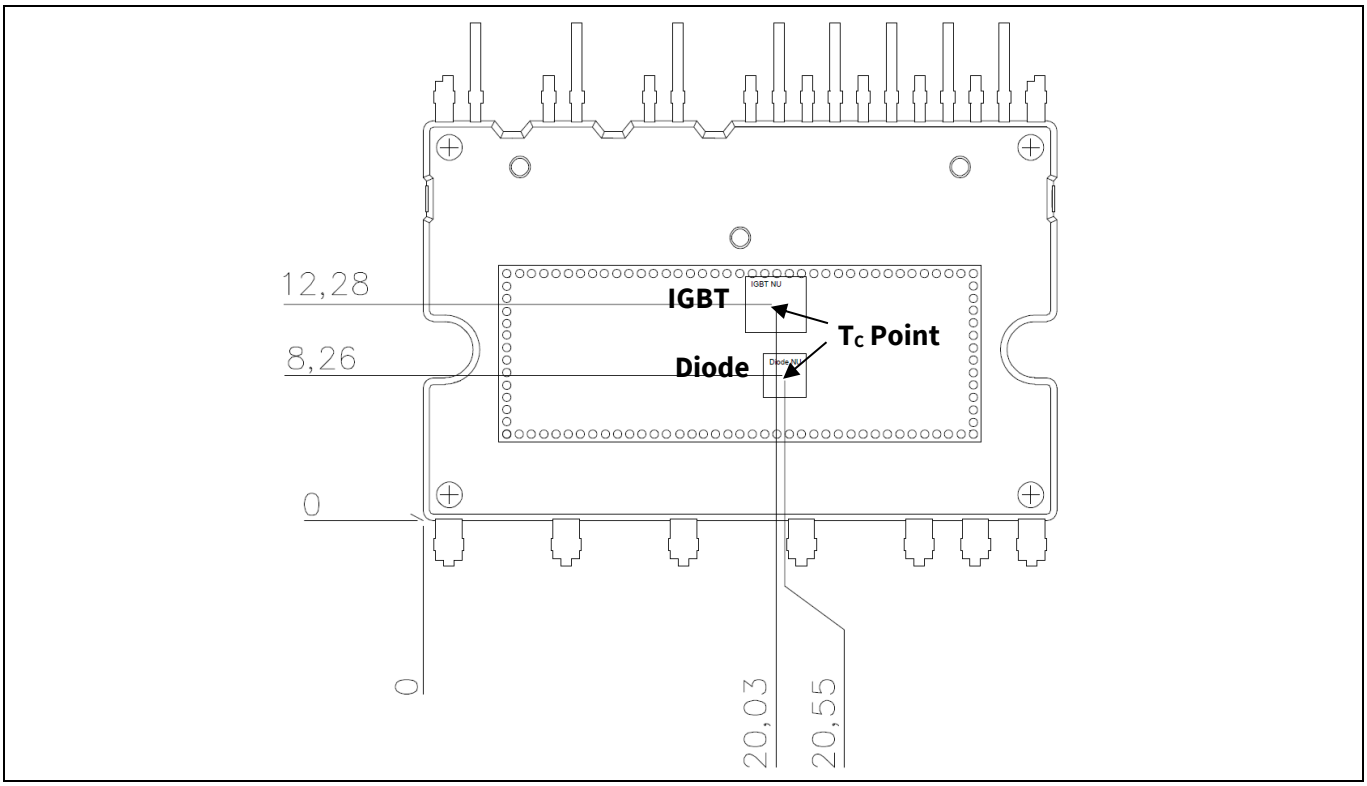


Figure 4 T_C measurement point (unit [mm])

3.3 Electrical characteristics

Table 4 and Table 5 shows static and dynamic characteristics of IM818-MCC.

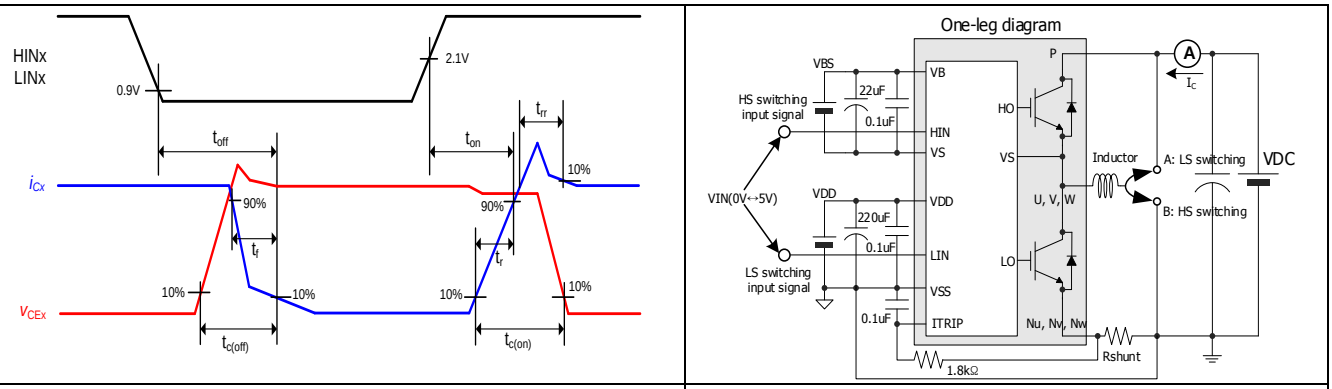
Table 4 Static characteristics of IM818-MCC(at V_{DD} = V_{BS} = 15 V)

Description	Symbol	Condition		Value			Unit
				Min.	Typ.	Max.	
Collector-emitter saturation voltage	$V_{CE(sat)}$	V_{IN} = 5 V, I_C = 10 A	T_J = 25°C	-	2.0	2.4	V
			T_J = 150°C	-	2.6	-	
Diode forward voltage	V_F	V_{IN} = 0 V, I_F = 10 A	T_J = 25°C	-	1.75	2.25	V
			T_J = 150°C	-	1.75	-	

Table 5 Dynamic characteristics of IM818-MCC (at V_{DD} = 15 V, T_J = 25°C)

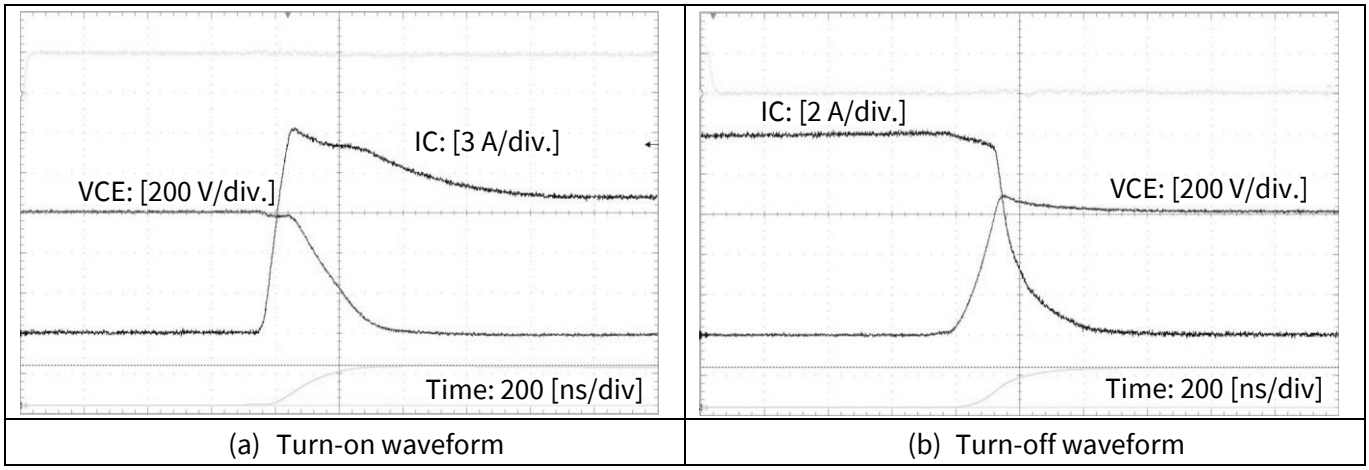
Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Turn-on propagation delay time	t_{on}	$V_{LIN, HIN}$ = 0 V ⟶ 5 V, I_C = 10 A, V_{DC} = 600 V	-	800	-	ns
Turn-on rise time	t_r		-	45	-	ns
Turn-on switching time	$t_{c(on)}$		-	230	-	ns
Reverse recovery time	t_{rr}		-	420	-	ns
Turn-off propagation delay time	t_{off}	$V_{LIN, HIN}$ = 5 V ⟶ 0 V, I_C = 10 A, V_{DC} = 600 V	-	960	-	ns
Turn-off fall time	t_f		-	100	-	ns
Turn-off switching time	$t_{c(off)}$		-	200	-	ns

The switching time definition and evaluation method are shown in Figure 5 (a) and (b). Switching characteristics measured by a half-bridge circuit with inductive load. Figure 6 shows a typical switching waveform of IM818-MCC at inductive load-switching test conditions as in Figure 5 (b).



(a) Switching time definition | (b) Inductive load switching test circuit

Figure 5 Switching time definition and evalution circuit for switching test

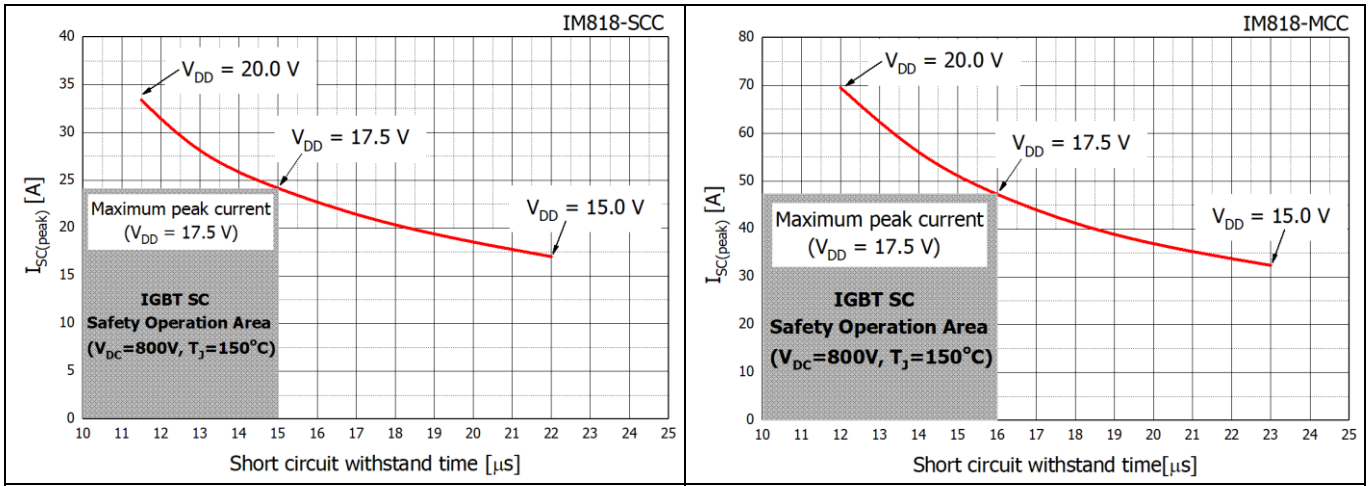


(a) Turn-on waveform | (b) Turn-off waveform

Figure 6 IM818-MCC typical switching waveform (V_{DC} = 600 V, V_{DD} = 15 V, I_C = 10 A, T_J = 150°C, inductive load = 3 mH)

3.4 SCSOA(short-circuit safety operation area) characteristics

Figure 7 shows the typical (not guaranteed) SCSOA performance graph of IM818 products under the short circuit status with the following conditions. In the case of IM818-MCC, the graph illustrates that if the short circuit time is less than 16.0 µs, IGBT has the ability to turn off safely. In this case, IGBT can shut down an SC current (non-repetitive) about 46.8 A_{peak} under a control supply voltage of 17.5 V.



(a) IM818-SCC | (b) IM818-MCC

Figure 7 Typical SCSOA graph of IM818 products(at V_{DC} = 800 V, $V_{PN(surege)}$ < 1200 V, T_J = 150°C)

3.5 Description of the input and output pins

Table 6 defines the IM818 input and output pins. The detailed functional descriptions are as follows:

Table 6 Pin descriptions of IM818

Pin Number	Pin Name	Pin Description
1	VS(U)	U-phase high side floating IC supply offset voltage
2	VB(U)	U-phase high side floating IC supply voltage
3	VS(V)	V-phase high side floating IC supply offset voltage
4	VB(V)	V-phase high side floating IC supply voltage
5	VS(W)	W-phase high side floating IC supply offset voltage
6	VB(W)	W-phase high side floating IC supply voltage
7	HIN(U)	U-phase high side gate driver input
8	HIN(V)	V-phase high side gate driver input
9	HIN(W)	W-phase high side gate driver input
10	LIN(U)	U-phase low side gate driver input
11	LIN(V)	V-phase low side gate driver input
12	LIN(W)	W-phase low side gate driver input
13	VDD	Low side control supply
14	RFE	Programmable fault clear time, fault output, enable input
15	ITRIP	Over current shutdown input
16	VSS	Low side control negative supply
17	VTH	NTC thermistor terminal
18	NW	W-phase low side emitter
19	NV	V-phase low side emitter
20	NU	U-phase low side emitter
21	W	Motor W-phase output
22	V	Motor V-phase output
23	U	Motor U-phase output
24	P	Positive bus input voltage

High-side bias voltage pins for driving the IGBT

Pins: VB (U, V, W) – VS (U, V, W)

- These pins provide the gate-drive power to the high-side IGBTs.
- The ability to utilize a bootstrap circuit scheme for the high-side IGBTs eliminates the need for external power supplies.
- Each bootstrap capacitor is charged from the VDD supply during the ON-state of the corresponding low-side IGBT or the freewheeling state of the low-side freewheeling diode.
- In order to prevent malfunctions caused by noise and ripple in the supply voltage, a good-quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins.

Low side-bias voltage pin

Pin: VDD

- This is the control supply pin for the internal IC.
- In order to prevent malfunctions caused by noise and ripples in the supply voltage, a good-quality (low ESR, low ESL) filter capacitor should be mounted very close to this pin.

Low-side common-supply ground pin

Pin: VSS

- This pin connects the control ground for the internal IC.

Signal input pins

Pins: HIN (U, V, W), LIN (U, V, W)

- These are pins used to control the operation of the internal IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt trigger circuit composed of 3.3 V/5 V-class CMOS.
- The signal logic of these pins is active-high. The IGBT associated with each of these pins will be turned "ON" when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the IM818 against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in Figure 10.

Over-current detection pin

Pin: ITRIP

- The current sensing shunt resistor should be connected between the N pin (emitter of low-side IGBT) and the power ground to detect short-circuit current (refer to Figure 15). An RC filter should be connected between the shunt resistor and the ITRIP pin to eliminate noise.
- The integrated comparator is triggered if the voltage V_{ITRIP} is higher than 0.5 V. The shunt resistor should be selected to meet this level for the specific application. In case of a trigger event, the voltage at the RFE pin is pulled down to LOW.
- The connection length between the shunt resistor and ITRIP pin should be minimized.

Fault output, fault-clear time, and enable pin

Pin: RFE

- The fault-out indicates a module failure in case of undervoltage at pin VDD or in case of triggered over-current detection at ITRIP. The alarm conditions are over-current detection and low-side bias UV (under voltage) operation.
- The programmable fault-clear time can be adjusted by the RC network, which is an external pull-up resistor and capacitor. For example, the typical value is about 1 ms at 1 MΩ and 2 nF.
- The microcontroller can pull this pin low to disable the IPM functionality. This is enable function.

NTC thermistor terminal pin

Pin: VTH

- This is the NTC thermistor terminal pin
- This pin provides direct access to the NTC thermistor, which is referenced to VSS. An external pull-up resistor connected to +5 V ensures that the resulting voltage can be directly connected to the microcontroller.

Positive DC-link pin

Pin: P

- This is the DC-link positive-power supply pin.
- It is internally connected to the collectors of the high-side IGBTs.
- In order to suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. (Typically metal film capacitors are used.)

Negative DC-link pins

Pins: NU, NV, NW

- These are the DC-link negative-power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of the each phase.

Inverter power output pins

Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e. g. motor).

3.6 Outline drawing

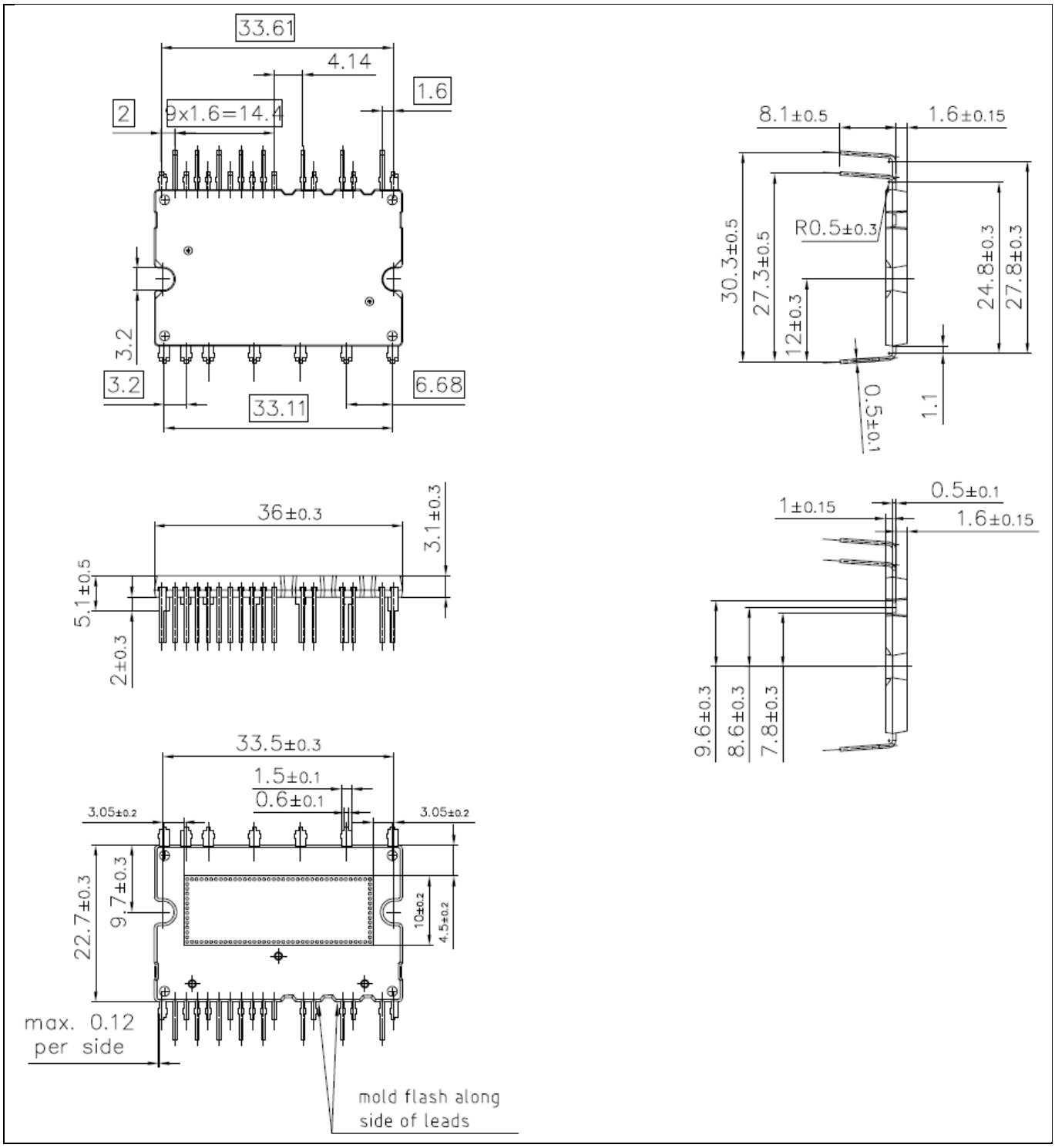


Figure 9 Package outline dimensions (Unit: [mm])

4 Interface circuit and layout guide

4.1 Input signal connection

Figure 10 shows the I/O interface circuit between micro-controller and IPM. The IPM input logic is active-high with internal pull-down resistors. External pull-down resistors are not needed.

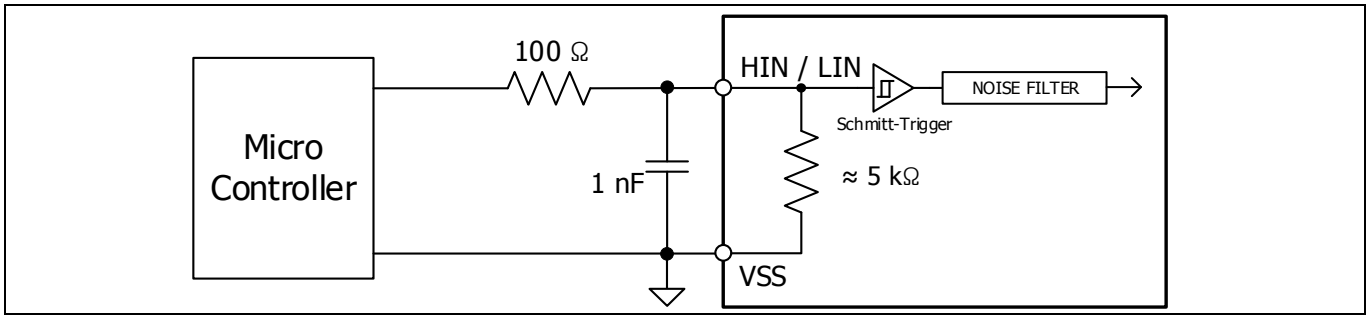


Figure 10 Recommended micro-controller I/O interface circuit

Table 7 Maximum ratings of inputs

Item	Symbol	Condition	Value	Unit
Module supply voltage	V_{DD}	Applied between VDD – VSS	-1 ~ 20	V
High- side floating supply voltage	V_{BS}	Applied between VB (U,V,W) – VS (U,V,W)	-1 ~ 20	V
Input voltage	V_{IN}	Applied between HIN (U,V,W) – VSS, LIN (U,V,W) – VSS	-1 ~ V_{DD}+0.3	V

The input maximum rating voltages are listed in Table 7. Since the input voltage rating is VDD+0.3 V, a 15 V supply interface is possible. However, it is recommended that the input signal be configured with the 5 V or 3.3 V logic supply for direct connect with the micro-controller. It is recommended to place bypass capacitors as close as possible to the signal lines from the micro-controller as well as the IPM.

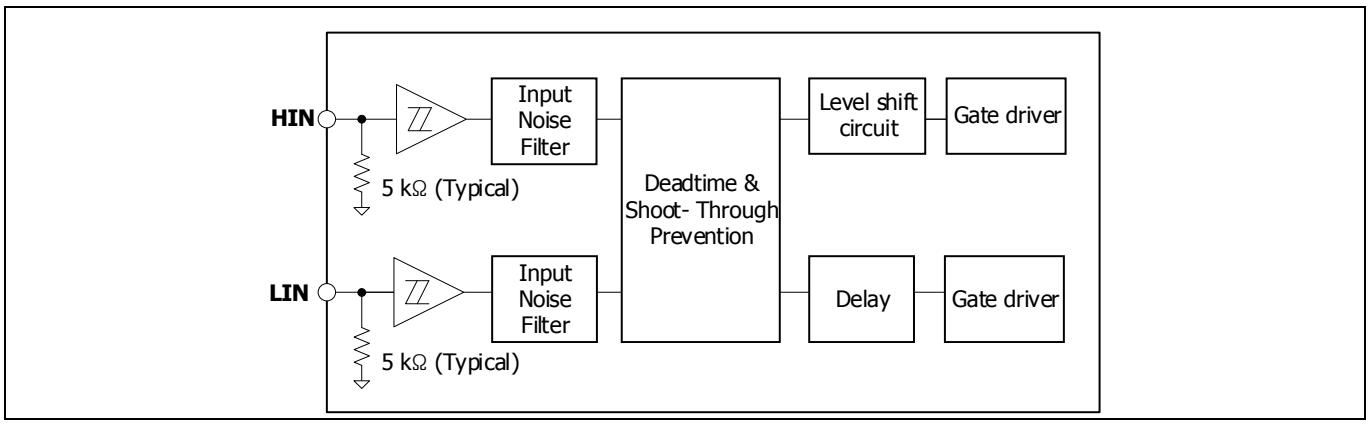


Figure 11 Simplified block diagram of IM818 gate driver IC

Because IM818 products employ active-high input logic, the power sequence restriction between the control supply and the input signal during start-up or shut-down operation does not exist. Therefore it makes the system fail-safe. In addition, pull-down resistors are built into each input circuit. Thus, external pull-down resistors are not needed. This reduces the required external component count. Input Schmitt-trigger, noise

filter, deadtime and shoot-through prevention functions provide beneficial noise rejection to short input pulses. Furthermore, the inputs of IM818 are compatible with standard CMOS and TTL outputs. The gate driver IC of IM818 has been designed to be compatible with 3.3 V and 5 V logic-level signals. Therefore, by lowering the turn-on and turn-off threshold voltage of input signal as shown in Table 8, a direct connection to 3.3 V / 5 V-class micro-controller or DSP is possible.

Table 8 Input threshold voltage (at VDD = 15 V, T_J = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic "1" input voltage (LIN, HIN)	V_{IH}	HIN – VSS	-	1.9	2.3	V
Logic "0" input voltage (LIN, HIN)	V_{IL}	LIN – VSS	0.7	0.9	-	V

As shown in Figure 11, the IM818 input signal section integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between micro-controller output and IPM input, pay attention to the signal voltage drop at the IPM input terminals. It should fulfill the logic "1" input voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown in Figure 10.

4.2 Internal deadtime

The gate driver IC of IM818 features integrated deadtime protection circuitry. The deadtime for gate driver IC is fixed. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on.
This minimum deadtime is automatically inserted whenever the external deadtime is shorter than DT_{IC}; external deadtimes larger than DT_{IC} are not modified by the gate driver IC.

Table 9 Internal deadtime (at VDD = 15 V, T_J = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal deadtime	DT_{IC}	V_{IN} = 0 or V_{IN} = 5 V	300	-	-	ns

4.3 Cross-conduction prevention circuitry

The gate driver IC of IM818 is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry or interlock circuitry). Figure 12 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time.

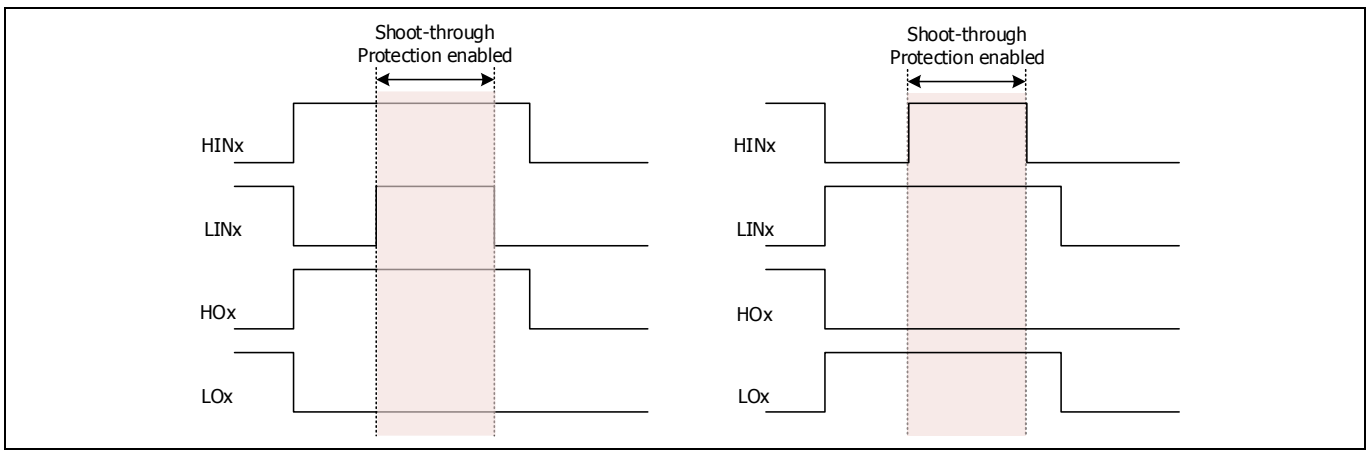


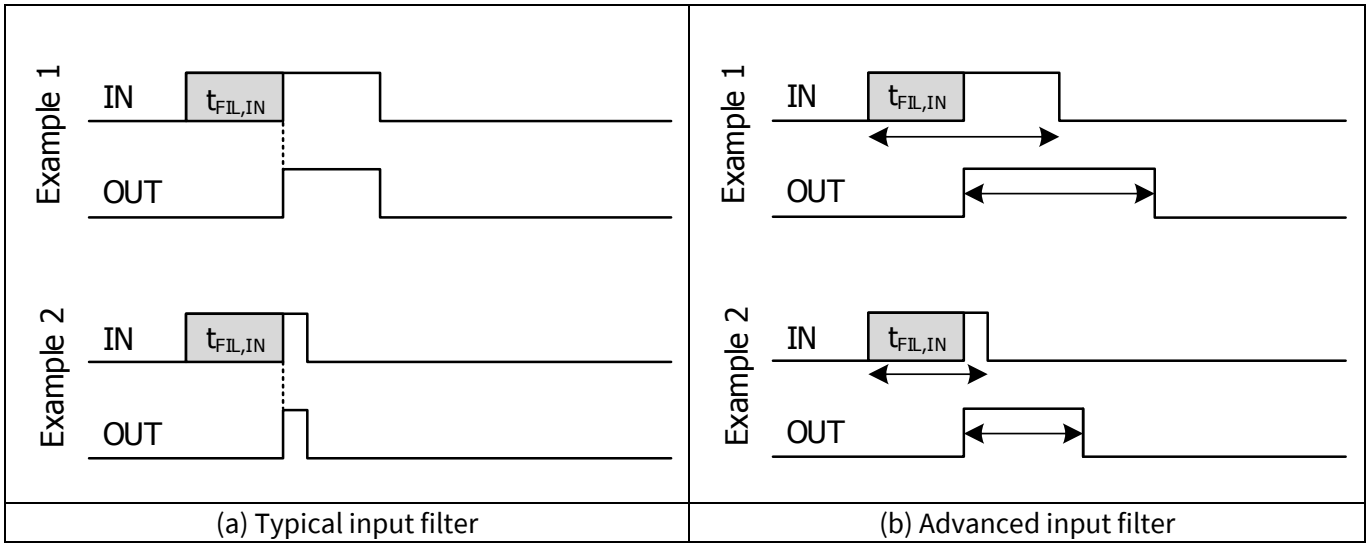
Figure 12 Illustration of shoot-through protection circuity

4.4 Advanced input filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the gate driver IC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN and LIN inputs. The working principle of the new filter is shown in Figure 13 (a), (b).
Figure 13 (a) shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal width with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.
Figure 13 (b) shows the advanced input filter of IM818 and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

Table 10 Input filter time (at VDD = 15 V, T_J = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input filter time at LIN, HIN for turn-on and off	$t_{FIL,IN}$	$V_{LIN, HIN}$ = 0 V or 5 V	-	350	-	ns



(a) Typical input filter (b) Advanced input filter

Figure 13 Internal Input filter characteristics

4.5 Matched propagation delay

The gate driver IC of IM818 is designed with propagation-delay matching circuitry. With this feature the internal gate driver IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay-matching parameter (M_T). The propagation turn-on delay (t_{ON}) of the IM818 is matched to the propagation turn-off delay (t_{OFF}). In other words, delay-matching turn-on/off between high-side and low-side meansthere is the time difference between the LO and HO outputs, when each output has reached 10% of its maximum (during turn-on), or when each output has decreased to 90% of its maximum (during turn-off), assuming that HINx and LINx are simultaneously applied. The shorter the delay-matching time, the better the circuit performance.

Table 11 Matching propagation delay time (at VDD = 15 V, T_J = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Matching propagation delay time (On & Off) all channels	M_T	External dead time >500 ns	-	-	130	ns

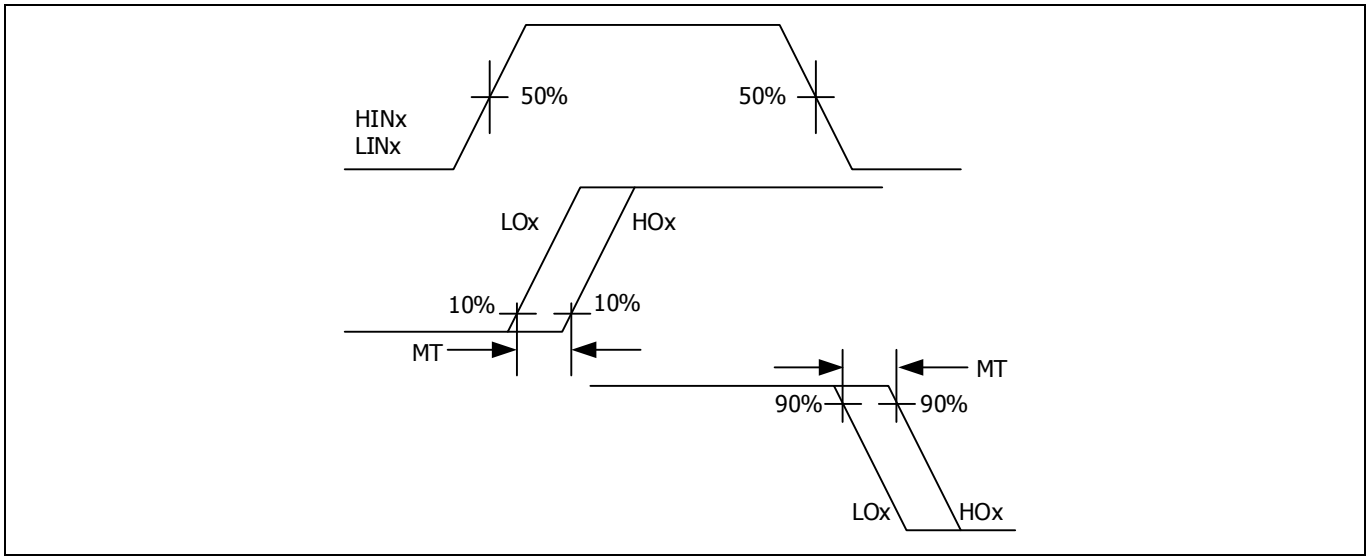


Figure 14 Delay-matching waveform definition

4.6 General interface circuit example

Figure 15 shows a typical application circuit of IM818 for interface schematic with control signals connected directly to a micro-controller.

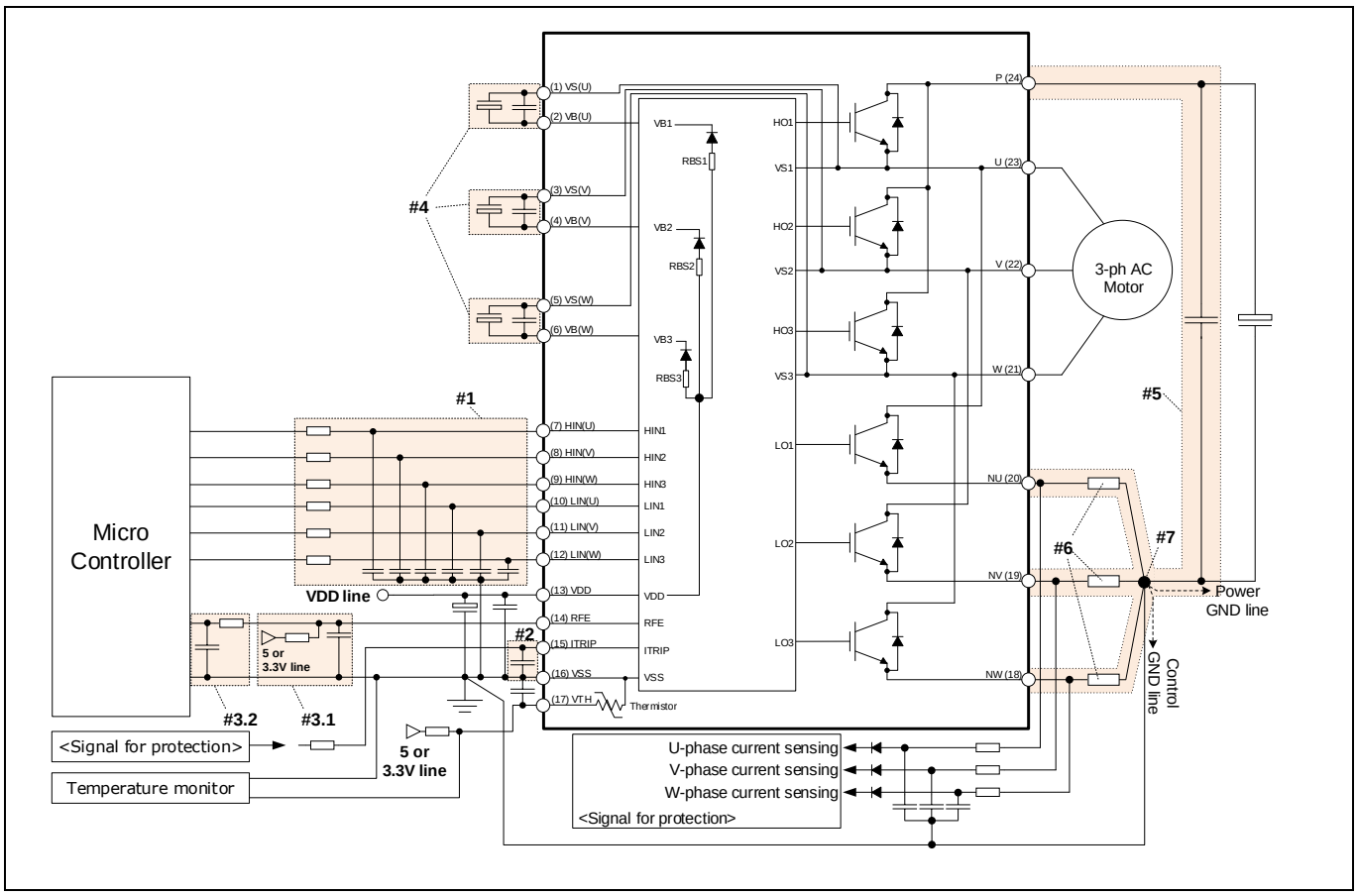


Figure 15 Application circuit example

Note:

1. Input circuit
   - To reduce input signal noise by high-speed switching, the R_{IN} and C_{IN} filter circuit should be mounted. (100 Ω, 1 nF)
   - C_{IN} should be placed as close to VSS pin as possible.
2. Itrip circuit
   - To prevent protection function errors, C_{ITRIP} should be placed as close to ITRIP and VSS pins as possible.
3. RFE circuit

   3.1 Pull-up resistor and pull-down capacitor
   - RFE output is an open-drain output. This signal line should be pulled up to the positive side of the 5 V / 3.3 V logic power supply with a proper resistor R_{PU}.
   - The fault-clear time is adjusted by RC network of a pull-up resistor, a pull-down capacitor and pull-up voltage.
     - $t_{FLTCLR} = -R_{pull\text{-}up} \cdot C_{pull\text{-}down} \cdot \ln(1 - V_{RFE,TH+} / V_{pull\text{-}up})$ + internal fault-clear time 160 µs
     - $t_{FLTCLR} = -1\ M\Omega \times 2\ nF \times \ln(1 - 1.9 / 5\ V) + 160\ \mu s \cong 1.1\ ms$ at R = 1 MΩ, C = 2 nF and $V_{pull\text{-}up}$=5 V
     - A pull-up resistor is limited to max. 2 MΩ

   3.2 RC filter
   - It is recommended that the RC filter be placed as close to the controller as possible.

4. VB-VS circuit
   - Capacitor for high-side floating supply voltage should be placed as close to VB and VS pins as possible.
5. Snubber capacitor
   - The wiring between IM818 and snubber capacitor including shunt resistor should be as short as possible.
6. Shunt resistor
   - The shunt resistor of SMD type should be used for reducing its stray inductance.
7. Ground pattern
   - Ground pattern should be separated at only one point of shunt resistor as short as possible.

4.7 Recommended rated output current of power supply

Control and gate drive power for the IM818 is normally provided by a single 15 V supply that is connected to the module VDD and VSS terminal. The circuit current of VDD control supply of IM818-MCC is shown in below Table 12.

Table 12 The circuit current of control power supply of IM818-MCC (Unit: [mA])

Item		Static (typ.)	Dynamic (typ.)	Total (typ.)
VDD = 15 V	FSW = 5 kHz	1.45	1.43	2.88
	FSW = 15 kHz	1.45	2.48	3.93
VDD = 20 V	FSW = 20 kHz	2.53	4.52	7.05

And, the circuit current of the 5 V logic power supply (RFE & input terminals) is about 5 mA.

Finally, the recommended minimum circuit currents of power supply are shown in Table 13 which takes into consideration ripple current and sufficient margins at the worst conditions, e.g. 5 times higher than the calculated value.

Table 13 The recommended minimum circuit current of power supply (Unit: [mA])

Item	The circuit current of +15 V control supply	The circuit current of +5 V logic supply
VDD ≤ 20 V, FSW ≤ 20 KHz	36.0	25.0

4.8 Recommended layout pattern for OCP & SCP function

It is recommended that the ITRIP filter capacitor connections to the IM818 pins be as short as possible. The ITRIP filter capacitor should be connected to the VSS pin directly without overlapped ground pattern. The signal ground and power ground should be as short as possible and connected at only one point via the filter capacitor of VDD line.

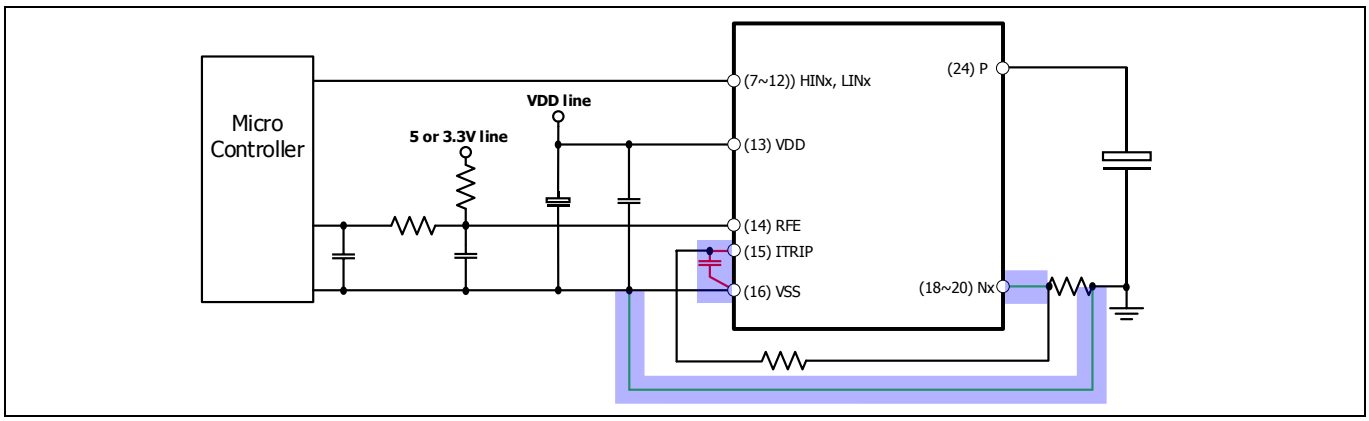


Figure 16 Recommended layout pattern for OCP & SCP function

4.9 Recommended wiring of shunt resistor and snubber capacitor

External current sensing resistors are applied to detect overcurrent of phase currents. A long wiring pattern between the shunt resistors and IM818 will cause excessive surges that might damage the IM818's internal IC and current detection components. This may also distort the sensing signals. To decrease the pattern inductance, the wiring between the shunt resistors and IM818 should be as short as possible.

As shown in Figure 17 snubber capacitors should be installed in the right location so as to suppress surge voltages effectively. Generally a high frequency non-inductive capacitor of around 0.1 ~ 0.22 µF is recommended. If the snubber capacitor is installed in the wrong location '1' as shown in Figure 17, the snubber capacitor cannot suppress the surge voltage effectively. If the capacitor is installed in location '2', the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current sensing signal and the SC protection level will be a little lower than the calculated design value. The "2" position surge suppression effect is greater than the location '1' or '3'. The '3' position is a reasonable compromise with better suppression than in location '1' without impacting the current sensing signal accuracy. For this reason, location '3' is generally used.

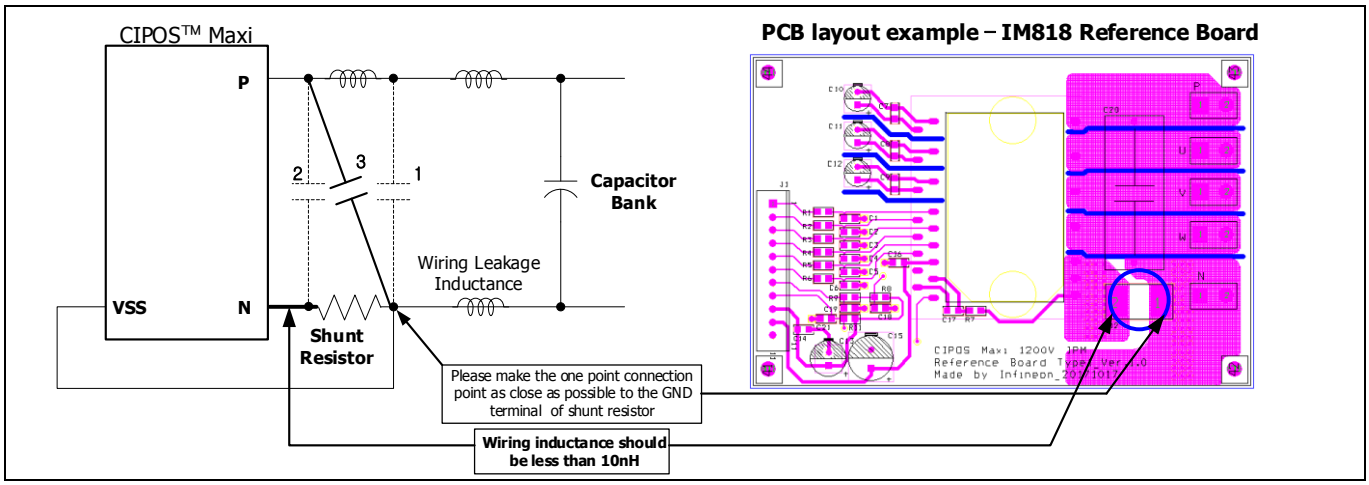


Figure 17 Recommended wiring of shunt resistor and snubber capacitor

4.10 Pin and screw hole coordinates for IM818 footprint

Figure 18 shows the IM818 position on the PCB to indicate center coordinates of each pin and screw hole in Table 14.

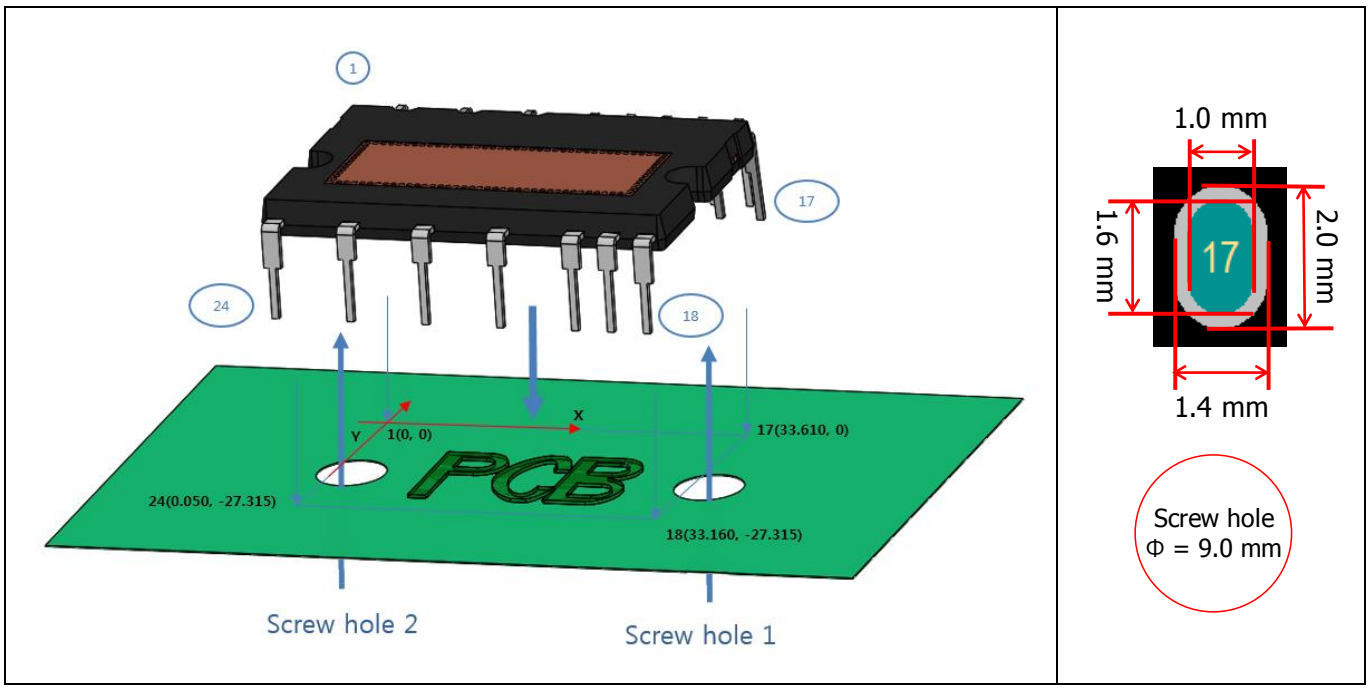


Figure 18 IM818 position on PCB (Unit: [mm]) and example of pad design(1~24pin)

Table 14 Pin & screw holes coordinates for IM818 footprint (Unit: [mm])

Pin Number		X	Y	Pin Number		X	Y
Signal Pin	1	0.000	0.000	Signal Pin	14	28.410	2.997
	2	1.600	2.997		15	30.010	0.000
	3	5.737	0.000		16	31.610	2.997
	4	7.337	2.997		17	33.610	0.000
	5	11.473	0.000	Power Pin	18	33.160	-27.315
	6	13.073	2.997		19	29.960	-27.315
	7	17.210	0.000		20	26.760	-27.315
	8	18.810	2.997		21	20.083	-27.315
	9	20.410	0.000		22	13.405	-27.315
	10	22.010	2.997		23	6.728	-27.315
	11	23.610	0.000		24	0.050	-27.315
	12	25.210	2.997	Screw Hole	1	33.355	-15.308
	13	26.810	0.000		2	-0.145	-15.308

5 Protection features

5.1 Under voltage protection

Control and gate drive power for the IM818 is normally provided by a single 15 V supply that is connected to the module VDD and VSS terminals. For proper operation this voltage should be regulated to 15 V±10%. Table 15 describes the behavior of the IM818 for various control supply voltages. The control supply should be well filtered with a low-impedance electrolytic capacitor and a high-frequency decoupling capacitor connected at the IM818's pins.

High-frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ± 1 V/µs.

The potential at the module's VSS terminal is different from that at the N power terminal by the voltage drop across the sensing resistor. It is very important that all control circuits and power supplies be referred to this point and not to the N terminal. If circuits are improperly connected, the additional current flowing through the sense resistor might cause improper operation of the short-circuit protection function. In general, it is best practice to make the common reference (VSS) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits to generate the floating supplies for the high-side gate drives.

When control supply voltage (V_{DD} and V_{BS}) falls down under UVLO (undervoltage lockout) level, IGBTs will turn off while ignoring the input signal.

Table 15 IM818 functions versus control power supply voltage

Control Voltage Range [V]	Function operations
0 ~ 4	Control IC does not operate. Undervoltage lockout and fault output do not operate.
4 ~ 12.5	When the undervoltage lockout function is activated, control input signals are blocked and a fault-out signal (V_{RFE}) is generated.
12.5 ~ 13.5	IGBTs will be operated in accordance with the control gate input. Driving voltage is below the recommended range, so the VCE (Sat) and the switching losses will be larger than under normal conditions. And high-side IGBTs cannot operate after V_{BS} initial charging, because VBS cannot reach V_{BSUV+}.
13.5 ~ 18.5 for VDD 12.5 ~ 18.5 for VBS	Normal operation. This is the recommended operating condition. VDD of 15 V is recommended when only integrated bootstrap circuitry is used.
18.5~ 20 for VDD, VBS	IGBTs are still operated. Because driving voltage is above the recommended range, IGBTs' switching is faster. It causes increasing system noise. And peak short-circuit current might be too large for proper operation of the short-circuit protection.
Over 20	Control circuit in the IM818 might be damaged.

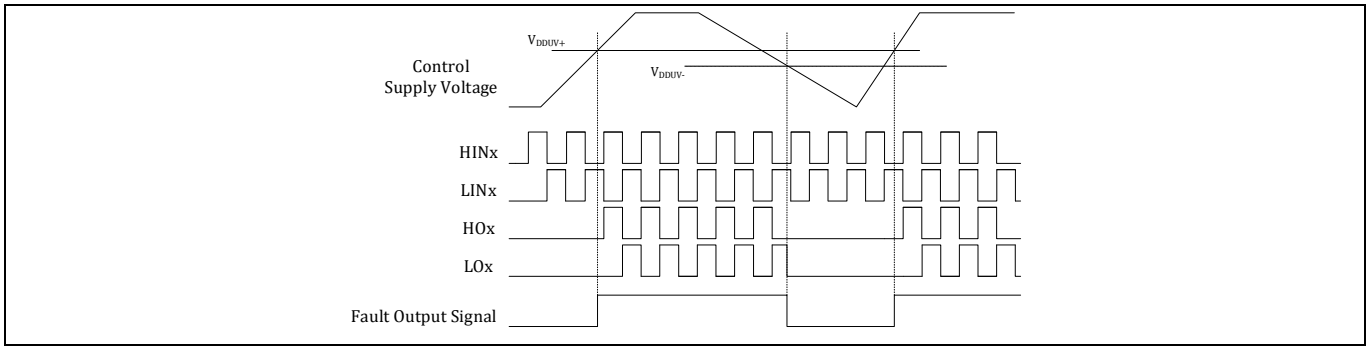


Figure 19 Timing chart of low-side undervoltage protection function

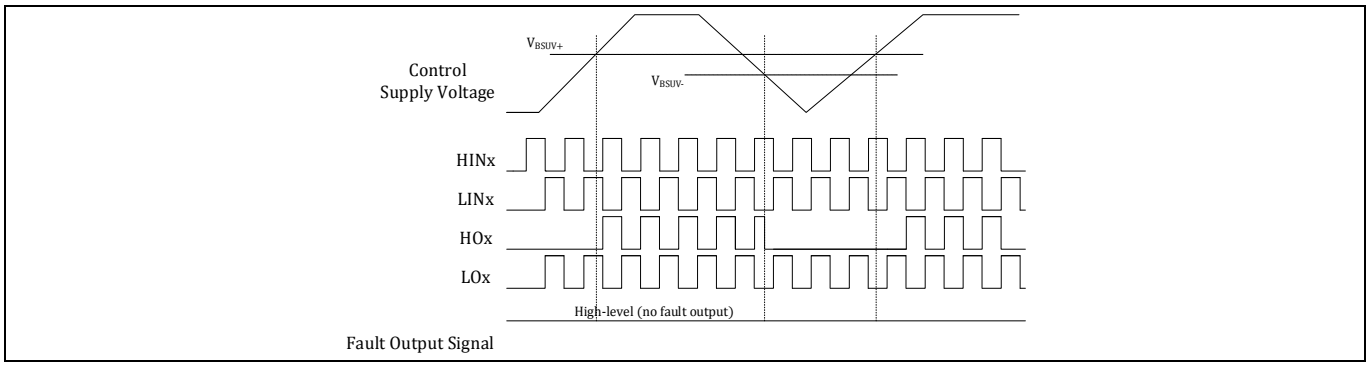


Figure 20 Timing chart of high-side undervoltage protection function

5.2 Overcurrent protection

5.2.1 Timing chart of overcurrent (OC) protection

The IM818 has an overcurrent shutdown function. Its internal IC monitors the voltage of the ITRIP pin, and if this voltage exceeds the $V_{IT,TH+}$, which is specified in the devices datasheets, a fault signal is activated and all IGBTs are turned off. Typically the maximum short-circuit current magnitude is gate-voltage dependant. A higher gate voltage results in a larger short-circuit current. In order to avoid this potential problem, the maximum over-current trip level is usually set to below 2 times the nominal rated collector current. The overcurrent protection-timing chart is shown in Figure 21.

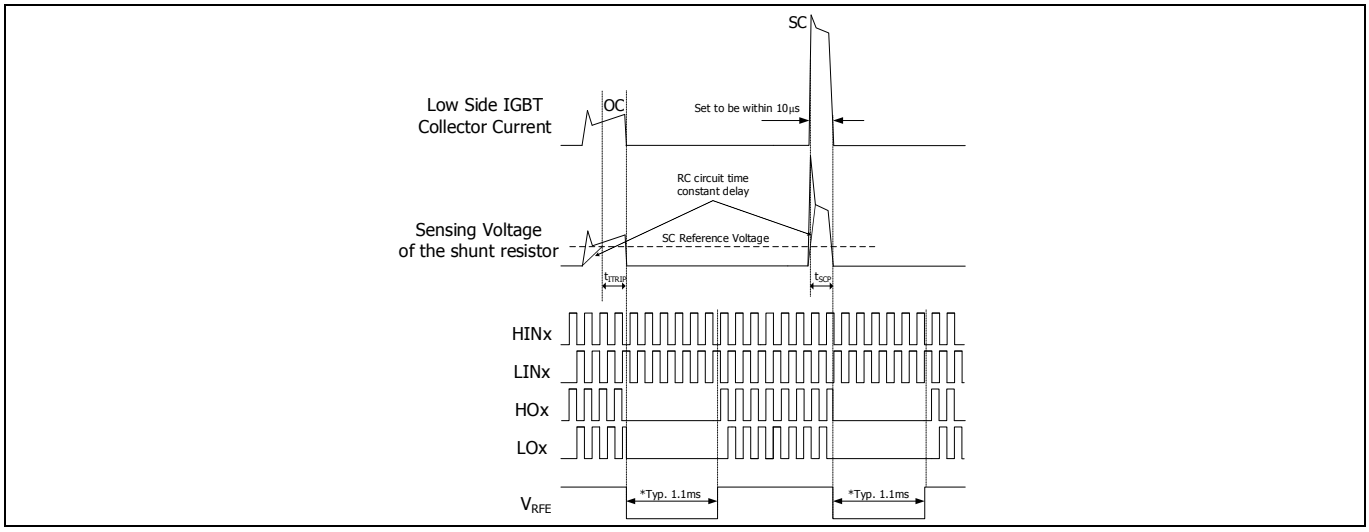


Figure 21 Timing chart of overcurrent protection function
(*$t_{FLT,CLR}$ is defined by R_{RCIN}, C_{RCIN}, please refer to section 5.3)

5.2.2 Selecting current sensing shunt resistor

The value of the current sensing resistor is calculated by the following expression:

$$R_{SH} = \frac{V_{IT,TH+}}{I_{OC}} \quad (1)$$

Where $V_{IT,TH+}$ is the ITRIP positive-going threshold voltage of IM818. It is typically 0.5 V. I_{OC} is the current of OC detection level.

The maximum value of OC protection level should be set lower than the repetitive peak collector current in the datasheet taking into consideration the tolerance of the shunt resistor. For example, the maximum peak collector current of IM818-MCC is 20 A_{peak}, and thus, the recommended value of the shunt resistor is calculated as

$$R_{SH(\min)} = \frac{0.5}{20} = 0.025\ \Omega$$

For the power rating of the shunt resistor, the following list should be considered:

- Maximum load current of inverter (I_{rms})
- Shunt resistor value at Tc = 25°C (R_{SH})
- Power derating ratio of shunt resistor at T_{SH}=100°C according to the manufacturer's datasheet
- Safety margin

The shunt resistor power rating is calculated by the following equation.

$$P_{SH} = \frac{I_{rms}^2 \times R_{SH} \times margin}{derating\ ratio} \quad (2)$$

For example, in the case of IM818-MCC and R_{SH} = 25 mΩ (LR2728: RARA)

- Max. load current of the inverter : 6 A_{rms}
- Power derating ratio of shunt resistor at T_{SH}=100°C: 65%
- Safety margin : 30%

$$P_{SH} = \frac{6^2 \times 0.025 \times 1.3}{0.65} = 1.8\ W$$

A proper power rating of shunt resistor exceeds 1.8 W, e.g. 2 W. In addition, we recommend SMD type shunt resistor in order to minimize surge voltage by stray inductance of shunt resistor.

Model	Power rating	Max. rating current [A]	Max. overload current [A]	Operating temp. range [°C]
LR2728	3.0 [W] at 70°C	27.39	47.43	-55 ~ 170

Based on the previous equations, conditions, and calculation method, the minimum shunt resistance and resistor power of IM818 products have been introduced as listed in Table 16. It is noted that a proper resistance and power rating higher than the minimum value should be chosen considering the over-current protection level required in the application.

Table 16 Minimum R_{SH} and P_{SH}

Product	Max. peak current	Min. shunt resistance, R_{SH}	Min. shunt resistor power, P_{SH}
IM818-MCC	20 A	25 mΩ	2.0 W
IM818-SCC	10 A	50 mΩ	2.0 W

5.2.3 Delay time

The RC filter is necessary in the overcurrent sensing circuit to prevent malfunction of OC protection caused by noise. The RC time constant is determined by considering the noise duration and the short-circuit withstand time capability of the IGBT.

When the sensing voltage on shunt resistor exceeds the ITRIP positive-going threshold ($V_{IT,TH+}$), this voltage is applied to the ITRIP pin of the IPM via the RC filter. Table 17 shows the specification of the OC protection reference level. The filter delay time (t_{Filter}) until that the input voltage of ITRIP pin rises to the ITRIP positive threshold voltage is defined by the following equation (3), (4).

$$V_{IT,TH+} = R_{SH} \cdot I_C \cdot (1 - \frac{1}{e^{\frac{t_{Filter}}{\tau}}}) \quad (3)$$

$$t_{Filter} = -\tau \cdot \ln(1 - \frac{V_{IT,TH+}}{R_{SH} \cdot I_C}) \quad (4)$$

Where, $V_{IT,TH+}$ is the ITRIP pin input voltage, I_C is the peak current, R_{SH} is the shunt resistor value and τ is the RC time constant. In addition there is a short-circuit propagation delay time of Itrip (t_{SCP}) which is defined by the propagation delay time from $V_{IT,TH+}$ to 10% of I_{SC}. Please refer to Table 18.

Table 17 Specification of OC protection reference level $V_{IT,TH+}$

Item	Symbol	Min.	Typ.	Max.	Unit
ITRIP positive-going threshold	$V_{IT,TH+}$	0.475	0.500	0.525	V

Table 18 Shut-down propagation delay

Item		Condition	Min.	Typ.	Max.	Unit
Short-circuit propagation delay time (t_{SCP})	IM818-SCC	From $V_{IT,TH+}$ to 10% I_{SC}	-	1100	-	ns
	IM818-MCC	From $V_{IT,TH+}$ to 10% I_{SC}	-	1200	-	

Therefore, the total time from ITRIP positive-going threshold ($V_{IT,TH+}$) to the shut-down of the IGBT becomes:

$$t_{total} = t_{Filter} + t_{SCP}$$

The short-circuit propagation delay can be changed by operating conditions such as operating temperature and V_{DD}, V_{DC}. The total delay must be less than the 10 µs of short-circuit withstand time (t_{SC}) in the datasheet. Thus, the RC time constant should be set in the range of 6 ~ 7 µs. However, the practical RC time constant value is 1 ~ 2 µs, so recommended values for the filter components are R7 = 1.8 kΩ and C17 = 1 nF.

5.3 RFE circuit

The RFE pin combines three functions in one pin: fault output, enable input, and RC-network-based programmable fault clear timing.

The RFE pin is normally connected to an RC network on the application circuit in Figure 22. Under normal operating conditions, R_{RCIN} pulls the RFE pin to 5 V, thus enabling all the functions in the IPM. The mircocontroller can pull this pin low to disable the IPM functionality. This is the Enable function.

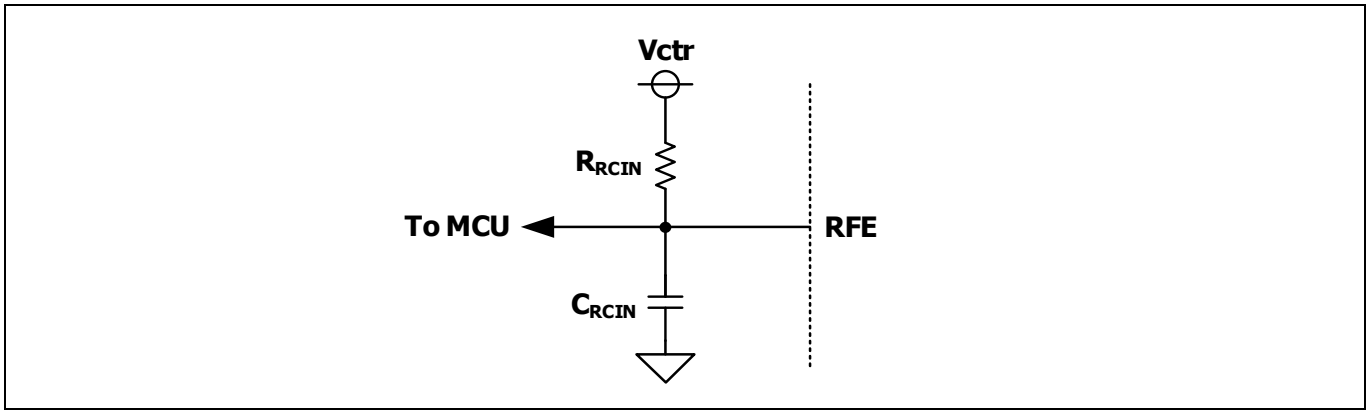


Figure 22 Typical application circuit for RFE pin

The fault-out function allows the IM818 to report a fault event to the MCU by pulling the RFE pin low in one of two situations. The first is an undervoltage condition on V_{DD} and the second is when the ITRIP pin detects a voltage rising above $V_{RFE,TH+}$.

The programmable fault-clear timing function provides a means of automatically re-enabling the IPM operation a preset amount of time ($T_{FLT,CLR}$) after the fault event has disappeared. Figure 23 shows the RFE-related circuit block diagram inside the IM818.

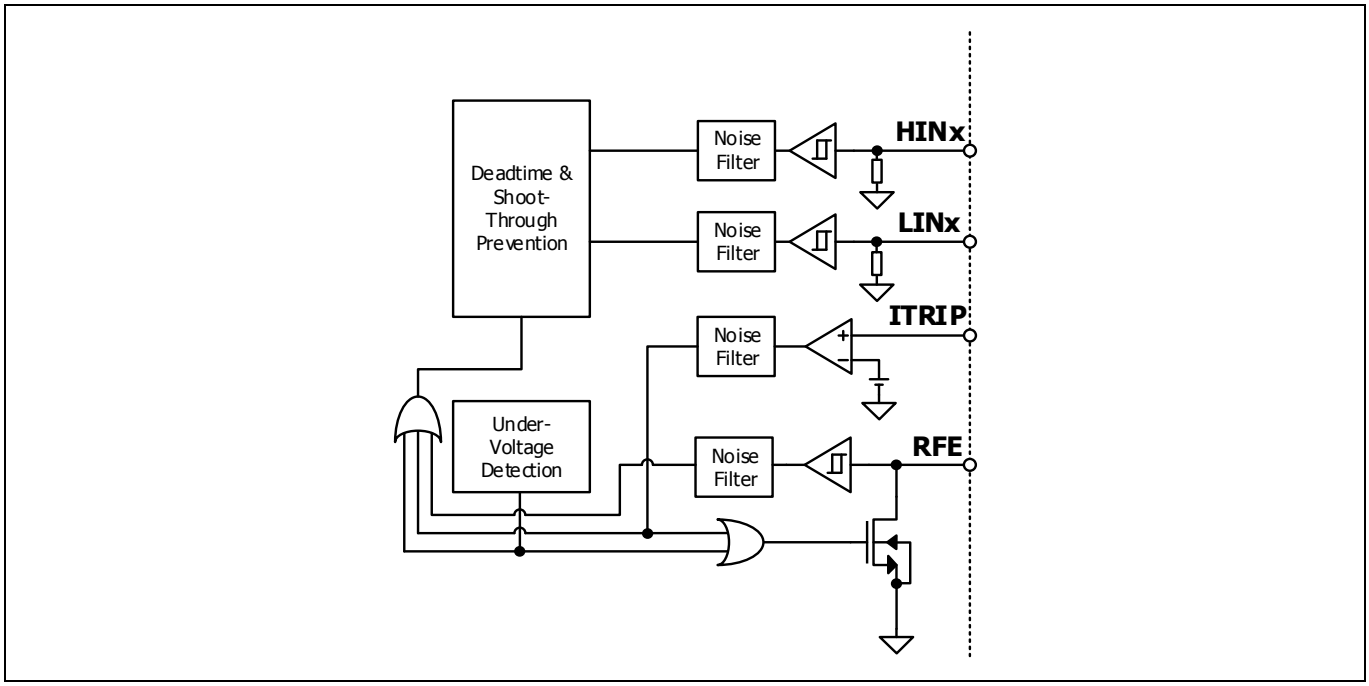


Figure 23 RFE internal circuit diagram

The legth of total $T_{FLT,CLR}$ can be determined by using the formula below.

$$RFE(t) = Vctr \times \left(1 - e^{-\frac{t}{RC}}\right)$$

$$Total\ T_{FLT,CLR} = -R_{RCIN} \times C_{RCIN} \times \ln\left(1 - \frac{V_{RFE,TH+}}{V_{ctr}}\right) + \text{Internal fault-clear time } (T_{FLT,CLR})$$

For example, if V_{ctr} is 5.0 V, R_{RCIN} is 1 MΩ , and C_{RCIN} is 2 nF,

$$Total\ T_{FLT,CLR} = -1\ M\Omega \times 2\ nF \times \ln\left(1 - \frac{1.9\ V}{5.0\ V}\right) + 160\ \mu s\ \cong 1.1\ ms$$

Table 19 Examples of total $t_{FLT,CLR}$

V_{CTR} [V]	R_{RCIN} [MΩ]	C_{RCIN} [nF]	Total $T_{FLT,CLR}$ [ms]	V_{CTR} [V]	R_{RCIN} [MΩ]	C_{RCIN} [nF]	Total $T_{FLT,CLR}$ [ms]
3.3	2.0	1.0	1.9	**5.0**	2.0	1.0	1.1
	1.0	1.0	1.0		1.0	1.0	0.6
	0.5	1.0	0.6		0.5	1.0	0.4
	2.0	2.0	3.6		2.0	2.0	2.1
	1.0	2.0	1.9		1.0	2.0	1.1
	0.5	2.0	1.0		0.5	2.0	0.6

Table 20 RFE maximum rating

Item	Symbol	Condition	Rating	Unit
RFE voltage	V_{RFE}	Applied between RFE-VSS	-1~ V_{DD} + 0.3	V

Table 21 Electric characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
RFE output voltage	V_{RFE}	I_{RFE} = 10 mA, V_{ITRIP} = 1 V	-	0.7	-	V
RFE MOSFET Resistance	$R_{ON,RFE}$	-	-	40	70	Ω
RFE positive-going threshold	$V_{RFE,TH+}$	-	-	1.9	2.3	V
RFE negative-going threshold	$V_{RFE,TH-}$	-	0.7	0.9	-	V

Because the RFE terminal is an open-drain type, it must be pulled up to the high level via a pull-up resistor. The resistor has to be calculated according to the above specifications.

5.4 Sleep function

The sleep function is activated after each trigger of ITRIP or undervoltage lockout. A new edge of each individual control signal LINx and HINx for activation of the outputs LOx or HOx is mandatory after release of signal RFE (fault out function). Please refer to Figure 24 for the description of the timing diagram.

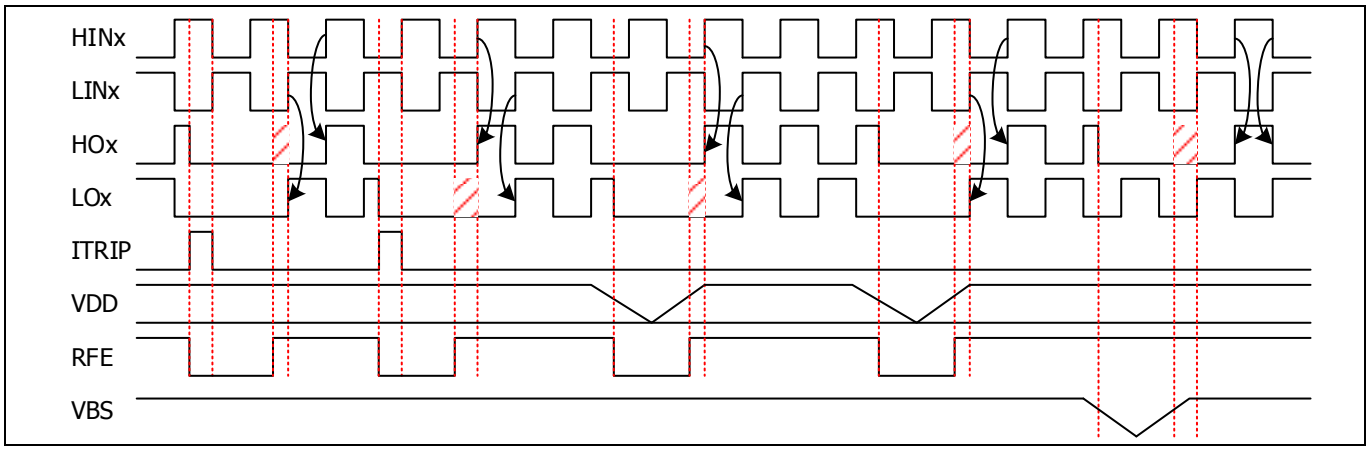


Figure 24 Sleep-function timing diagram ITRIP and UVLO

5.5 Temperature monitor and thermal protection

The IM818 have independent pins for internal thermistors (85 kΩ at 25°C). The built-in thermistor is directly connected to the VSS internally. The typical application circuit looks like Figure 26. An external pull-up resistor connected to V_{ctr} ensures that the resulting voltage can be directly connected to the MCU.

In this reference board, the pull-up resistor is set to 18 kΩ so that the VTH voltage becomes 1.15 V and 0.75 V respectively for 5 V and 3.3 V control voltage (V_{ctr}) when the thermistor temperature is 100°C, as shown in Figure 27.

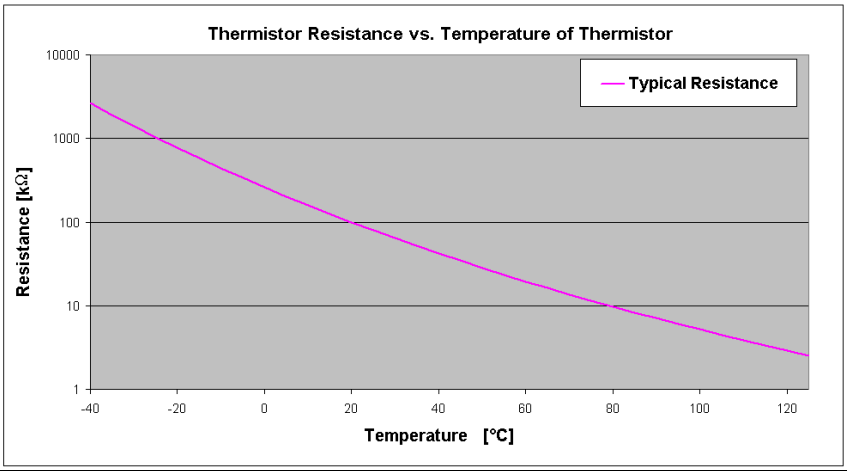


Figure 25 Internal thermistor resistance characteristics as a function of thermistor temperature

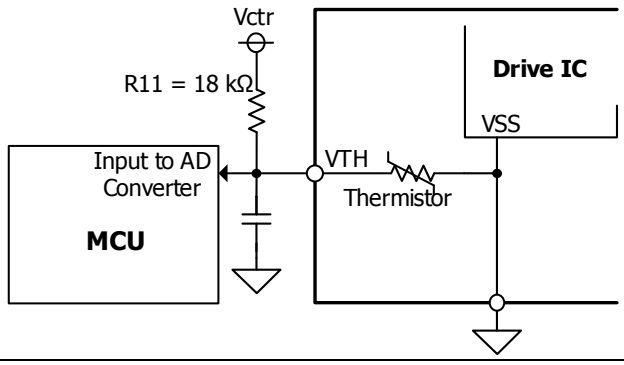


Figure 26 Circuit proposals for overtemperature protection

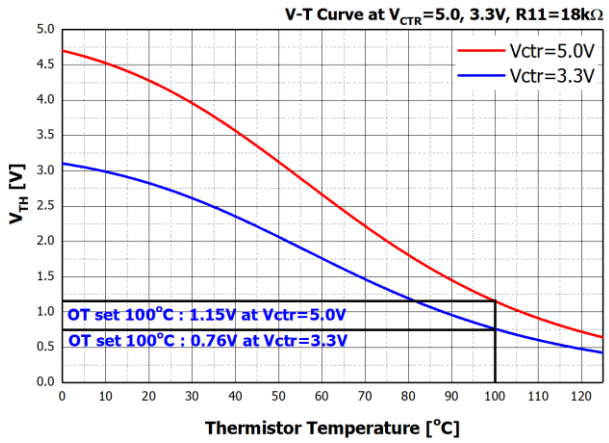
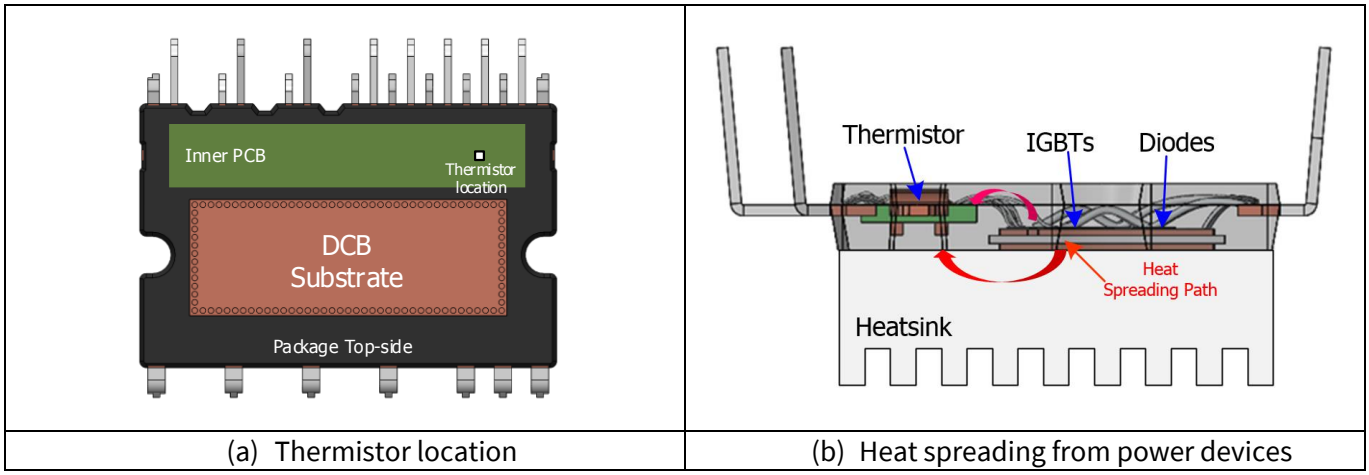


Figure 27 Voltage of VTH pin according to thermistor temperature

The NTC thermistor is located on the inner PCB of the IPM as in Figure 28(a). So, thermistor temperature can not reflect power chip temperature directly. When the IPM is operated, the heat of power devices is transferred to the thermistor through the heatsink and package as seen in Figure 28(b).

Figure 29 shows the relationship between $T_{J(ave)}$(IGBT's average junction temperature), T_C (IPM case temperature), and T_{NTC}(thermistor temperature) under given conditions. However, this relationship is just one of example, as the relationship depends on the system conditions such as heatsink size, cooling system, control scheme, etc. Therefore, if the user would like to know the relationship between $T_{J(ave)}$, T_C, and T_{NTC} on their system, we recommend that they define the relationship by themselves with their own system.



(a) Thermistor location | (b) Heat spreading from power devices

Figure 28 Thermistor location and heat spreading from power devices

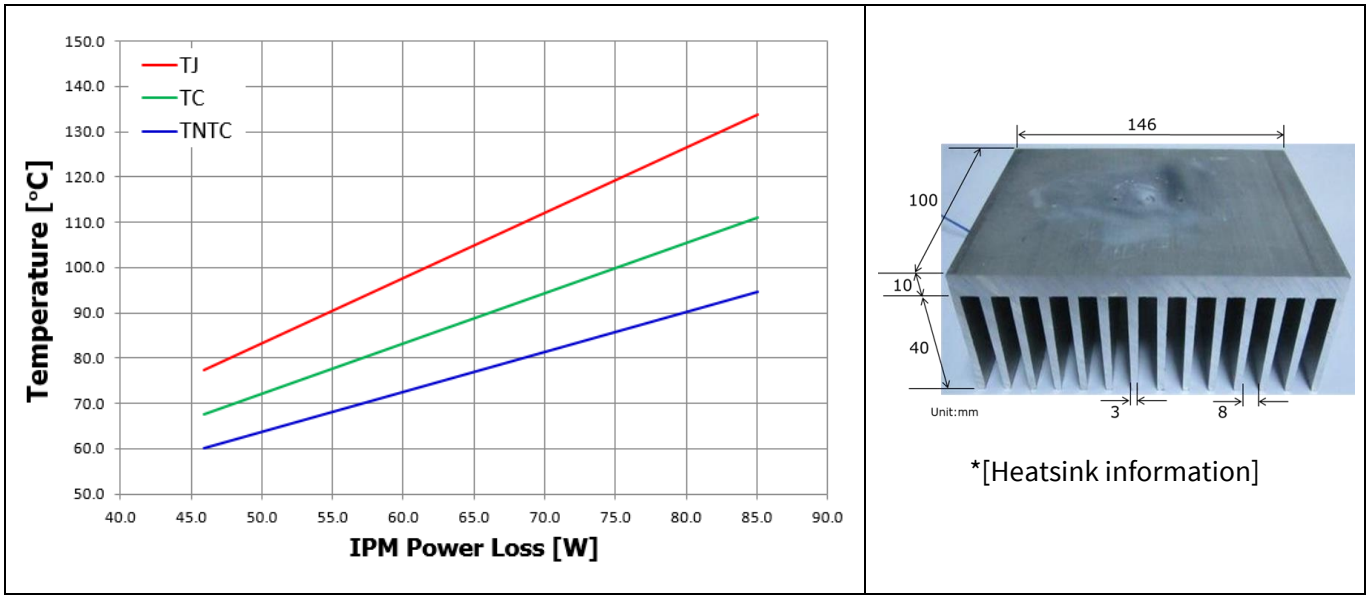


Figure 29 Example of relationship between T_J, T_C, and T_{NTC} (Test conditions: V_{DC} = 600 V, V_{DD} = 15 V, I_O = 1 ~ 4 Apeak, F_{SW} = 15 ~ 20 kHz, F_O = 3 Hz, SVPWM, convection cooling with *heatsink, T_J is measured by Infrared camera, T_C measurement point refer to Figure 4)

6 Bootstrap circuit

6.1 Bootstrap circuit operation

The V_{BS} voltage, which is the voltage difference between $V_{B\,(U,V,W)}$ and $V_{S\,(U,V,W)}$, provides the supply to the gate driver IC within the IM818. This supply voltage is recommended to be in the range of 13.5 ~ 18.5 V to ensure that the gate driver IC can fully drive the high-side IGBT. The IM818 includes an undervoltage detection function for the V_{BS} to ensure that the IC does not drive the high-side IGBT if the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating in a high dissipation mode. Please note here that the undervoltage lockout function of any high-side section acts only on the triggered channel without any feedback to the control level.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and cheap. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of an external diode, resistor and capacitor as shown in Figure 30. The current flow path of the bootstrap circuit is shown in Figure 30. When V_S is pulled down to ground (either through the low side or the load), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

6.2 Internal bootstrap functionality characteristics

The IM818 includes three bootstrap functionalities in the internal gate driver IC, which consist of three diodes and three resistors, as shown in Figure 4. A typical value of the internal bootstrap resistor is 120 Ω at room temperature. For more information, please refer to Table 22.

VDD of 15 V is recommended when only the integrated bootstrap circuitry is used.

Table 22 Electrical characteristics of internal bootstrap parameters

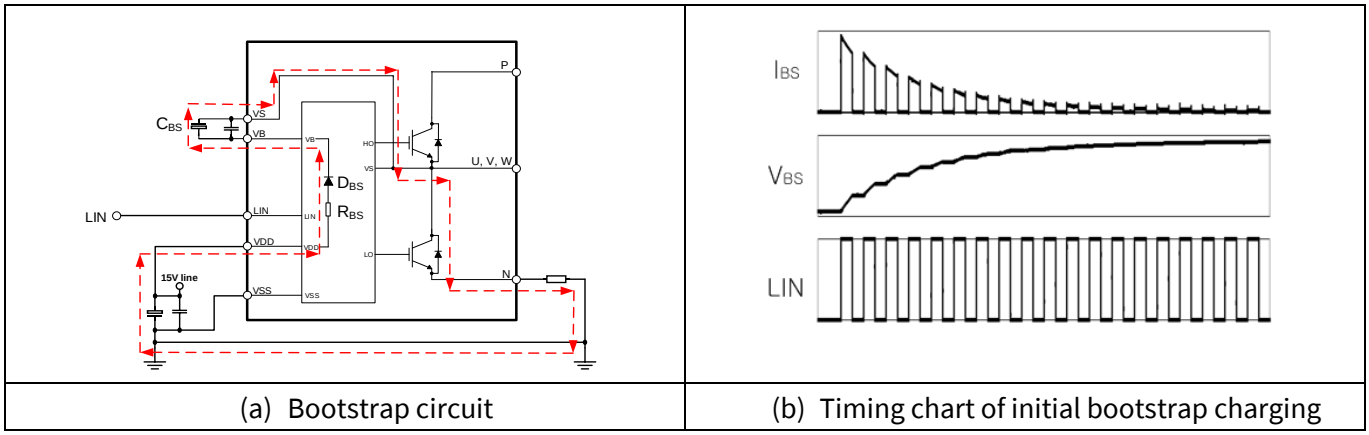
Description	Condition	Symbol	Value			Unit
			Min.	Typ.	Max.	
Repetitive peak-reverse voltage		V_{RRM}	1200	-	-	V
Diode resistance	Between V_F = 4 V and V_F = 5 V	R_{BSD}	-	120	-	Ω
Diode forward voltage	I_F = 0.3 mA	V_{F_BSD}	-	0.9	-	V

6.3 Initial charging of bootstrap capacitor

Adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} \geq C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln\left(\frac{V_{DD}}{V_{DD} - V_{BS} - V_{FD} - V_{LS}}\right) \quad (4)$$

- V_{FD} = Forward voltage drop across the bootstrap diode
- $V_{BS(min)}$ = The minimum value of the bootstrap capacitor voltage
- V_{LS} = Voltage drop across the low-side IGBT
- δ = Duty ratio of PWM



(a) Bootstrap circuit (b) Timing chart of initial bootstrap charging

Figure 30 Bootstrap circuit operation and initial changing

6.4 Bootstrap capacitor selection

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{discharge} \times \Delta t}{\Delta V} \quad (5)$$

- Where,
- Δt = maximum ON pulse width of high-side IGBT
- ΔV = the allowable discharge voltage of the C_{BS}.
- $I_{discharge}$= maximum discharge current of the C_{BS} mainly via the following mechanisms:
  - Gate charge for turning on the high-side IGBT
  - Quiescent current to the high-side circuit in the IC
  - Level-shift charge required by level shifters in the IC
  - Leakage current in the bootstrap diode
  - C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
  - Bootstrap diode reverse-recovery charge

In practice a discharge current of 1 mA is recommended as a calculation basis for IPM. By taking in consideration dispersion and reliability, the capacitance is generally selected to be 2 ~ 3 times higher than the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the VS voltage is pulled down to ground. Therefore, the on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, inherently there is a minimum on-time of the low-side IGBT (or off-time of the high side IGBT). The bootstrap capacitor should always be placed as close to the pins of the IPM as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example,

a separate ceramic capacitor close to the IPM is essential, if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local decoupling.

6.5 Charging and discharging of the bootstrap capacitor during PWM-inverter operation

The bootstrap capacitor C_{BS} charges through the bootstrap diode D_{BS} and resistor R_{BS} according to Figure 30 from the V_{DD} supply when the high-side IGBT is off, and the V_S voltage is pulled down to ground. It discharges when the high-side IGBT or diode are on.

Example 1: Selection of the initial charging time

An example of the calculation of the minimum value of the initial charging time is given with reference to equation (4).

Conditions:

- C_{BS} = 4.7 µF, R_{BS} = 120 Ω, Duty Ratio(δ) = 0.5, D_{BS} = Internal bootstrap diode, V_{DD} = 15 V, V_{FD} = 0.9 V
- $V_{BS\,(min)}$ = 13.5 V, V_{LS} = 0.1 V

$$t_{charge} \geq \frac{4.7\,\mu F \times 120\,\Omega}{0.5} \times \ln\left(\frac{15\,V}{15\,V - 13.5V\ - 0.9\,V - 0.1\,V}\right) \cong 8.2\,ms$$

In order to ensure safety, it is recommended that the charging time must be at least three times longer than the calculated value.

Example 2: The minimum value of the bootstrap capacitor

Conditions:

- ΔV = 0.1 V, $I_{discharge}$ = 1 mA

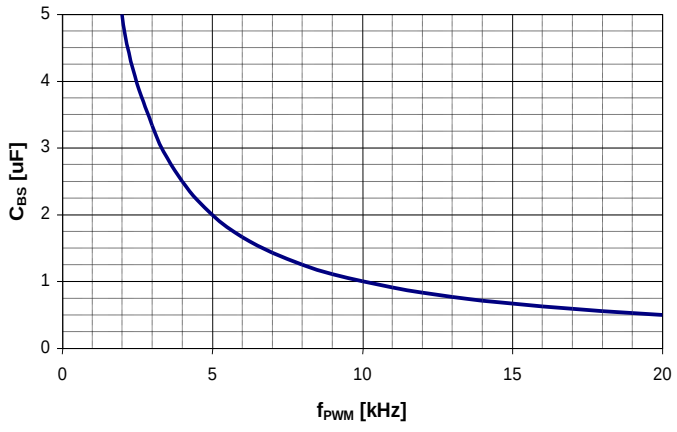


Figure 31 Bootstrap capacitance as a function of the switching frequency

Figure 31 shows the curve corresponding to equation (5) for a continuous sinusoidal modulation, if the voltage ripple ΔV_{BS} is 0.1 V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range of up to 4.7 µF for most switching frequencies. In other PWM method cases such as discontinuous sinusoidal modulation, the t_{charge} must be set at the longest period of the low-side IGBT off.

Note that this result is only an example. It is recommended that the system design consider the actual control pattern and lifetime of the used components.

7 Themral system design

7.1 Introduction

The thermal design of a system is a key issue of IM818 included in electronic systems such as drives. In order to avoid overheating and/or to increase the reliability, two design criteria are of importance:

- Low power losses
- Low thermal resistance from junction to ambient

The first criterion is already fulfilled when choosing IM818 as intelligent power module for the application. To get the most out of the system, a proper heat sink choice is necessary. A good thermal design either allows to maximize the power or to increase the reliability of the system (by reducing the maximum temperature). This application note will give a short introduction to power losses and heat sinks, helping to understand the mode of operation and to find the right heat sink for a specific application.

For the thermal design, one needs:

- The maximum power losses $P_{sw,i}$ of each power switch
- The maximum junction temperature $T_{J,max}$ of the power semiconductors
- The junction to ambient thermal resistance impedance $Z_{th,J-A}$. For stationary considerations the static thermal resistance $R_{th,J-A}$ is sufficient. This thermal resistance comprises the junction-to-case thermal resistance $R_{th,J-C}$ as provided in datasheets, the case to heat sink thermal resistance $R_{th,C-HS}$ accounting for the heat flow through the thermal interface material between heat sink and the power module and the heatsink to ambient thermal resistance $R_{th,HS-A}$. Each thermal resistance can be extended to its corresponding thermal impedance by adding the thermal capacitances.
- The maximum allowable ambient temperature $T_{A,max}$

Furthermore all heat flow paths need to be identified. Figure 32 presents a typical simplified equivalent circuit for the thermal network. This circuit is simplified, as it omits thermal capacitances and typically negligible heat paths such as the heat transfer from the module surface directly to the ambient via convection and radiation.

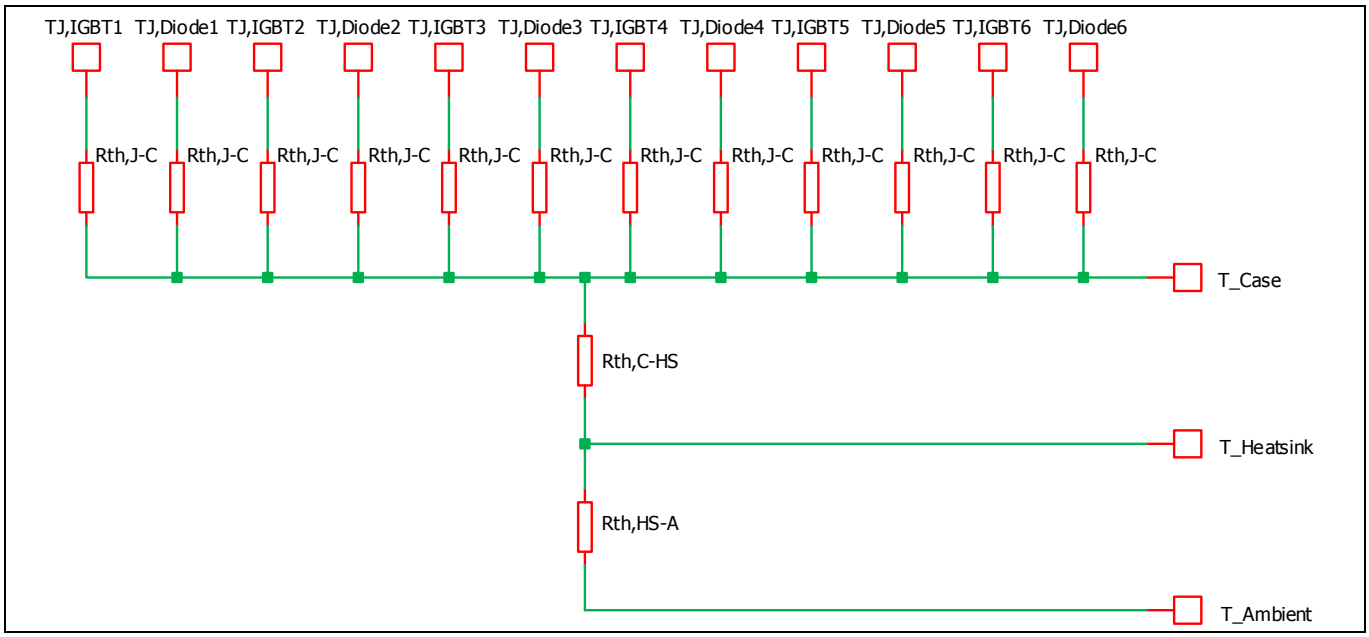


Figure 32 Simplified thermal equivalent circuit

7.2 Power loss

The total power losses in the IM818 are composed of conduction and switching losses in the IGBTs and diodes. The loss during the turn-off steady state can be ignored because it is very small and has little effect on increasing the temperature in the device. The conduction loss depends on the DC electrical characteristics of the device, i.e. saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature. On the other hand the switching loss is determined by the dynamic characteristics like turn-on/off time and over-voltage/current. Hence, in order to obtain the accurate switching loss, the DC link-voltage of the system, the applied switching frequency and the power circuit layout in addition to the current and temperature should be considered. In this chapter, based on a PWM inverter system for motor control applications, detailed equations are shown to calculate both losses of the IM818 for a 3-phase continuous sinusoidal PWM. For other cases like 3-phase discontinuous PWMs, please refer to [4].

7.2.1 Conduction losses

The typical characteristics of forward drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively.

$$V_{IGBT} = V_I + R_I \cdot i$$
$$V_{DIODE} = V_D + R_D \cdot i \quad (6)$$

- V_I = threshold voltage of IGBT
- V_D = threshold voltage of anti-parallel diode
- R_I = on-state slope resistance of IGBT
- R_D = on-state slope resistance of anti-parallel diode

Assuming that the switching frequency is high, the output current of the PWM inverter can be assumed to be sinusoidal. That is,

$$i = I_{peak}\cos(\theta - \varphi) \quad (7)$$

Where, φ is the phase-angle difference between output voltage and current. Using equations (6) and (7), the conduction loss of one IGBT and its anti-parallel diode can be obtained as follows.

$$P_{con.I} = \frac{1}{2\pi}\int_0^{\pi} \xi(V_{IGBT} \times i)d\theta = \frac{I_{peak}}{2\pi}V_I + \frac{I_{peak}}{8}V_I MI\cos\varphi + \frac{{I_{peak}}^2}{8}R_I + \frac{{I_{peak}}^2}{3\pi}R_I MI\cos\varphi \quad (8)$$

$$P_{con.D} = \frac{1}{2\pi}\int_0^{\pi} (1-\xi)(V_{DIODE} \times i)d\theta = \frac{I_{peak}}{2\pi}V_D - \frac{I_{peak}}{8}V_D MI\cos\varphi + \frac{{I_{peak}}^2}{8}R_D - \frac{{I_{peak}}^2}{3\pi}R_D MI\cos\varphi \quad (9)$$

$$P_{con} = P_{con.I} + P_{con.D} \quad (10)$$

Where ξ is the duty cycle in the given PWM method.

$$\xi = \frac{1 + MI\cos\theta}{2} \quad (11)$$

Where, MI is the PWM modulation index (MI is defined as the peak-phase voltage divided by the half of DC- link voltage).

It should be noted that the total inverter conduction losses are six times the P_{con}.

7.2.2 Switching losses

Different devices have different switching characteristics, which also vary according to the handled voltage/current and the operating temperature/frequency. However, the turn-on/off loss energy (joule) can be experimentally measured indirectly by multiplying the current and voltage and integrating over time, under a given circumstance. Therefore the linear dependency of the switching energy loss on the switched current is expressed during one switching period as follows.

$$Swtitching \quad energy \quad loss = (E_I + E_D) \times i \ [joule] \tag{12}$$

$$E_I = E_{I.ON} + E_{I.OFF} \tag{13}$$

$$E_D = E_{D.ON} + E_{D.OFF} \tag{14}$$

Where, E_I i is the switching loss energy of the IGBT and E_D i is for its monolithic body diode. E_I and E_D can be considered a constant approximately.

As mentioned in the equation (7), the output current can be considered a sinusoidal waveform; and the switching loss occurs every PWM period for the continuous PWM schemes. Therefore, depending on the switching frequency f_{SW}, the switching loss of one device is represented in the following equation (15).

$$P_{sw} = \frac{1}{2\pi}\int_0^{\pi}(E_I + E_D)\ i\ f_{sw}\,d\varphi = \frac{(E_I + E_D)f_{sw}I_{peak}}{\pi} \tag{15}$$

Where, E_I is a unique constant of IGBT related to the switching energy, and different IGBTs have different E_I values. E_D is one for diode. These should be derived by experimental measurement. From the equation (15), it should be noted that the switching losses are a linear function of current, and directly proportional to the switching frequency.

7.3 Thermal impedance

In practical operation, the power loss P_D is cyclic and therefore the transient impedance needs to be considered. The thermal impedance is typically represented by a RC equivalent circuit (Foster model) as shown in Figure 33. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature, and thus permits a heavier loading of the IM818. Figure 34 shows thermal impedance from the junction-to-case curves of IM818-SCC, MCC. The thermal resistance in Table 23 goes into saturation in about 10 seconds. Other kinds of IM818 also show similar characteristics.

Table 23 Thermal resistance of IM818 products

Description	Symbol	Condition		Value			Unit
				Min.	Typ.	Max.	
Single-IGBT thermal resistance, junction-case	R_{thJC}	Low-side U-phase IGBT (See Figure 4 for T_C measurement point)	IM818-SCC IM818-MCC	-	-	2.52 1.85	K/W
Single-diode thermal resistance, junction-case	$R_{thJC,D}$	Low-side U-phase diode (See Figure 4 for T_C measurement point)	IM818-SCC IM818-MCC	-	-	3.60 2.50	K/W

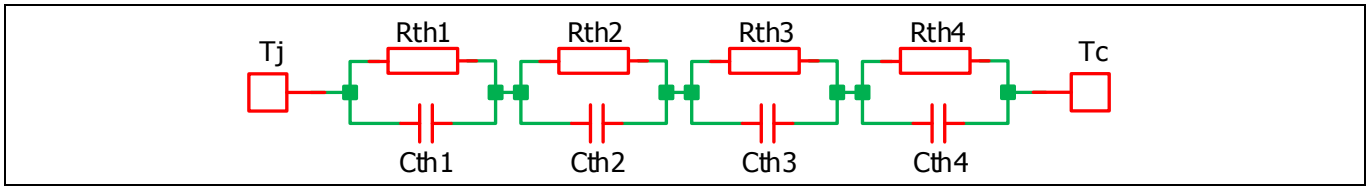


Figure 33 Thermal impedance RC equivalent circuit

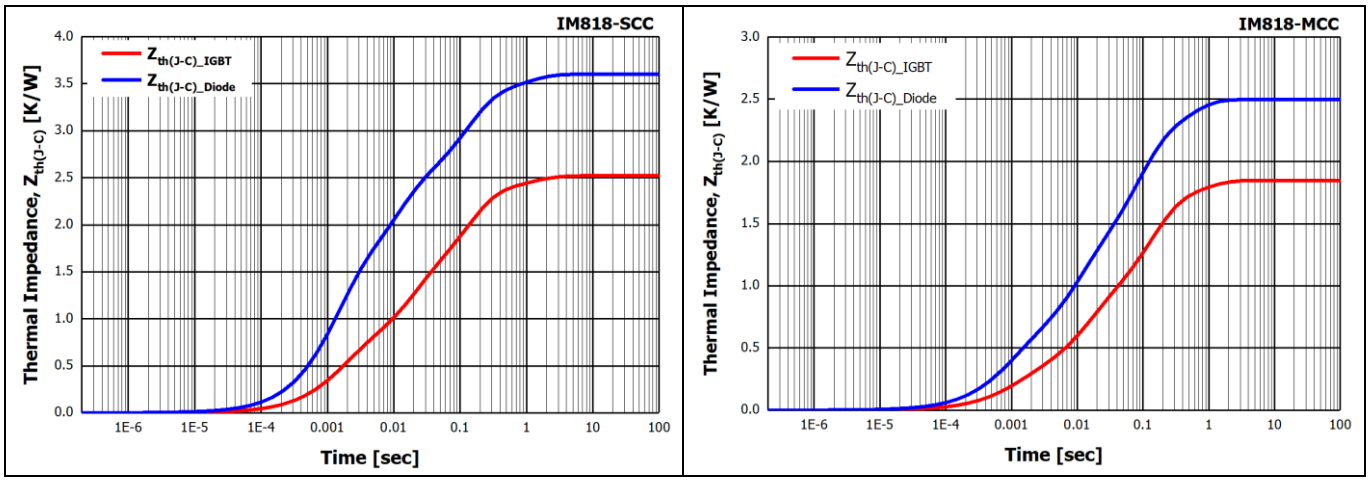


Figure 34 Thermal impedance curves (IM818-SCC, MCC, based on single-chip heating)

7.4 Temperature rise considerations and calculation example

The simulator CIPOSIM allows users to calculate power losses and temperature profiles for a constant case temperature. The result of loss calculation using the typical characteristics is shown in Figure 35 as “Effective current versus carrier frequency characteristics” (for V_{PN} = 600 V, V_{DD} = 15 V, $V_{CE(sat)}$ = typical, switching loss = typical, T_J = 150°C, T_C = 100°C, $R_{th(J-C)}$ = Max., P.F = 0.8, 3-phase continuous PWM modulation, 60 Hz sine waveform output).

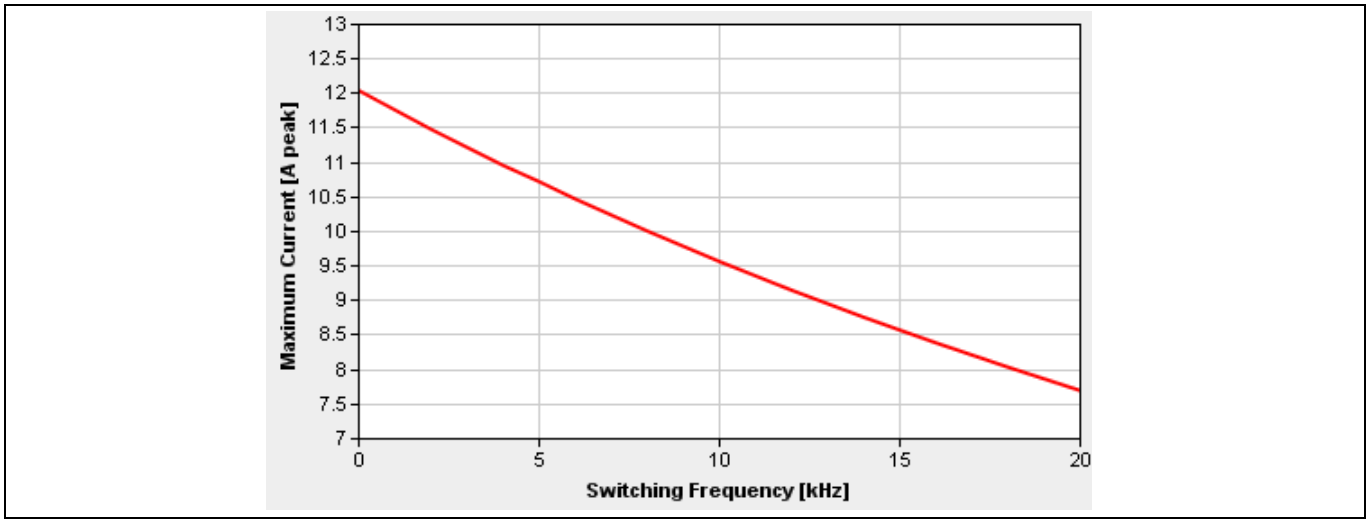


Figure 35 Effective current – carrier frequency characteristics of IM818-MCC [5]

Figure 35 shows an example of an inverter operated under the condition of T_C = 100°C. It indicates the effective current I_o output when the junction temperature T_J rises to the maximum junction temperature of 150°C (up to which the IM818 operates safely).

7.5 Heat sink selection guide

7.5.1 Required heat sink performance

If the power losses $P_{sw,i}$, $R_{th(J-C)}$ and the maximum ambient temperature are known, the required thermal resistance of the heat sink and the thermal interface material can be calculated according to Figure 33 from,

$$T_{J,max} = T_{A,max} + \sum_i P_{sw,i} \cdot R_{th,HS-A} + \sum_i P_{sw,i} \cdot R_{th,C-HS} + Max(P_{sw,i} \cdot R_{th,JC,i}) \quad (16)$$

For three- phase bridges, one can simply assume that all power switches dissipate the same power and all have the same $R_{th,J-C}$. This leads to the required thermal resistance from case to ambient.

$$R_{th,C-A} = R_{th,C-HS} + R_{th,HS-A} = \frac{T_{J,max} - P_{sw} \cdot R_{th,JC} - T_{A,max}}{\sum P_{sw}} \quad (17)$$

For example, the power switches of a washing machine drive dissipate 3.5 W maximum each, the maximum ambient temperature is 50°C, the maximum junction temperature is 150°C and $R_{th(J-C)}$ is 3 K/W. It results in:

$$R_{th,C-A} \leq \frac{150°C - 3.5W \cdot 3\frac{K}{W} - 50°C}{6 \cdot 3.5W} = 4.3\frac{K}{W}$$

If the heat sink temperature shall be limited to 100°C, an even lower thermal resistance is required:

$$R_{th,C-A} \leq \frac{100°C - 50°C}{6 \cdot 3.5W} = 2.4\frac{K}{W}$$

Smaller heat sinks with higher thermal resistance may be acceptable if the maximum power is only required for a short time (times below the time constant of the thermal resistance and the thermal capacitance). However, this requires a detailed analysis of the transient power and temperature profiles. The larger the heat sink, the larger the thermal capacitance and the longer it takes to heat up the heat sink.

7.5.2 Heat sink characteristics

Heat sinks are characterized by three parameters:

- Heat transfer from the power source to heat sink
- Heat transfer within the heat sink (to all the surfaces of the heat sink)
- Heat transfer from heat sink surfaces to ambient

7.5.2.1 Heat transfer from heat source to heat sink

There are two factors which need to be considered in order to provide a good thermal contact between power source and heat sink:

- **Flatness of the contact area**
  - Due to the unevenness of surfaces, a thermal interface material needs to be supplied between heat source and heat sink. However, such materials have a rather low thermal conductivity (< 10 K/W). Hence these materials should be as thin as possible. On the other hand, they need to fill out the space between heat source and heat sink. Therefore, the unevenness of the heat sink should be as low as possible. In addition, the particle size of the interface material must fit to the roughness of the module and the heat sink surfaces. Particles that are too large will unnecessarily increase the thickness of the interface layer, and hence increase the thermal resistance. Particles that are too small will not provide a good contact between the two surfaces and will lead to a higher thermal resistance as well.
- **Mounting pressure**
  - The higher the mounting pressure, the better the interface material disperses. Also excessive interface material is squeezed out resulting in a thinner interface layer with a lower thermal resistance.

7.5.2.2 Heat transfer within the heat sink

The heat transfer within the heat sink is mainly determined by:

- **Heat sink material**
  - The material needs to be a good thermal conductor. Most heat sinks are made of aluminum ($\lambda \approx 200$ W/(m*K)). Copper is heavier and more expensive but also nearly twice as efficient ($\lambda \approx 400$ W/(m*K)).
- **Fin thickness**
  - If the fins are too thin, the thermal resistance from heat source to fin is too high, and the efficiency of the fin decreases. Hence it does not make sense to make the fins as thin as possible in order to make more fins and therefore to increase the surface area

7.5.2.3 Heat transfer from heat sink surface to ambient

The heat transfers to the ambient mainly by convection. The corresponding thermal resistance is defined as

$$R_{th,conv} = \frac{1}{\alpha \cdot A} \qquad (18)$$

Where α is the heat transfer coefficient and A is the surface area.

Hence there are two important parameters:

- **Surface area:** Heat sinks require a huge surface area in order to easily transfer the heat to the ambient. However, as the heat source is assumed to be concentrated at a point and not uniformly distributed, the total thermal resistance of a heat sink does not change linearly with length. Also, increasing the surface area by increasing the number of fins does not necessarily reduce the thermal resistance as discussed in section 7.5.2.2.
- **Heat transfer coefficient (aerodynamics):** This coefficient is strongly depending on the air flow velocity as shown in Figure 36. If there is no externally induced flow, one speaks of natural convection. Otherwise it is forced convection. Heat sinks with very small fin spacing do not allow a good air flow. If a fan is used, the fin gap may be lower than for natural convection, as the fan forces the air through the space between the fins.

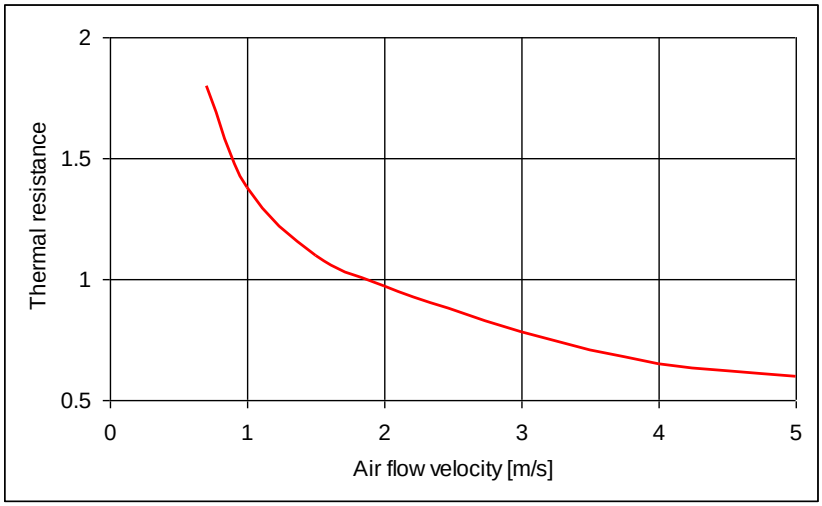


Figure 36 Thermal resistance as a function of the air flow velocity

Furthermore, in the case of natural convection, the heat sink efficiency depends on the temperature difference of heat sink and ambient, i.e. on the dissipated power. Some manufacturers, like Aavid Thermalloy, provide a correction table which allows the user to calculate the thermal resistance depending on the temperature difference. Figure 37 shows the heat sink efficiency degradation for natural convection as provided in [6]. Please note that the thermal resistance is 25% higher at 30 W than at 75 W.

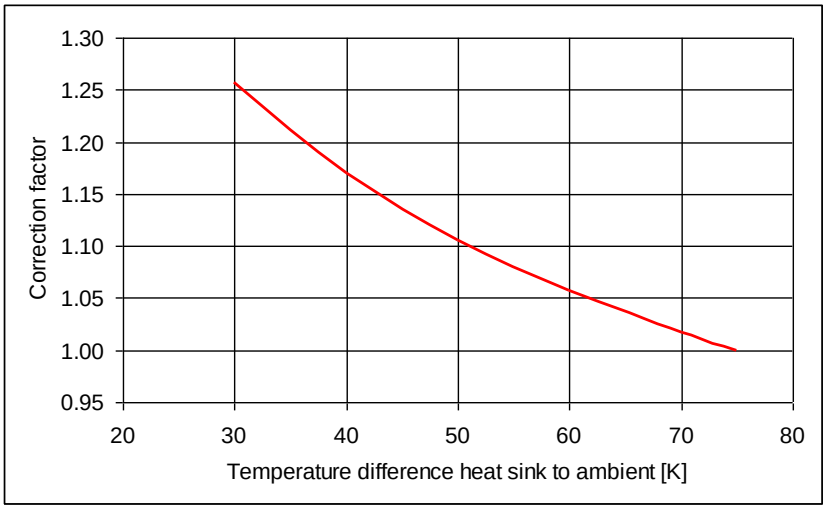


Figure 37 Correction factors for temperature

The positioning of the heat sink plays also an important role for the aerodynamics. In the case of natural convection, the best mounting is done with vertical fins, as the heated air tends to move upwards due to buoyancy. Furthermore, one should make sure that there are no significant obstructions impeding the air flow.

Radiation occurs as well supporting the heat transfer from heat sink to ambient. In order to increase radiated heat, one can use anodized heat sinks with a black surface. However, this decreases the thermal resistance of the heat sink only by a few percentage pointsin the case of natural convection. Radiated heat is negligible in the case of forced convection. Hence blank heat sinks can be used if no fan is used with the heat sink.

The discussions in this section clearly show that there cannot be a single thermal resistance value assigned to a certain heat sink.

7.5.3 Selecting a heatsink

Unfortunately there are no straightforward formulas for selecting heat sinks. Finding an appropriate heat sink will include an iterative process of choosing and testing heat sinks. In order to get a first rough estimation of the required volume of the heat sink, one can start with estimated volumetric thermal resistances as given in Table 24 (Taken from [7]). This table gives only a first clue, as the actual resistance may vary depending on many parameters like actual dimensions, type and orientation, etc.

Table 24 Volumetric thermal resistance

Flow conditions [m/s]	Volumetric resistance [cm^3 °C/W]
Natural convection	500 ~ 800
1.0	150 ~ 250
2.5	80 ~ 150
5.0	50 ~ 80

One can roughly assume that the volume of a heat sink needs to be quadrupled in order to halve its thermal resistance. This gives a hint whether natural convection is sufficient for the available space, or whether forced convection is required.

In order to get an optimized heat sink for a given application, one needs to contact heat sink manufacturers or consultants. Further hints and references can be found in [8].

When contacting heat sink manufacturers in order to find a suitable heat sink, please note the conditions under which the given thermal resistance values are valid. They might be given either for a point source or for a heat source which is evenly distributed over the entire base area of the heat sink. Also take care that the fin spacing is optimized for the corresponding flow co

8 Heatsink mounting and hanling guidelines

8.1 Electrical spacing

The electric spacing specifications of IM818 are shown in Table 25. The IM818 package(DIP 36X23D) does not satisfied clearance and creepage distance between pins and heatsink (earthed) and creepage distance on PCB between signal pins such as (2) to (3), (4) to (5), (6) to (7). Based on IEC and UL standards, to secure a clearance and creepage distance between the pins and the heatsink (earthed), a convex-shaped heatsink is necessary as shown in Figure 38, and the PCB slot is required to keep 4.0 mm creepage on the PCB between the signal pins.

Table 25 Electrical spacing (*not compliant to IEC)

Standard & CIPOS™ Maxi	IPM Unit				PCB		Remark
	Basic insulation pin to heat sink(earthed) [mm]		Functional insulation between pin and pin [mm]		PWB (solder to solder) [mm]		
	Clearance	Creepage	Clearance	Creepage	Clearance	Creepage	
IEC60335-1 IEC60664-1 IEC67800-5-1 UL840	5.5	4.0	3.0	4.0	3.0	4.0	Refer to Table 21
CIPOS™ Maxi IM818 IPM	*1.6	*1.62	Power pins : 4.97 Signal pins : 4.12	Power pins : 5.17 Signal pins : 4.12	Power pins : 4.94 Signal pins : 3.53	Power pins : 4.94 Signal pins : *3.53	PCB slot is necessary.

Table 26 Boundary Conditions

Isolation	Rated voltage	Overvoltage category	Inpulse voltage	Working voltage	Working voltage	Pollution degree	IPM CTI
Pin to heat sink (earthed)	480 V_{ac}	III	6000 V	679 V_{dc}	Max. 800 V_{dc}	II	> 600
Pin to pin	480 V_{ac}	II	4000 V	679 V_{dc}	Max. 800 V_{dc}	II	> 600

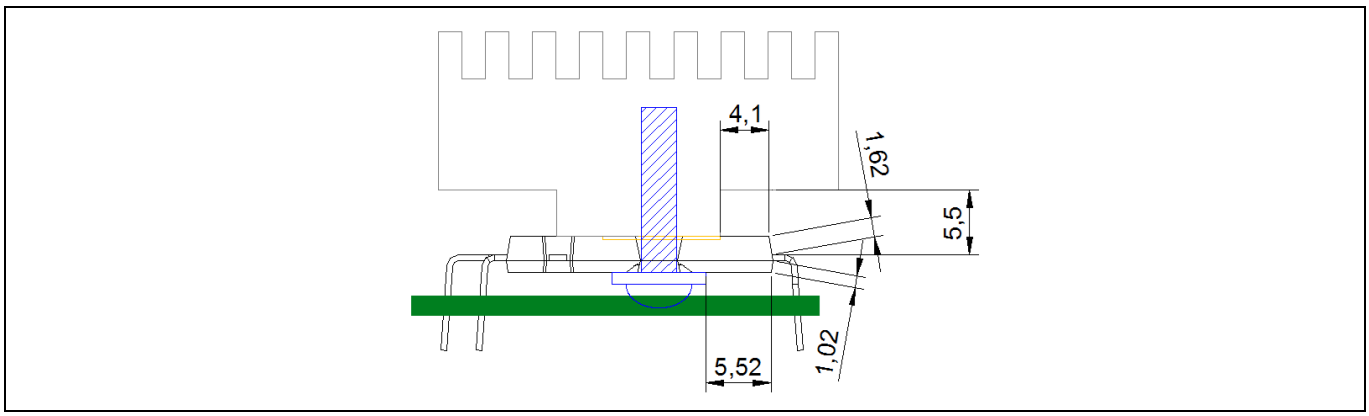


Figure 38 Recommended heat sink shape to get creepage and clearance distance between pins and heat sink

8.2 Heat sink mounting

8.2.1 General guidelines

An adequate heat-sinking capability of the IPM is only achievable if the heat sink is suitably mounted. This is the fundamental requirement in order to meet the electrical and thermal performance criteria of the module. The following general points should be observed when mounting the IPM on a heat sink. Verify the following points related to the heat sink:

a) There must be no burrs on aluminum or copper heat sinks.
b) Screw holes must be countersunk.
c) There must be no unevenness or scratches in the heat sink.
d) The surface of the module must be completely in contact with the heat sink.
e) There must be no oxidation, stain or burrs on the heat-sink surface.

To improve the thermal conductivity, apply silicone grease to the contact surface between the IPM and heat sink. Spread a homogenous layer of silicone grease with a thickness of 100 µm over the IPM substrate surface. Non-planar surfaces of the heat sink may require a thicker layer of thermal grease. Please refer here to the specifications of the heat sink manufacturer. It is important to note here that the heat sink covers the complete backside of the module. There may be different functional behavior if there is a portion of the backside of the module which is not in contact with the heat sink.

To prevent a loss of heat dissipation effect due to warping of the substrate, tighten down the mounting screws gradually and sequentially while maintaining a left/right balance in pressure applied.

It must be assured by design of the application PCB, that the plane of the back side of the module and the plane of the heat sink are parallel in order to achieve minimal tension of the package and an optimal contact of the module with the heat sink. Please refer to the mechanical specifications of the module given in the datasheets.

It is the basics of good engineering to verify the function and thermal conditions by means of detailed measurements. It is best to use a final application inverter system, which is assembled with the final production process. This helps to achieve high-quality applications.

8.2.1.1 Recommended tightening torque

As shown in Table 27, the tightening torque of M3 screws is specified for a minimum MS = 0.49 N·m and a maximum MS = 0.78 N·m. The screw holes must be centered to the screw openings of the mold compound, so that the screws do not contact the mold compound. If an insulating sheet is used, use a sheet larger than the IPM, which should be aligned accurately when attached. It is important to ensure that no air is enclosed by the insulating sheet. Generally speaking, insulating sheets are used in the following cases:

- When the ability of withstanding primary and secondary voltages is required to achieve required safety standard against a hazardous situation.
- When the IM818 must be insulated from the heat sink.
- When measuring the module, to reduce radiated noise or eliminate other signal-related problems.

Table 27 Mechanical characteristics and ratings

Item	Condition	Value			Unit
		Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3	0.49	-	0.78	N·m
Backside curvature	(Note Figure 39)	0	-	+150	µm
Heat sink flatness	(Note Figure 40)	0	-	+100	µm
Weight		-	7.1	-	g

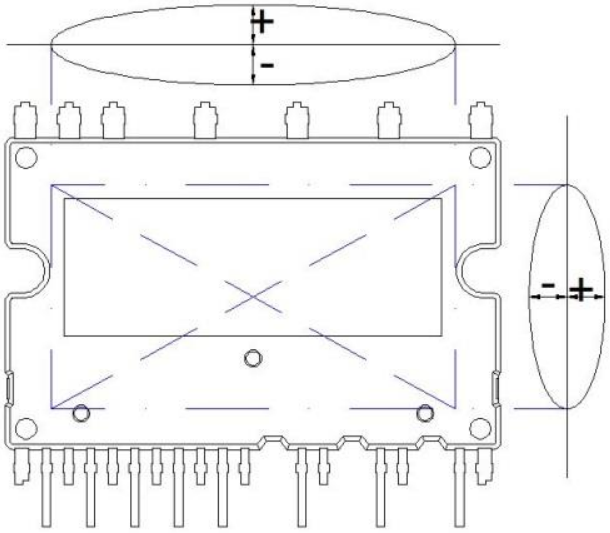


Figure 39 Backside curvature measurement position

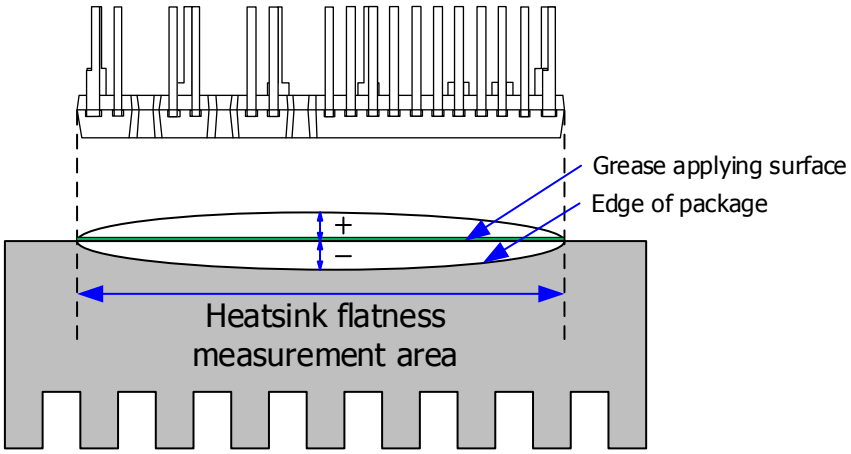


Figure 40 Heatsink flatness measurement position

8.2.1.2 Screw-tightening to heat sink

The tightening of the screws is the main process of attaching the module to the heat sink. It is assumed that an interface pad is attached to the heat sink surface, which extends to the edge of the module and is located for the fixing holes. It is recommended that M3 fixing screws are used in conjunction with a spring washer and a plain washer. The spring washer must be assembled between the plain washer and the screw head. The screw torque must be monitored by the fixing tool.

Tightening process:

- Align module with the fixing holes.
- Insert screw A with washers to touch only position (pre-screwing).
- Insert screw B with washers (pre-screwing).
- Tighten screw A to final torque.
- Tighten screw B to final torque.

Note: The pre-screwing torque is set to 20~30% of maximum torque rating.

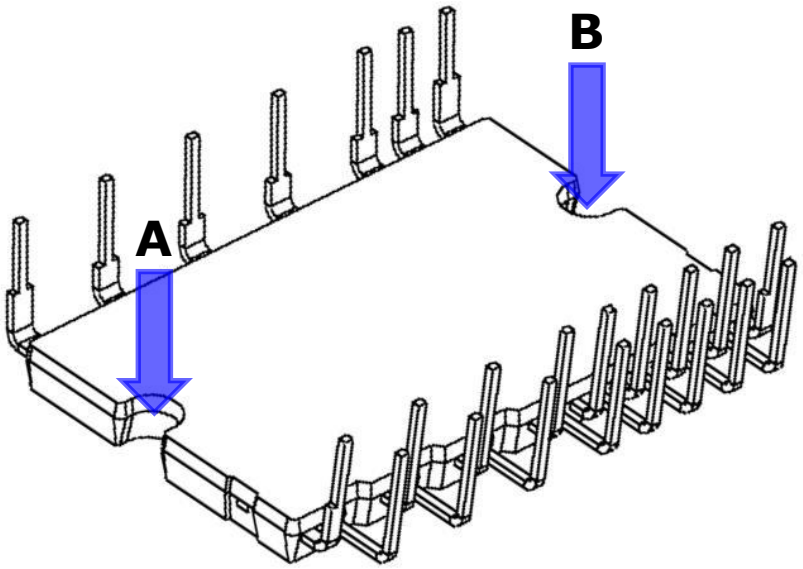


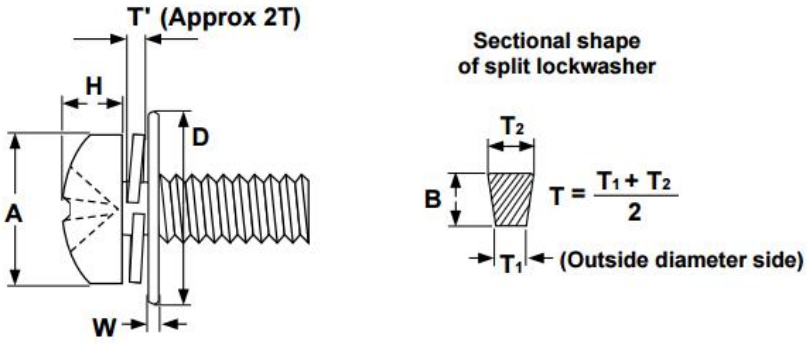
Figure 41 Reommended screw-tightening order : Pre-screwing A → B, Final screwing A → B

8.2.1.3 Mounting screw

When we attach module to heatsink, we recommend M3 SEMS screws (JIS B1256/JIS B1188) as shown in Table 28.

Table 28 Recommended screw specifications (Typical)

Screw dimensions				Flat washer		Spring washer	
Size	Thread pitch	A Head diameter	H Head height	D Outer diameter	W Thickness	D1 Outside diameter	B x T
M3	0.5	5.2	2.0	7.0	0.5	5	1.1 x 0.7



8.2.2 Recommended heat-sink shape and mechanical assembly

A shock or vibration through PCB or heat sink might cause the crack of the package mounted on the heat sink. To avoid a broken or cracked package and to endure shock or vibration through PCB or heat sink, a heat sink shape is recommended as shown in Figure 42. The heat sink needs to be fixed to the PCB with screws or eyelets. In the mass-production stage, the process sequence for system assembly in terms of device soldering on PCB, heat sink mounting and casing etc., should be taken into account to avoid mechanical stress on the device pins, package mold compound, heat sink and system enclosure, etc.

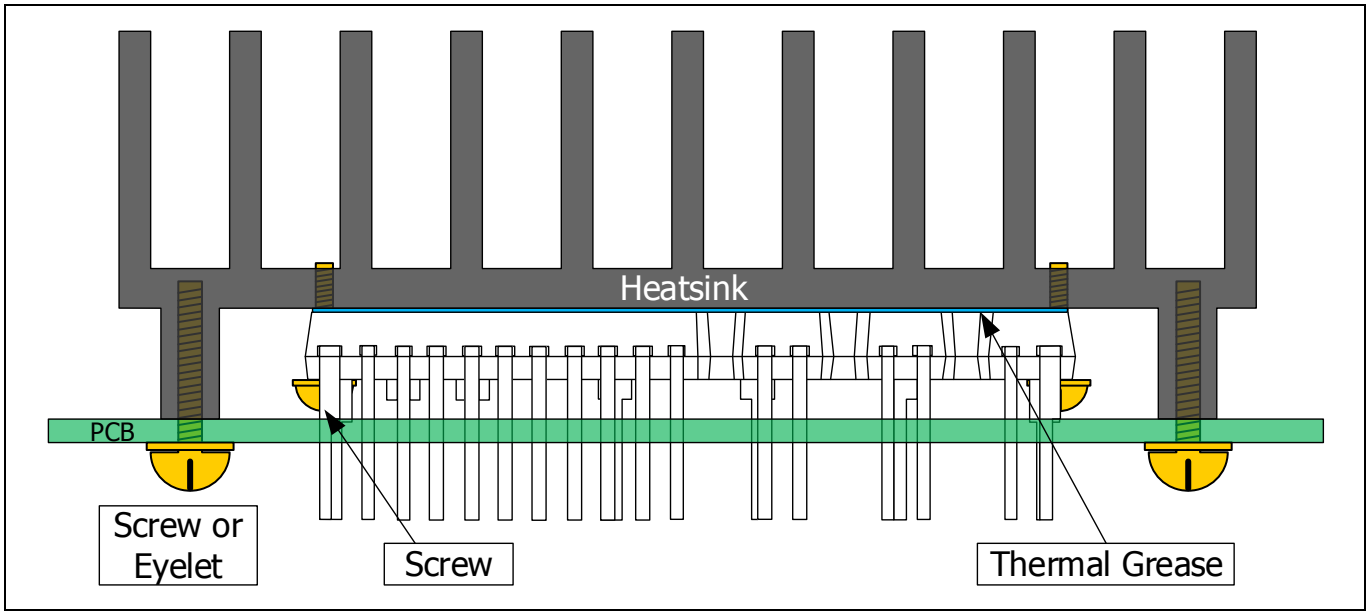


Figure 42 Recommended heat sink shape

8.3 Handling guide line

When installing a module to a heat sink, excessive uneven tightening force might apply stress to inside chips, which will lead to breaking or degradation of the device. An example of recommended fastening order is shown in Figure 41.

- Do not over-torque when mounting the screws. Excessive mounting torque may cause damage to module holes as well as to the screws and heat sink.
- Avoid one-side tightening stress. Uneven mounting can cause the module holes to be damaged.

To get effective heat dissipation, it is necessary to enlarge the contact area as much as possible, which minimizes the contact thermal resistance.

Properly apply thermal conductive grease over the contact surface between the module and the heat sink, which is also useful for preventing the contact surface from corrosion. Furthermore, the grease should be of stable quality and long-term durability within a wide operating-temperature range. Use a torque wrench to tighten to the specified torque rating. Exceeding the maximum torque limitation might cause a module to be damaged or degraded. Make sure there is no dirt remaining on the contact surface between the module and the heat sink. All equipment used to handle or mount the IPM must comply with the relevant ESD standards. This includes transportation, storage and assembly. The module itself is an ESD-sensitive device. It may therefore be damaged in case of ESD shocks.

Do not shake or grasp the heat sink; in particular, avoid any chocks to the PCB by grasping only the heat sink. This could cause package cracking or breaking.

8.4 Storage guidelines

8.4.1 Recommended storage conditions

Temperature: 5 ~ 35℃

Relative humidity: 45 ~ 75%

- Avoid leaving the IM818 exposed to moisture or direct sunlight. In particular be careful during periods of rain or snow.
- Use storage areas where there is minimal temperature fluctuation.

Rapid temperature changes can cause moisture condensation on the stored IM818, resulting in lead oxidation or corrosion as a result, leading to degraded solderability.

- Do not allow the IM818 to be exposed to corrosive gasses or dusty conditions.
- Do not allow excessive external forces or loads to be applied to the IM818 while they are in storage.

9 References

1. [1] M. Bäßler, P.Kanschat, F.Umbach, C. Schaeffer, “1200V IGBT4-High Power-new technology gernation with optimized characteristics for high current modules“, PCIM Europe 2006, Nuremberg, Germany
2. [2] R. Keggenhoff, Z.Liang, Andre Arens, P. Kanschat, R. Rudolf. ‘Novel SOI Driver for Low Power Drive Applications’, Power Systems Design Europe Nov. 2005
3. [3] M. Lee, M. Baek, J. Lee, D. Chung “A New Smallest 1200V Intelligent Power Module for Three Phase Motor Drives”, IPEC 2018, Niigata, Japan
4. [4] D. Chung, S. Sul , "Minimum-Loss Strategy for three-Phase PWM Rectifier”, IEEE Transactions on Industrial Electronics, Vol. 46, No. 3, June, 1999
5. [5] CIPOSIM - CIPOS™ Mini Simulator, Infineon Technologies Power Semitech, 2009
6. [6] Aavid Thermalloy, http://www.aavidthermalloy.com/technical/correct.shtml
7. [7] S. Lee, “How to select a heat sink”, Electronics Coolings, Vol.1, No.1, June 1995

Revision History

Major changes since the last revision

Page or Reference	Description of change
Ver1.1, 07th Jun. 2019	AN number change from AN2018-09 to AN2019-16 Correct data in section 8.2.1.1 Table 27. (package warpage from -50 ~ +100 µm to 0 ~ +150 µm)
Ver1.0, 08th Aug. 2018	Initial release

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Edition 2019-06-07

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN2019-16

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