600 V High Voltage 3 Phase Bridge Driver

BS2132F

Contents

1. Product summary

1.1 Applications

- Application for driving N-channel MOSFET and IGBT

1.2 Series line-up

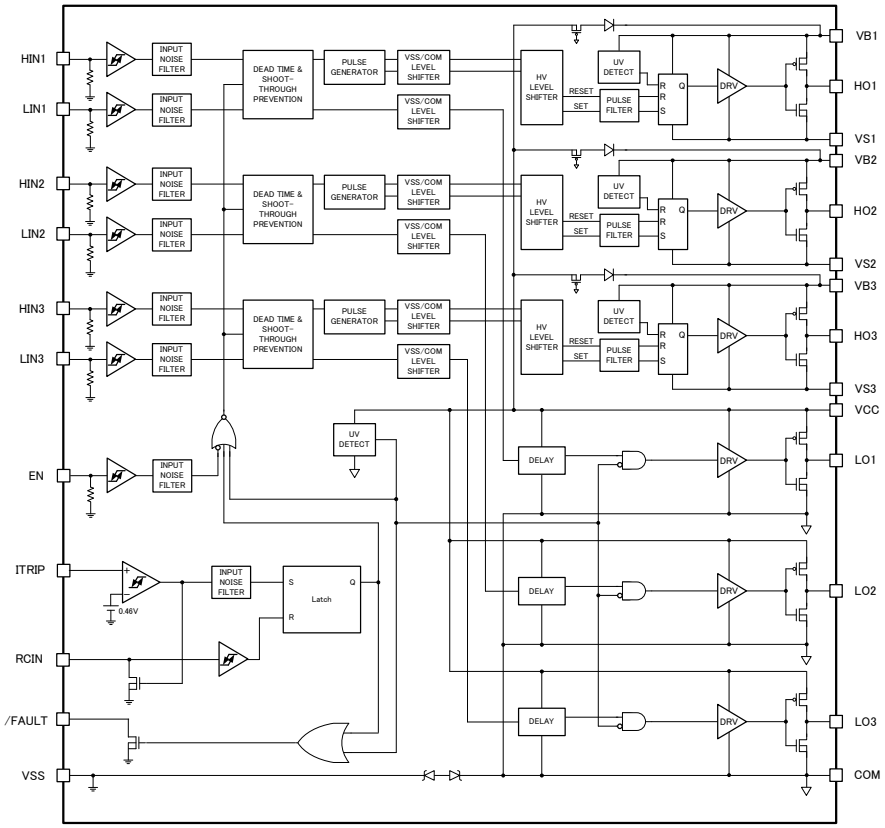
Table 1.2.1 Line-up

Series	Model	Absolute maximum rating	VCC recommended operating range	Output stage capacity (min) (source／sink)	Protection function	Dead time (typ)	Package
6 ch (3 arm)	BS2130F-G	625V/25V	11.5－20V	200mA／350mA	UVLO, OCP	300ns	SOP-28
	BS2132F	625V/25V	11.5—20V	200mA／350mA	UVLO, OCP	300ns	SOP-28
2 ch (1 arm)	BS2101F	620V/20V	10－18V	60mA／130mA	UVLO	–	SOP-8
	BS2103F	620V/20V	10－18V	60mA／130mA	UVLO	160ns	SOP-8
	BS2114F	625V/25V	10－20V	500mA／500mA	UVLO	160ns	SOP-8

1.3 Functions and features

- Floating terminal withstanding voltage: Up to 600 V
- Gate driver voltage range: 11.5 V to 20V
- Integrated 600V High Voltage Bootstrap Diodes Between the VCC pin and the VB pin
- SOI (silicon on insulator) process is employed
- Under voltage lock out (UVLO) circuit is installed for the supply voltage on the upper drive (voltage between the VB and VS terminals) and the supply voltage on the lower drive (voltage between the VCC and COM terminals)
- Enable (EN) terminal is installed for I/O signal
- Built-in over current protection (OCP) function
- Alarm signal when a protection function (UVLO or OCP) is activated
  Output terminal (/FAULT) installed
- Holding time of OCP can be adjusted with external CR (RCIN terminal)
- Logic voltage of 3.3 V or 5.0 V can be input
- Output common-mode for input signal

1.4 Block diagram



2. Specifications

2.1 Details of absolute maximum rating

Table 2.1.1 provides details of the absolute maximum ratings.

Table 2.1.1 Absolute maximum rating (Unless specified otherwise, Ta = 25°C and V_{SS} is set to the reference at 0 V.)

Item	Symbol	Rating (Min)	Rating (Max)	Unit	Description
High side offset voltage	V_S	V_B-25	V_B+0.3	V	Maximum voltage between the VB1 and VS1 terminals, between the VB2 and VS2 terminals, and between the VB3 and VS3 terminals
High side floating supply voltage	V_B	V_{COM}-0.3	V_{COM}＋625V	V	Maximum voltage between the VB1 and COM terminals, between the VB2 and COM terminals, and between the VB3 and COM terminals
High side floating output voltage HO	V_{HO}	V_S-0.3	V_B+0.3	V	Maximum voltage on the HO1, HO2, and HO3 terminals
Low side and logic fixed supply voltage(VCC vs. VSS)	V_{CC}	-0.3	+25	V	Maximum voltage that can be applied between the VCC and VSS terminals
Low side and logic fixed supply voltage(VCC vs. COM)	V_{CCCOM}	-0.3	+25	V	Maximum voltage that can be applied between the VCC and COM terminals
Low side output voltage LO (LO vs COM)	V_{LO}	-0.3	V_{CCCOM} +0.3	V	Maximum voltage between the COM and LO1 terminals, between the COM and LO2 terminals, and between the COM and LO3 terminals
Logic input voltage HIN, LIN, EN	V_{IN}	-0.3	V_{CC}+0.3	V	Input voltage of the logic signal
/FAULT output voltage	V_{FLT}	-0.3	V_{CC}+0.3	V	Maximum applied voltage on the /FAULT terminal
RCIN input voltage	V_{RCIN}	-0.3	V_{CC}+0.3	V	Maximum input voltage for the RCIN terminal
ITRIP input voltage	V_{ITRIP}	-0.3	V_{CC}+0.3	V	Maximum input voltage for the ITRIP terminal
Power ground	V_{COM}	-5.5	+5.5	V	Maximum voltage for the COM terminal
Allowable offset voltage SLEW RATE	dV_S/dt	–	50	V/ns	Maximum slew rate for the VS1, VS2, and VS3 terminals
Junction temperature	Tjmax	–	150	℃	Maximum allowable junction temperature of the chip
Storage temperature	Tstg	-55	+150	℃	LSI storage temperature

2.2 Protection function and operation sequence

2.2.1 Pins for functions associated with the over current protection (OCP) circuit: COM, RCIN, and ITRIP terminals

By connecting an external shunt resistance (for current detection) and feeding back the voltage generated at the resistance to the ITRIP terminal, the over current protection can be provided.

The internal threshold voltage of the ITRIP terminal is 0.46 V (typical value). When the voltage on the ITRIP terminal exceeds the threshold voltage, the protection is activated, the output from the HO/LO terminal is then set to “Low”, and the external power element is turned OFF.

At the same time, the discharge switch inside the IC is turned ON, the RC terminal is then switched from “High” to “Low”, and the /FAULT terminal is switched from “High impedance” to “Low”.

■ Setting of the shunt resistor value (setting of the current value at which the over current protection circuit is activated)

The shunt resistor value R_S for setting the current value of the over current protection function is set from the threshold voltage of over current detection V_{IT_TH+} and the external resistor values R_S, R1, and R2 according to the following equation. When the value of over current detection is Iocp, the shunt resistor value R_S to be set is described as follows.

$$R_S = \frac{V_{IT\_TH+}}{Iocp} \qquad (2.2.1)$$

Iocp: Overcurrent detection value

V_{IT_TH+}: Threshold voltage for over current detection, 0.46 V (typ)

R_S: Current detection resistance

Numerical example

When Iocp = 5 A,

$$R_S = \frac{V_{IT\_TH+}}{Iocp} = \frac{0.46V(typ)}{5A} = 92m\Omega$$

As a value close to this value, 91mΩ is selected from the E24 series. Then, the over current detection value is determined as follows.

$$Iocp = \frac{V_{IT\_TH+}}{R_S} = \frac{0.46V(typ)}{91m\Omega} = 5.05A(typ)$$

When a DC current of this value flows, Pc_{RS} (consumption power of R_S) is given by $Pc_{RS} = R_S \cdot Iocp^2 = 91m\Omega \cdot (5.05\ A)^2 =$ 2.32 W (typ). Therefore, care must be taken regarding the power dissipation of the resistance.

When the power is applied on the resistance as pulses, the pulse limit power is treated as the actual value for the product. However, the guaranteed range for the pulse power is the rated power of each resistor, irrespective of the pulse times.

The maximum value of Iocp should be set to remain less than the rated current of the power element of the output stage, considering variations in the shunt resistance and V_{IT_TH+}.

In addition, a resonance waveform due to the parasitic inductance and capacitance of external wiring may activate the protection at a current lower than the set value. Eventually, adjust the shunt resistor value based on a detailed evaluation on the actual equipment.

Although the non-responding (blank) time t_{bl} = 150 ns (typ) is provided inside the IC to prevent a false detection by the OCP due to noise, it is recommended to place an RC filter immediately next to the ITRIP terminal. It is recommended to use ceramic capacitors.

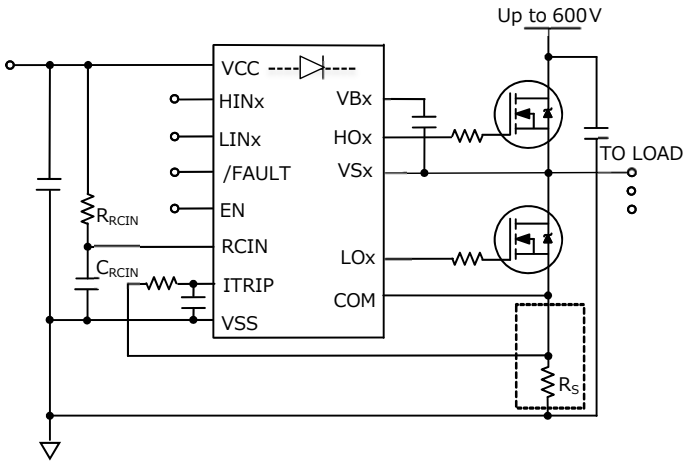


Figure 2.2.1. OCP detection schematic
(When inputting into the ITRIP terminal via an RC filter)

■ Release of the over current protection

Since the over current protection circuit has a hysteresis, the current value to be released is (V_{IT_TH+} - V_{IT_HYS})/R_S.

Numerical example

When R_S = 91mΩ,

($V_{IT\_TH+} - V_{IT\_HYS}$)／R_S=(0.46V(typ) – 0.07V(typ)) / 91mΩ= 4.29A(typ)

■ When the voltage generated at the shunt resistance is divided by the resistances (R1, R2) and input into the ITRIP terminal

Depending on the relation between the shunt resistor value and the set value for the over current protection, the voltage at the ends of the shunt resistor may exceed the threshold voltage. In this case, prepare a voltage to be input into the ITRIP terminal by dividing the voltage at the shunt resistor with R1 and R2, and set the voltage to the threshold voltage of the ITRIP terminal. Then, the value obtained by dividing the voltage at both ends of the shunt resistor with the resistances is compared with $V_{IT,TH+}$.

The calculation formula is as follows. Set the values of R1 and R2 between several kΩ to several tens of kΩ.

$$Iocp = \frac{R1+R2}{R2} \times \frac{V_{IT\_TH+}}{R_S} \rightarrow R_S = \frac{V_{IT\_TH+}}{Iocp} \times \frac{R1+R2}{R2} \quad (2.2.2)$$

Iocp: Overcurrent detection value

V_{IT_TH+}: Threshold voltage for over current detection, 0.46 V (typ)

R_S: Resistor value for current detection

R1,R2: Resistance for resistance division

Numerical example

When Iocp = 5 A and R_S = 0.15Ω,

$$\frac{R1+R2}{R2} = Iocp \times \frac{R_S}{V_{IT\_TH+}} = 5A \times \frac{0.15\Omega}{0.46V(typ)} = 1.630$$

Therefore,

$$\frac{R1}{R2} = 0.630$$

From the E24 series, select resistors that provide a similar ratio: R1 = 15kΩ and R2 = 24kΩ.

$$\frac{R1}{R2} = \frac{15k\Omega}{24k\Omega} = 0.625$$

Then, we obtain,

$$Iocp = (1 + 0.625) \times \frac{0.46V(typ)}{0.15\Omega} = 4.98A(typ)$$

When a DC current of this value flows, Pc_{RS} (consumption power of R_S) is given by $Pc_{RS} = R_S \cdot Iocp^2 = 0.15\Omega \cdot (4.98)^2 = 3.72$ W (typ). Therefore, care must be taken regarding the power dissipation of the resistance.
When the power is applied on the resistance as pulses, the pulse limit power is treated as the actual value for the product. However, the guaranteed range for the pulse power is the rated power of each resistor, irrespective of the pulse times.

Although the non-responding (blank) time t_{bl} = 150 ns (typ) is provided inside the IC to prevent a false detection by the OCP due to noise, it is recommended to place a ceramic capacitor immediately next to the ITRIP terminal.

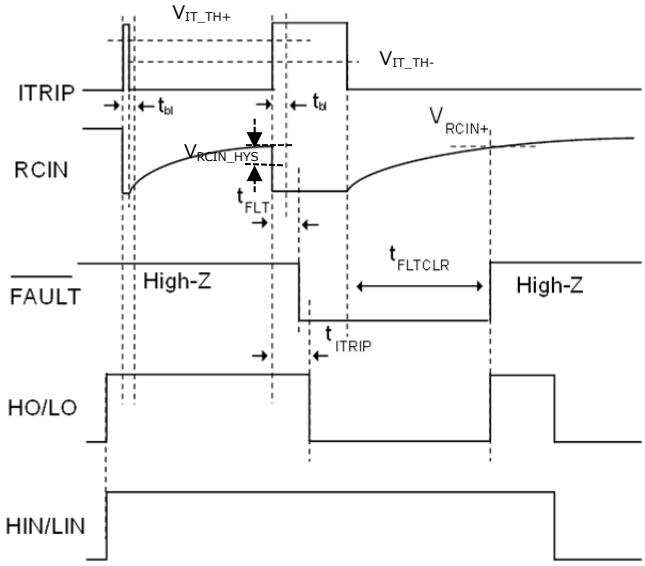


Figure 2.2.2 OCP Detection timing

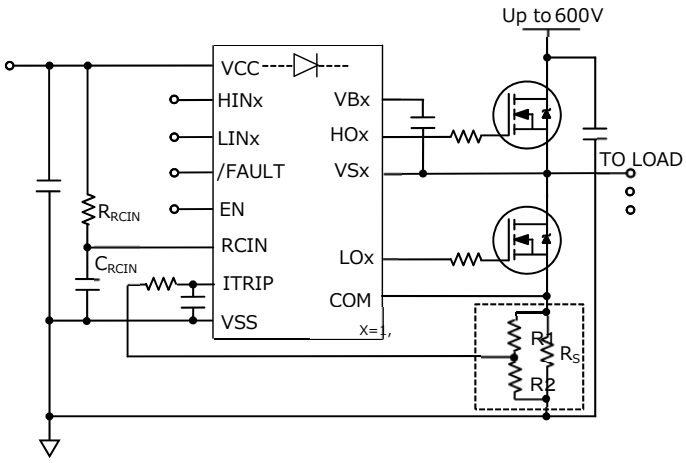


Figure 2.2.3 OCP detection schematic (When inputting into the ITRIP terminal using resistance division)

■ Setting of the OFF time (t_{FLTCLR}) of the power output stage

With an external CR (R_{RCIN}, C_{RCIN}), you can set the reset time (t_{FLTCLR}) when the /FAULT terminal is switched from “Low” to “High impedance” after the over current protection is released. Since the LO/HO terminal is switched to “Low” at this time, this is the OFF time of the power output stage.

Using the threshold voltage of the RCIN terminal V_{RCIN+} (8 V (typ)), the OFF time is determined by the following equation.

$$t_{FLTCLR} = -(R_{RCIN} \times C_{RCIN}) \times ln(1 - \frac{V_{RCIN+}}{V_{CC}}) \quad (2.2.3)$$

R_{RCIN}: Resistor value connected to the RCIN terminal

C_{RCIN}: Capacitor value connected to the RCIN terminal

Numerical example

V_{CC} = 15 V (typ) and t_{FLTCLR} = 0.1 s.

$$R_{RCIN} \times C_{RCIN} = -t_{FLTCLR} / \ln(1 - \frac{V_{RCIN+}}{V_{CC}}) = -0.1s / \ln\left(1 - \frac{8V(typ)}{15V(typ)}\right) = 0.81$$

When C_{RCIN} = 0.22 μF,

R_{RCIN} = 0.81/ 0.22μF = 595kΩ

Select a similar value from the E24 series. When the value is 620kΩ,

$$t_{FLTCLR} = -(620k\Omega \times 0.22\mu F) \times ln\left(1 - \frac{8V(typ)}{15V(typ)}\right) = 0.104s$$

The voltage on the RCIN terminal is increased with the time constant of the external RC. When the voltage exceeds 8 V (typ), the power output stage returns to the normal operation and the /FAULT terminal is switched from “Low” to “High impedance”.

The normal operation is also performed when the voltage on the RCIN terminal is less than V_{RCIN+} (8 V (typ)). However, the operation is suspended and will not recover once the voltage on the ITRIP terminal exceeds the threshold voltage V_{IT_TH+} (0.46 V (typ)). Set the voltage on the RCIN terminal to V_{RCIN+} (8 V (typ)) or higher during the normal operation.

■ Setting range of external constants for the RCIN terminal

Since Ron of the internal discharge switch of the RCIN terminal is 50Ω (typ), the latch does not work when the terminal voltage remains higher than 5 V (typ) with a low pull-up resistance. In this case, the /FAULT, HO, and LO terminals recover as soon as the over current protection is released. In the case of a high resistance, the charge current is reduced and a difference may be generated compared with the set time due to external noise. Therefore, a pull-up resistance between several tens of kΩ to 1MΩ is recommended.

2.2.2 Under voltage lock out (UVLO) circuit for control supply voltage

Reduction in the control supply voltage (voltage between the VB1 and VS1 terminals, between the VB2 and VS2 terminals, between the VB3 and VS3 terminals, or between the VCC and COM terminals) decreases the “High” voltage of the HO and LO terminals that is the gate driving voltage for external power elements. As a result, the gate voltage of the external power elements is reduced, causing problems such as insufficient capacity. Therefore, keep the supply voltage within the recommended range. When the control supply voltage is reduced below a specified voltage, the under voltage lock out (UVLO) circuit for the control supply voltage is activated.

The UVLO circuits are installed for the upper driving supply voltage on the VB1 terminal (voltage between the VB1 and VS1 terminals), the VB2 terminal (voltage between the VB2 and VS2 terminals), and the VB3 terminal (voltage between the VB3

and VS3 terminals) as well as for the lower control supply voltage V_{CC} (voltage between the VCC and COM terminals). However, only an activation of the UVLO for the VCC terminal voltage outputs the FAULT signal (error output).

■ Operation sequence of under voltage lock out (UVLO) circuit for the control supply voltage input V_{CC}

a. The protection is activated when V_{CC} is reduced to V_{CCUV-}.

b. The LO terminals on all of the lower phase change to “Low” (power elements are turned OFF).

c. The /FAULT output changes to “Low”. (The “Low” output continues until V_{CC} returns.)

d. When V_{CC} returns to V_{CCUV+}, the protection is released.

e. When the protection is released, an output logic is output according to the input signal.

f. In addition, the /FAULT terminal is switched from “Low” to “High impedance”.

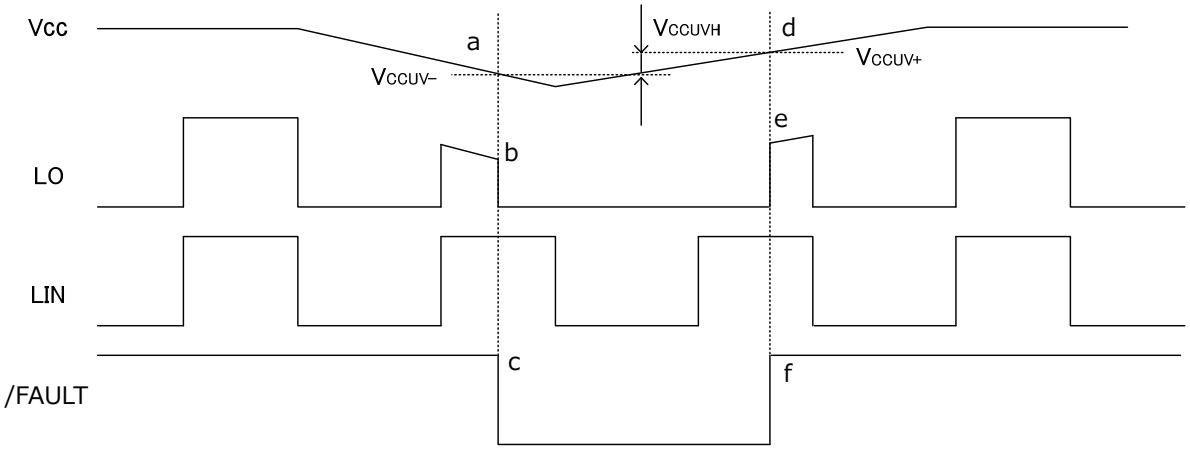


Figure 2.2.4 Timing chart of V_{CC} UVLO

■ Operation sequence of under voltage lock out (UVLO) circuit for the VB1, VB2, and VB3 control supply voltages

a. The protection is activated when the voltage between the VB1 and VS1 terminals, between the VB2 and VS2 terminals, or between the VB3 and VS3 terminals is reduced to V_{BSUV-}.

b. The HO terminals on all of the upper phase become “Low” (power elements are turned OFF).

c. The /FAULT output remains at “High”. (The UVLO for the VB1, VB2, or VB3 terminals does not affect the /FAULT terminal output.)

c. When all of VB1, VB2, and VB3 return to V_{BSUV+}, the protection is released.

e. Even when the protection is released, the output logic “High” is not output until a rising edge of the input signal arrives.

f. The /FAULT terminal remains at “High impedance”.

g. After the protection is released, the output logic “High” is output when a rising edge of the input signal arrives.

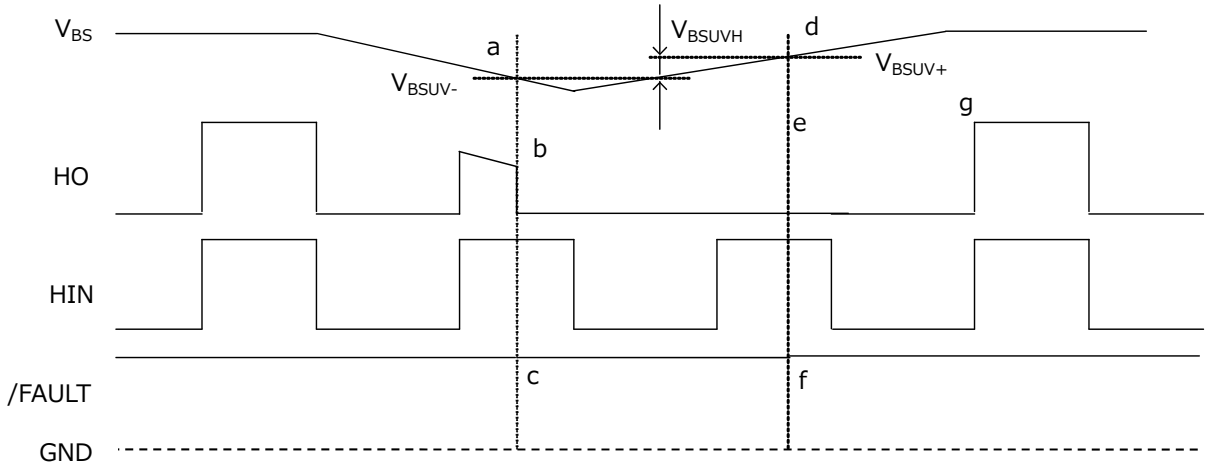


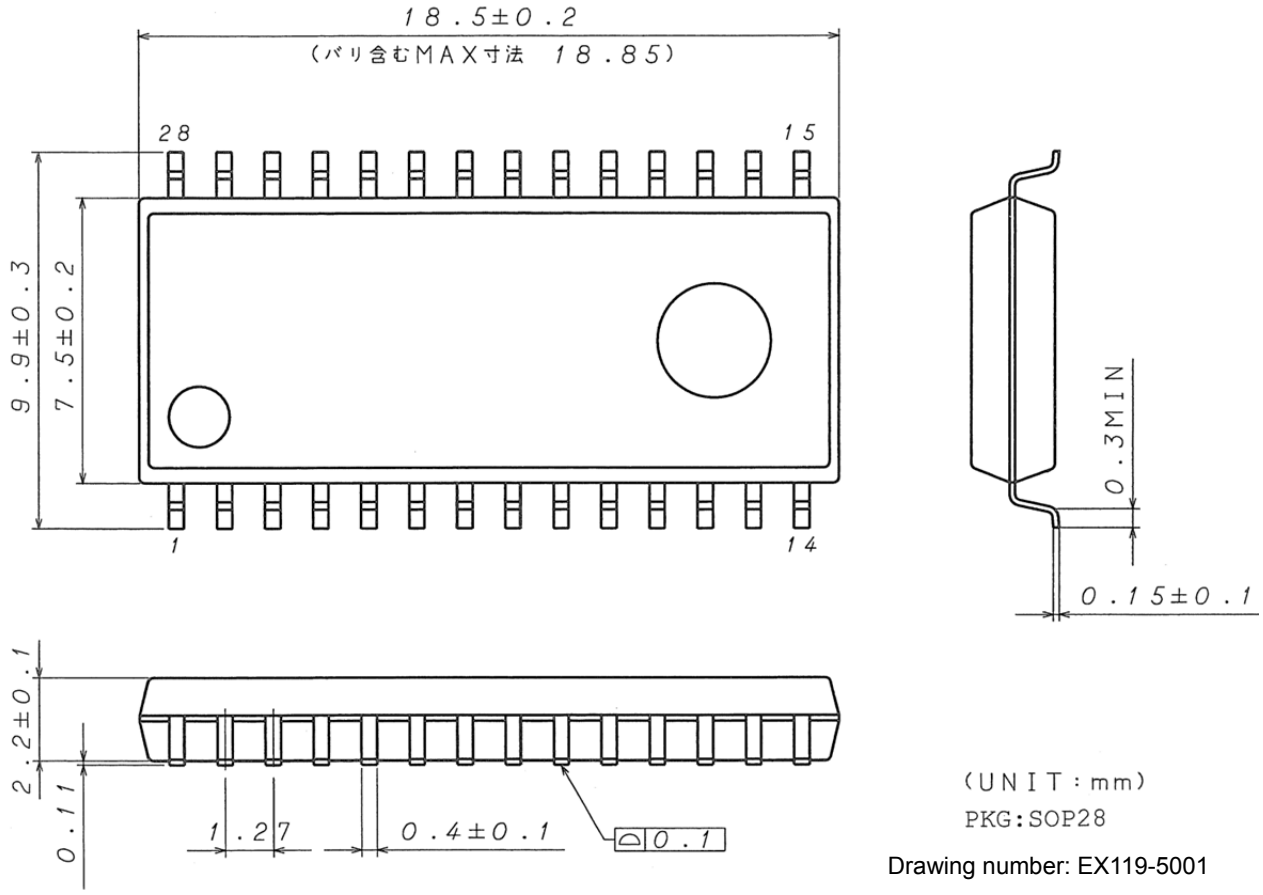
Figure 2.2.5 Timing chart of V_{BS} UVLO

2.3 Package

The SOP28 package is employed.

2.3.1 Outer dimensions drawing

Package Name	SOP28

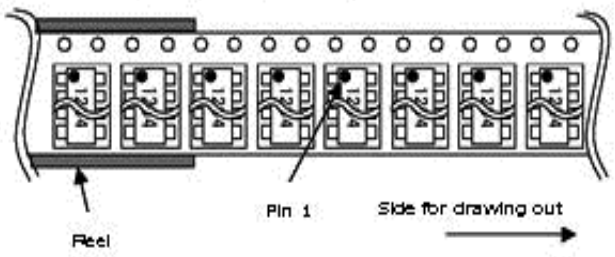


(UNIT:mm)
PKG:SOP28

Drawing number: EX119-5001

Packaging type, number of packages, packaging direction

Packaging type	Embossed taping
Number of packages	1500pcs
Packaging direction	E2 (direction in which pin 1 of the product is located on the upper left when you hold the reel in your left hand and draw out the tape with your right hand)



2.3.2 Terminal configuration

Table 2.3.1 Terminal descriptions

Pin No.	Pin Name	Function
1	VCC	Low-side supply voltage
2	HIN1	Logic input for high-side gate driver output (HO1), in phase
3	HIN2	Logic input for high-side gate driver output (HO2), in phase
4	HIN3	Logic input for high-side gate driver output (HO3), in phase
5	LIN1	Logic input for low-side gate driver output (LO1), in phase
6	LIN2	Logic input for low-side gate driver output (LO2), in phase
7	LIN3	Logic input for low-side gate driver output (LO3), in phase
8	/FAULT	OCP or low-side UVLO(VCC-COM) detect signal output (negative logic, open-drain output)
9	ITRIP	Analog input for over current shutdown, activates /FAULT and RCIN to VSS
10	EN	Logic input to enable I/O functionality (positive logic)
11	RCIN	External RC-network to define /FAULT clear delay after the /FAULT signal
12	VSS	Logic ground
13	COM	Power ground
14	LO3	Low-side gate drive output
15	LO2	Low-side gate drive output
16	LO1	Low-side gate drive output
17	NC	Non-Connection
18	VS3	High-side negative power supply
19	HO3	High-side gate drive output
20	VB3	High-side positive power supply
21	NC	Non-Connection
22	VS2	High-side negative power supply
23	HO2	High-side gate drive output
24	VB2	High-side positive power supply
25	NC	Non-Connection
26	VS1	High-side negative power supply
27	HO1	High-side gate drive output
28	VB1	High-side positive power supply

3. Applications

3.1 Example of practical application circuit (IGBT output stage)

In this example of an application circuit, the circuit design also considers external components for handling phenomena (or problems) that occur in the actual equipment.

Since some of the components included may be unnecessary in the actual equipment, an evaluation should be performed using a finalized actual set to optimize the circuit design.

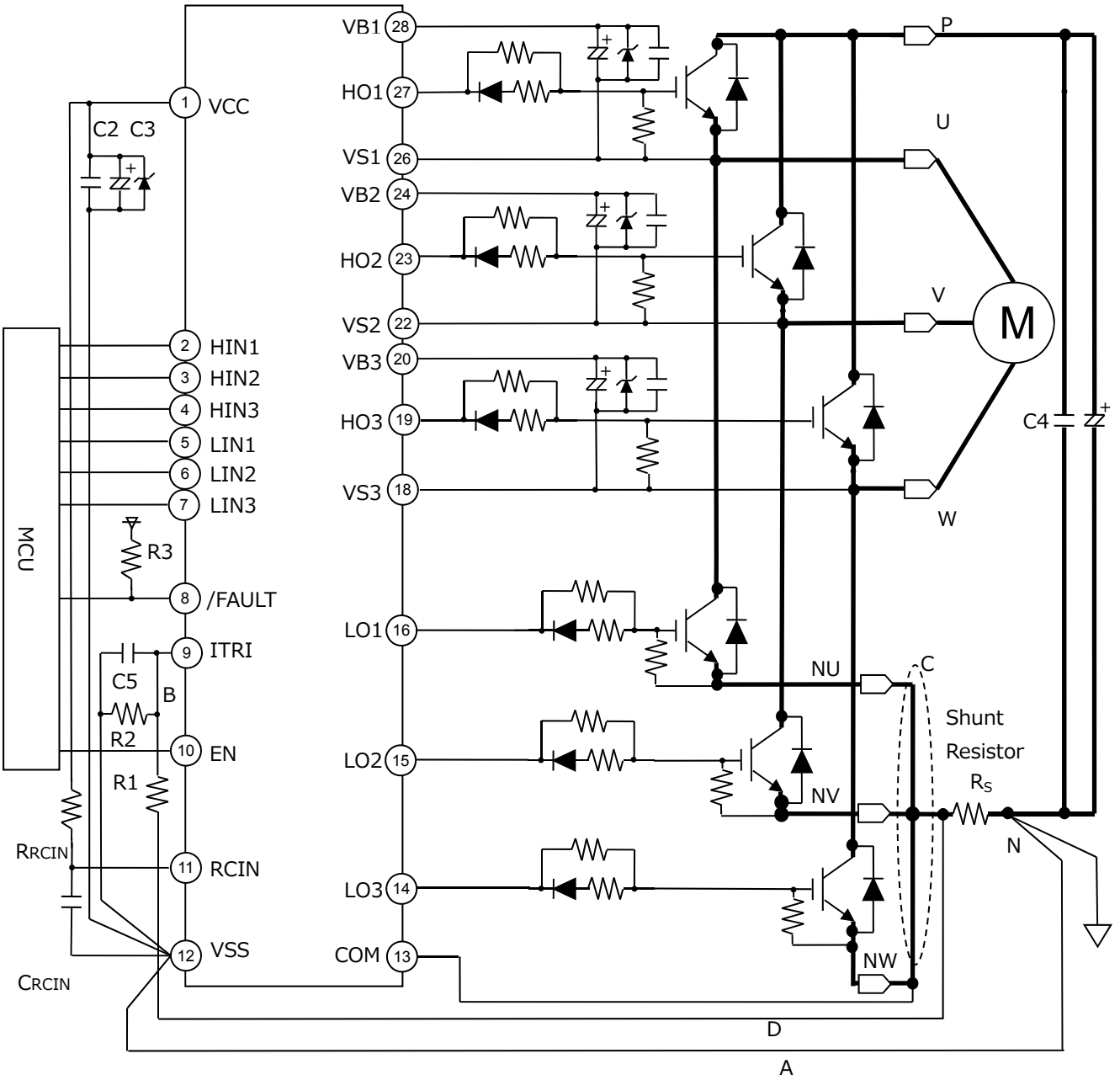


Figure 3.1.1 Example of application circuit

- When the wiring for A and D is long, a variation in the over current protection detection level is increased and a malfunction of the over current protection (OCP) circuit may be caused.
  When the wiring of C is too long, the output may be short-circuited.
- In this circuit example, the voltage generated at the shunt resistance is divided by R1 and R2 and input into the ITRIP terminal. When the resistance division is unnecessary, remove R2.

3.2 Selection method of application components (refer to Figure 3.1.1)

3.2.1 Bootstrap circuit (VB1, VB2, and VB3 terminals)

By creating a floating power supply with a bootstrap circuit, you can obtain the four independent power supplies that are normally necessary for driving an inverter (power supplies for driving the upper power elements in three phases and for driving the lower power elements) from a single V_{CC} power supply.

Installing an external bootstrap capacitor (C_{BS}) allows you to configure a bootstrap circuit (Figure 3.2.1). C_{BS} functions as a power supply, providing the upper power element driving current and the upper gate drive supply current. Electric charges consumed for driving the circuit are charged into C_{BS} from the VCC power supply through the BSD, when the potential of the VS1, VS2, or VS3 terminal (external output terminal for each phase) is reduced to near the ground level. Depending on the driving methods, the capacitance value of C_{BS}, or other factors, the electric charge may not be charged adequately, reducing the C_{BS} potential. This can lead to deterioration of losses in the power elements, heating, or activation of the UVLO. Therefore, the circuit constants such as the capacitance value of C_{BS} should be determined based on a detailed evaluation on the actual equipment.

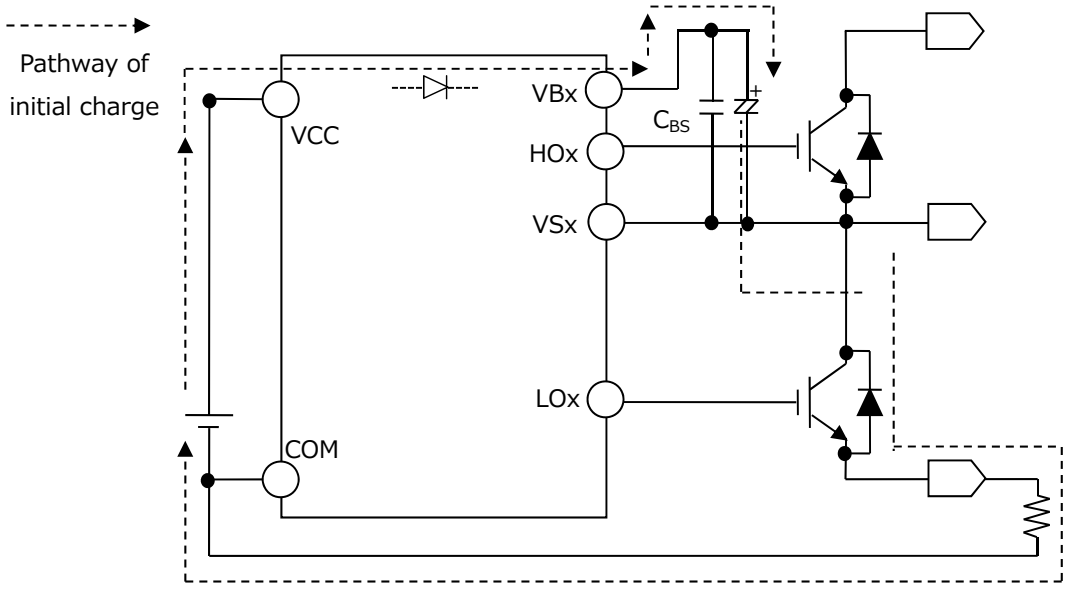


Figure 3.2.1 Bootstrap circuit (with IGBT power element, simplified single phase)

■ Initial charge

When you use a bootstrap circuit, it is necessary to charge C_{BS} in advance before starting the circuit. Normally, C_{BS} is charged by turning ON all phases of the lower power element. When a motor load is connected, the charging may be performed via the motor winding by turning on only one phase. However, it should be noted that the charging efficiency is reduced due to the resistance in the motor winding and wiring.

The initial charge can be performed using two methods: single pulse method (Figure 3.2.2) and multiple ON pulses method when there is a limitation such as the supply capacity of the 15 V control power supply (Figure 3.2.3). The time required for the initial charge depends on the capacitance of C_{BS} and the resistance for the current limit. Therefore, you should secure an adequate charge time according to the capacitance value of C_{BS}, based on a detailed evaluation on the actual equipment.

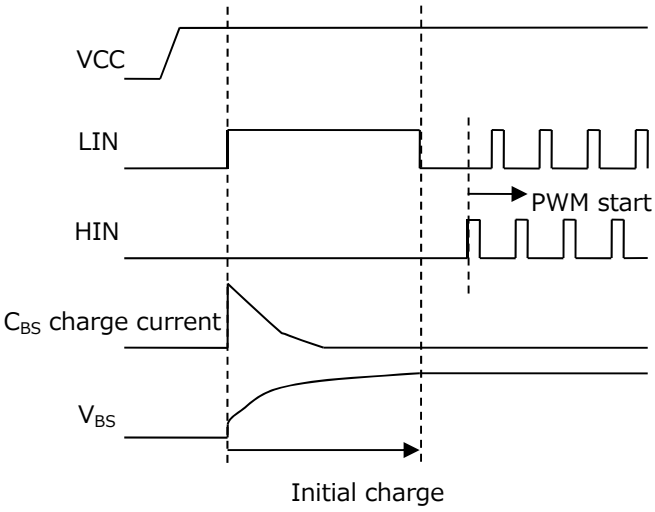


Figure 3.2.2
Initial charge sequence with a single pulse

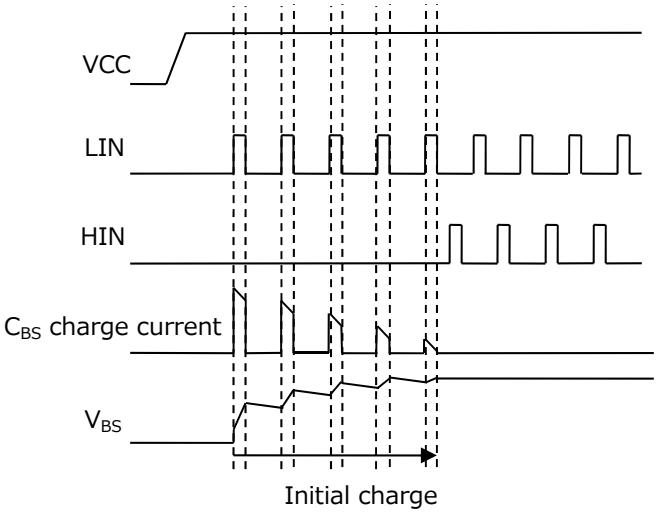


Figure 3.2.3
Initial charge sequence with multiple pulses

■ Design method of bootstrap capacitor C_{BS}

For capacitors to be used in bootstrap circuits, we recommend ceramic capacitors with low ESR in order to reduce a ripple voltage. When the capacitance of a ceramic capacitor is insufficient, connect an electrolytic capacitor in parallel to the ceramic capacitor.

The size of the bootstrap capacitor is determined by the value of the voltage drop and the total amount of supplied charges. The minimum voltage drop ΔV_{BS} that can turn ON power devices on the high side is determined by the following equation.

$$\Delta V_{BSMAX} = V_{CC} - V_F - V_{GEMIN} - V_{OL} - V_{RS} \quad (3.2.1)$$

V_{CC}: Supply voltage for the gate driver
V_{BOOT}: Forward voltage drop in the bootstrap diode
V_{GEMIN}: Minimum voltage between the gate and source that can keep the upper side power elements ON
V_{OL}: ON voltage for the lower side power elements
V_{RS}: Voltage between the current detection resistances

Since BS2132F has a built-in diode for the bootstrap, V_{BOOT} is the voltage between VCC and VB terminals.
To obtain this V_{BOOT}, obtain the average current (I_{CHARGE}) which charges from VCC to CBS during operation, and read the voltage between VCC and VB terminals from Figure 3.2.4

$$I_{CHARGE} = I_{GC} + I_{LV} = C_{ISS} \times V_{BSO} \times F_{OSC} + 2.5 \times 10^{-9} \times F_{OSC} \quad \cdots\cdot(3.2.2)$$

I_{GC}: Average gate charge current of power device
I_{LV}: Average consumption current of the level shift circuit of gate driver
V_{BSO}: V_S=0, steady state voltage between VB and VS terminal (V_{BSO}=V_{CC}-VF)
C_{ISS}: Input capacitance of the power device
F_{OSC}: High-side operating frequency

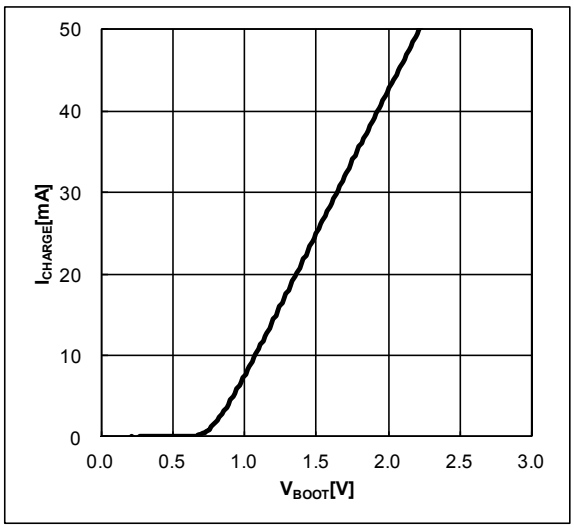


Figure 3.2.4 I_{CHARGE} VS V_{BOOT} (VCC-VB voltage)

In addition, total charge amount Q_{Total} is determined by the following equation.

$$Q_{Total} = Q_G + \left(I_{LKGS} + I_{LK} + I_{LKDIO} + I_{QBS}\right) \times t_{HON} \quad (3.2.3)$$

Q_G: Gate charge required to turn ON the power element
I_{LKGS}: Leakage current between the gate and emitter of the power element
I_{LK}: Leakage current in the level shift circuit of the gate driver IC
I_{LKDIO}: Leakage current in the bootstrap diode
I_{QBS}: Supply current in the high side of the gate driver IC
T_{HON}: ON time for the high side

Accordingly, set the capacitance value of the bootstrap capacitor so that the following equation is satisfied.

$$C_{BS} \geq \frac{Q_{Total}}{\Delta V_{BS}} \quad (3.2.4)$$

Please decide the C_{BS} value of the capacitor that is actually used by providing a sufficient margin, by considering the variations in power-supply voltage, the variations in the electrical characteristics of each element and the temperature characteristics etc., with respect to the C_{BS} that is calculated here.
(Please be sure to confirm the operation with the actual machine, by picking the suitable margins in every C_{BS} value.)
Substitute the determined value of C_{BS} to be used in the following equation to find the voltage drop value ΔV_{BS} between the VCC and VB terminals in the C_{BS} to be used.

$$\Delta V_{BS} = \frac{Q_{Total}}{C_{BS}}$$

Also, in order to prevent ULVO between VB and VS from operating under each condition including ΔV_{BS} obtained above, the following equation must be satisfied.

$$V_{cc} - V_{BOOT} - V_{OL} - V_{RS} - \Delta V_{BS} \geq V_{BSUV+} \quad \cdots (3.2.5)$$

V_{BSUV+}:minimum operating voltage between VB and BS terminals (Max. value of V_{BSUV+})

In the case that it is not possible to satisfy the Equation (3.2.5), there is a possibility that UVLO detection may not operate properly. In that case, it is necessary to take countermeasures such as adding a fast recovery diode with small reverse recovery time (trr) at low VF externally etc., hence, please be sure to check thoroughly with the real machine.

Numerical example

Use an IGBT RGT8BM65D (V_{CES} = 650 V, $I_{C(100°C)}$ = 4 A) as the power element.

1. To obtain V_F

Ciss=220pF(from the electrical characteristics in RGT8BM65D data sheet)
V_{BSO}=14.3V
F_{OSC}=10kHz
From the above, I_{GC}=Ciss ＊ V_{BSO} ＊ F_{OSC}=31.5μA、 I_{LV}=2.5 ＊ 10-9 ＊ F_{OSC}=25μA
I_{CHARGE}=I_{GC} + I_{LV}=56.5μA
When VBOOT at this time is read from the graph (Figure 3.2.4), VBOOT≒0.7V

2. To otain ΔV_{BSMAX}

V_F = 0.7 V (typ) from above equation

V_{GEMIN} = 9.7 V (typ) [V_{GE} when I_C = 4.0 A] (from the electrical characteristics curve in the RGT8BM65D data sheet)

V_{OL} = 1.65 V (typ) [$V_{CE(sat)}$ when I_C = 4.0 A] (from the electrical characteristics in the RGT8BM65D data sheet)

$V_{RS} = I_C \cdot R_S$ = 4.0 A·0.15Ω (typ) = 0.6 V (typ)

When these values are substituted in Equation (3.2.1),

ΔV_{BS} = 15 V (typ) - 0.7 V (typ) - 9.7 V (typ) - 1.65 V (typ) - 0.6 V (typ) = 2.35 V (typ)

is obtained.

3. To obtain the amount of total charge supplied to the high side circuit.

Q_G = 13.5 nC (typ) [when I_C = 4.0 A] (from the electrical characteristics in the RGT8BM65D data sheet)

I_{LKGE} = 200 nA (max) (from the electrical characteristics in the RGT8BM65D data sheet)

I_{LK} = 50 μA (max) (from the electrical characteristics in the BS2132F data sheet)

I_{LKDIO} = 50 μA (max) (from the electrical characteristics in the RFN1L6S data sheet)

I_{QBS} = 120 μA (max) (from the electrical characteristics in the BS2132F data sheet)

T_{HON} = 100 μs (typ) (when the PWM frequency is 10 kHz and the ON time of the upper side power element is the maximum of the PWM period)

When these values are substituted in Equation (3.2.3),

Q_{Total}=13.5nC(typ) + {200nA(max) + 50μA(max) + 50μA(max) + 120μA(max)}·100μs(typ)

=13.5nC(typ) + 22.0 nC = 35.5nC

is obtained.

4. To obtain the value of the bootstrap capacitor

When the values of ΔV_{BS} and Q_{Total} are substituted in Equation (3.2.4),

$$C_{BS} \geq \frac{35.5\text{nC}}{2.35\text{V}} = 14.3\text{nF}$$

is obtained.

By providing a margin for the 14.3nF that was calculated, adopt a 2.2μF capacitor this time as the bootstrap capacitor CBS.

When ΔVBS is obtained in the case of adopting 2.2 μF, it will turn out to be 16mV.

$$\Delta V_{BS} = \frac{35.3nC}{2.2\mu F} = 0.016V$$

Meanwhile, since the UVLO (10.2 V (typ)) is installed between VB and VS, C_{BS} should also be set so that the voltage between VB and VS remains at higher than the voltage that will activate the UVLO by ΔV_{BS}.

In order to prevent the UVLO between the VB and VS terminals from operating, it is necessary to satisfy the following equation.

$V_{CC} - V_{BOOT} - V_{OL} - V_{RS} - \Delta V_{BS} > V_{BSUV-}$

Left side of the above equation =15V-0.7V-1.65V-0.6V-0.016V=12.0V, and it can be seen that it is larger than V_{BSUV-}.

In additional, if a countermeasure against surge is necessary, place a Zener diode(21V～24V) for surge absorption immediately next to the terminal.

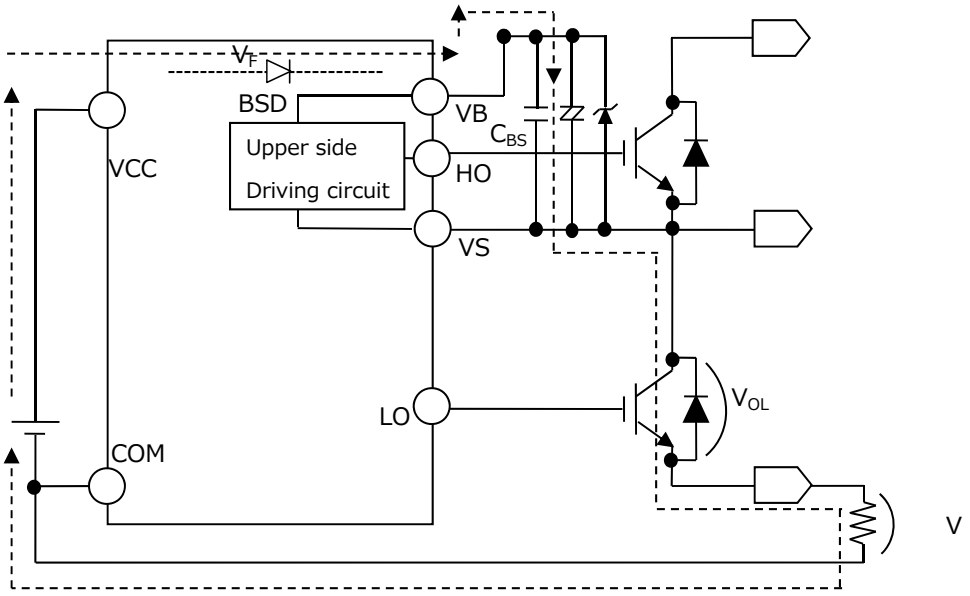


Figure 3.2.5 Bootstrap circuit (with IGBT power element, simplified single phase)

3.2.2 Design method for output gate resistance

With an output gate resistance, you can set the switching time t_{SW} or the variation rate of the output voltage dV_S/dt (the slew rate of the output voltage).

For the gate resistance setting, consider the switching time or the variation rate of the output voltage that is required for the set, and determine the gate resistance that provides such characteristics.

■ Value of the gate resistance at turn-on

(1) Method for calculating the gate resistance from the switching time t_{SW}

The switching time t_{SW} is defined as the time shown in Figure 3.2.5.

•The current that flows through the gate of the power device is described by the following equation.

$$I_g = \frac{Q_{ge}+Q_{gc}}{t_{SW}} \qquad (3.2.6)$$

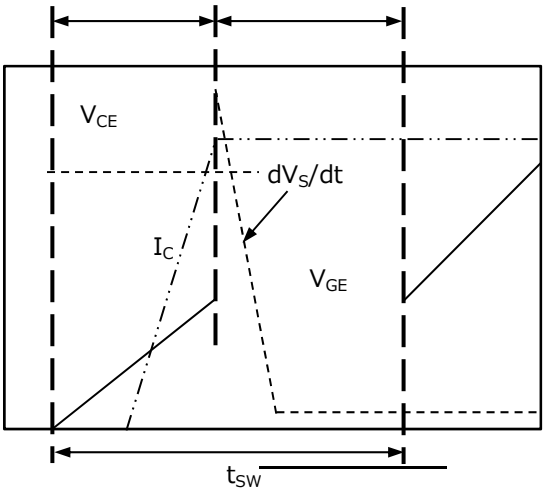


Figure 3.2.6 Gate charge transfer characteristics

•The gate resistance at turn-on is described by the following equation.

$$R_{TOTAL(on)} = R_{pon} + R_{G(on)} = \frac{V_{BS}-V_{ge(th)}}{I_g} \qquad (3.2.7)$$

By substituting Equation (3.2.6) into Equation (3.2.7), the gate resistance is determined as follows.

$$R_{G(on)} = \frac{(V_{BS} - V_{ge(th)}) \times t_{SW}}{Q_{ge} + Q_{gc}} - R_{pon} \quad (3.2.8)$$

t_{SW}: Required switching time

V_{BS}: Gate drive voltage in the high side

$V_{ge(th)}$: ON threshold of the power element

Q_{ge}: Charge between the gate and emitter of the power element

Q_{gc}: Charge between the gate and collector of the power element

R_{pon}: ON-resistance in the high side of the output stage of the gate driver

Numerical example

Use an IGBT RGT8BM65D (V_{CES} = 650 V, $I_{C(100°C)}$ = 4 A) as the power element.

t_{SW} = 1 μs (with the PWM frequency of 10 kHz, the switching time should be less than 1/100 of the PWM period)

$V_{BS} = V_{CC} - V_F$ = 15V(typ) -0.7V(typ) = 14.3V(typ) (V_{CC} = 15 V (typ) and)

$V_{ge(th)}$ = 9.7 V (typ) [V_{GE} when I_C = 4.0 A] (from the electrical characteristics curve in the RGT8BM65D data sheet)

Q_{ge} = 4.0 nC (typ) (from the electrical characteristics in the RGT8BM65D data sheet)

Q_{gc} = 5.5 nC (typ) (from the electrical characteristics in the RGT8BM65D data sheet)

R_{pon} = 28Ω (typ) (from the electrical characteristics curve in the BS2130F data sheet)

When these values are substituted in Equation (3.2.8),

$$\mathrm{R_{G(on)}} = \frac{(14.3\mathrm{V(typ)} - 9.7\mathrm{V(typ)}) \times 1\mu\mathrm{s(typ)}}{4.0\mathrm{nC} + 5.5\mathrm{nC}} - 28\Omega(\mathrm{typ}) = 484\Omega(\mathrm{typ}) - 28\Omega(\mathrm{typ}) = 456\Omega(\mathrm{typ})$$

is obtained.

(2) Method for calculating the gate resistance from the variation rate of the output voltage (slew rate of the output stage)

•The value of dV_S/dt can be determined from the value of the gate resistance. The slew rate of a power device is determined by the following equation.

$$\frac{dV_S}{dt} = \frac{I_g}{C_{res}} \quad (3.2.9)$$

• The gate resistance at turn-on is described by the following equation.

$$R_{TOTAL(on)} = R_{pon} + R_{G(on)} = \frac{V_{BS} - V_{ge(th)}}{I_g} \quad (3.2.10)$$

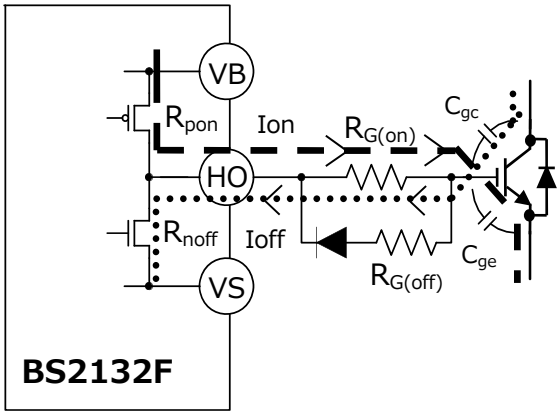


Figure 3.2.7 Gate Driver Equivalent Circuit

By substituting Equation (3.2.9) into Equation (3.2.10), the gate resistance $R_{G(on)}$ is determined as follows.

$$R_{G(on)} = \frac{V_{BS} - V_{ge(th)}}{C_{res} \times \frac{dV_S}{dt}} - R_{pon} \quad (3.2.11)$$

dV_S/dt: Variation rate of the output voltage (slew rate of the output stage)

C_{res}: Feedback capacitance of the power element

V_{BS}: Gate drive voltage in the high side

$V_{ge(th)}$: ON threshold of the power element

R_{pon}: ON-resistance in the high side of the output stage of the gate driver

Numerical example

Use an RFN1L6S fast recovery diode (V_R = 600 V, I_O = 0.8 A) as the bootstrap diode and an IGBT RGT8BM65D (V_{CES} = 650 V, $I_{C(100°C)}$ = 4 A) as the power element.

dV_S/dt = 3.0 V/ns (a value that satisfies the noise and heating requirements based on an empirical rule)

C_{res} = 4.5 pF (from the electrical characteristics in the RGT8BM65D data sheet)

$V_{BS} = V_{CC}-V_F$ = 15V(typ)-0.7V(typ) = 14.3V(typ)

(V_{CC} = 15 V (typ))

$V_{ge(th)}$ = 9.7 V (typ) [V_{GE} when I_C = 4.0 A] (from the electrical characteristics curve in the RGT8BM65D data sheet)

R_{pon} = 28Ω (typ) (from the electrical characteristics curve in the BS2130F data sheet)

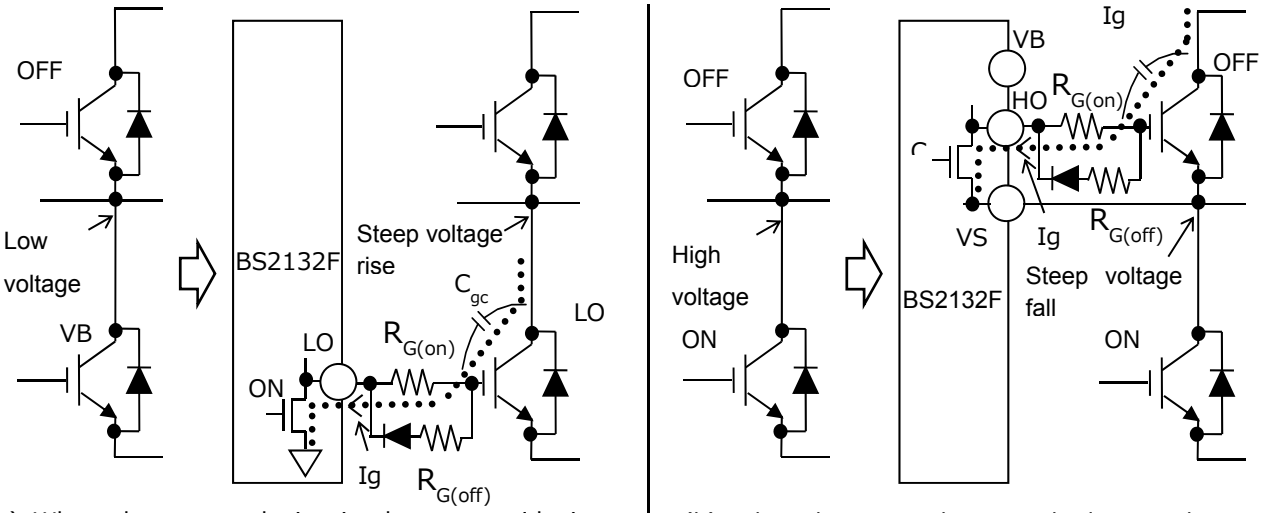
When these values are substituted in Equation (3.2.11),

$$R_{G(on)} = \frac{14.3V(typ)-9.7V(typ)}{4.5pF(typ)\times 3V/ns} - 28\Omega(\text{typ}) = 340\Omega(\text{typ}) - 28\Omega(\text{typ}) = 279\Omega(\text{typ})$$

is obtained.

■ Value of the gate resistance at turn-off

When the power device in either the upper or lower side is turned OFF, turning ON the power device in the other side causes a current (Ig) flowing via C_{gc} of the power device in the side that is turned OFF. (Figure3.2.8)



(a) When the power device in the upper side is turned ON

(b) When the power device in the lower side is turned ON

Figure 3.2.8 Rise in the gate voltage of the power device that is turned OFF

At this point, set the value of the gate resistance ($R_{G(off)}$) so that the gate voltage does not exceed the threshold of the power element ($V_{ge(th)}$) and turn ON the element itself.

$$V_{ge(th)} \geq \left(R_{noff} + R_{g(off)}\right) \times I_g + V_F = \left(R_{noff} + R_{g(off)}\right) \times C_{gc}\frac{dV_S}{dt} + V_F \qquad (3.2.12)$$

By transforming the above equation, we obtain the following equation.

$$R_{g(off)} \leq \frac{V_{ge(th)}-V_F}{C_g\frac{dV_S}{dt}} - R_{noff} \quad (3.2.13)$$

dV_S/dt: Variation rate of the output voltage (slew rate of the output stage) of the power element in the side that is turned ON

C_{gc}: Capacitance between the gate and collector ($C_{gc} = C_{res}$)

$V_{ge(th)}$: ON threshold of the power element

V_F: Forward voltage drop in the diode that is connected in series to the gate resistance ($R_{G(off)}$)

R_{noff}: ON-resistance in the low side of the output stage of the gate driver

Numerical example

Use an IGBT RGT8BM65D (V_{CES} = 650 V, $I_{C(100°C)}$ = 4 A) as a power element and an RB160VAM-40 Schottky barrier diode (V_R = 40 V, I_O = 1.0 A) as the diode that is connected in series to the gate resistance ($R_{G(off)}$).

dV_S/dt = 3.0 V/ns (from a standard setting for the slew rate of the output stage of the power element that is turned ON)

$C_{gc} = C_{res}$ = 4.5 pF (typ) (from the electrical characteristics in the RGT8BM65D data sheet)

$V_{ge(th)}$ = 6.0 V (typ) [when IC = 2.8 mA] (from the electrical characteristics in the RGT8BM65D data sheet)

V_F = 0.50 V (typ) [when I_F = 0.7 A] (from the electrical characteristics in the RB160VAM-40 data sheet)

R_{noff} = 13Ω (typ) (from the electrical characteristics curve in the BS2130F data sheet)

When these values are substituted in Equation (3.2.11),

$$\mathrm{R_{g(off)}} \leq \frac{6.0\mathrm{V(typ)}-0.5\mathrm{V(typ)}}{4.5\mathrm{pF(typ)}\times\frac{3.0\mathrm{V}}{\mathrm{ns}}} - 19\Omega\mathrm{(typ)} = 444\Omega\mathrm{(typ)} - 19\Omega\mathrm{(typ)} = 425\Omega$$

is obtained.

$R_{g(off)}$ is set to a value that is 1/3 to 1/10 of $R_{g(on)}$ to adjust the slew rate and prevent the power elements in the upper and lower sides from being turned ON simultaneously.

3.2.3 VCC terminal (V_{CC})

- To prevent a malfunction or breakdown due to a switching noise or power supply ripple, install electrolytic capacitor C3, which has excellent temperature and frequency characteristics as a bypass capacitor immediately next to the terminal. To reduce the power supply impedance over a broad frequency bandwidth, also install ceramic capacitor C2 (characteristics B or R recommended) with a capacitance of 0.1 μF to 0.22 μF, which have excellent temperature, frequency, and DC bias characteristics in parallel to the electrolytic capacitor immediately next to the terminal.
- If a countermeasure against surge is necessary, place a zener diode (20 V to 22 V) with a power loss of approximately 1 W for surge absorption immediately next to the terminal.
- Since the V_{CC} capacitor of BS2132F supplies charges to the high and low sides and it also supplies a large amount of charge for the initial charge of bootstrap capacitor C_{BS}, a capacitor that has a capacitance larger than the total capacitance of the bootstrap capacitors in three phases by a factor of 2 (larger than the capacitance of a bootstrap capacitor by a factor of 4) is recommended.
- Design a power supply circuit that satisfies $V_{ripple} \leq 2\ V_{p\text{-}p}$ with the power supply noise of dV/dt ≤ 1 V/μs. (Reference value)

3.2.4 Power supply for external power element

- To prevent an over voltage breakdown due to a surge voltage, keep the wiring between the smoothing capacitor and points P and N (the terminal parts of the shunt resistor) as thick and short as possible.
- It is recommended to install snubber capacitor C4 with a capacitance of 0.1 μF to 0.22 μF between points P and N.

3.2.5 Control input terminal (HIN1, HIN2, HIN3, LIN1, LIN2, and LIN3)

• To prevent a malfunction, keep the wiring as short as possible.

• The input signal is high-active. A pull-down at approximately 33kΩ (typ) is performed inside the LSI. When inserting an RC filter, adjust the setting to satisfy the input threshold voltage.

• Be sure to observe the rest time (Δt_{IN}) for the upper and lower arms as described below.

• Input signal interval Δt_{IN}

The minimum interval between input signals ($\Delta t_{IN(min)}$) that is required to prevent the power elements in the high and low sides from being turned ON simultaneously can be calculated by the following equation.

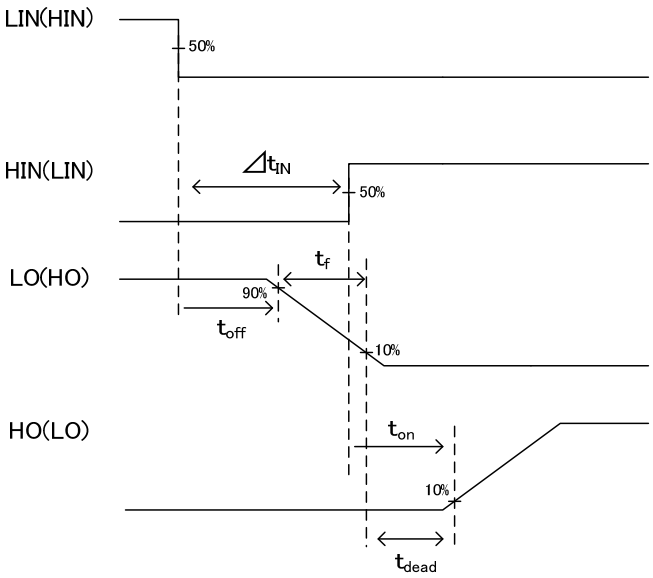


Figure 3.2.9 Shoot-through prevention timing

$$t_{dead} \approx (t_{on} + \Delta t_{IN}) - (t_{off} + t_f) \quad (3.2.14)$$

$$t_f = -\tau \times (ln0.1 - ln0.9) \quad (3.2.15)$$

$$\tau = (R_{non} + R_G) \times C_L \quad (3.2.16)$$

t_{on}: Propagation delay in the ON side

t_{off}: Propagation delay in the OFF side

t_f: Fall time

R_{non}: N-channel on-resistance of the final stage of the gate driver

R_G: Gate resistance

C_L: Load capacitance

To prevent the simultaneous ON, design the timing to satisfy the following conditions.

$$t_{dead} > 0 \quad (3.2.17)$$

$$(t_{on} + \Delta t_{IN}) - (t_{off} + t_f) > 0 \quad (3.2.18)$$

$$\Delta t_{IN} > (t_{off} - t_{on}) + t_f \quad (3.2.19)$$

$$\Delta t_{IN(min)} > (t_{off(max)} - t_{on(min)}) - (R_{non(max)} + R_G) \times C_L \times (ln0.1 - in0.9) \quad (3.2.20)$$

3.2.6 /FAULT terminal

• The output is open-drain. The on-resistance of the internal element is 50Ω (typ.). Using resistance R3, pull up to a voltage that is less than the Vcc supply voltage in order to obtain $I_{/FAULT}$ = 5 mA or less.

A rough estimation can be made using $I_{/FAULT}$ = pull-up supply voltage/pull-up resistor value R3.

3.2.7 ITRIP terminal (input terminal for output stage current monitor signal)

• When the over current protection is used, the signal at the end of the shunt resistor is input. To prevent a malfunction due to a recovery current or noise during the switching, connect a C filter immediately next to the ITRIP terminal. For C filter C5, a filter with a small variation, such as a filter for temperature compensation, is recommended. Since the cutoff time varies with the wiring pattern of the board, etc., perform evaluation thoroughly on the actual application.

• Separate the wiring to the ITRIP terminal at point D immediately next to the terminal part of the shunt resistor. Keep the wiring as short as possible.

3.2.8 RCIN terminal (refer to Page 7)

With an external CR (R_{RCIN}, C_{RCIN}), you can set the reset time (t_{FLTCLR}) when the FAULT terminal is switched from “Low” to “High impedance” after the over current protection is released. For more details on the setting method, refer to Page 7.

3.2.9 VSS and COM terminals

• The ground terminals are placed at two locations: 12-pin (VSS terminal) and 13-pin (COM terminal). The 12-pin (VSS) terminal is the ground of the control system. The 13-pin (COM) terminal serves as the ground of the output stage part of the IC.

• When an external shunt resistance is connected, connect the shunt resistance to the side of the common emitter (or source) of the external power device in the lower side and do not connect it to the ground. When three external shunt resistances are connected, connect the shunt resistances to the ground. At this point, it is recommended to separate the wiring for the 12-pin (VSS terminal) and 13-pin (COM terminal), so that they will not have a common impedance. Keep the wiring for the 13-pin (COM terminal) as thick and short as possible.

• If the ground of the control system is affected by the variation in the ground of the power device part where a large current flows, the IC malfunction may be caused. Therefore, separate the wiring for the ground of the control system and the ground of the power device part and connect them at a single point N (the terminal part of the shunt resistor). Also keep the wiring for the ground of the control system as thick and short as possible.

3.2.10 Shunt resistor

(1) Driving with one shunt resistor

Notes for the wiring around an external shunt resistor when driving with one shunt resistor are shown in the figure below.

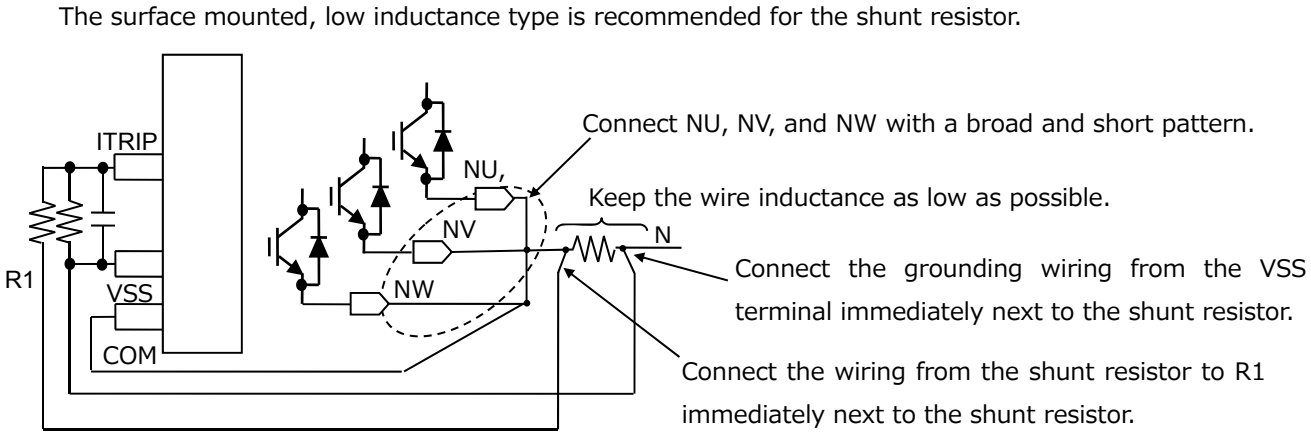


Figure 3.2.10 Wiring around an external shunt resistor when driving with one shunt resistor

(2) Driving with three shunt resistors

• When driving with three shunt resistors, since the voltage of the shunt resistors on three phases cannot be input directly to the ITRIP terminal, an external circuit is required for the short-circuit current protection. An example of the external circuit and notes for the wiring around external shunt resistors are shown in the figure below.

• Set the time constants of the RC filter (R_f, C_f) for the malfunction prevention sufficiently short to prevent transistors on the power output stage from breaking during a delay time when a short-circuit occurs. Since the cutoff time depends on the wiring pattern of the board, reaction time of the comparator, etc., perform evaluation thoroughly on the actual application.

• The recommended value for the threshold voltage VREF is 0.46 V (typ), which is the same as the standard value for the trip voltage of the over current protection $V_{IT,TH+}$ of the IC.

• To prevent a malfunction, keep the wiring for A, B, and C as short as possible.

• Set the High level (output during protection) of the OR output to the maximum value of the trip voltage of the over current protection $V_{IT,TH+}$ (0.483 V) or higher. At the same time, the High level should remain lower than the absolute maximum rating V_{CC} for the ITRIP terminal.

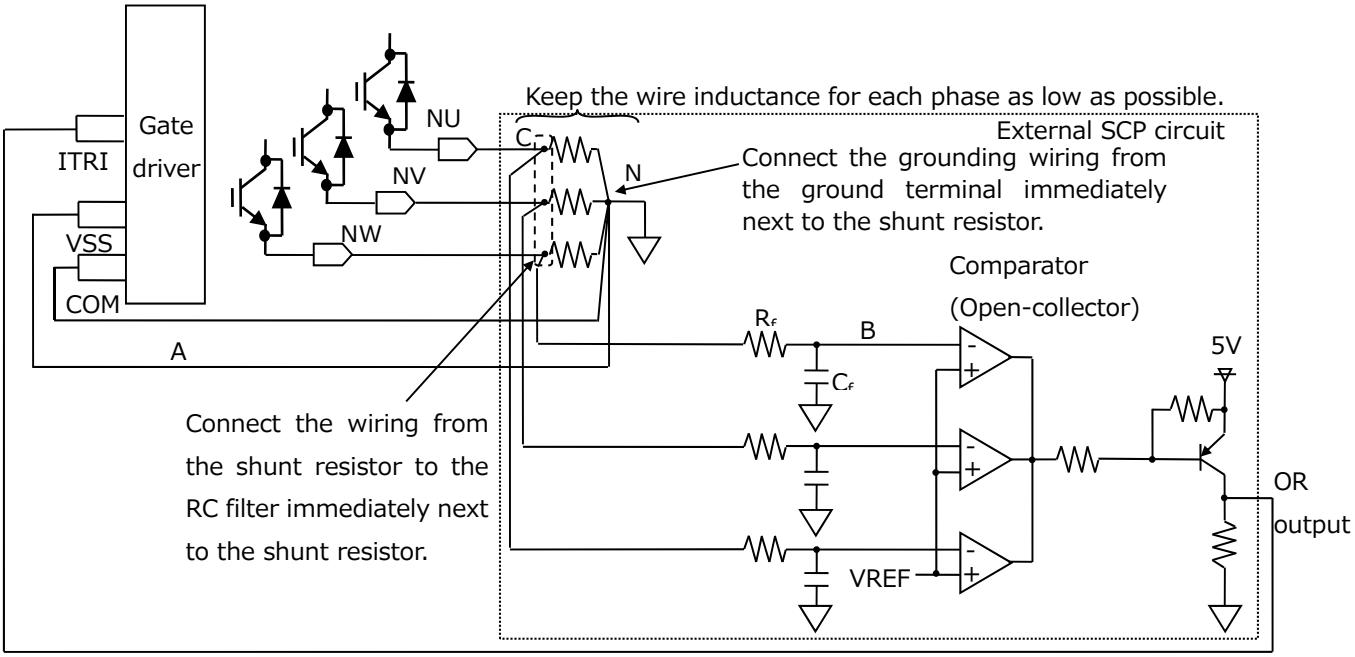


Figure 3.2.11 Example of the external SCP circuit and peripheral wiring when driving with three shunt resistors

3.3 Notes for PCB pattern designing including the power elements

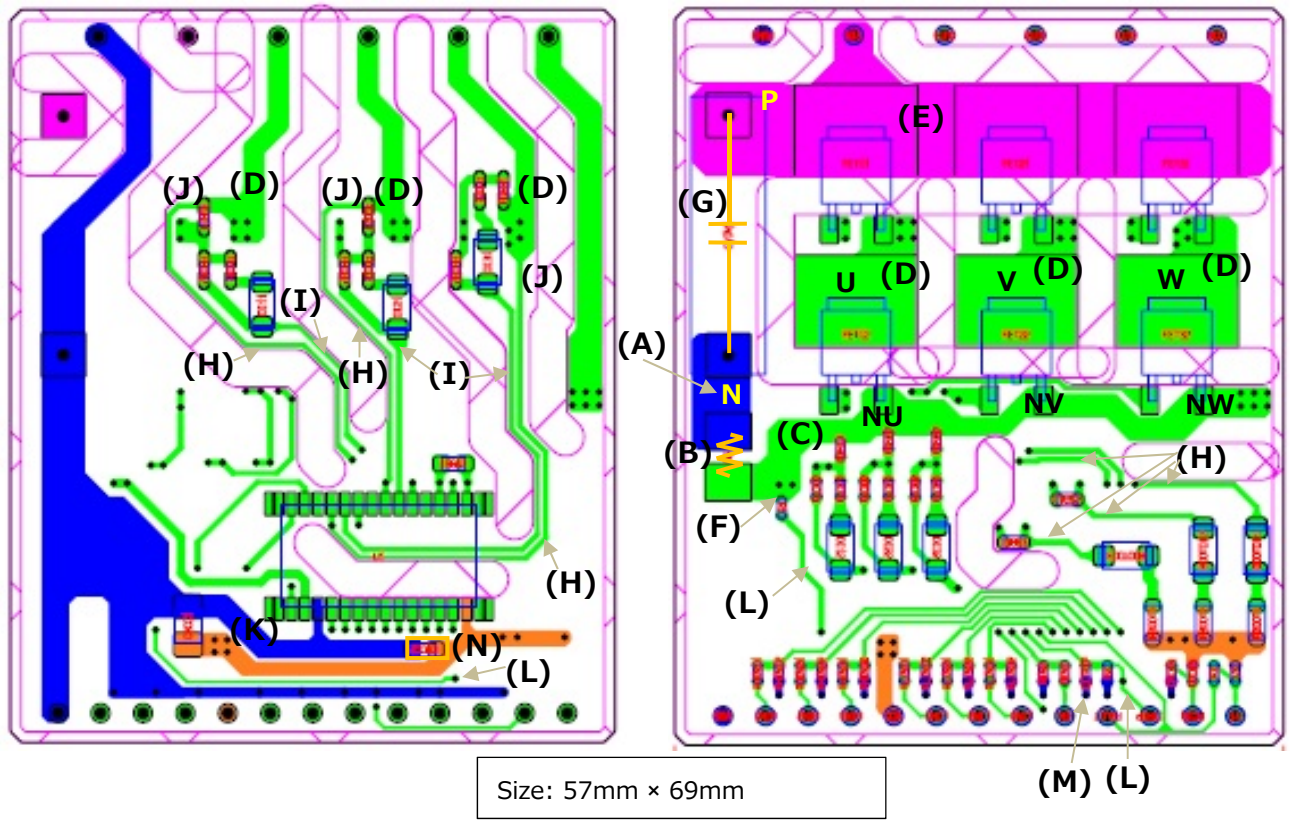


Figure 3.3.1 Example of PCB pattern

(A) Connect the power ground and the control system ground at a single point immediately next to the terminal part of the shunt resistor (point N).

(B) The surface mounted, low inductance type is recommended for the shunt resistor.

(C) Keep the wiring from points NU, NV, and NW to the shunt resistor as short as possible.

(D) Keep the wiring for output points U, V, and W itself and the wiring to the motor as short and broad as possible.

(E) Keep the wiring of the power supply for power elements as broad and short as possible.

(F) Separate the wiring to the ITRIP terminal via resistances at a point immediately next to the terminal part of the shunt resistor.

(G) Place the snubber capacitor immediately next to and between points P and N.

(H) To minimize the parasitic inductance, keep the wiring for the capacitor as short as possible. Since the wiring for the VB1, VB2, and VB3 terminals and the VS1, VS2, and VS3 terminals swings at a high voltage during the switching, any adjacent wiring may result in superimposing noise, causing a malfunction. When using a multilayer board, etc., design the circuit so that these wirings will not be placed adjacent to or cross low voltage wirings, such as the wiring for the control input signal.

(I) Since the wiring from the HO1, HO2, and HO3 terminals to the gate of the power element in the upper side also swings at a high voltage during the switching, any adjacent wiring may result in superimposing noise, causing a malfunction. When using a multilayer board, etc., design the circuit so that these wirings will not be placed adjacent to or cross low voltage wirings, such as the wiring for the control input signal.

(J) Separate the wiring for the VS1, VS2, and VS3 terminals at the output point (U, V, or W) from the main wiring for the motor, so that they will not have a common impedance.

(K) Since the charge current for the bootstrap flows to the ground for the control system, keep the wiring as short and low impedance as possible.

(L) To avoid superimposition of noise or a malfunction, keep the wiring from the shunt resistors to the ITRIP terminal via resistances as short as possible.

(M) Place the filter capacitor to the ITRIP terminal immediately next to and between the ITRIP and ground terminals (ground of the control system).

(N) Place the capacitor immediately next to the VCC terminal.

3.4 Snubber capacitor connection

To prevent an over voltage breakdown due to a surge voltage, make the wiring between the smoothing capacitor and points P and N (the terminal parts of the shunt resistor) as thick and short as possible. In addition, install a snubber capacitor with a capacitance of 0.1 μF to 0.22 μF immediately next to the collector (or drain) of the power elements in the upper side and immediately next to the ground side of the shunt resistor.

Figure 3.4.1 shows an example for the positions to insert the snubber capacitors.

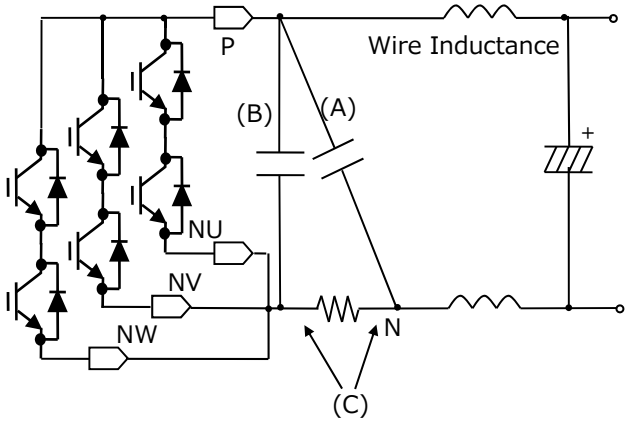


Figure 3.4.1 Connection method of snubber capacitor

To remove a surge voltage as much as possible, the snubber capacitor should be installed on position (B). However, care must be taken because the charge/discharge current (resonance current between the wire inductance and the snubber capacitor) flows in the shunt resistor through the snubber capacitor, activating the protection circuit against the short-circuit current if the wire inductance is large. A recommended connection is as follows: connect the snubber capacitor to the outside of the shunt resistor (A), keep the wiring (C) as short as possible to remove the surge voltage as much as possible, and connect the snubber capacitor immediately next to point P.

● **Revision history**

Date	Revision	Revised content
Aug 1 2018	001	Newly created

Notes

1) The information contained herein is subject to change without notice.

2) Before you use our Products, please contact our sales representative and verify the latest specifications :

3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. ROHM shall have no responsibility for any damages arising out of the use of our Poducts beyond the rating specified by ROHM.

4) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

5) The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM or any other parties. ROHM shall have no responsibility whatsoever for any dispute arising out of the use of such technical information.

6) The Products specified in this document are not designed to be radiation tolerant.

7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a ROHM representative : transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

8) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

9) ROHM shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions and specifications contained herein.

10) ROHM has used reasonable care to ensure the accuracy of the information contained in this document. However, ROHM does not warrants that such information is error-free, and ROHM shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

11) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. ROHM shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

12) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

13) This document, in part or in whole, may not be reprinted or reproduced without prior consent of ROHM.

ROHM SEMICONDUCTOR

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