Switching Regulator Series

PCB Layout Techniques of Buck Converter

No.12027EBY05

PCB layout design for switching power supply IC is as important as the circuit design. Appropriate layout can avoid various problems caused by power supply circuit. Major problems that arise from inappropriate layout may cause increase in noise superposed by output and switching signal, the deterioration of regulator, and also lack of stability. Adopting an appropriate layout will suppress these problems to occur.

Current Path

Figure 1-a to 1-c shows current path in a buck converter circuit. In Figure 1-a, the red line illustrates the main current flow in the converter when switching element Q_1 is ON. C_{BYPASS} is a decoupling capacitor for high frequency and C_{IN} is the capacitor with large capacitance. The instance when the switching element Q_1 is turned ON, most of the steep part of current waveform is supplied by C_{BYPASS} and then from C_{IN}.

In Figure 1-b, the red line illustrates the condition of current flow when the switching element Q_1 is OFF. Free-wheel diode D_1 turns ON and energy stored in inductor L gets released to output side. For Buck converter topology, since inductor is inserted at output in series the output capacitor current is smooth.

Refer Figure 1-c, the red line shows the difference between Figure 1-a and 1-b. Current in this red line changes violently each time the switching element Q_1 changes from OFF to ON, and vice versa. These sharp changes induce several harmonics in the waveform. This difference in system needs to be paid maximum attention during PCB layout and an important caution point.

PCB Layout Procedure

General points of PCB layout procedure are as follows.

1. Place input capacitor and free-wheel diode on the same PCB surface layer as the IC terminal and as close as possible to IC.
2. Include thermal via if necessary to improve heat dissipation.
3. Place inductor close to IC, no need to be as close as input capacitor. This is to minimize radiation noise from the switching node and do not expand copper area more than needed.
4. Place output capacitor close to inductor.
5. Keep wiring of return path away from noise causing areas, such as inductor and diode.

Placing of input Capacitor and Free-wheel Diode

First of all, start placing the most important parts, such as the input capacitor and free-wheel diode. A Single ceramic capacitor may serve as both C_{IN} and C_{BYPASS} for smaller capacitance value of input capacitor, in designs with small current power supply ($I_O \leq 1A$). This is because the frequency characteristics get better, as ceramic capacitor's capacitance value gets smaller. But ceramic capacitor has different frequency characteristics, so confirming it for actual parts being used is important.

As in Figure 2, when a large capacitance value capacitor is used for C_{IN}, generally it has bad frequency characteristics. Therefore place a decoupling capacitor C_{BYPASS} for high frequency with good frequency characteristics in parallel to C_{IN}. For C_{BYPASS}, use surface mount type laminated ceramic capacitor with value of 0.1µF to 0.47µF, X5R or X7R type.

Figure 3-a shows layout example for a suitable input capacitor. Place C_{BYPASS} near IC terminal on the top layer. As in Figure 3-b, large capacitance capacitor C_{IN} can be separated about 2cm from C_{BYPASS} that supplies most of the pulse-current. When difficulty in space occupied, and if cannot place C_{IN} on the same surface as IC, it can be placed at the bottom layer through via like in Figure 3-c. Risks regarding noise can be avoided with this, but there is a possibility of ripple-voltage to increase at high-current, influenced by via resistance.

Figure 3-d shows the layout of C_{BYPASS} and C_{IN} placed on the reverse side. In such case, voltage noise is created by inductance of the via, and the bypass capacitor operates as a reverse effect. Do not carry out this kind of layout design.
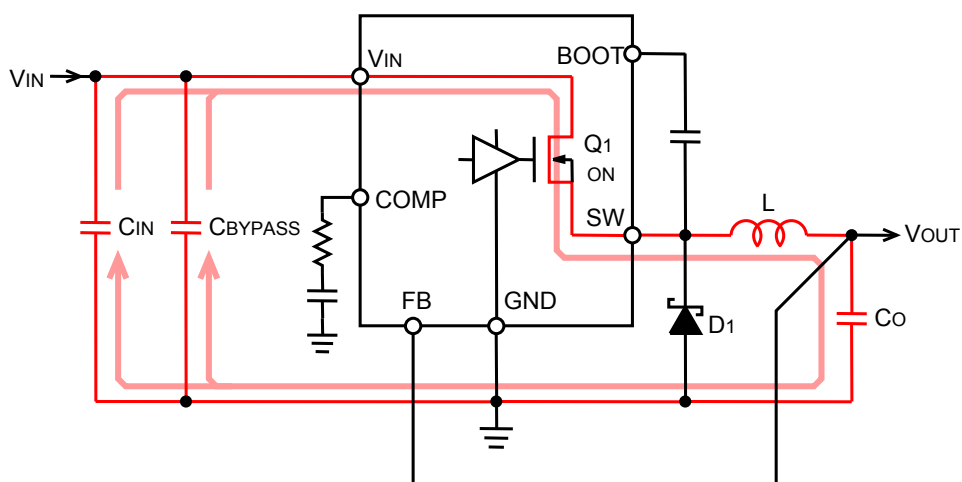
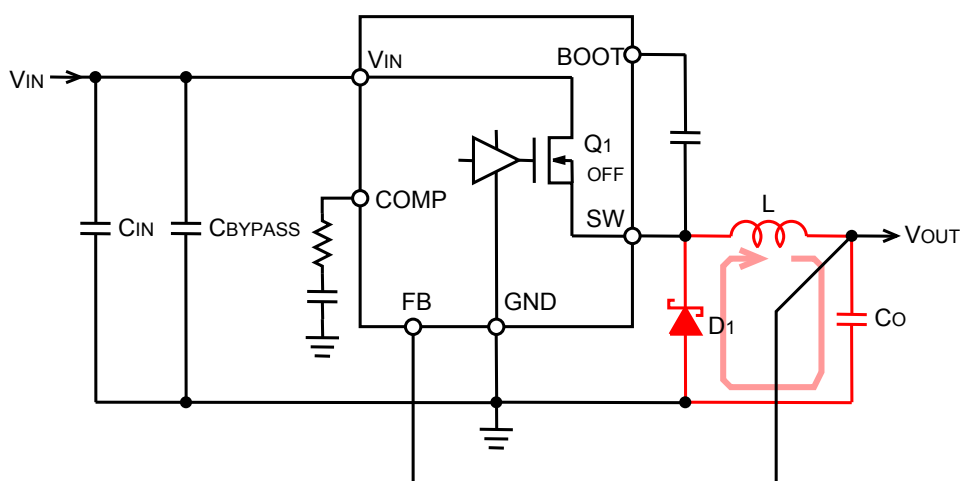Figure 1-a. Current path when switching element Q1 is ON

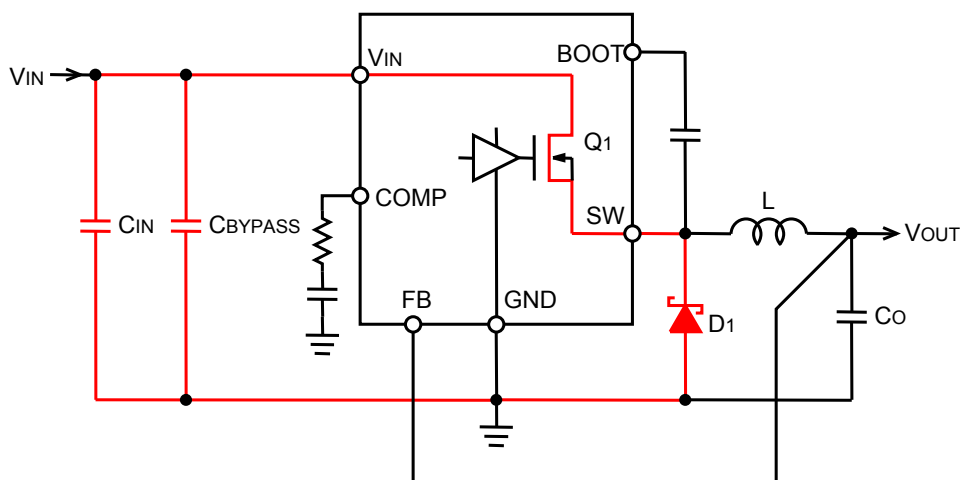Figure 1-b. Current path when switching element Q1 is OFF

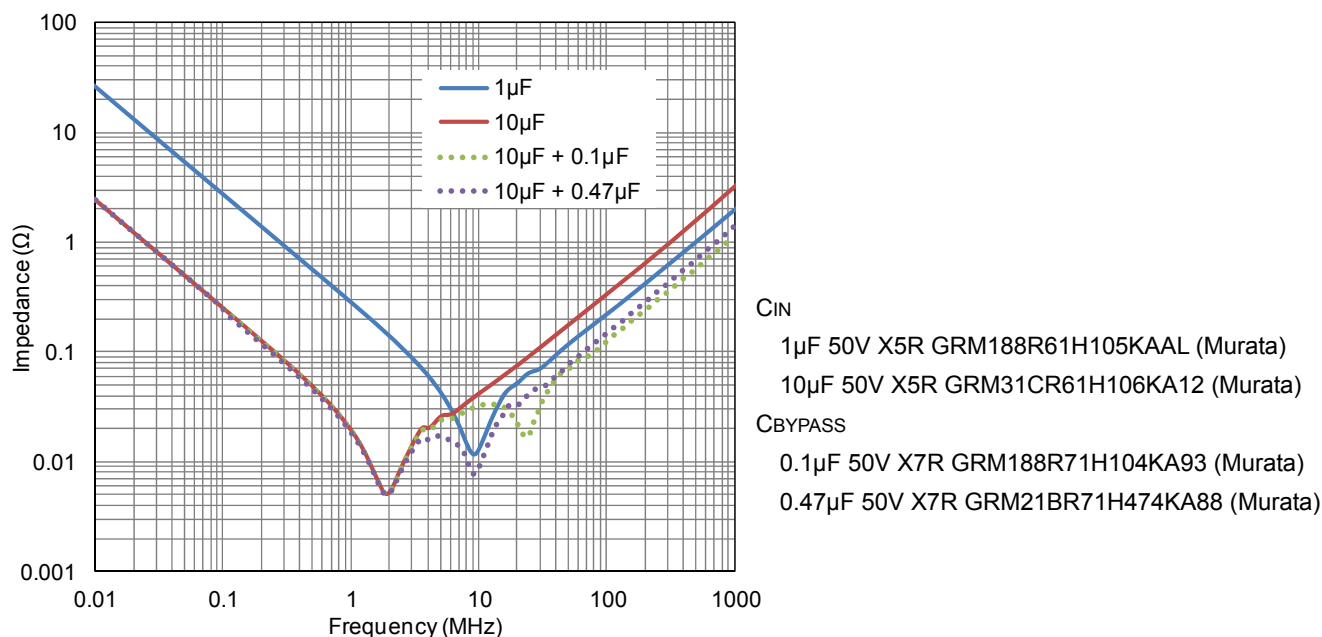Figure 1-c. Current difference, an important part in layout

Figure 2. Frequency characteristics of Ceramic capacitor

Figure 3-f shows unsuitable layout. Voltage noise will be generated by the influence of wiring inductance for C_{BYPASS}, VIN terminal and GND terminal of IC has some distance. Shortening the wiring even by 1mm is highly recommended.

In case of buck converter, high frequency of several hundred MHz will be loaded to the ground of C_{IN} even with C_{BYPASS} placed close to IC. Therefore placing ground of C_{IN} and C_O must be separated from each other by at least 1cm to 2cm.

Free-wheel diode D_1 must be placed closer and on same surface of IC terminal. Figure 3-e shows suitable layout. With long distance between IC terminal and diode, the spike noise will be induced due to wiring inductance, that will be piled up at the output. Use short and wide wiring for free-wheel diode, and connect directly to GND terminal and switching terminal of IC. Do not place it on bottom surface layer through via, as noise will be worse, which is influenced by via inductance.

Figure 3-f shows unsuitable layout. Wiring inductance increases due to distance between diode and switching terminal, and GND terminal of IC and spike noise gets higher. To improve spike noise caused by unsuitable layout the RC snubber-circuit may be added as a countermeasure. This snubber-circuit must be placed closer to switching terminal and GND terminal of IC (Figure 3-g). Placing it at the both ends of diode will not absorb spike noise generated by wiring inductance. (Figure 3-h).

Introduce Thermal Via

Copper area of PCB contributes to heat dissipation, but because it does not have enough thickness, the heat dissipation result that meets area cannot be achieved from limited PCB size. Heat is dissipated using base material of board as a radiator. To deliver heat to opposite layer of the board efficiently and to highly reduce heat resistance, the thermal via are introduced.

Thermal via dimension of HTSOP-J8, reverse-side thermal pad package is shown in Figure 4. To increase heat conductivity, thermal via with small-diameter, inner diameter of 0.3mm which can fill solder, is recommended. With large diameter, problem of solder suction may occur at reflow solder process. Spacing between thermal via is about 1.2mm and placed directly below the thermal pad which is at the reverse-side of IC.

Place additional thermal via around IC like in Figure 3-a, if via below the IC's reverse-side thermal pad are not enough. Heat sink of HTSOP-J8 reverse-side thermal pad package is at ground potential, so EMI does not increase with wide copper pattern.
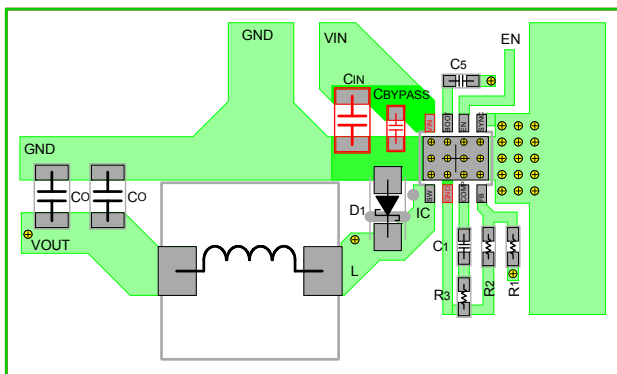
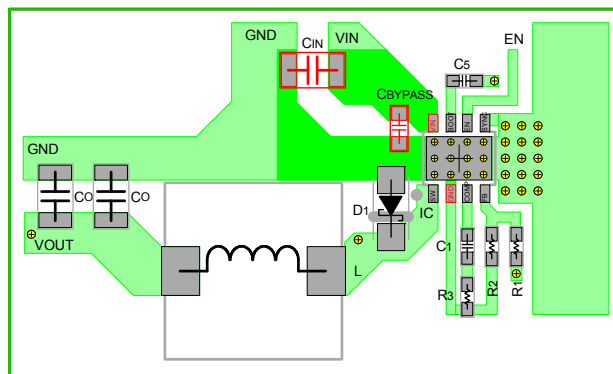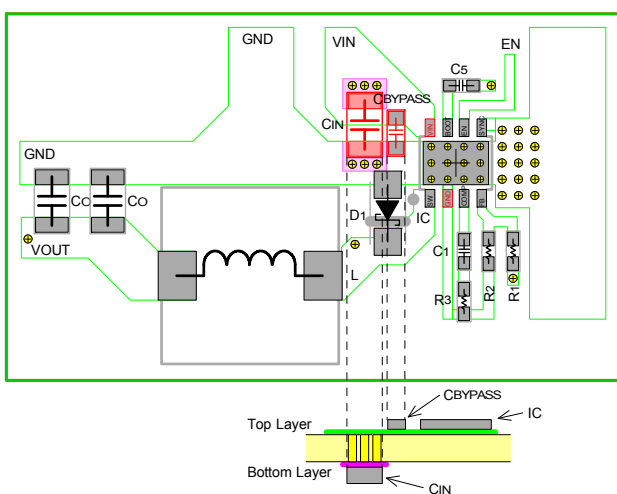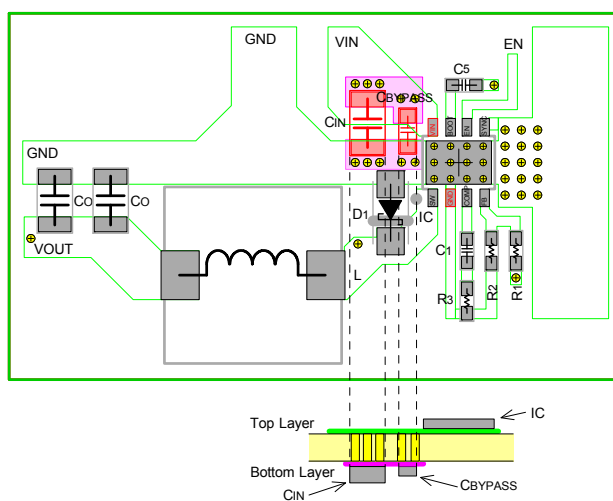Figure 3-a. Placement of suitable input capacitor

Figure 3-b. No problem with C_{IN} separated about 2cm when C_{BYPASS} is closely placed on same surface

Figure 3-c. Increase of ripple voltage is concerned when C_{IN} is placed on bottom layer.

Figure 3-d. Unsuitable layout for input capacitor. Noise increased by via inductance
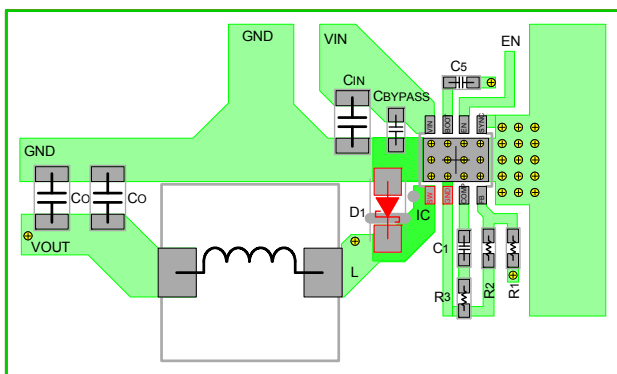

Figure 3-e. Suitable placement of free-wheel diode
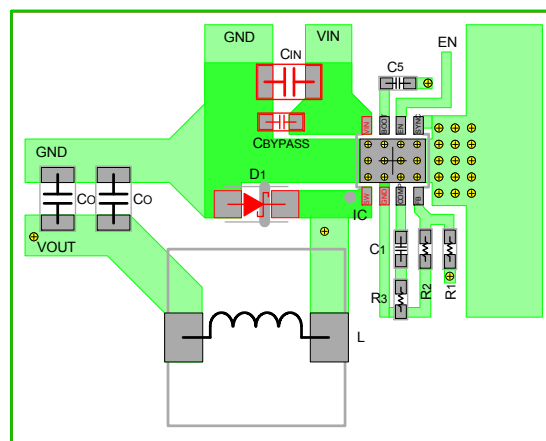

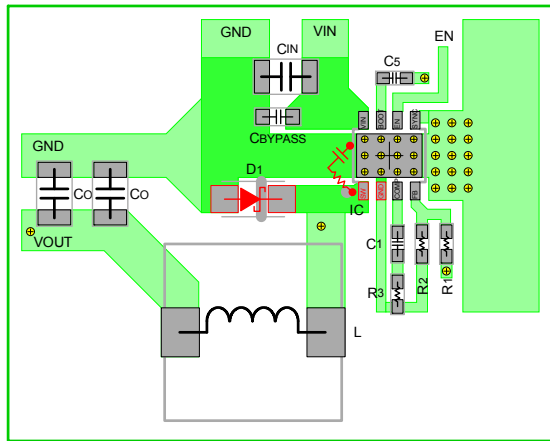Figure 3-f. Unsuitable layout for diode
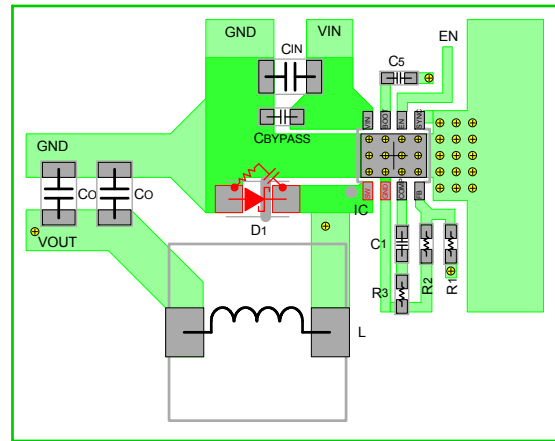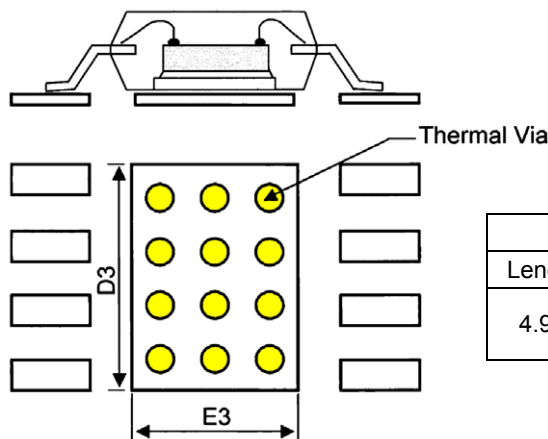
Figure 3-g. Suitable placement of snubber circuit

Figure 3-h. Unsuitable placement of snubber circuit

Central land		Thermal via	
Length D3	Width E3	Pitch	Diameter
4.90mm	3.20mm	1.20mm	φ0.30mm

Figure 4. Thermal via dimension of reverse side thermal pad package

Placing Inductor

Place inductor close to IC, no need to place it as close as the input capacitor, to minimize radiation noise from switching node, and do not expand copper pattern area if not necessary. Increasing copper area is most likely to be thought of to improve wire resistance and to cool down device, but enlarged area may work as an antenna and may lead to increase in EMI.

Permissible current flow is one of the guideline to determine wiring width. Figure 5 shows a graph of rising temperature due to self-heating and conductor width when certain amount of current is flowing. For example, when 2A current is flowing through the wire with conductor thickness of 35µm, keeping conductor width of 0.53mm is suitable to prevent temperature to rise by 20°C.

Wiring can be affected by heat from surrounding parts and surrounding temperature, therefore using conductor width with enough margins is recommended. As an example, for 1 ounce (35µm) board conductor, width more than 1mm per 1A, and for 2 ounce (70µm) board conductor, width more than 0.7mm per 1A is used for wiring.

Figure 6-a shows layout considering wiring area from EMI point of view. Also, unsuitable layout which has unnecessary wide copper area is shown in Figure 6-b.

Not placing ground layer directly below the inductor (Figure 6-c) is also a point to pay attention to, when placing inductor. Due to the eddy current occurring in the ground layer, the inductor value decreases and the loss increases (decrease of Q) with set-off effect from line of magnetic force. Signal line other than ground also has the possibility of propagating switching noise caused by eddy current. It is better to avoid wiring directly under inductor. If wiring is unavoidable, please use closed magnetic circuit structured inductor with small leak from line of magnetic force.

With Conductor thickness of 35μm

Δt = 10°C
Δt = 20°C
Δt = 30°C
Δt = 40°C
Δt = 50°C

With Conductor thickness of 70μm

Δt = 10°C
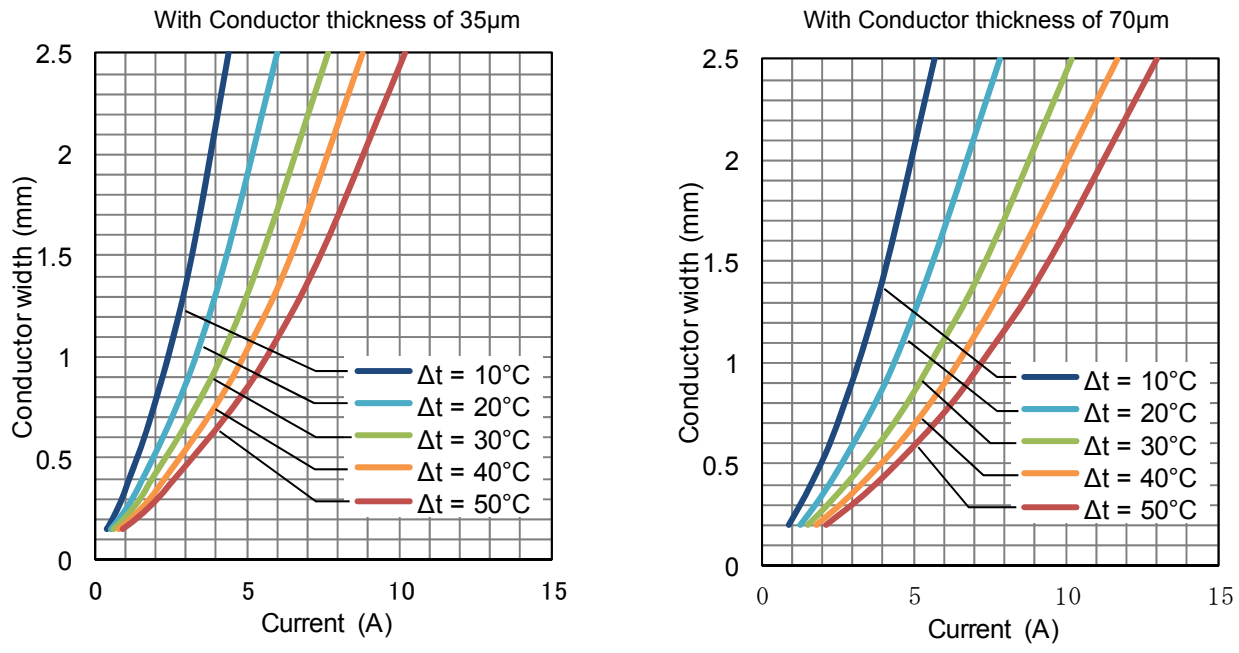Δt = 20°C
Δt = 30°C
Δt = 40°C
Δt = 50°C

Figure 5. Temperature increase by wiring conductor thickness and width, with current flow
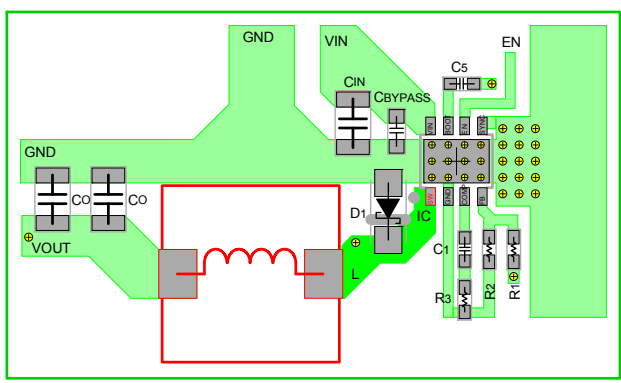

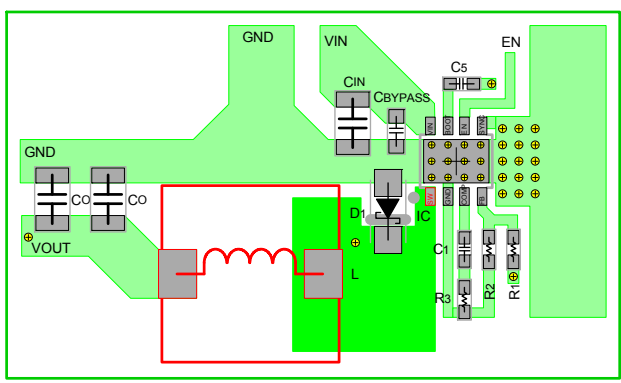Figure 6-a. Suitable wiring to inductor

Figure 6-b. Unsuitable wiring to inductor
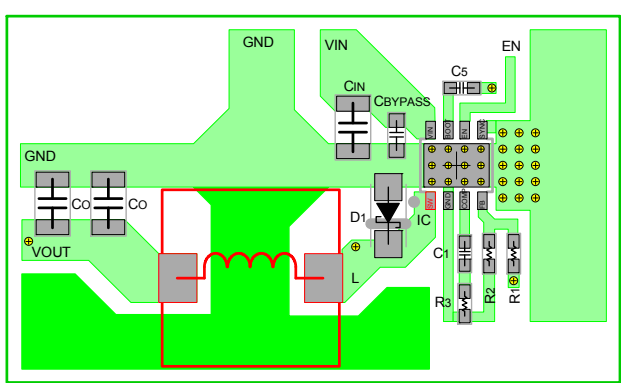Unnecessary wide copper area

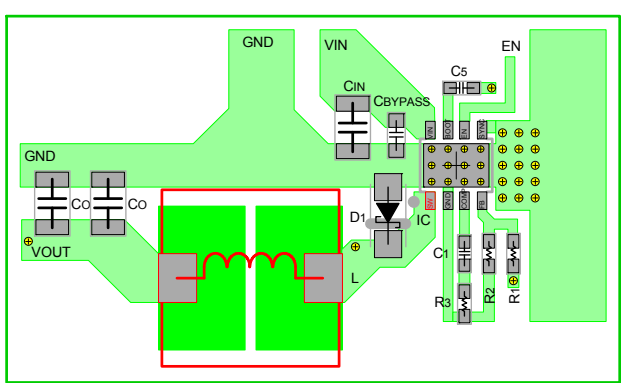Figure 6-c. Unsuitable wiring directly below inductor

Figure 6-d. Unsuitable wiring between inductor terminals

Space between inductor terminals must also be paid attention. If distance between terminals are close like in Figure 6-d, high frequency signal of switching node is induced to output through stray capacitance.

Place Output Capacitor Close to Inductor

Output current is smooth in buck converter as inductor is inserted to output in series. Place output capacitor close to inductor; no need to place it as close as input capacitor. Because high frequency of several hundred MHz is loaded on ground of input, so placing ground of C_{IN} and C_O 1cm to 2cm apart is recommended. If they are close to each other, high frequency noise of input may be propagated to output through C_O.

Wire Feedback Route

Feedback signal route is a wire which needs most attention in signal wiring. If this wire has noise, an error will occur in output voltage and the operation will become unstable.

Figure 7-a, shows the points to be aware of when wiring feedback route.

a). Feedback terminal of IC which inputs feedback signal, is normally designed with high impedance. Output of this terminal and resistor crossover network must be connected with short wire.
b). Part which detects the output voltage must be connected after output capacitor or at both ends of output capacitor.
c). Wiring the resistor-divider circuit nearby and parallel, makes it better for noise tolerance.
d). Draw wire far away from switching node of inductor and diode. Do not wire directly below the inductor and diode, and not parallel to power supply line. Multilayer board must be also wired in the same way.

In wiring of Figure 7-b, the voltage drops due to resistor component of ground wiring and gets slightly affected by load regulation, but if voltage alternation is within target specification, this drawing is worth examining. Layout example is shown in Figure 7-c. Transfer the feedback route to bottom layer of PCB through via, and the layout away from the switching node.

Feedback route is laid parallel beside inductor in Figure 7-d. In this case, noise is induced to feedback route by magnetic field generated around the inductor.
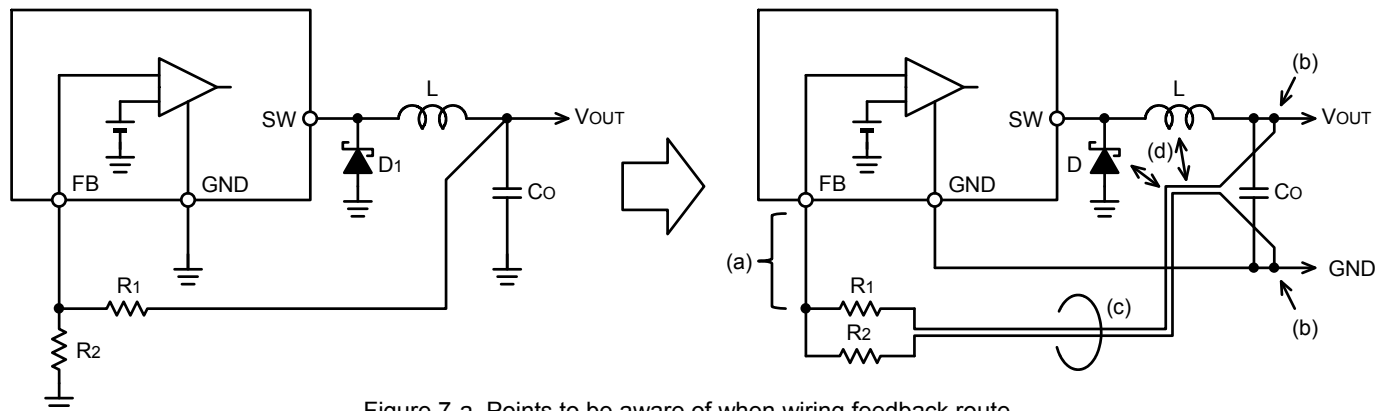

Figure 7-a. Points to be aware of when wiring feedback route
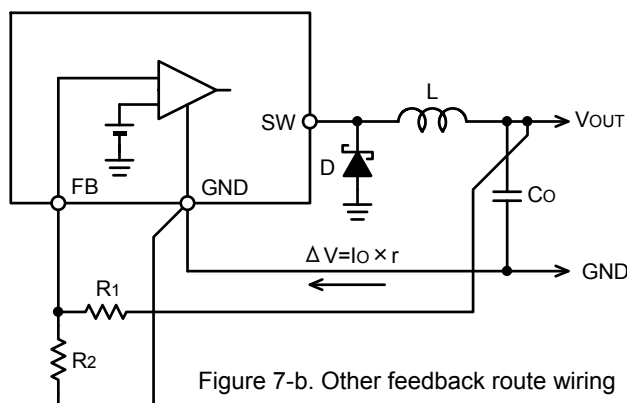

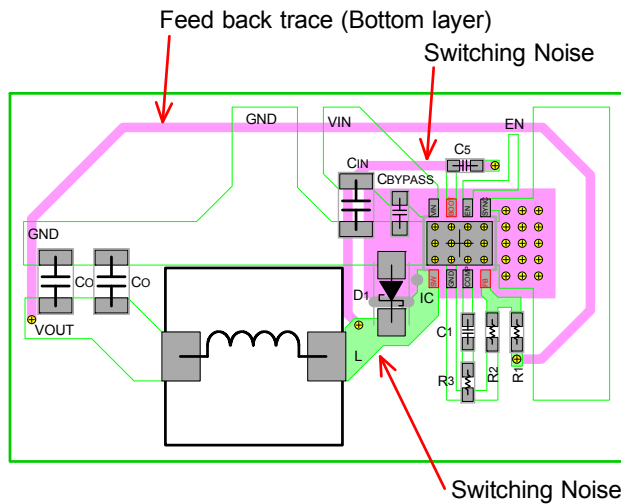Figure 7-b. Other feedback route wiring

Figure 7-c. Layout example of feedback route.
Wiring through bottom layer
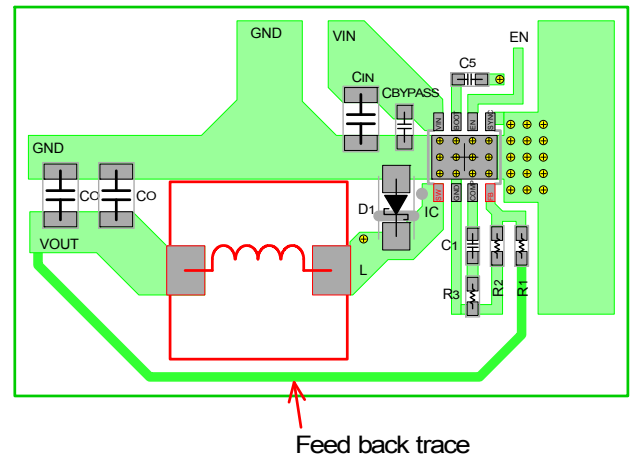
Figure 7-d. Unsuitable feedback route layout
Wiring beside inductor

Ground

Analog small-signal ground and power-ground must be isolated. Laying power-ground without separating from top layer is very ideal（Figure 8）. Connecting isolated power-ground on bottom layer through via causes losses and aggravate the noise due to the effect of inductance and resistance of via. Providing ground plane in PCB inner layer and bottom layer is to reduce and shield DC loss, and to radiate heat better, but it is only a supplementary ground.
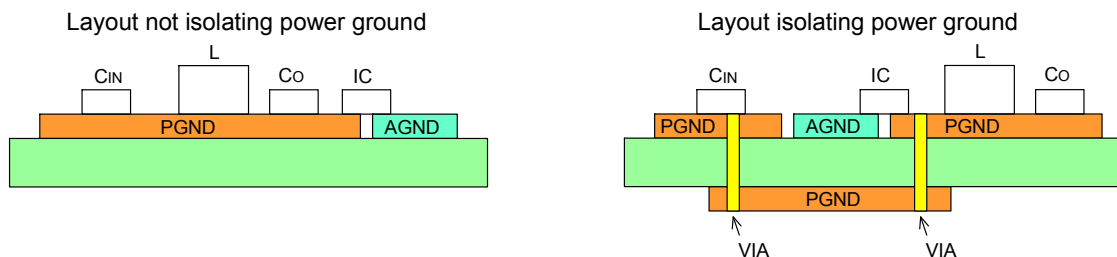
Figure 8. Layout of power ground

When placing ground plane on bottom layer, and in PCB inner-layers of a multilayer board, connection of input power-ground and the ground for free-wheel diode with high frequency switching noise, must be taken care. With power-ground plane in 2nd layer to reduce losses like in Figure 9, connect top layer and 2nd layer with many via and reduce impedance of power-ground. Also, with common-ground in 3rd layer, signal-ground in 4th layer, connect only the power-ground around output capacitor with lower high-frequency switching noise, to power-ground and 3rd / 4th layers. Never connect the power-ground with high noise of free-wheel diode and the input.

Figure 9. Power ground connecting method for multilayer board

Resistance of Copper and Inductance

1. Resistance of Copper

Figure 10 shows resistance value per unit area of copper. This resister value is for copper thickness 35μm, width 1mm, and length 1mm.

General resistance can be calculated by following formula.

$$R = \frac{\rho \times l}{t \times w} \times 10 \quad [m\Omega] \quad\quad (1)$$

   l   : Conductor length [mm]

   w : Conductor width [mm]

   t   : Copper thickness [μm]

   ρ   : Resistivity of copper [μΩcm]

       $\rho_{(T=25°C)} = 1.72 \ \mu\Omega cm$

       $\rho_{(T)} = \rho_{(Ta=25°C)} \times \{1+0.00385(T-25)\} \quad [\mu\Omega cm]$

        T : Temperature

Calculating from resistance value R_P per unit area referring to graph on the right,

$$R = R_P \times \frac{l}{w} \times \frac{35}{t} \quad [m\Omega] \quad\quad (2)$$
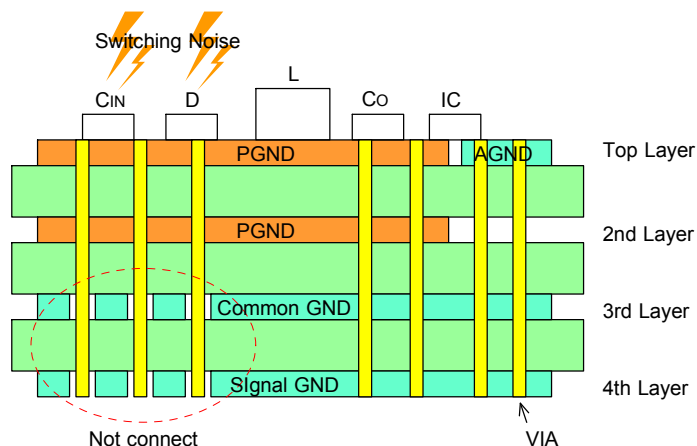
   Rp : Resistance value referred from graph [mΩ]

   l   : Conductor length [mm]

   w : Conductor width [mm]

   t   : Copper thickness [μm]
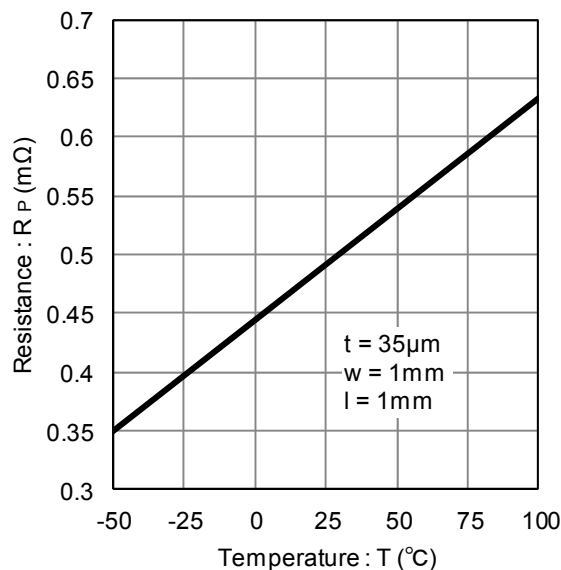
Figure 10. Resistance value per unit area of copper

For example resistance value at 25°C, width 3mm, length 50mm is $R = R_P \times \frac{l}{w} \times \frac{35}{t} = 0.49 \times \frac{50}{3} \times \frac{35}{35} = 8.17 \quad [m\Omega]$

Voltage drop when 3A current is flowing becomes 24.5mV. In case of temperature at 100°C the resistance value increases 29% and voltage drop becomes 31.6mV.

2. Inductance of Copper

Inductance of copper is calculated by following formula. In PCB wiring the inductance value does not totally depend on thickness of copper.

$$L = 0.2 \times l \times \left(\ln \frac{2 \times l}{w+t} + 0.2235 \times \frac{w+t}{l} + 0.5 \right) \quad [nH] \quad\quad\quad (3)$$

   l   : Conductor length [mm]

   w : Conductor width [mm]

   t   : Copper thickness [mm]

Calculated value of copper inductance is shown in Figure 11. This graph shows that inductance value does not drop as much as expected even with doubled line width. To control the effect from parasitic inductance wiring shorting is the best solution

When current that propagate print pattern of inductance L [H] changes i [A] to time t [s], following voltage occurs in both ends of print pattern.

$$|V| = L \times \frac{di}{dt} \quad [V] \quad\quad (4)$$

For example, when 2A current flow in 6nH print pattern for 10ns the following voltage is generated.

$$|V| = 6 \times 10^{-9} \times \frac{2}{10 \times 10^{-9}} = 1.2 \quad [V] \quad\quad (5)$$

Figure 11. Inductance of Copper

Resistance and Inductance of Via

1. Resistance of Via

   Resistance of via can be calculated by following formula. Figure 12 shows via resistance value when board thickness 1.6mm metal planting thickness 0.015mm (15μm)

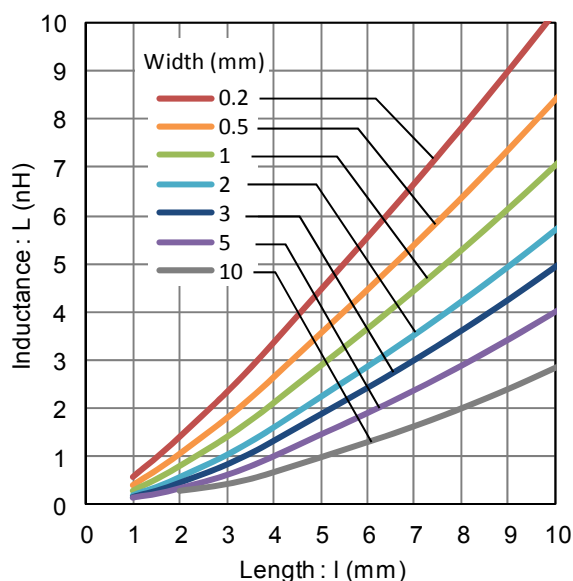$$R_V = \frac{\rho \times h}{\pi \left\{ \left(\frac{d}{2}\right)^2 - \left(\frac{d}{2} - t_m\right)^2 \right\}} \times 0.01 \quad [m\Omega] \tag{6}$$

   h : Board thickness [mm]

   d : Via diameter [mm]

   t_m : Through hole metal planting thickness [mm]

   ρ : Copper resistivity [μΩcm]

       $\rho_{(T=25°C)}$ = 1.72 μΩcm

       $\rho_{(T)} = \rho_{(Ta=25°C)} \times \{1 + 0.00385(T-25)\}$ [μΩcm]

         T : Temperature

2. Inductance of Via

   According to Frederick W. Grover the inductance of via can be calculated by following formula. Figure 13 shows the result.

$$L = \frac{h}{5} \times \left(\ln \frac{4 \times h}{d} + 1 \right) \quad [nH] \tag{7}$$

   h : Board thickness [mm]

   d : Via diameter [mm]

   Wire bending in right angle makes EMI worse even with small inductance. Refer to "Corner wiring" described at end of this page.

3. Allowable Current of Via

   π multiplied by diameter of Via is equivalent to line width. Allowable current value can be expected from the graph on Figure 5, the temperature increases with conductor current, but current capacity will drop compared to conductor thickness 35μm graph for via metal planting thickness is 18μm.

   In previous wiring passage, conductor width of more than 1mm/A was recommended in wiring when conductor thickness was 35μm. But in case of via, half of the thickness is metal planting, so conductor width of more than 2mm/A is recommended. Figure 14 shows example of allowable current.

   Number of via must be placed so the value of allowable current, resistance, inductance satisfies with the standards of the usage.
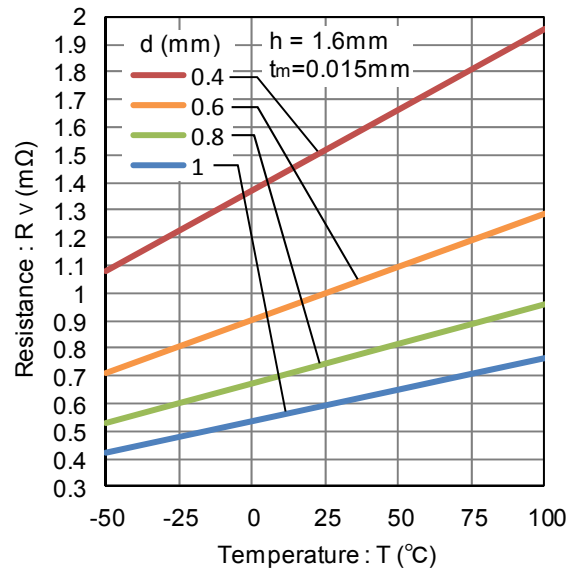
Figure 12. Resistance of Via
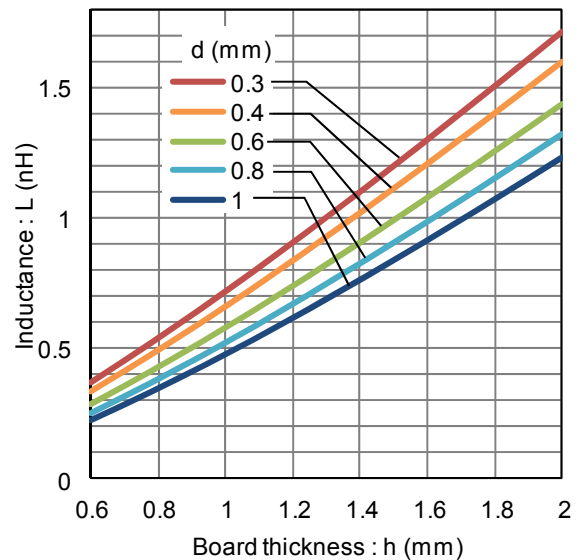
Figure 13. Inductance of Via

Via diameter d (mm)	Conductor width d×π (mm)	Allowable Current (A)
0.3	0.94	0.4
0.4	1.26	0.6
0.6	1.88	0.9
0.8	2.51	1.2
1	3.14	1.5

Figure 14. Example of allowable current of via

Corner Wiring

Bending corner wiring in right angle can cause current waveform to reflect and to be disordered for impedance changes at the corner. Wire with high frequency such as switching node causes EMI to degenerate. Corner must be bent at 45° or circularly. With bigger diameter of bending, smaller will be the change in impedance.

Figure 15. Layout of Corner wiring

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Switching Regulator IC Series

Inductor Calculation for Buck Converter IC

No.12027ECY01

This application note covers the steps required in choosing the inductor and to calculate the value used in buck regulator IC circuits.

● Buck (Step-Down) Converter

Switching regulators are used in a variety of applications to provide stable and efficient power conversion.   A buck converter is a specific type of switching regulator that steps down the input voltage to a lower level output.

Fig. 1 shows a typical buck converter circuit when switching element Q_1 is ON.   When N-ch MOSFET Q_1 is ON, current flowing from input V_{IN} to coil L charges the output capacitor C_O and supplies output current I_O.   In this scenario, the current flowing through coil L produces a magnetic field and electric energy is converted to magnetic energy to be stored.

Fig. 2 illustrates the same circuit when switching element Q_1 is in an OFF state.   When Q_1 is OFF, free-wheeling diode D_1 is activated, and the energy stored in coil L is released.
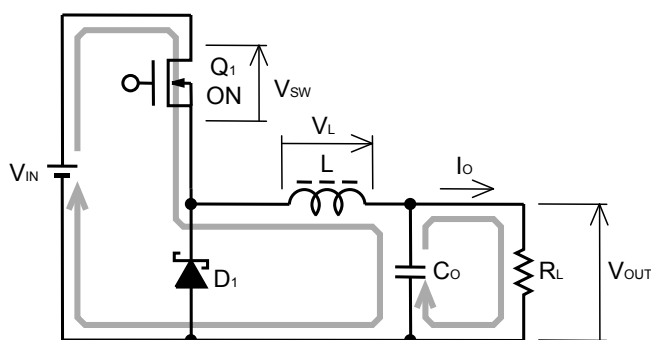
Fig. 1: Basic Buck Converter Circuit
Switching Element ON
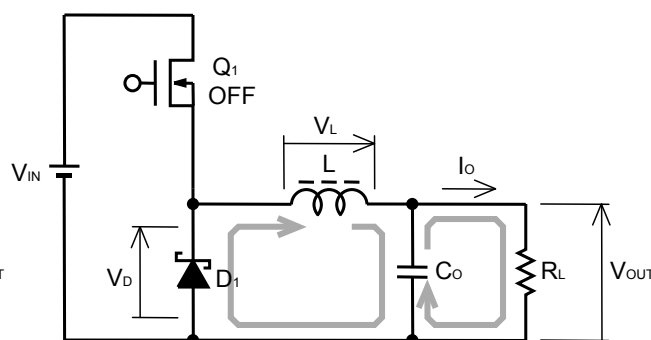
Fig. 2: Basic Buck Converter Circuit
Switching Element OFF

● Inductor Current Waveform

Fig. 3 shows the inductor's current waveform. I_{OUT} is the average inductor current value.   When switching element Q_1 is ON, current flow is shown during ON period t_{ON} of Q_1, and voltage $V_{L(ON)}$ of coil L can be calculated by the following equation:

$$V_{L(ON)} = -(V_{IN} - V_{SW} - V_{OUT}) \tag{1}$$

V_{IN}:   Input Voltage (V)
V_{SW}: Q_1 ON-state Voltage Drop (V)
V_{OUT}:   Output Voltage (V)

The relation between current I_L and voltage V_L of coil L, which has self-inductance, can be calculated using the equation below:

$$V_L = -L \frac{dI_L}{dt} \tag{2}$$

From equation (2), it is clear that by applying additional voltage to the inductor, the reverse-current direction increases by slope V/L.
Current flowing through the coil during t_{ON} can be calculated using equation (1), (2), and by the following method; I_{LT} represents current right before switching element Q_1 turns ON, I_{LP} represents current right before switching element Q_1 turns OFF.

$$I_{LP} - I_{LT} = -\frac{(V_{SW} - V_{IN} + V_{OUT}) \times t_{ON}}{L} \tag{3}$$

The next step is to determine current flow in coil L when the switching element is OFF.

Fig. 3: Inductor Current Waveform

From Fig. 2, the coil voltage when Q1 in OFF- state is $V_{L(OFF)}$, can be calculated using the following method:
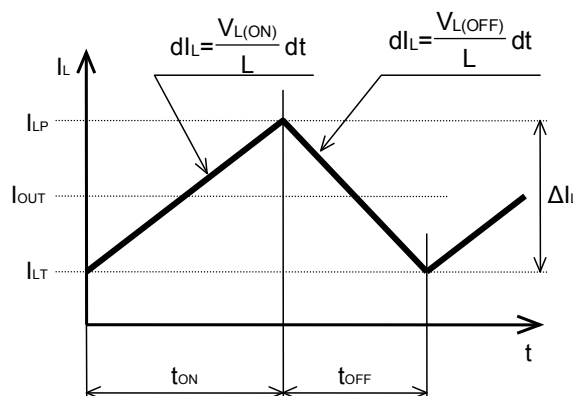
$$V_{L(OFF)} = V_D + V_{OUT} \tag{4}$$

$\quad\quad V_D$:   Forward Voltage Drop across D1 (V)
$\quad\quad V_{OUT}$:   Output Voltage (V)

Using equations (2) and (4), the current flowing through coil L when Q1 is OFF is as follows:

$$I_{LP} - I_{LT} = \frac{(V_D + V_{OUT}) \times t_{OFF}}{L} \tag{5}$$

Current flow in the coil L is almost the same as the output current; consequently,

$$I_{LP} + I_{LT} = 2 \times I_{OUT} \tag{6}$$

From equations (3) and (6), I_{LP} during Q1 ON-state is

$$I_{LP} = I_{OUT} + \frac{(V_{IN} - V_{SW} - V_{OUT}) \times t_{ON}}{2 \times L} \tag{7}$$

Using equations (5) and (6), I_{LP} can be calculated during the period when the switching element is OFF:

$$I_{LP} = I_{OUT} + \frac{(V_D + V_{OUT}) \times t_{OFF}}{2 \times L} \tag{8}$$

● On-Duty Calculation
On-duty D is the ratio of time the switching element is ON t_{ON} versus the switching oscillatory cycle T_{SW}:

$$D = \frac{t_{ON}}{T_{SW}} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW} = 1 - (t_{OFF} \times f_{SW}) \tag{9}$$

Using (7), (8), and (9), the duty can be calculated using the expression below:

$$D = \frac{V_D + V_{OUT}}{V_{IN} - V_{SW} + V_D} \tag{10}$$

By ignoring the voltage drop V_{SW} of the switching element and voltage drop of the diode in equation (10), it is clear that on-duty is fixed by the ratio of output voltage over input voltage:

$$D \cong \frac{V_{OUT}}{V_{IN}} \tag{11}$$

● Maximum Coil Current Value
Use equations (9) and (10) to determine t_{ON}:

$$t_{ON} = \frac{D}{f_{SW}} = \frac{V_D + V_{OUT}}{(V_{IN} - V_{SW} + V_D) \times f_{SW}} \tag{12}$$

The equation below determines the maximum value of I_{LP} by substituting (12) into (7):

$$I_{LP} = I_{OUT} + \frac{(V_{IN} - V_{SW} - V_{OUT}) \times (V_D + V_{OUT})}{(V_{IN} - V_{SW} + V_D) \times 2 \times L \times f_{SW}} \tag{13}$$

Equation (14) is used to determine the minimum value I_{LT} by substituting (13) into (6):

$$I_{LT} = I_{OUT} - \frac{(V_{IN} - V_{SW} - V_{OUT}) \times (V_D + V_{OUT})}{(V_{IN} - V_{SW} + V_D) \times 2 \times L \times f_{SW}} \tag{14}$$

Current-difference between max. and min. ($I_{LP}-I_{LT}$) is as follows:

$$\left(I_{LP} - I_{LT}\right) = \frac{\left(V_{IN} - V_{SW} - V_{OUT}\right) \times \left(V_D + V_{OUT}\right)}{\left(V_{IN} - V_{SW} + V_D\right) \times L \times f_{SW}} \tag{15}$$

Equations (13) and (15) show that large inductance L and high switching frequency will reduce maximum current (I_{LP})and current difference between max. and min. ($I_{LP}-I_{LT}$).

● Inductance L Value Calculation
Define the ratio of current-difference flowing in coil L (I_{LP}-I_{LT}) versus output current I_{OUT} as current ripple-ratio "r".

$$r = \frac{\Delta I_L}{I_{OUT}} = \frac{I_{LP} - I_{LT}}{I_{OUT}} \tag{16}$$

Substitute (15) into (16):

$$r = \frac{\left(V_{IN} - V_{SW} - V_{OUT}\right) \times \left(V_D + V_{OUT}\right)}{\left(V_{IN} - V_{SW} + V_D\right) \times f_{SW} \times L \times I_{OUT}} \tag{17}$$

Then, solve (17) for L to calculate the inductance value:

$$\boxed{L = \frac{\left(V_{IN} - V_{SW} - V_{OUT}\right) \times \left(V_D + V_{OUT}\right)}{\left(V_{IN} - V_{SW} + V_D\right) \times f_{SW} \times r \times I_{OUT}} \quad (H)} \tag{18-1}$$

When the output voltage is high, the calculation can be simplified.

$$\boxed{L = \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN} \times f_{SW} \times r \times I_{OUT}} \quad (H)} \tag{18-2}$$

The inductor value can be increased to reduce the ripple-ratio; however, this will typically result in an inductor size that is physically too big for practical use.   Consequently, "r" is usually set between 0.2 and 0.5 for buck converters.

● Maximum Current Flow through the Coil
Maximum current flow through the coil can be calculated using the following equation:

$$\boxed{I_{Lpeak} = I_{OUT} + \frac{r \times I_{OUT}}{2} \quad (A)} \quad \text{or} \quad \boxed{= I_{OUT} + \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{2 \times V_{IN} \times f_{SW} \times L} \quad (A)} \tag{19}$$

Current flowing through the coil is a combination of output current and ripple-current.   When an abnormality occurs (ex. output short) in a transient load condition and there will be a power surge due to the absence of soft-start feature, and it is possible that the actual current flow through the inductor will exceed the maximum calculated current.   Under transient conditions, coil current may increase up to the IC's switching current limit.   Therefore, the safest approach is to select an inductor with a saturation current rating that exceeds the switching current limit, and not the maximum coil current.

● Effective RMS current flowing through the coil
Effective current value of triangular wave can be calculated by the following method.

$$\boxed{I_{Lrms} = \sqrt{\frac{I_{LP}{}^2 + I_{LT}{}^2 + I_{LP} \times I_{LT}}{3}}} \tag{20}$$

By substituting equations (13) and (14) into (20), we arrive at the following:

$$I_{Lrms} = \sqrt{I_{OUT}{}^2 + \frac{1}{12} \times \left(\frac{\left(V_{IN} - V_{SW} - V_{OUT}\right) \times \left(V_D + V_{OUT}\right)}{\left(V_{IN} - V_{SW} + V_D\right) \times L \times f_{SW}}\right)^2} \quad (A) \tag{21}$$

● Example for Coil selection:

Determine the operating conditions of the buck converter:
- V_{IN} = 12V   Input Voltage
- V_{OUT} = 3.3V   Output Voltage
- I_{OUT} = 2A   Output Current
- r = 0.3   Output Current Ripple Ratio
- V_{SW} = 0.30   ON State Voltage Drop of Switching Element Q_1
- V_D = 0.26 *   Forward Voltage Drop of Free Wheel Diode
- f_{SW} = 380 kHz   Switching Frequency

* For synchronized rectifier type power conversion, specify ON-state voltage drop of lower side element Q_2 (Fig. 4).

Calculate the inductance value of the coil by substituting the above parameters into equation (18-1) or (18-2).

As per equation (18-1), $L = \dfrac{(12 - 0.30 - 3.3) \times (0.26 + 3.3)}{(12 - 0.30 + 0.26) \times 380000 \times 0.3 \times 2} = 10.663$ (µH)

As per equation (18-2), $L = \dfrac{(12 - 3.3) \times 3.3}{12 \times 380000 \times 0.3 \times 2} = 10.493$ (µH)

Using equation (19), the maximum current flowing through the coil is as follows:

$$I_{Lpeak} = I_{OUT} + \frac{r \times I_{OUT}}{2} = 2 + \frac{0.3 \times 2}{2} = 2.3 \ \ (A)$$

As per equation (21), the effective current value flowing through the coil is

$$I_{Lrms} = \sqrt{2^2 + \frac{1}{12} \times \left(\frac{(12 - 0.30 - 3.3) \times (0.26 + 3.3)}{(12 - 0.30 + 0.26) \times 10.663 \times 10^{-6} \times 380000} \right)^2} = 2.008 \ \ (A)$$

Coil selection should be based on the results of the calculations.   For this design, 10µH is chosen as the closest standard inductance value.   If the selected inductor value is different from the calculated result, adjust the current ripple value "r" using equation (17), and substitute the revised value into equation (19) to recalculate the maximum current flowing through the coil.

$$r = \frac{(12 - 0.30 - 3.3) \times (0.26 + 3.3)}{(12 - 0.30 + 0.26) \times 380000 \times 10 \times 10^{-6} \times 2} = 0.329$$

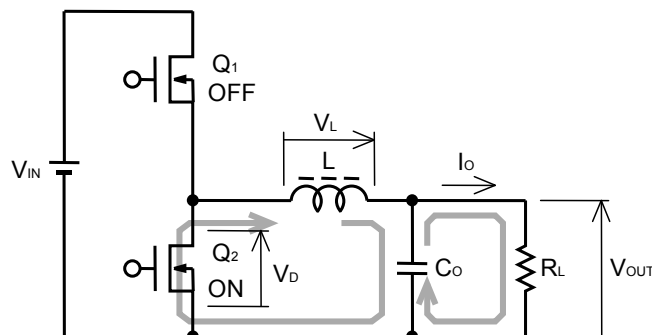$$I_{Lpeak} = 2 + \frac{0.329 \times 2}{2} = 2.33 \ \ (A)$$

Fig. 4: Basic circuit configuration of a buck converter using synchronous rectification power conversion.   In this example, the upper switching element is in OFF-state.

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Switching Regulator IC series
Capacitor Calculation for Buck converter IC

No.14027ECY02

This application note explains the calculation of external capacitor value for buck converter IC circuit.

●Buck converter

Figure 1 is the basic circuit of buck converter. When switching element Q_1 is ON, current flows from V_{IN} through the coil L and charges the output smoothing capacitor C_o, and the output current I_o is supplied. The current which flows into the coil L at this time induces a magnetic field, and electric energy is transformed into magnetic energy and accumulated for storage.

When switching element Q_1 is OFF, free-wheeling diode D turns ON and energy stored in L is then released to the output side.
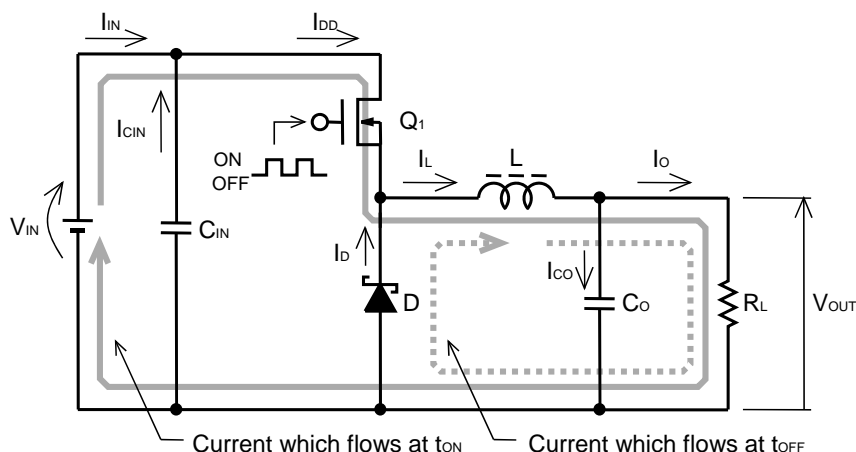

Figure 1   Basic buck converter circuit

●Calculation of Input capacitor

Rated voltage of input capacitor must be higher than the maximum input voltage.

Also rated ripple-current of the capacitor must be higher than the maximum input ripple-current of the IC.

Although the average value of an input current becomes smaller in proportion to the transformation ratio, momentarily the same current equal to output current flows through the buck converter as shown as I_{DD} in Figure 2.

This will be averaged by the input capacitor, but as it is clearly shown as I_{CIN} of Figure 2, the alternating ripple-current flowing in the input capacitor, is higher than I_{CO} of the output.

Effective value of I_{CIN} can be calculated by following equation:

$$I_{CIN} = \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}}\left\{I_O{}^2\left(1 - \frac{V_{OUT}}{V_{IN(MIN)}}\right) + \frac{1}{12}\Delta I_L{}^2\right\}} \; [A_{RMS}] \quad (1)$$

Figure 3 shows the ripple heat generation characteristics of a ceramic capacitor (by Murata Manufacturing Co.). Whether it can be used as input capacitor or not is decided by this graph and the absolute maximum rating of ripple-current.

Be well aware of the temperature and DC bias impressed to the capacitor when using ceramic capacitor.
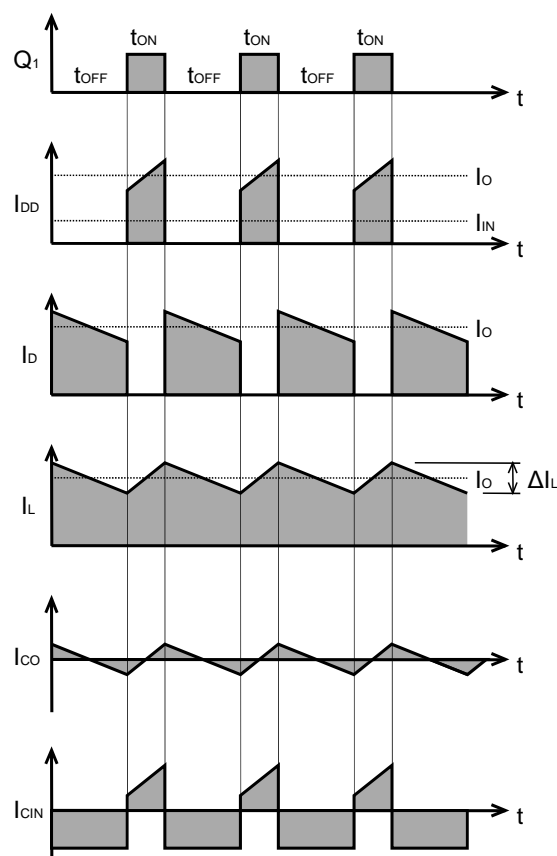

Figure 2   Current waveform of each part

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Change of capacitance value due to temperature can obtain stable temperature characteristic by using high permittivity ceramic capacitor with the characteristics of X5R and X7R.

Capacitance value reduces when DC bias at both sides of ceramic capacitor increases. Figure 4 shows the DC bias characteristics (by Murata Manufacturing Co.).

Example: Characteristic of Ceramic Capacitor (make: Murata Manufacturing Co.)
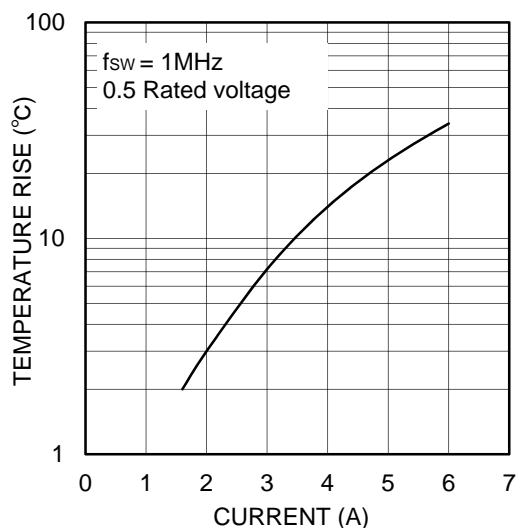GRM32ER7YA106KA12   10µF±10%, 35V, X7R

Figure 3   Ripple heat generation
characteristic
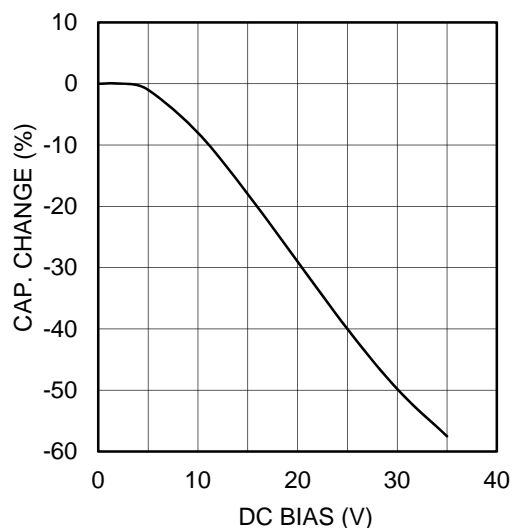
Figure 4   DC bias characteristic

Input ripple voltage of regulator is decided by the value of input capacitance. Input ripple voltage ΔV$_{IN}$ can be calculated by the following equation.

$$\Delta V_{IN} = \frac{I_{O(MAX)} \times V_{OUT}}{C_{IN} \times f_{SW} \times V_{IN}} + \left(I_{O(MAX)} \times ESR_{MAX} \right) \quad [\text{V}_{\text{P-P}}]$$

(2)

V_{IN}: Input voltage [V]

V_{OUT}: Output voltage [V]

$I_{O(MAX)}$: Maximum load current [A]

C_{IN}: Input capacitor [F]

f_{SW}: Switching frequency [Hz]

ESR_{MAX}: Maximum equivalent series resistance ESR [Ω] of input capacitor

● Calculation example of input capacitor

For this design example, parameters listed in Table1 will be used. As for the input capacitor, Murata Manufacturing Co. make10µF / 35V ceramic capacitor is considered for reference.

Parameter	Value
Input voltage range V_{IN}	7V to 28V
Output voltage V_{OUT}	3.3V
Input ripple voltage ΔV_{IN}	300mV
Output ripple voltage ΔV_O	33mV (1% of output voltage)
Output rating current I_O	3A
Inductor ripple current ΔI_L	0.9A (30% of output rating current)
Operation frequency f_{SW}	1MHz

Table1   Design parameter

Calculate input ripple current by substituting each parameter to the equation (1).

$$I_{CIN} = \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}}\left\{I_O{}^2\left(1 - \frac{V_{OUT}}{V_{IN(MIN)}}\right) + \frac{1}{12}\Delta I_L{}^2\right\}} = \sqrt{\frac{3.3}{7}\left\{3^2\left(1 - \frac{3.3}{7}\right) + \frac{1}{12} \times 0.9^2\right\}} = 1.508 \ [A_{RMS}] \quad (3)$$

From Figure 3 ripple current capacitance obtains enough margins.

Next, calculate input ripple voltage by substituting each parameter to equation (2). At this point consideration for DC bias characteristic of ceramic capacitor is necessary. In this example, since the maximum voltage impressed to capacitor is 28V, 48% will be reduced from rating capacitance value as from Figure 4. Also, ESR of ceramic capacitor is 2mΩ.

$$\Delta V_{IN} = \frac{I_{O(MAX)} \times V_{OUT}}{C_{IN} \times f_{SW} \times V_{IN}} + \left(I_{O(MAX)} \times ESR_{MAX}\right)$$

$$= \frac{3 \times 3.3}{(10 \times 10^{-6} \times 0.52) \times 1 \times 10^6 \times 28} + (3 \times 2 \times 10^{-3}) = 74 \ [mV_{P\text{-}P}] \quad (4)$$

Ripple voltage of minimum input voltage can be shown as below method.

$$\Delta V_{IN} = \frac{3 \times 3.3}{(10 \times 10^{-6} \times 0.96) \times 1 \times 10^6 \times 7} + (3 \times 2 \times 10^{-3}) = 153.3 \ [mV_{P\text{-}P}] \quad (5)$$

The design requirement for input ripple voltage below 300mV can be confirmed. Maximum voltage at both ends of input capacitor is $V_{IN(MAX)} + \Delta V_{IN}/2$. To obtain more voltage margins, give consideration of using two 4.7µF / 50V capacitors in parallel. Also, be cautious for actual input ripple voltage that may get higher than the calculated value, due to output impedance of the voltage source (preceding circuit) and parasitic component resulting from the PCB layout.

●Calculation of output capacitor

   Important elements in designing output capacitor are rating voltage, ripple rating current, and ESR (equivalent series resistance). Ripple current and voltage impressed to the capacitor must be less than the maximum rating. ESR is an important element to decide the output ripple voltage with the inductor current.

   The effective value of ripple current, the alternating component included in the output current, can be calculated by the following equation as it is a triangular waveform like I_{CO} of Figure 2.

$$I_{CO} = \frac{1}{\sqrt{12}} \times \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{L \times f_{SW} \times V_{IN(MAX)}} \quad [\text{A}_{RMS}] \tag{6}$$

$V_{IN(MAX)}$: Maximum input voltage [V]

V_{OUT}: Output voltage [V]

L: Inductor value [H]

f_{SW}: Switching frequency [Hz]

   Output ripple voltage is the composite waveform created by the ripple current of the inductor flowing through the output capacitor depending on electrostatic capacitance, ESR, and ESL. It can be calculated by the following equation.

$$\Delta V_{ORPL} = \Delta I_L \left(\frac{1}{8 \times C_O \times f_{SW}} + ESR \right) + ESL \frac{V_{IN(MAX)}}{L} \quad [\text{V}_{P\text{-}P}] \tag{7}$$

$V_{IN(MAX)}$: Maximum input voltage [V]

ΔI_L: Inductor ripple current [A]

C_O: Output capacitor [F]

L: Inductor value [H]

f_{SW}: Switching frequency [Hz]

ESR: Equivalent series resistor of output capacitor [Ω]

ESL: Equivalent series inductor of output capacitor [H]

   When using leaded type aluminum electrolytic capacitor with high ESR and ESL as an output capacitor, notice that ripple by ESR and ESL may get bigger than the ripple by capacitance.

●Calculation example of output capacitor

For this design example, parameters listed in Table 1 will be used.   As for the input capacitor, Murata Manufacturing Co. make 22μF / 25V ceramic capacitor is considered as reference. Calculate ripple current by substituting each parameter to equation (6). Use 4.7μH value for coil L.

$$I_{CO} = \frac{1}{\sqrt{12}} \times \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{L \times f_{SW} \times V_{IN(MAX)}} = \frac{1}{\sqrt{12}} \times \frac{3.3(28-3.3)}{4.7 \times 10^{-6} \times 1 \times 10^{6} \times 28} = 0.18 \quad [A_{RMS}] \tag{8}$$

From Figure 5 ripple current capacitance obtains enough margin.

Next, calculate output ripple voltage by substituting each parameter to equation (7).   At this point consideration for DC bias characteristic of ceramic capacitor is necessary. In this example, because the voltage impressed to capacitor is 3.3V, 2% will be reduced from rating capacitance value as in Figure 6. Also, ESR of ceramic capacitor is 2mΩ and ESL is 0.4nH.

$$\Delta V_{ORPL} = \Delta I_L \left(\frac{1}{8 \times C_O \times f_{SW}} + ESR\right) + ESL \frac{V_{IN(MAX)}}{L}$$

$$= 0.9 \left(\frac{1}{8 \times (22 \times 10^{-6} \times 0.98) \times 1 \times 10^{6}} + 2 \times 10^{-3}\right) + 0.4 \times 10^{-9} \left(\frac{28}{4.7 \times 10^{-6}}\right) = 9.4 \ [mV_{P-P}] \tag{9}$$

Output ripple voltage requirement is 33mV, meaning that the above value satisfies. But, the actual output ripple voltage can be influenced by ESR, ESL elements of capacitor and by parasitic element originated in PCB layout, causing difference from the calculated value.

Example: Characteristic of Ceramic Capacitor (make: Murata Manufacturing Co.)
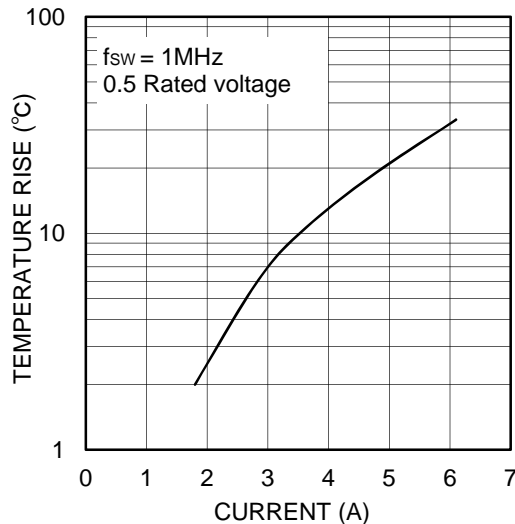GRM32ER71E226ME15   22μF±20%, 25V, X7R

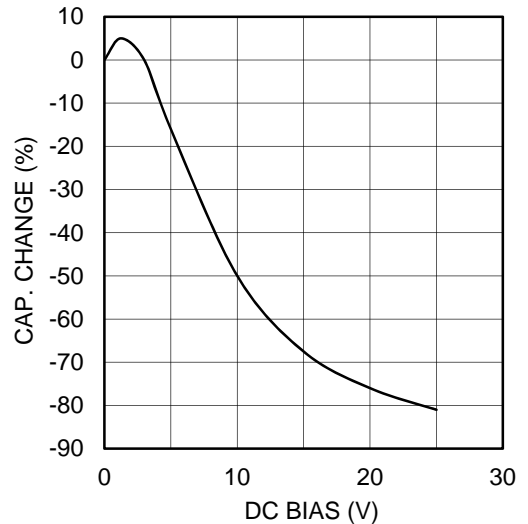Figure 5   Ripple heat generation characteristic

Figure 6   DC bias characteristic

●Equation of buck converter

・Effective value of ripple current flowing in input capacitor

$$I_{CIN} = \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}}\left\{I_O^2\left(1 - \frac{V_{OUT}}{V_{IN(MIN)}}\right) + \frac{1}{12}\Delta I_L^2\right\}} \quad [\text{A}_{\text{RMS}}]$$

・Input ripple voltage

$$\Delta V_{IN} = \frac{I_{O(MAX)} \times V_{OUT}}{C_{IN} \times f_{SW} \times V_{IN}} + \left(I_{O(MAX)} \times ESR_{MAX}\right) \quad [\text{V}_{\text{P-P}}]$$

V_{IN}: Input voltage [V]

$V_{IN(MIN)}$: Minimum input voltage [V]

V_{OUT}: Output voltage [V]

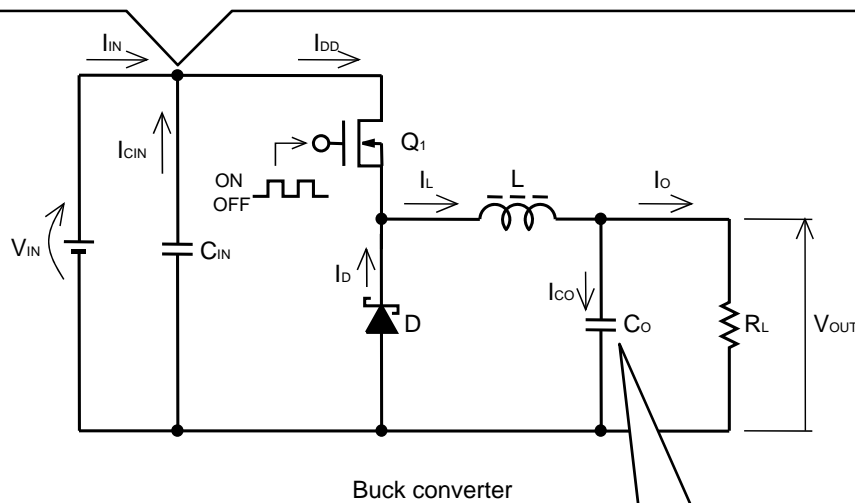I_O: Output rating current [A]

ΔI_O: Inductor ripple current [A]
    (Usually set between 20% and 50% of I$_O$)

$I_{O(MAX)}$: Maximum load current [A]

C_{IN}: Input capacitor [F]

f_{SW}: Switching frequency [Hz]

ESR_{MAX}: Maximum equivalent series resistance
    (ESR) of Input capacitor [Ω]

Buck converter

・Effective value of ripple current flowing in output capacitor

$$I_{CO} = \frac{1}{\sqrt{12}} \times \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{L \times f_{SW} \times V_{IN(MAX)}} \quad [\text{A}_{\text{RMS}}]$$

・Output ripple voltage

$$\Delta V_{ORPL} = \Delta I_L\left(\frac{1}{8 \times C_O \times f_{SW}} + ESR\right) + ESL\frac{V_{IN(MAX)}}{L} \quad [\text{V}_{\text{P-P}}]$$

$V_{IN(MAX)}$: Maximum input voltage [V]

V_{OUT}: Output voltage [V]

L: Inductor value [H]

f_{SW}: Switching frequency [Hz]

ΔI_L: Inductor ripple current [A]
    (Usually set between 20% and 50% of I$_O$)

C_O: Output capacitor [F]

ESR: Equivalent series resistance of
    output capacitor [Ω]

ESL: Equivalent series inductance of
    output capacitor [H]

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